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Closed-Form Formulas for Automated Design of SiC-Based Phase-Shifted Full Bridge Converters in Charger Applications

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Abstract: Phase-Shifted Full Bridge (PSFB) topology in its four-diode variant is the choice with the lowest part count in applications that demand high power, high voltage, and galvanic isolation, such as in Electric Vehicle (EV) chargers. Even though the topology is prevalent in power electronics applications, no single, unified analytical model has been proposed for the design process of four-diode PSFB converters. As a result, engineers must rely on simulations and empirical results obtained from previously built converters when selecting components to properly match the DC source voltage level with the DC load voltage requirements. In this work, the authors provide a design-oriented analysis approach for obtaining the output voltage and semiconductor current values, ready for implementation in a spreadsheet- or MATLAB-type software to automate design optimization. The proposed formulas account for all the first-order nonlinear dependencies by considering the impact of each of the following eight design parameters: DC-link voltage, load resistance, phase-shift ratio, switching frequency, transformer turns ratio, magnetizing inductance, series inductance, and output inductance. The results are verified through experiments at the power level of 10 kW and the DC-link voltage level of 800 V by using a grid simulator and a SiC-based two-level Active Front End (AFE) with a DC–DC stage based on the PSFB topology. The accuracy of the output voltage formula is determined to be around 99.6% in experiments and 100.0% in simulations. Based on this exact model, an automated design procedure for high-power high-voltage SiC-based PSFB converters is developed. By providing the desired DC-link voltage, output voltage, output power, output current ripple factor, maximum temperatures, and semiconductor and heatsink databases, the algorithm calculates a set of feasible designs and points to the one with the lowest semiconductor losses, dimensions, or cost.

Keywords: phase-shifted full bridge; PSFB; grid-tied isolated unidirectional converter; three-phase Active Front End; AFE; EV charger; SiC; high power; high-frequency planar transformer

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1. Introduction

With the rapidly growing share of Electric Vehicles (EVs) in the overall vehicle market, the numbers of required On-Board Chargers (OBCs) and DC fast chargers are expected to rise at an unprecedented rate. To meet that demand, automated design tools [1] will be necessary, especially for the more complex stage of a charger—the isolated DC–DC converter. In contrast to the plethora of new topologies that feature an increasingly high component count, the Phase-Shifted Full Bridge (PSFB) effectively combines the relative simplicity of a bridge converter with the benefits of zero-voltage switching (ZVS) without the need for resonant tanks [2]. The four-diode variant is well-suited for high-voltage operation (as opposed to the two-diode variant [3]) and, if equipped with SiC devices, it can also accommodate high switching frequencies [4]. The PSFB, in conjunction with a three-phase two-level Active Front End (AFE), allows AC–DC transfer of electric energy at high power and voltage levels while providing galvanic isolation and requiring a minimum number of components.

This specification enables the two converters to operate together in applications such as EV chargers [5] (see Figure 1a) or photovoltaic (PV) inverters [6] (see Figure 1b). In such configurations, the AFE provides a power factor correction feature [7–9], while the PSFB is responsible for the DC voltage control. Sample specification requirements for an EV charger are presented in Table 1.

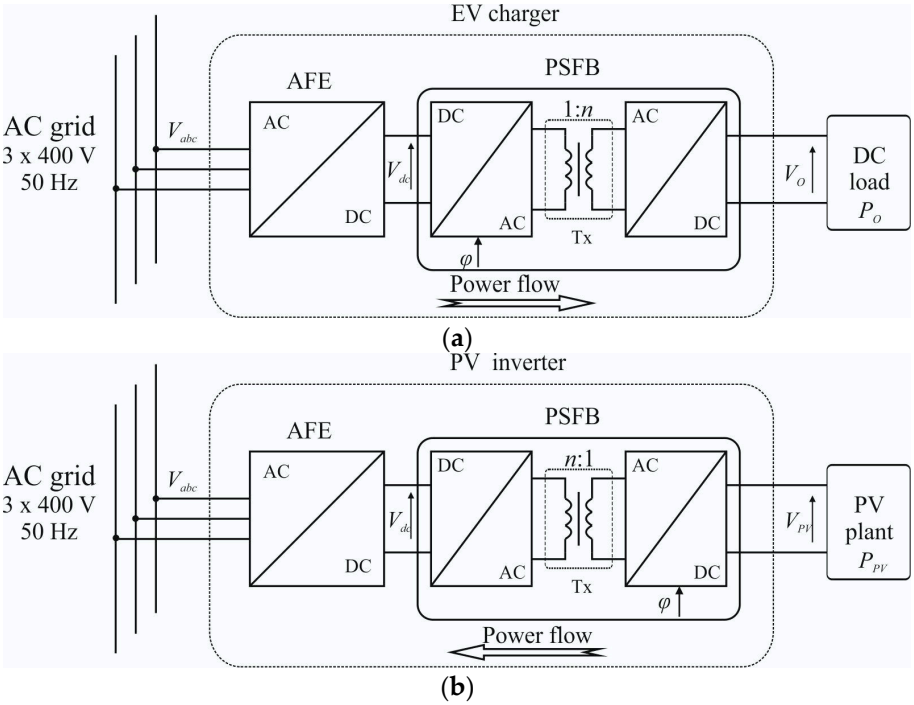


Figure 1. Sample applications of the AFE + PSFB isolated grid-connected AC–DC converter: (**a**) EV charger; (**b**) PV Inverter.

Table 1. Example design parameters of an AC-DC charger.

Parameter	Symbol	Value
Input voltage	V_{abc}	3 × 400 V, 50 Hz
DC-link voltage	V_{dc}	800 V
Output voltage	V_o	650 V
Output power	P_o	20 kW

While the selection of components for the AFE is relatively straightforward and the relationship between the input (grid) voltage V_{abc} and the dc-link voltage V_{dc} is simple, the same is not the case with regard to the PSFB part of the charger. The output voltage V_o has an intricate dependence on eight design parameters: V_{dc}, load resistance R_o, phase-shift ratio φ, switching frequency f_s, transformer turns ratio n, magnetizing inductance L_m, series inductance L_l, and output inductance L_o; however, the literature provides no closed-form formulas that encompass all of these dependencies. So far, one approach to this problem has been to design the converter based on some very approximate calculations and then to let the voltage controller set φ to obtain the desired value of V_o. However, the problem is that for many combinations of the design parameters there is simply no value of φ that leads to a particular required V_o value at the given output power level (P_o). Additionally, if the converter does work at the required voltage and power conditions, it is certain to be overdesigned, which implies unnecessarily high losses, dimensions, and costs. Another, more prevalent method is to conduct simulations at the required V_{dc}, V_o, and P_o values [10]. This is a valid but not scalable solution, i.e., it cannot be efficiently automated for multi-objective optimization of the design.

For that, one needs closed-form expressions, which enable a spreadsheet- or MATLAB-type software to calculate various solutions quickly, based only on a closed set of design

parameters. Some advanced mathematical models related to the output voltage and losses were presented in the literature; however, these concerned the two-diode PSFB version, which is suited for low-voltage applications [11–15]. Research was also performed in the area of the PSFB with a voltage doubler [16], and even though this topology is well-suited for high-voltage applications, it lacks in power throughput. Many analyses for resonant variants of PSFB were conducted [17–19], including the development of an accurate output voltage formula reported for the LLC Full-Bridge topology [20]. As for the four-diode PSFB, only non-closed-form expressions have been provided, such as the ones in [2], which, in addition, do not consider the impact of all eight design parameters. Similar formulas later appeared in other works related to PSFB modeling [21–23]; however, the problem remains unsolved—if an engineer wants to accurately calculate the output voltage, closed-form expressions are required—otherwise it is not feasible. There is a similar situation regarding the PSFB loss calculations, where it is common to provide general loss formulas without stating how the related rms and average semiconductor current values were calculated [24,25]. Recently, a thorough analytical investigation was presented [26] that outlined the relationship between the output voltage and the parasitic components of the PSFB, which cause certain second-order effects. However, it is the first-order, verified relationships between the values of main components that are primarily required for the design automation.

This publication takes a deep dive into analytical expressions for the four-diode PSFB topology related to output voltage and semiconductor currents that are required for an automated design procedure. Section 2 presents the conducted analysis and compares results obtained from the developed expression to those from simulations. This section also shows the derivation of resulting semiconductor-related current formulas, which are vital for enabling a loss-based automated semiconductor selection process. Furthermore, control methods for both AFE and PSFB are discussed, including their implementation. In Section 3, the laboratory setup is discussed and the results of steady-state experiments are shown and analyzed. As demonstrated in Figure 2, the analytical model based on the eight design parameters is first developed throughout Formulas (1)–(36) and then the resulting expressions for output voltage (37) and semiconductor-related currents (41), (42), (46), (47) are verified. Upon this verification, automated design procedure for the four-diode PSFB is presented for the first time, based on the presented analytical model. Using only the knowledge of the application requirements and the devices available, selection of components and parameters is automated to take into consideration voltage level issues, output current continuity, and semiconductor temperatures calculated based on accurate loss formulas. In Section 4, conclusions are drawn regarding the applicability of the developed expressions and the potential of this approach for computer-aided design automation.

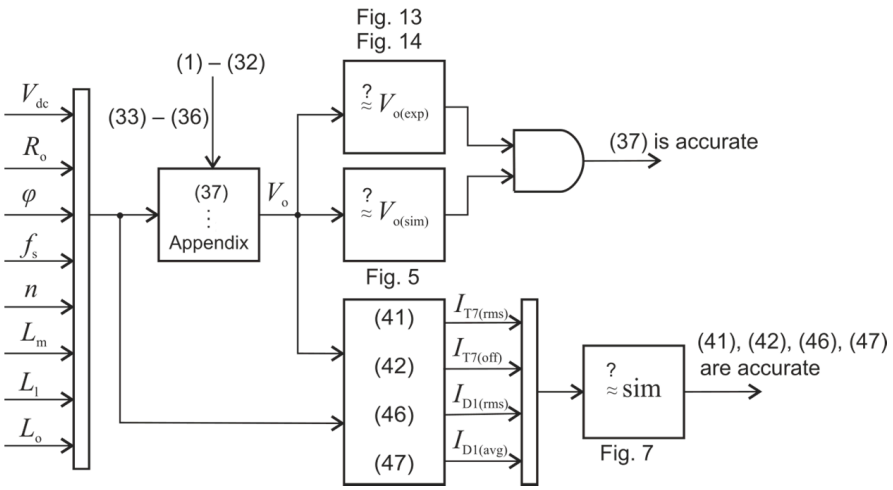


Figure 2. Verification process of the analytical model.

2. Materials and Methods

2.1. Topological Details

The two-stage charger with its topological details is shown in Figure 3a. The AFE consists of three input inductors (L_{AC}), six SiC MOSFETs (T_1–T_6), as well as a DC-link capacitor (C_{dc}). The PSFB consists of a transformer with turns ratio n and magnetizing inductance L_m, two inductors (L_l, L_o), four SiC MOSFETs (T_7–T_{10}), four SiC diodes (D_1–D_4), and two capacitors (C_{dc}', C_o). As depicted in Figure 3b, the AFE controller takes in six measurements (input currents i_b and i_c, input voltages v_a, v_b, and v_c, and the DC-link voltage v_{dc}) and provides six control signals (s_1–s_6). On the other hand, the PSFB controller requires one measurement (output voltage v_o) and provides four control signals (s_7–s_{10}). The role of the inductor L_l should be elaborated here: in certain operating conditions, its presence is not necessary. The converter can operate using only the energy accumulated in the magnetic field of the primary-side leakage inductance of the transformer to charge and discharge parasitic output capacitances of the switches [27,28]. However, at light-load high-voltage conditions that magnetic energy might be insufficient [29], and the result may be not only lower efficiency due to lack of zero-voltage switching but also the destruction of the transistors due to entering undesirable off-states, in which DC-link voltage is almost evenly divided between the high-side and the low-side switch.

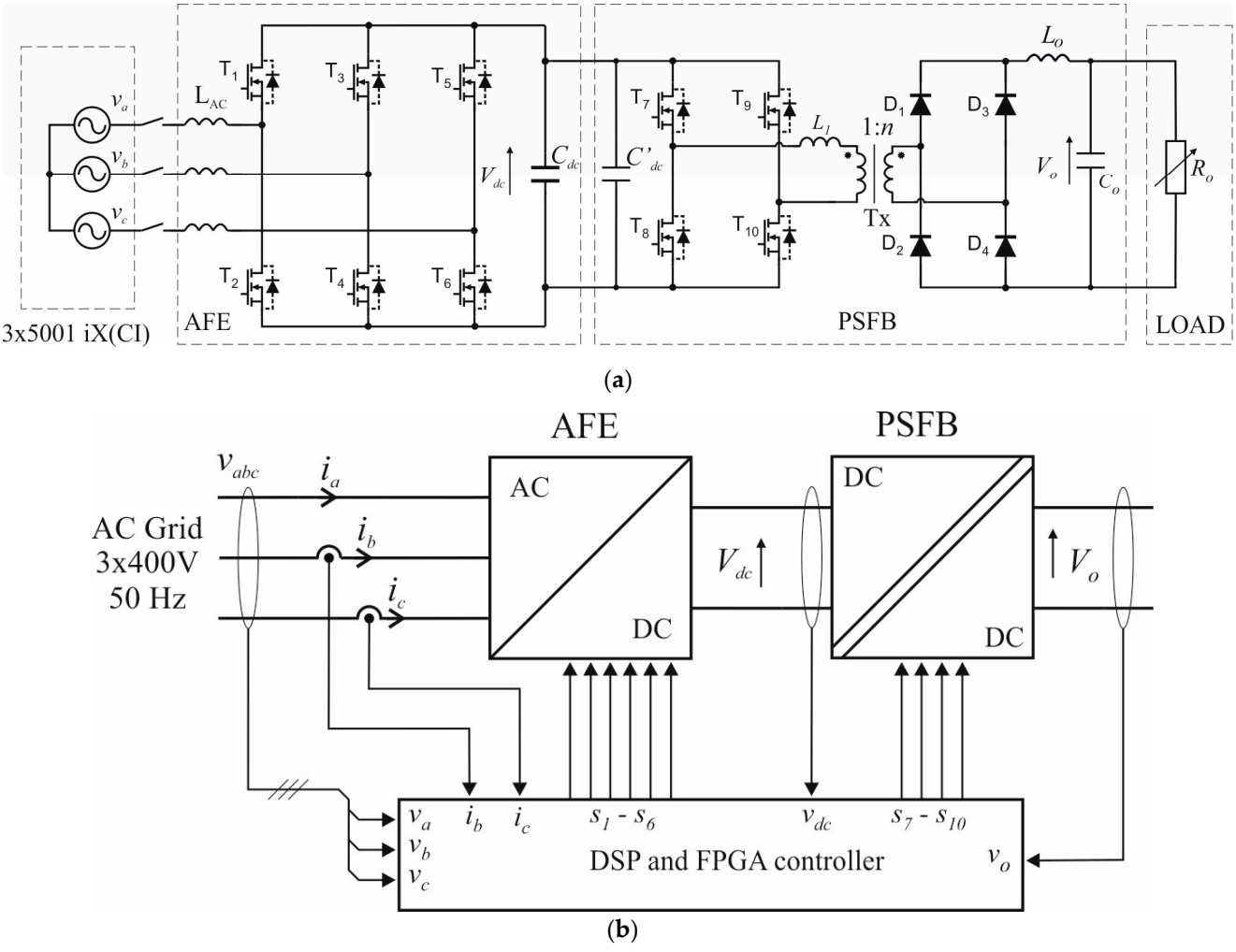


Figure 3. Schemes: (**a**) detailed, showing components; (**b**) generalized, with control and measurement signals.

2.2. Topology Analysis

The PSFB converter can be analyzed in the following way by means of averaging inductor voltage waveforms and the AC component of the output inductor current (capacitor current), and equating these averaged values to zero. Due to the multitude of significant parameters, all of which are interacting with each other, the entire derivation process takes a couple of pages. For clarity, only the initial analysis stage and the final results that can be readily implemented into a spreadsheet or other similar software are presented. It should be noted that the derived formula has a closed form, i.e., it contains only specification parameters that are provided to an engineer and design parameters that must be selected by the engineer. These parameters are DC-link voltage (V_{dc}), load resistance (R_o), phase shift ratio (φ), switching frequency (f_s), transformer turns ratio (n), magnetizing inductance (L_m), series inductance (L_l), and output filter inductance (L_o). These parameters can be observed throughout Figure 4.

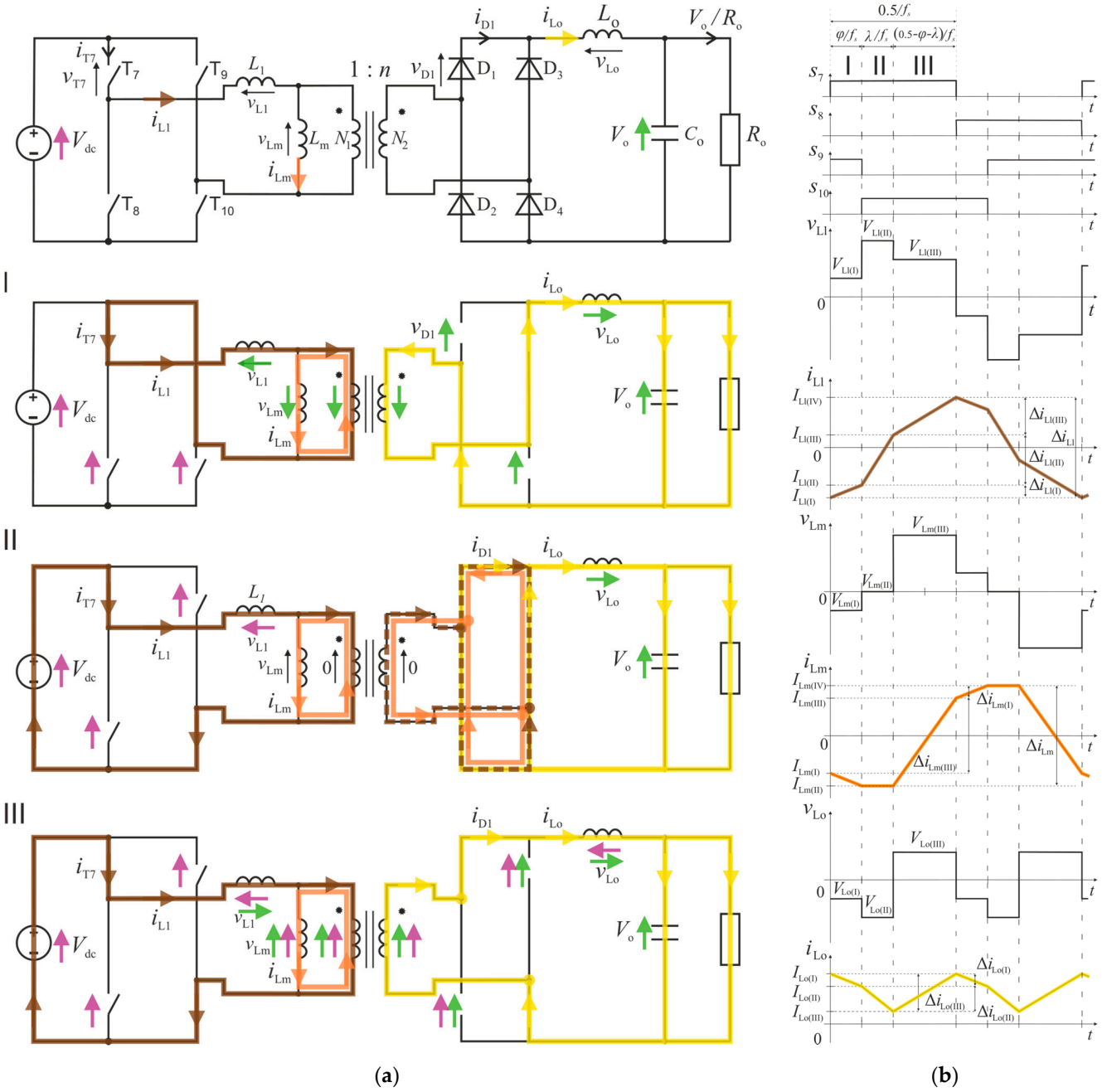


Figure 4. Analysis of PSFB operation: (**a**) independent states; (**b**) vital waveforms.

Figure 4a presents equivalent circuits of the PSFB in three main, independent states that can be reached (I–III). These states correspond directly to the control signal configurations (s_7–s_{10}) shown in Figure 4b, and have the total duration of half of the switching period $1/f_s$. Note that the remaining three states are not discussed here since inductor-related waveforms in the second half of the switching period are symmetrical to those in the first half. Furthermore, due to its relatively low value in SiC applications (c.a. 100 ns), deadtime is omitted, and additional states resulting from it are not considered.

2.2.1. State I Analysis

In state I (with duration of φ/f_s) it can be observed that there is no energy transfer from the DC-link to the load. Magnetic energy accumulated in various inductances is redistributed between these inductances and between them and the load. The exact nature of the energy flow is dictated by how voltage is shared among these inductances. Voltage V_o, which is kept constant by the output capacitor C_o, is divided between the transformer and the output inductor proportionally, as resulting from the inductance values and the turns ratio. It should be noted that, starting from (1), only the eight aforementioned design parameters are used, and, as in the case of (2), the previously defined expressions. Thereby, final expressions will also depend exclusively on the design parameters set. The levels of voltage applied during state I across inductances L_m ($V_{Lm(I)}$), L_l ($V_{Ll(I)}$), and L_o ($V_{Lo(I)}$) can be obtained in the following manner:

$$V_{Lm(I)} = -V_o \cdot \frac{n \cdot L_l \cdot L_m}{L_l \cdot L_m \cdot n^2 + L_o \cdot (L_l + L_m)} \tag{1}$$

$$V_{Ll(I)} = -V_{Lm(I)} \tag{2}$$

$$V_{Lo(I)} = -V_o \cdot \frac{L_o}{L_o + \frac{L_l \cdot L_m \cdot n^2}{L_l + L_m}} \tag{3}$$

Given the polarities of the voltage applied across the particular inductances, it can be inferred that in state I currents i_{Lm} and i_{Lo} decrease, while i_{Ll} increases. The changes in i_{Lm}, i_{Ll}, and i_{Lo} in this state are defined as $\Delta i_{Lm(I)}$, $\Delta i_{Ll(I)}$, and $\Delta i_{Lo(I)}$, respectively.

$$\Delta i_{Lm(I)} = \frac{-V_{Lm(I)}}{L_m} \cdot \frac{\varphi}{f_s} \tag{4}$$

$$\Delta i_{Ll(I)} = \frac{V_{Ll(I)}}{L_l} \cdot \frac{\varphi}{f_s} \tag{5}$$

$$\Delta i_{Lo(I)} = \frac{-V_{Lo(I)}}{L_o} \cdot \frac{\varphi}{f_s} \tag{6}$$

2.2.2. State II Analysis

Similar analysis can be undertaken for state II, which lasts for λ/f_s. Parameter λ is not directly set by the control signals, as in the case of φ, but it rather depends on a couple of parameters, including φ:

$$\lambda = L_o \cdot \frac{L_m \cdot (V_{dc} \cdot n \cdot (1 - 2 \cdot \varphi) - V_o) - L_l \cdot V_o}{2 \cdot L_m \cdot n \cdot (L_o \cdot V_{dc} + L_l \cdot V_o \cdot n)} \tag{7}$$

In state II there is still no energy flow between the DC-link source and the load since the voltage across the transformer windings equals zero. In this state, levels of voltage applied across inductances L_m, L_l, and L_o are defined as $V_{Lm(II)}$, $V_{Ll(II)}$, and $V_{Lo(II)}$, respectively.

$$V_{Lm(II)} = 0 \tag{8}$$

$$V_{Ll(II)} = V_{dc} \tag{9}$$

$$V_{Lo(II)} = -V_o \tag{10}$$

Considering the values and polarities of (8)–(10), it can be inferred that in state II current i_{Lm} does not change, i_{Ll} continues to increase, and i_{Lo} decreases. In this state,

absolute values of change in i_{Lm}, i_{Ll}, and i_{Lo} are defined as $\Delta i_{Lm(II)}$, $\Delta i_{Ll(II)}$, and $\Delta i_{Lo(II)}$, respectively.

$$\Delta i_{Lm(II)} = 0 \tag{11}$$

$$\Delta i_{Ll(II)} = \frac{V_{dc}}{L_l} \cdot \frac{\lambda}{f_s} \tag{12}$$

$$\Delta i_{Lo(II)} = \frac{V_o}{L_o} \cdot \frac{\lambda}{f_s} \tag{13}$$

2.2.3. State III Analysis

In state III energy flow between the DC-link source and the load takes place. This state has a duration of $(0.5 - \varphi - \lambda)/f_s$ and the voltage values across inductances L_m, L_l, and L_o are defined as $V_{Lm(III)}$, $V_{Ll(\mathrm{III})}$, and $V_{Lo(III)}$, respectively.

$$V_{Lm(III)} = L_m \cdot \frac{L_o \cdot V_{dc} + L_l \cdot V_o \cdot n}{L_l \cdot L_m \cdot n^2 + L_o \cdot (L_l + L_m)} \tag{14}$$

$$V_{Ll(III)} = V_{dc} - V_{Lm(III)} \tag{15}$$

$$V_{Lo(III)} = V_{Lm(III)} \cdot n - V_o \tag{16}$$

Given the voltage polarities of (14)–(16), it can be inferred that in state III currents i_{Lm}, i_{Ll}, and i_{Lo} all increase, as energy from the DC-link is accumulated in magnetic fields. In this state increments of i_{Lm}, i_{Ll}, and i_{Lo} are defined as $\Delta i_{Lm(III)}$, $\Delta i_{Ll(III)}$, and $\Delta i_{Lo(III)}$, respectively.

$$\Delta i_{Lm(III)} = \frac{V_{Lm(III)}}{L_m} \cdot \frac{0.5 - \varphi - \lambda}{f_s} \tag{17}$$

$$\Delta i_{Ll(III)} = \frac{V_{Ll(III)}}{L_l} \cdot \frac{0.5 - \varphi - \lambda}{f_s} \tag{18}$$

$$\Delta i_{Lo(III)} = \frac{V_{Lo(III)}}{L_o} \cdot \frac{0.5 - \varphi - \lambda}{f_s} \tag{19}$$

Note that the converter in Figure 4b operates in Continuous Conduction Mode (CCM). There is a CCM condition that must be met, which states that the Ripple Factor (RF) of the i_{Lo} current must satisfy the following condition:

$$RF = \frac{0.5 \cdot \Delta i_{Lo(III)} \cdot R_o}{V_o} \leq 1 \tag{20}$$

2.2.4. Derivation Results—Output Voltage Expression

Based on the current and voltage analysis in particular states, certain key inductance-current-related parameters can be obtained. As for inductance L_m, it is important to know the instantaneous current values at the beginning of state I ($I_{Lm(I)}$) and at the beginning of state II ($I_{Lm(II)}$). These values can be obtained based on the total increment of the magnetizing inductance current (Δi_{Lm}), calculated using partial increments from (4) and (17).

$$\Delta i_{Lm} = \Delta i_{Lm(I)} + \Delta i_{Lm(III)} \tag{21}$$

$$I_{Lm(II)} = -0.5 \cdot \Delta i_{Lm} \tag{22}$$

$$I_{Lm(I)} = I_{Lm(II)} + \Delta i_{Lm(I)} \tag{23}$$

For inductance L_l, on the other hand, it is instrumental to know the instantaneous values at the beginning of the first four states ($I_{Ll(I)}$, $I_{Ll(II)}$, $I_{Ll(III)}$, $I_{Ll(IV)}$). These parameters can be calculated based on the total current swing of the series-inductance current (Δi_{Ll}) and the partial increments obtained in (5), (12), and (18):

$$\Delta i_{Ll} = \Delta i_{Ll(I)} + \Delta i_{Ll(II)} + \Delta i_{Ll(III)} \tag{24}$$

$$I_{Ll(I)} = -0.5 \cdot \Delta i_{Ll} \tag{25}$$

$$I_{Ll(II)} = I_{Ll(I)} + \Delta i_{Ll(I)} \tag{26}$$

$$I_{Ll(III)} = I_{Ll(II)} + \Delta i_{Ll(II)} \tag{27}$$

$$I_{Ll(IV)} = -I_{Ll(I)} \tag{28}$$

To gain a full perspective, instantaneous values of i_{Lo} at the beginning of the first four states ($I_{Lo(I)}$, $I_{Lo(II)}$, $I_{Lo(III)}$, $I_{Lo(IV)}$) are also required. These can be calculated based on the design parameter n, instantaneous current values obtained in (23) and (25), and partial increments from (6) and (13).

$$I_{Lo(I)} = \frac{I_{Lm(I)} - I_{Ll(I)}}{n} \tag{29}$$

$$I_{Lo(II)} = I_{Lo(I)} - \Delta i_{Lo(I)} \tag{30}$$

$$I_{Lo(III)} = I_{Lo(II)} - \Delta i_{Lo(II)} \tag{31}$$

$$I_{Lo(IV)} = I_{Lo(I)} \tag{32}$$

Based on Formulas (1)–(32), a set of equations can be formulated, as shown below. These expressions equate to zero the average values of voltage across the inductances and the average value of current flowing into the output capacitor:

$$\int_0^{\frac{1}{f_s}} v_{Lm}(t)\, dt = 0 \tag{33}$$

$$\int_0^{\frac{1}{f_s}} v_{Ll}(t)\, dt = 0 \tag{34}$$

$$\int_0^{\frac{1}{f_s}} v_{Lo}(t)\, dt = 0 \tag{35}$$

$$\int_0^{\frac{1}{f_s}} \left(i_{Lo}(t) - \frac{V_o}{R_o} \right) dt = 0 \tag{36}$$

Upon solving (33)–(36), one obtains a formula that can be easily (although carefully) implemented in MATLAB- or Excel-type software to enable comprehensive data analysis without the need for simulation or an actual prototype.

$$V_o = V_{dc} \cdot \frac{\sqrt{m + p + c + d + e} - h - g - b}{z} \tag{37}$$

The expression (37) in its original form, just after solving (33)–(36), is an extensive formula that spans almost half of a page. To facilitate its implementation into MATLAB- or spreadsheet-based software, it has been carefully optimized for simplicity and divided into several less intricate parts. These are represented by nine auxiliary parameters—m, p, c, d, e, h, g, b, and z—and are elaborated on in Appendix A. Due to the level of complexity of the whole expression, it is necessary to confirm its correctness by means of simulation. This has been shown in Figure 5. The data set from Table 2 has been used to obtain these characteristics. It should be noted that throughout Figure 5, only one parameter out of eight presented in Table 2 is varied at the same time.

Table 2. Default parameters selected for verification of the Formula (37) for the PSFB converter.

Parameter	Symbol	Value
DC-link voltage	V_{dc}	800 V
Load resistance	R_o	21.125 Ω
Phase shift ratio	φ	1.43%
Switching frequency	f_s	25 kHz
Turns ratio	n	0.9
Magnetizing inductance	L_m	792 µH
Series inductance	L_l	14.15 µH
Output inductance	L_o	60 µH

The simulation and calculation results from Figure 5 confirm a 100% analytical accuracy of (37). What is more, the impact of each design parameter on the value of V_o is clearly shown. Especially noteworthy is the influence of f_s and L_l, since setting either of these values too high can greatly limit the available range of V_o. This can be, in turn, partially remedied by increasing n; however, such action would have its own downsides, as will be shown in the following subsection. It should also be kept in mind that aside from the first-order parameters listed in Table 2 and used in (37), there are many second-order

parasitic parameters present in any laboratory prototype. Their absence from (37) indicates that the accuracy of the laboratory experiments will be slightly lower than 100%.

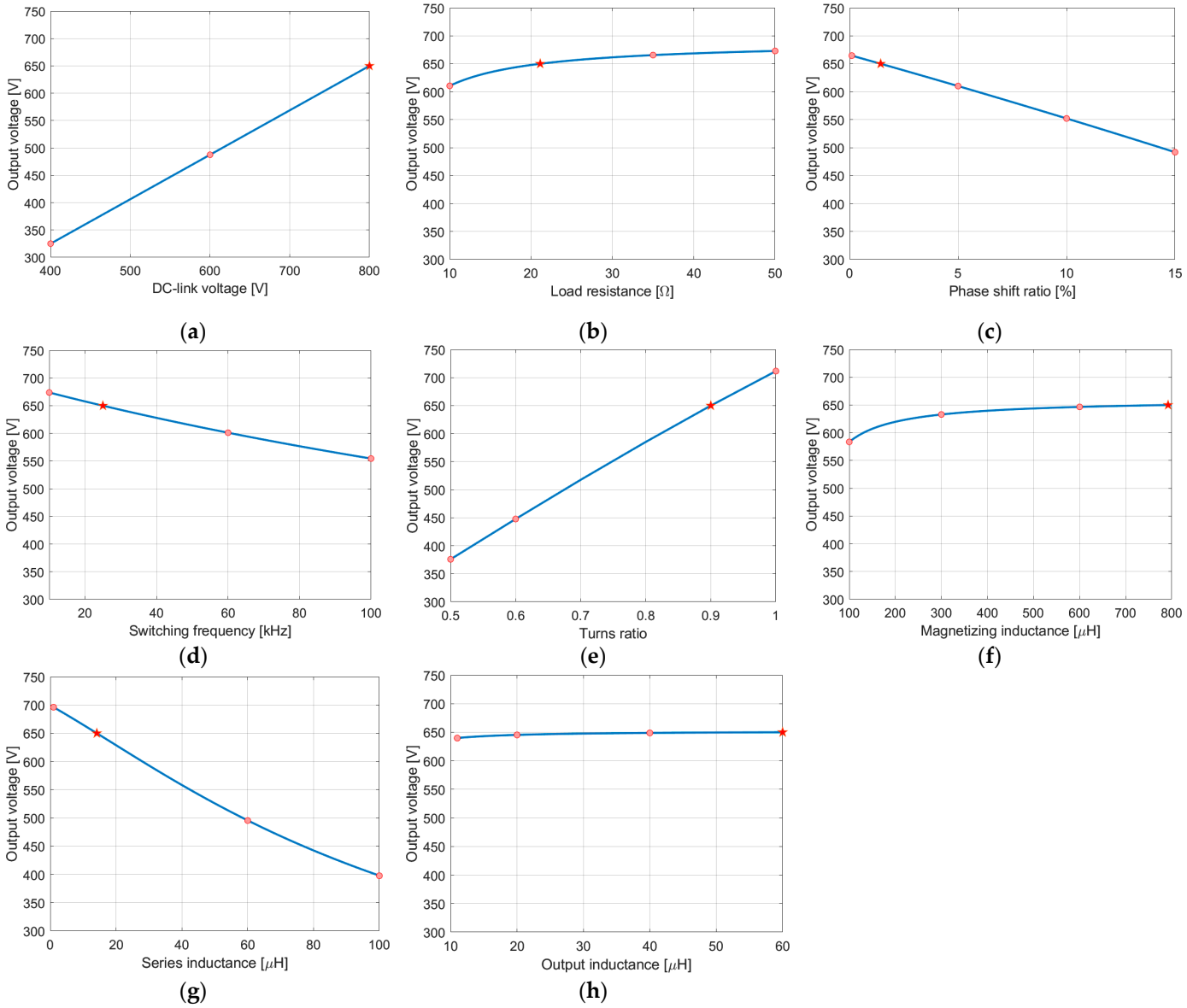


Figure 5. Output voltage calculation as a function of design parameters. Blue lines show the results according to Formula (37), PLECS simulation results for various parameters are in red, while results for selected parameters are symbolized by stars. The design parameters are: (**a**) V_{dc}; (**b**) R_o; (**c**) φ; (**d**) f_s; (**e**) n; (**f**) L_m; (**g**) L_l; (**h**) L_o.

2.2.5. Derivation Results—Semiconductor-Loss-Related Parameters

Having solved for the closed-form expression of the output voltage, all other vital waveform parameters of the system can be related to the initial set of design parameters. It is useful to be able to calculate semiconductor losses based only on the input design parameters. Due to the fact that semiconductor currents and voltages are not symmetrical between the first and the second half of the switching period, the circuit analysis must be complemented at this point by two additional states: IV and V (see Figure 6). Based on a full analysis that considers how particular semiconductor currents are composed of the given inductance currents in each state, loss-related current expressions can be developed for the transistors and the diodes using some auxiliary parameters. As for transistors, r_1, r_2, and r_3 can be calculated based on design parameter φ and (5), (7), (12), (18), and (25)–(28).

The actual rms value of the transistor, $I_{T7(rms)}$, can be obtained directly from r_1–r_3, while the turn-off instantaneous transistor current value $I_{T7(off)}$ is equal to (28).

$$r_1 = \varphi \cdot \frac{{I_{Ll(II)}}^3 - {I_{Ll(I)}}^3}{\Delta i_{Ll(I)}} \tag{38}$$

$$r_2 = \lambda \cdot \frac{{I_{Ll(III)}}^3 - {I_{Ll(II)}}^3}{\Delta i_{Ll(II)}} \tag{39}$$

$$r_3 = (0.5 - \varphi - \lambda) \cdot \frac{{I_{Ll(IV)}}^3 - {I_{Ll(III)}}^3}{\Delta i_{Ll(III)}} \tag{40}$$

$$I_{T7(rms)} = \sqrt{\frac{1}{3} \cdot (r_1 + r_2 + r_3)} \tag{41}$$

$$I_{T7(off)} = I_{Ll(IV)} \tag{42}$$

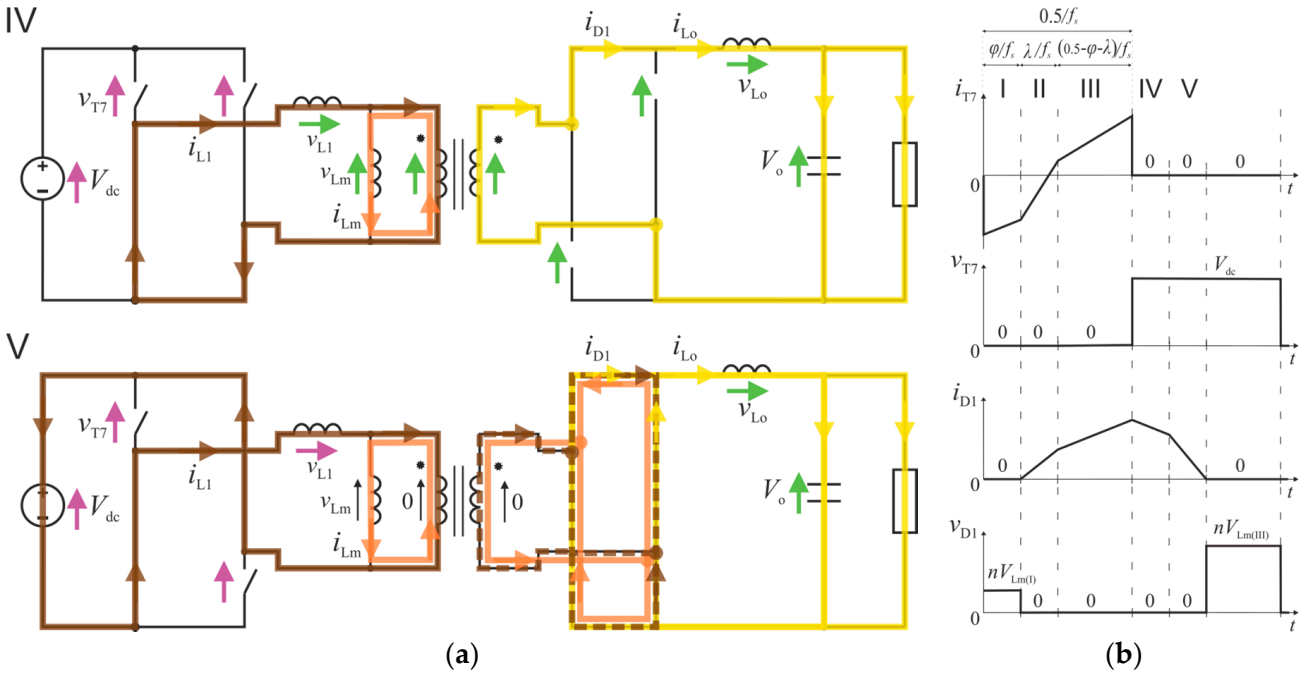


Figure 6. Analysis of PSFB operation continued: (**a**) independent states IV and V; (**b**) vital semiconductor waveforms.

Auxiliary parameters for the diode current rms ($I_{D1(rms)}$) calculation, q_1–q_3, can be obtained based on the design parameter φ and Formulas (6), (7), (19), and (30)–(32), while the average diode current value ($I_{D1(avg)}$) can be calculated using φ, (7), and (30)–(32).

$$q_1 = \varphi \cdot \frac{{I_{Lo(IV)}}^3 - {I_{Lo(II)}}^3}{\Delta i_{Lo(I)}} \tag{43}$$

$$q_2 = \lambda \cdot \left({I_{Lo(III)}}^2 + {I_{Lo(IV)}}^2 \right) \tag{44}$$

$$q_3 = (0.5 - \varphi - \lambda) \cdot \frac{{I_{Lo(IV)}}^3 - {I_{Lo(III)}}^3}{\Delta i_{Lo(III)}} \tag{45}$$

$$I_{D1(rms)} = \sqrt{\frac{1}{3} \cdot (q_1 + q_2 + q_3)} \tag{46}$$

$$I_{D1(avg)} = \frac{\varphi \cdot \left(I_{Lo(II)} - I_{Lo(III)} \right) + \lambda \cdot \left(I_{Lo(II)} - I_{Lo(IV)} \right) + 0.5 \cdot \left(I_{Lo(III)} - I_{Lo(IV)} \right)}{2} \tag{47}$$

Figure 7 shows the impact of design parameters from Table 2 on each of the four key semiconductor current parameters. With the PLECS simulation results superimposed on

the results of calculations using (41), (42), (46), and (47), it is confirmed that these formulas also are analytically correct.

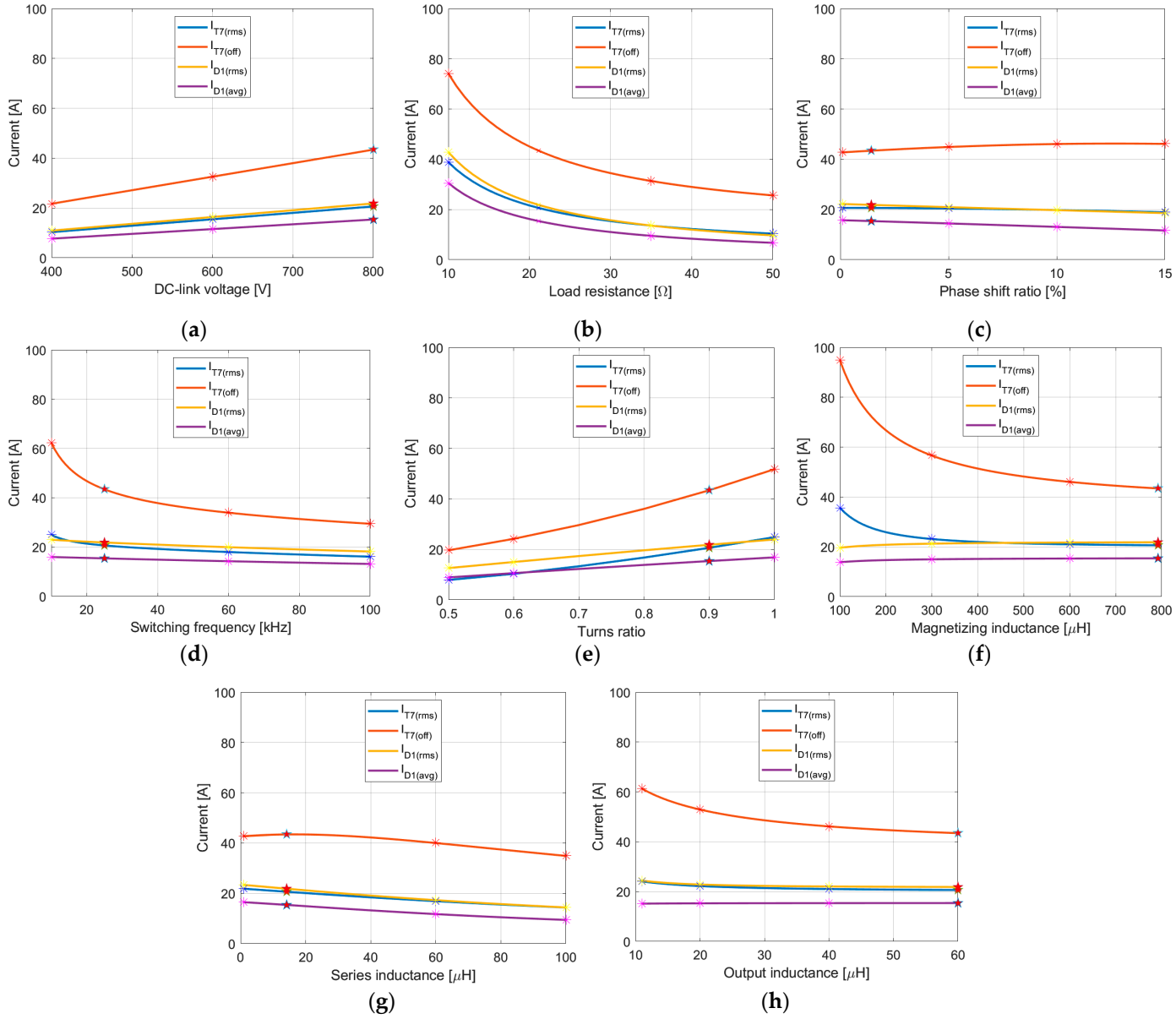


Figure 7. Semiconductor current parameters—Formulas (41), (42), (46), (47) shown as lines vs. PLECS simulation results shown as symbols. Varied design parameter: (**a**) V_{dc}; (**b**) R_o; (**c**) φ; (**d**) f_s; (**e**) n; (**f**) L_m; (**g**) L_l; (**h**) L_o.

Having confirmed the accuracy of (41), (42), (46), and (47), it is possible to calculate conduction and switching losses of the semiconductor devices. Considering that the diodes are based on SiC, their switching losses can be omitted. Similarly, due to the zero-voltage turn-on of the transistor (as shown in Figure 6b), turn-on losses can be omitted. Conduction power loss of a single MOSFET, $P_{T7(cond)}$, can be calculated based on the on-state resistance value of the transistor r_{T7} obtained from a datasheet and on (41). Switching power loss of a transistor, $P_{T7(sw)}$, can be calculated based on the switching frequency and on turn-off energy $E_{off\_T7}(I_{T7(off)}; V_{dc})$. It should be noted that using a datasheet, approximating functions should be used to calculate E_{off_T7} based on the switching current value (42) and the switching voltage value (V_{dc}). Such functions depend on the shapes of the characteristics in a datasheet and, in some cases, a first-order approximation can be assumed whereby the turn-off energy is linearly proportional to both the current and the voltage. As for the diode

conduction loss, $P_{D1(cond)}$, it can be obtained based on the piecewise linear approximation of forward characteristics from a datasheet, where $V_{D1(th)}$ is the threshold voltage and r_{D1} is the slope of the characteristic beyond the threshold. Often there is no need to manually extract the data from the characteristics as ready formulas are provided in the datasheet. Finally, total semiconductor losses $P_{loss(tot)}$ can be calculated by multiplying all the losses of single switches by the number of each type of switch—4.

$$P_{T7(cond)} = r_{T7} \cdot I_{T7(rms)}^{\ 2} \tag{48}$$

$$P_{T7(sw)} = f_s \cdot E_{off\_T7}\left(I_{T7(off)}; V_{dc}\right) \tag{49}$$

$$P_{D1(cond)} = V_{D1(th)} \cdot I_{D1(avg)} + r_{D1} \cdot I_{D1(rms)}^{\ 2} \tag{50}$$

$$P_{loss(tot)} = 4 \cdot \left(P_{T7(cond)} + P_{T7(sw)} + P_{D1(cond)}\right) \tag{51}$$

As a result, a full semiconductor loss parametrization can be obtained based simply on the initial set of eight design parameters. Sample results of loss calculations are shown in Figure 8. For these calculations, DC-link voltage, output voltage, and output power are kept constant. As a result of that, not all parameter configurations are allowed. For example, in Figure 8b to obtain V_o = 650 V at V_{dc} = 800 V and P_o = 10 kW one cannot use n lower than around 0.85, since at this point the required value of φ reaches 0% and it cannot decrease any further. On the other hand, one cannot use n higher than approximately 1.0, since above that value the circuit leaves the CCM. Operation in Discontinuous Conduction Mode (DCM) would lead to high output capacitor current stress and increased electromagnetic interference (EMI). This figure shows that the transformer turns ratio has the greatest impact on the total switching and conduction semiconductor losses; therefore, n should be kept as small as possible. On the other hand, too small values of L_m, L_l, and L_o as well as of f_s should be avoided to limit these losses.

$$T_{jT} = T_a + R_{th(hs)} \cdot P_{loss(tot)} + R_{th,j-c(T)} \cdot \left(P_{T7(cond)} + P_{T7(sw)}\right) \tag{52}$$

$$T_{jD} = T_a + R_{th(hs)} \cdot P_{loss(tot)} + R_{th,j-c(D)} \cdot P_{D1(cond)} \tag{53}$$

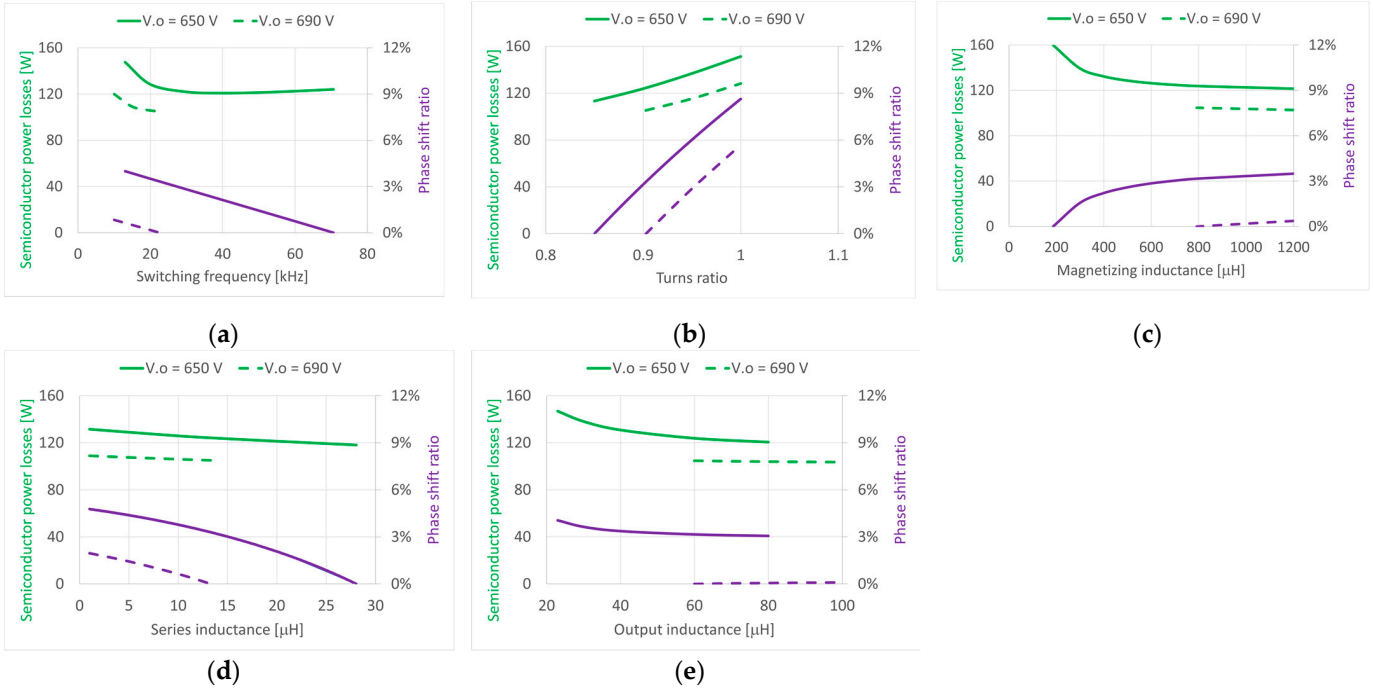


Figure 8. $P_{loss(tot)}$ (green) and φ (purple) at constant input and output parameters with V_{dc} = 800 V, V_o = 650 V / 690 V, P_o = 10 kW. Varied design parameters are: (**a**) f_s; (**b**) n; (**c**) L_m; (**d**) L_l; (**e**) L_o.

2.3. Control Scheme for Grid-Connected Operation

Upon having completed the analytical part, some consideration should be given to the closed-loop control structure of the prototypes, as shown in Figure 9. To properly operate in a grid-connected mode (or while working with a grid simulator), a robust PLL method must be applied for the AFE. In this case, a DSOGI-FLL [8] together with SRF-PLL is used, and a high level of disturbance rejection is reached. Aside from that, the inner decoupled current control loop in *dq* frame is applied with an outer DC-link voltage (v_{dc}) control loop, both PI-based. As for the PSFB, PI-based control of the output voltage (v_o) is implemented. A Phase-Shift Modulation (PSM) block is applied to delay control signals of the second phase-leg (s_9, s_{10}) with relation to the first phase-leg signals (s_7, s_8) by keeping the value of φ between 0 and 0.5 (see Figure 4b).

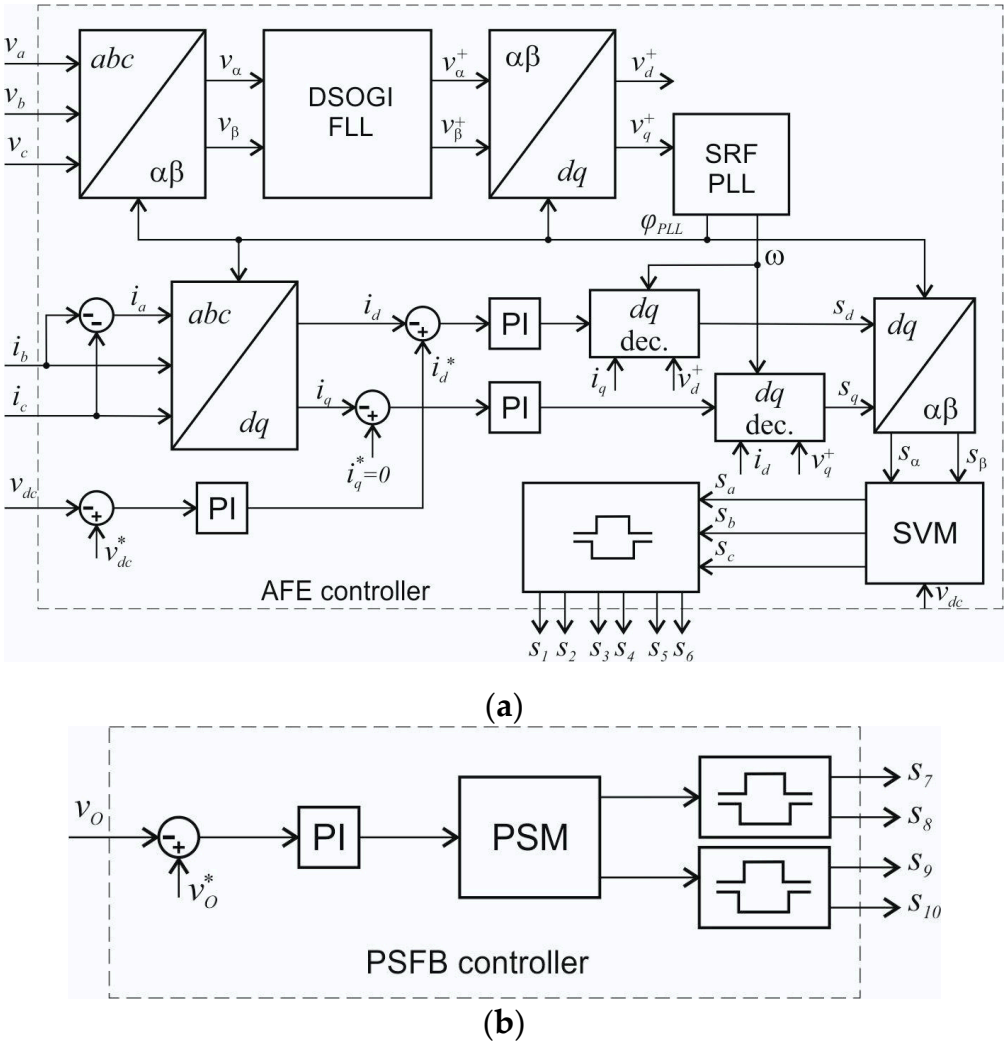


Figure 9. Control schemes of the charger stages: (**a**) AFE; (**b**) PSFB.

Control system parameters are shown in Table 3. The AFE control system was implemented using TMS320F28379D from Texas Instruments. The control algorithm presented in Figure 9a is realized in an interrupt at the frequency of 60 kHz, which is equivalent to the switching frequency of the AFE. At the beginning of the interrupt, measurement values from the Analog-Digital Converter (ADC) are read, including voltage (v_a, v_b, v_c, v_{dc}) and current (i_b, i_c) values. A doubled sampling frequency of 120 kHz was used to decrease control loop delay. As a result, the delay between the measurements and the control loop response equal to 1.5 times the control period was obtained. Three ADC channels were used to reduce measurement latency so that the total of six signals could be converted to

digital form during two ADC conversion cycles. Furthermore, each measurement channel features analogue low-pass filters with a cut-off frequency of around 300 kHz.

Table 3. Control system parameters.

	AFE	**PSFB**
Controller	TMS320F28379D DSP	10CL025 FPGA
Control frequency	60 kHz	25 kHz
Deadtime	100 ns	165 ns
ADC sampling	12 bit, 120 kS/s	12 bit, 250 kS/s
Resources used	CPU + CLA	~20k LE

AFE control software can be divided into two main parts: the control algorithm (as in Figure 9a) and the TMS320 hardware settings. In the second part, operations such as conditioning of measurement signals, protection, logging of the results, and updating of PWM duty cycle values take place. An initial approach of using only a single CPU core resulted in using up all the processing power and not being able to operate in a deterministic manner at the control frequency of 60 kHz. To circumvent that, the Control Law Accelerator (CLA) was chosen to operate in parallel with the CPU core. As a result, all the operations that the CPU could not handle in time were shifted to CLA, and the control frequency equal to the switching frequency became obtainable. Due to the high processing power required by the AFE control algorithm (advanced PLL, multiple Clarke and Park transformations and control loops), code optimization was necessary.

For the PSFB control system, an additional Field-Programmable Gate Array (FPGA) 10CL025 was selected due to versatility and simpler implementation of the PSM. It features 24,624 Logic Elements (LEs) and is clocked at the frequency of 200 MHz. Aside from the PSM, the closed-loop voltage control (as shown in Figure 9b) was implemented in the FPGA. Considering the selected control loop frequency of 25 kHz, the phase shift ratio φ in the time domain was varied in the range from 0 to 20 µs, and the control resolution of 5 ns was achieved. Implementation of the control algorithm took up around 20,000 LEs, which means that close to 80% of processing resources were used (without optimization of the logic structure). The PSFB control loop presented in Figure 9b was realized using an external, two-channel ADC, ADS7863, which features a sampling speed of 1 MS/s. A realization example of this type of converter has been discussed in [30].

3. Results

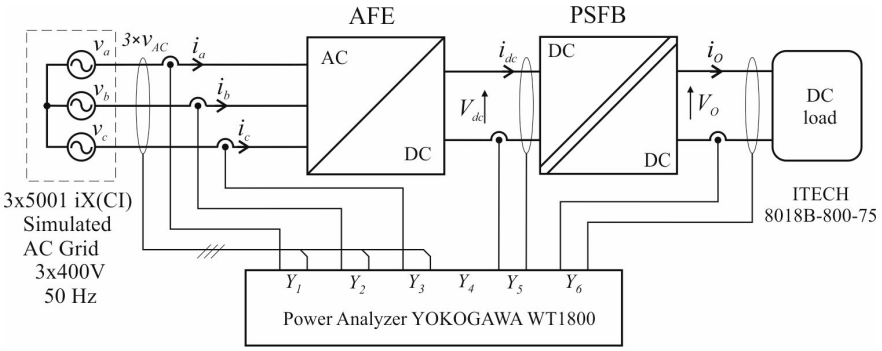
The main aims of the experiments were twofold: to verify the correctness of the Formula (37) and to confirm the proper operation of the control system presented in Figure 9. Components of the prototype are listed in Table 4. Transformer parameters were identified based on [31].

Table 4. Selected components of the AC–DC–DC charger prototype operating at V_{abc} = 3 × 400 V, V_{dc} = 600 V–800 V, P_o = 5 kW–10 kW, f_s = 25 kHz, $f_{s(\mathrm{AFE})}$ = 60 kHz.

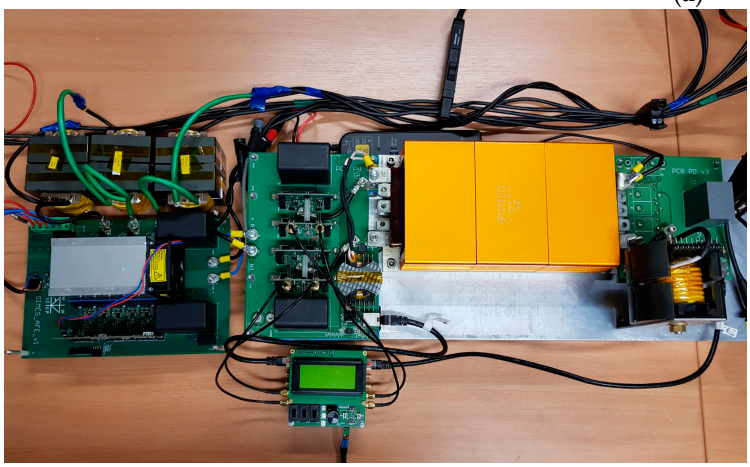
Component	**Parameter**	**Value**	**Model**
PSFB transformer	n	0.9	Payton T10000AC-9-10
	L_m	792 µH	
PSFB series inductor	L_l	14.15 µH (incl. transf. leak.)	Custom-made
PSFB output inductor	L_o	60 µH	Custom-made
AFE input inductors	L_{AC}	210 µH	Custom-made
AFE transistors	T_1–T_6	-	C3M0021120K
PSFB transistor	T_7–T_8	-	2 × SCTH100N120G2-AG
PSFB diodes	D_1–D_4	-	2 × STPSC20H12CWL

3.1. Laboratory Setup

The charger setup is powered by three modules of 5001 iX(C1) grid simulator connected in a star configuration. ITECH 8018B-800-75 is used as an active load to simulate a resistor of an accurately tunable resistance value. The device also allows programming sudden resistance changes, which is used in dynamic tests of the control system. As for measurements, the WT1800 power analyzer is connected at the input of AFE, between AFE and PSFB, and at the output of PSFB. This way, efficiencies of both power conversion stages can be measured separately. The connection scheme is shown in Figure 10a. Figure 10b, on the other hand, shows a photograph of the AFE connected with the PSFB. It should be noted that twisted wires go from AFE to the power analyzer and return to PSFB. AFE consists of a single power board with three external inductors, while PSFB is composed of a planar transformer, primary-side power board, and a separate secondary-side power board. Figure 10c presents the entire laboratory setup.



(**a**)



(**b**)

(**c**)

Figure 10. Laboratory setup: (**a**) connection scheme; (**b**) AFE (left side) with PSFB (right side); (**c**) entire experimental setup.

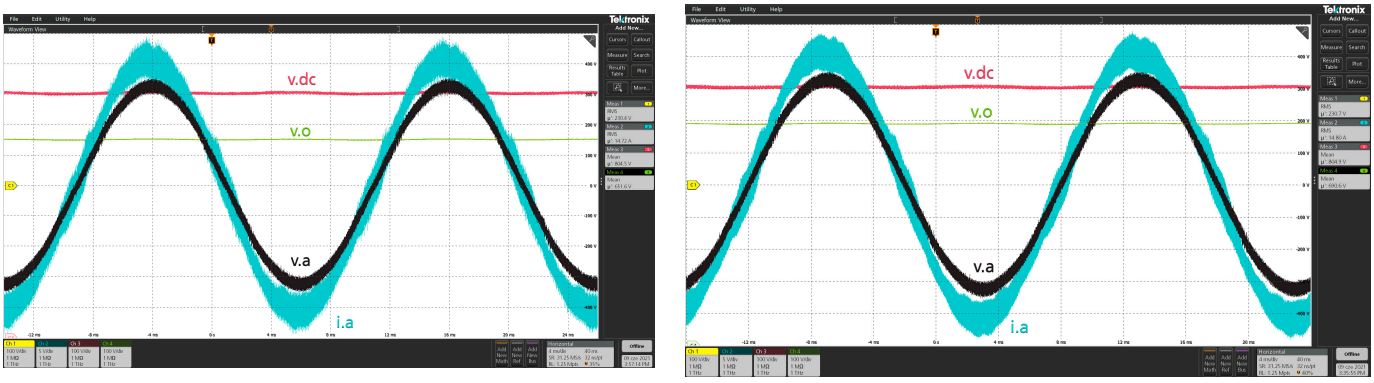
3.2. Laboratory Tests

Steady-State Operation

First, the charger was thoroughly tested in steady-state conditions at several DC-link voltage and output voltage levels as well as at a couple of power levels. Oscilloscope results from two points of operation are shown in Figure 11a,b. These waveforms prove proper PLL and current control operation of the AFE stage since AC current is in phase with AC voltage. Additionally, both the DC-link voltage v_{dc} and output voltage v_o are kept constant with the exception of some acceptable amount of ripple.

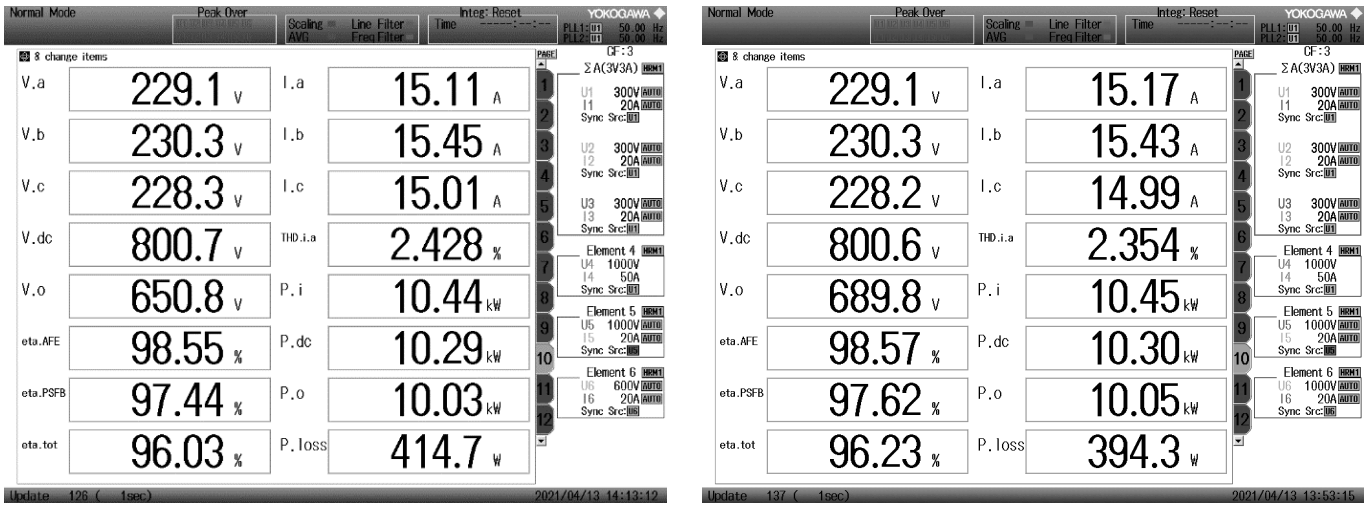
Figure 12a,b shows power analyzer results for two operating points. Based on the values of V_{dc} read from these screenshots, as well as from screenshots for all other operating points, V_o values were calculated with the Formula (37) and compared with V_o values

obtained from the power analyzer. Results were juxtaposed in the following figures. Figure 13 shows two modes in which the steady-state experiments were conducted: fixed output voltage mode and maximum output voltage mode. In the first one, the output voltage was fixed at a particular value, which meant that the device was operated with closed-loop voltage control, and the value of φ was varied at levels above zero. In the second mode, the PSFB was operated in the open loop with phase shift ratio φ equal to zero to obtain the highest possible value of output voltage V_o (see Figure 5c). It should be noted that the dots in Figure 13 correspond to the results obtained from the laboratory experiments, while the lines are values calculated using (37). Due to the parasitic resistances of the laboratory setup, the fitting cannot be ideal; however, the results predicted by the model are very close to the measured ones.



(**a**) (**b**)

Figure 11. Waveforms of the converter with voltage of phase a (v_a) in black, current of phase a (i_a) in light blue, DC-link voltage (v_{dc}) in red, and output voltage (v_o) in green at V_{dc} = 800 V, P_o = 10 kW and: (**a**) V_o = 650 V; (**b**) V_o = 690 V.



(**a**) (**b**)

Figure 12. Power analyzer measurements of the converter at V_{dc} = 800 V, P_o = 10 kW and: (**a**) V_o = 650 V; (**b**) V_o = 690 V.

The absolute error values are shown in Figure 14. Figure 14a,b demonstrates the high accuracy of the developed model, with absolute error values kept firmly below 1%. High nonlinearity is shown, which results from the complexities of this topology, as shown mathematically in the formula set in Appendix A.

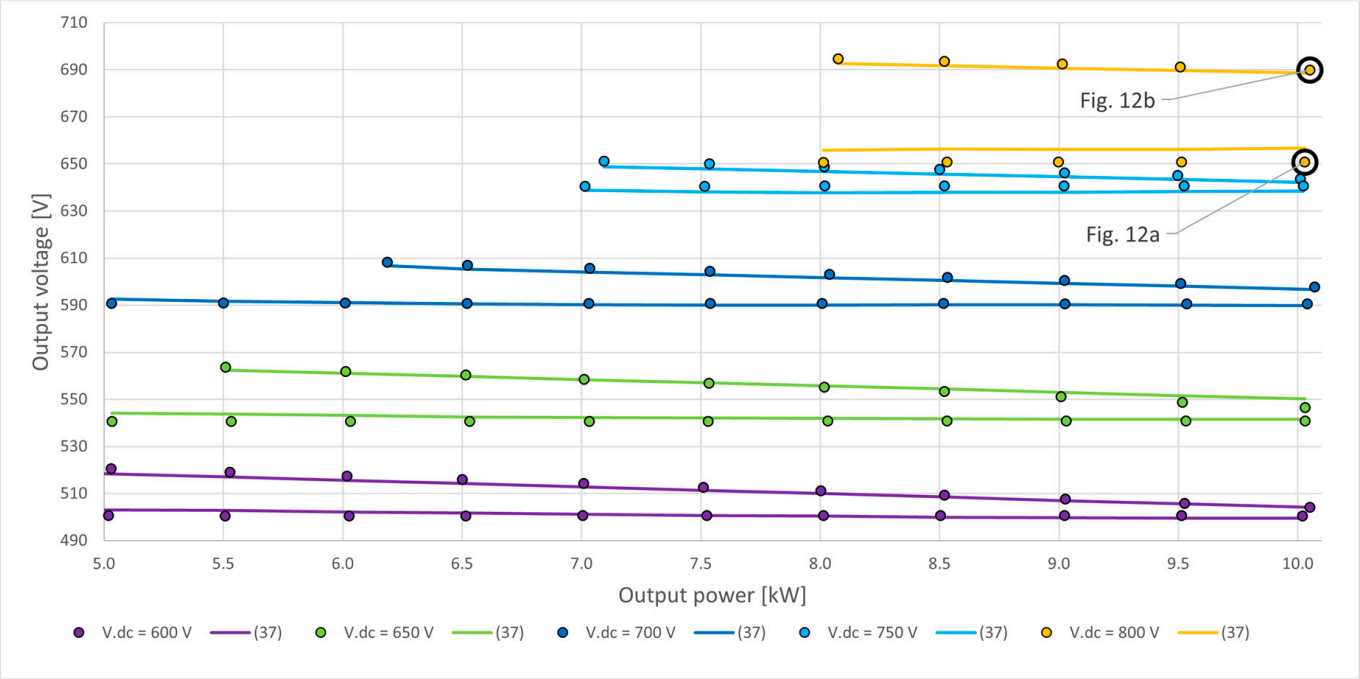
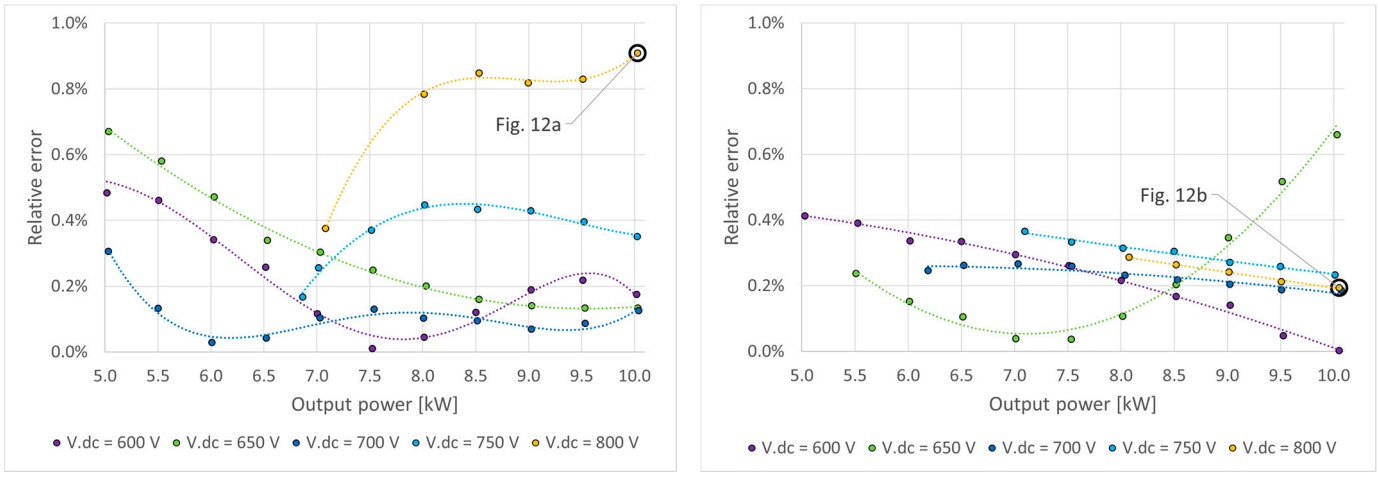


Figure 13. Output voltage as a function of output power in both examined modes—the fixed and the maximum output voltage mode. The symbols represent the experimental results, and the lines are obtained using Formula (37).



(**a**) (**b**)

Figure 14. Relative error of Formula (37) in both examined modes: (**a**) fixed output voltage; (**b**) maximum output voltage.

The non-zero error values in Figure 14 result from the omission of the second-order parasitic components of the laboratory prototype; however, the accuracy is deemed high enough. Aside from proving the correctness of the Formula (37), which includes all first-order design parameters, the efficiency of both stages was also measured at every operating point and in both measurement modes. Regarding the PSFB, from Figure 15a,b it can be inferred that for constant V_{dc} and P_o values, the higher is V_o, the lower are the losses. This conclusion is in line with the analytical results shown in Figure 8. On the other hand, the efficiency of the AFE in these two modes remains unchanged.

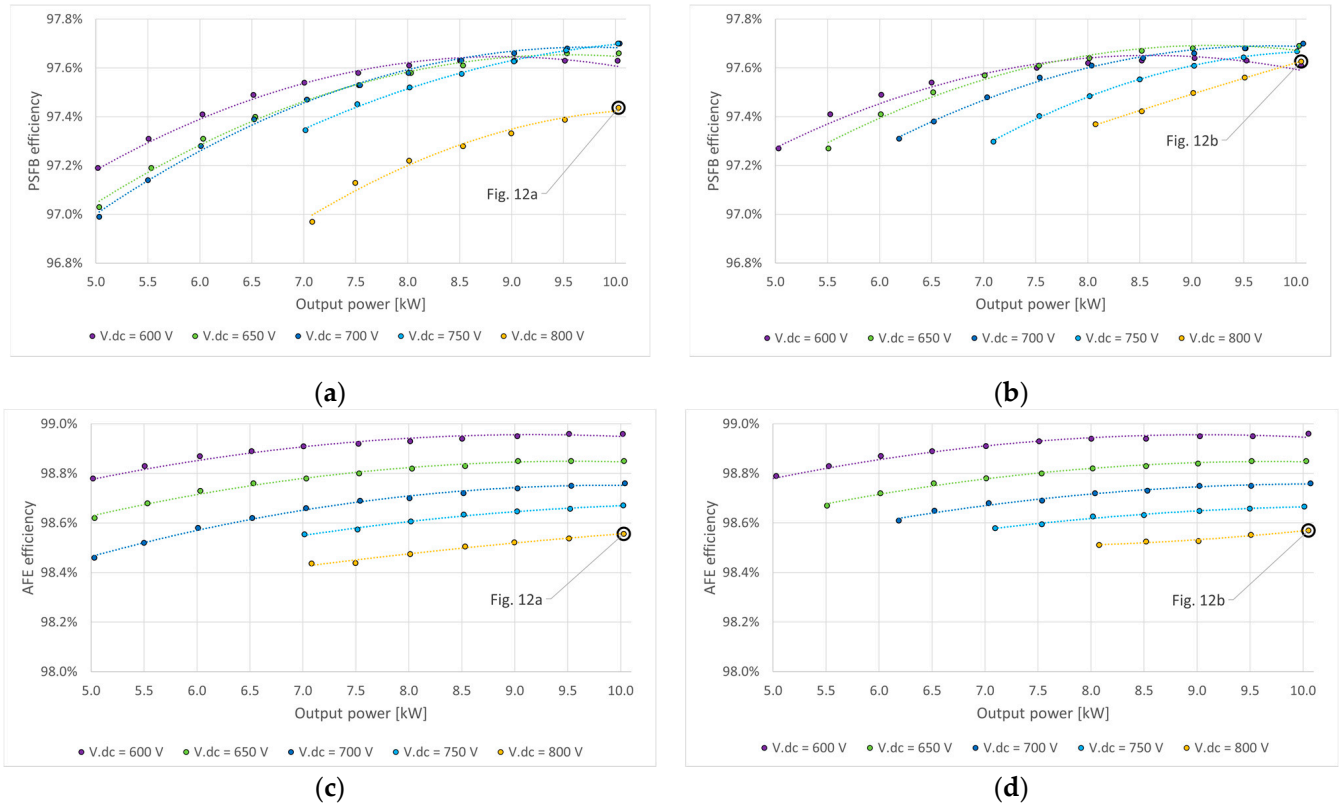


Figure 15. Efficiency characteristics of both stages in both modes: (**a**) PSFB in fixed output voltage mode; (**b**) PSFB in maximum output voltage mode; (**c**) AFE in fixed output voltage mode; (**d**) AFE in maximum output voltage mode.

3.3. The Design Procedure

Having confirmed the accuracy of the developed expressions using simulations and laboratory experiments, it is possible to create a design procedure based on this analytical model. The proposed process makes use of MATLAB environment and the Symbolic Math Toolbox for dealing with the complex formulas. The first and most important step is to import the Formulas (1)–(32), (37)–(53), and (A1)–(A33) into MATLAB. Using the Symbolic Math Toolbox parameters can be automatically substituted for other parameters and formulas can be solved for any parameter. Therefore, the Formula (37), which is of the form:

$$V_o = f(V_{dc}, R_o, \varphi, f_s, n, L_m, L_l, L_o) \tag{54}$$

can be automatically converted by MATLAB into the form that includes the output power P_o by substituting R_o with ${V_o}^2/P_o$:

$$V_o = f(V_{dc}, P_o, \varphi, f_s, n, L_m, L_l, L_o) \tag{55}$$

The only step missing at this point is to automatically solve (55) for the phase shift ratio φ and obtain:

$$\varphi = f(V_{dc}, P_o, V_o, f_s, n, L_m, L_l, L_o) \tag{56}$$

Please note that the automatic conversions eliminate the possibility of a human error, which exists only at the stage of implementing the Formulas (1)–(32), (37)–(53), and (A1)–(A33). Having the full set of formulas, the following design procedure, as shown in Figure 16, can be conducted. A single set of application requirements data is introduced. This set consists of electrical specification and thermal specification. The electrical part defines the desired DC-link voltage V_{dc}, output voltage V_o, output power P_o, and maximum allowable ripple factor $RF_{\max}$ of the output inductor current. The thermal part, on the other hand, provides the requirements regarding the operating ambient temperature T_a, and maximum allowable junction temperatures of the transistors ($T_{jT(max)}$) and the diodes ($T_{jD(max)}$).

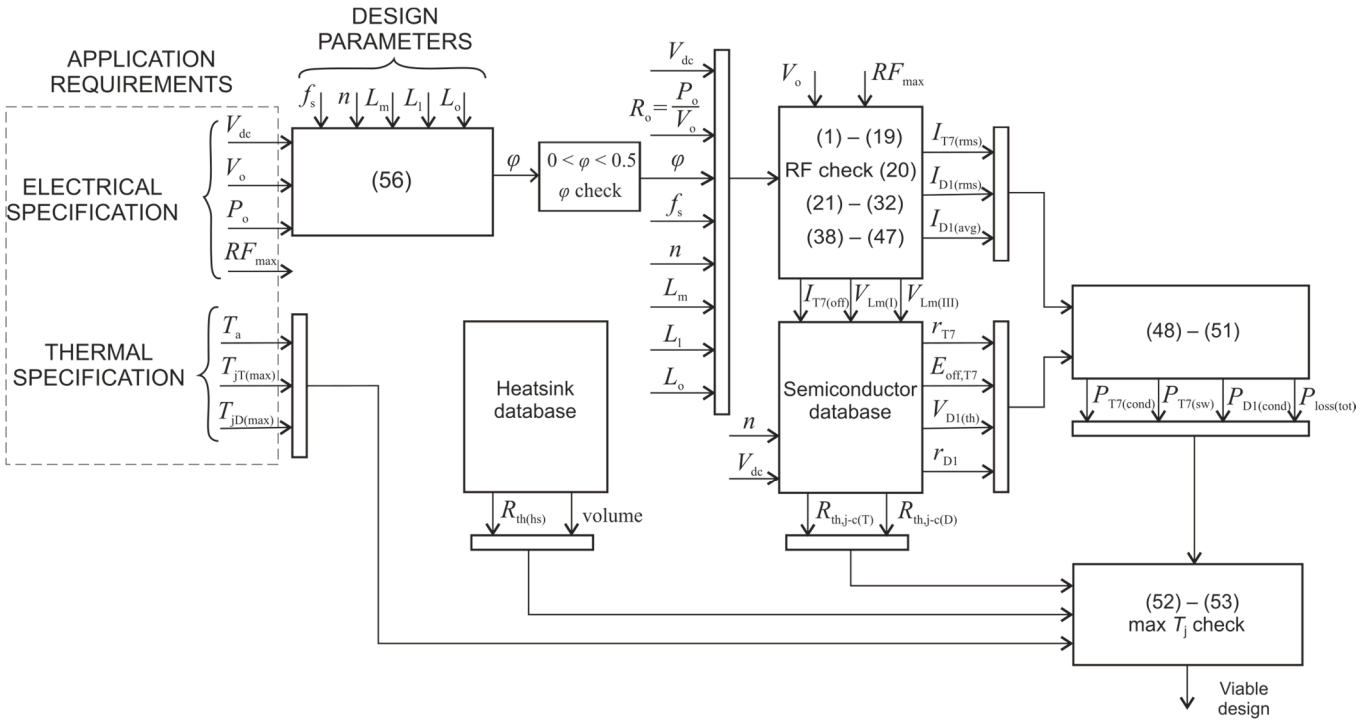


Figure 16. Design optimization approach for a PSFB-based converter.

To satisfy all of these application requirements, multiple design variants must be checked for viability and the most optimal one must be selected. Switching frequency f_s, turns ratio n, magnetizing inductance L_m, series inductance L_l, and output inductance L_o can be therefore provided in array forms with several values of each parameter in its particular array. The same is the case with the heatsink and the semiconductor database. As a result, the entire procedure is repeated as many times as there are unique combinations of each value of f_s, n, L_m, L_l, L_o, and each model of the heatsink, transistor, and diode. Throughout each iteration, first, φ is calculated using (55) and it is checked whether its value lies between 0 and 0.5. If it does not, then this iteration is stopped, and the next set of design parameters is loaded, restarting from (55). If φ is located in the range (0; 0.5), the phase shift ratio is used for further calculations using Formulas (1)–(19), after which the value of RF is obtained based on (20) and compared with $RF_{\max}$ from the application requirements. If RF is higher than $RF_{\max}$, the iteration is cancelled, and the next parameter set is selected. If RF is low enough, calculations (21)–(32) and (38)–(47) are conducted and the following values are obtained: $I_{T7(rms)}$, $I_{T7(off)}$, $I_{D1(rms)}$, $I_{D1(avg)}$, but also $V_{Lm(I)}$ and $V_{Lm(III)}$. Using values of voltages $V_{Lm(I)}$, $V_{Lm(III)}$, and also n, the diode database is restricted to only those diodes with a high enough breakdown voltage value. Formulas for this can be observed in the diode waveforms in Figure 6b. Similar exclusion of the lower-voltage transistors is conducted based on the value of V_{dc}. For the remaining diodes, the following values are imported from the database: threshold voltage $V_{D1(th)}$, dynamic resistance r_{D1}, and junction-case thermal resistance $R_{th,j\text{-}c(D)}$. For the remaining transistors, the following values are obtained: on-state resistance r_{T7}, switch-off energy E_{off_T7} (calculated using V_{dc} and $I_{T7(off)}$), and junction-case thermal resistance $R_{th,j\text{-}c(T)}$. Afterwards, calculations using Formulas (48)–(51) are conducted to obtain losses in each transistor and diode, as well as the total losses. Using the thermal specification from the application requirements, a component from the heatsink database, and the results obtained so far, calculations (52) and (53) are realised. If any of the maximum junction temperatures are exceeded (T_{jT} higher than $T_{jT(max)}$ or T_{jD} higher than $T_{jD(max)}$), the iteration stops and the next set of design parameters is considered, starting from (56). If the calculated temperatures are low enough, this particular design set is added to a viable design set and placed on a characteristic, such

as these shown in Figure 17. After all defined sets are analyzed and qualified as either viable or not viable, the characteristics are completed and a design is selected according to the desired priority, e.g., lowest semiconductor losses, smallest volume, or lowest cost. Such results are provided in Table 5, where the application requirements used are provided in the table caption and the results of the automatic selection are provided in the table body. For each power level, three optimization directions were taken, and the appropriate fields contain underlined values to show this. For example, for the 20-kW PSFB with the lowest cost in mind, one should opt for C3M0032120J1 SiC transistors, STPSC20H12C SiC diodes, and LA V 6 150 12 heatsink. In that case, the recommended series inductance L_l is 25 µH. This is almost the maximum inductance value that will allow obtaining V_o = 650 V for the given conditions, while minimizing the total losses (see Figure 8d). Of course, a more developed semiconductor and heatsink database could provide results that are even better than these. By comparing the results from Table 5 and Figure 17 it can be seen that the optimal designs are placed in the lower left corners of the characteristics.

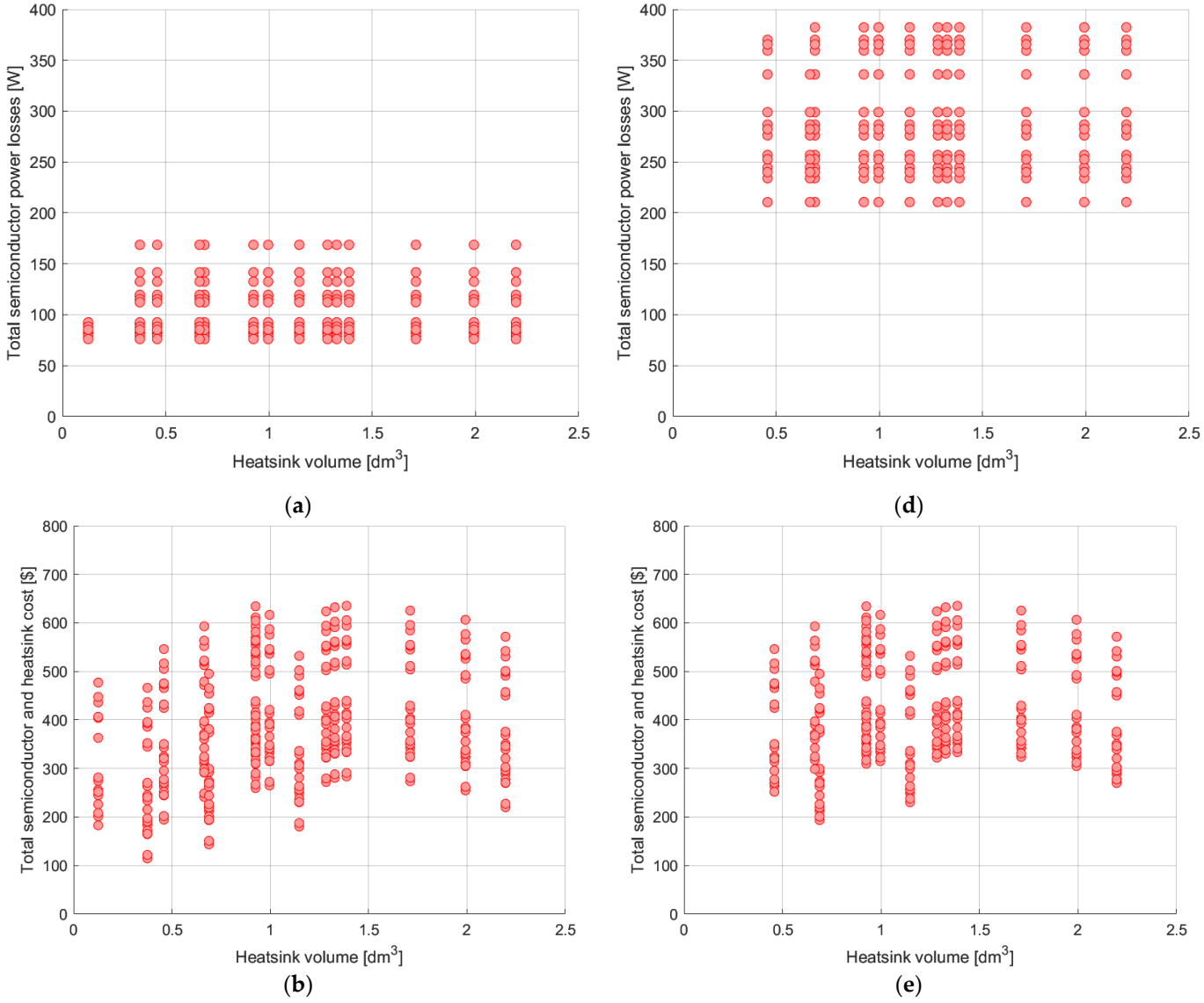


Figure 17. *Cont.*

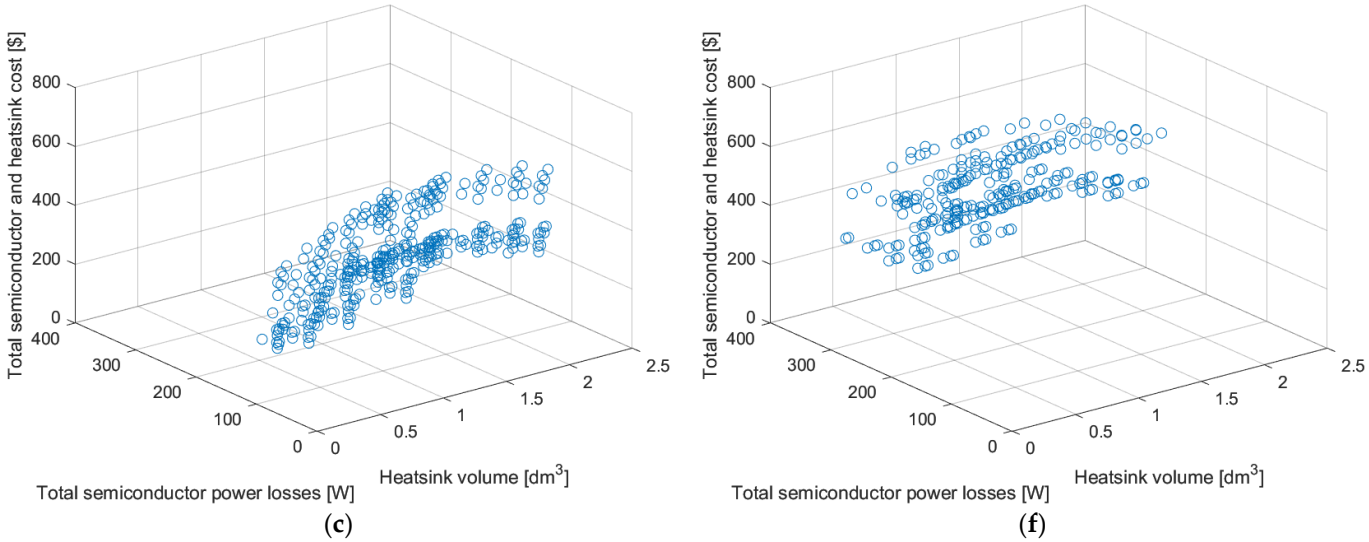


Figure 17. Sets of automatically generated designs using the developed analytical model and databases of various types of transistors, diodes, and heatsinks. The application requirements are V_{dc} = 800 V, V_o = 650 V, $RF_{\max}$ = 1, T_a = 25 °C, $T_{jT(max)}$ = 150 °C, $T_{jD(max)}$ = 150 °C, P_o = 10 kW: (**a**) losses vs. volume; (**b**) cost vs. volume; (**c**) cost vs. losses vs. volume; and P_o = 20 kW: (**d**) losses vs. volume; (**e**) cost vs. volume; (**f**) cost vs. losses vs. volume.

Table 5. Results of operation of the automated component selection tool for PSFB. The following specification requirements are assumed: V_{dc} = 800 V, V_o = 650 V, $RF_{\max}$ = 1, T_a = 25 °C, $T_{jT(max)}$ = 150 °C, $T_{jD(max)}$ = 150 °C, P_o = 10 kW / 20 kW.

P_o	Volume [dm^3]	Cost	$P_{loss(tot)}$ [W]	T_7–T_{10}	D_1–D_4	Heatsink	f_s [kHz]	n	L_m [mH]	L_l [µH]	L_o [µH]
10 kW	0.375	$115	169	C3M0120100K	STPSC20H12C	LAM 5 150 12	20	0.9	1.5	36	130
	0.375	$466	76	CAB011M12FM3	C4D40120D	LAM 5 150 12	20	0.9	1.5	36	130
	0.125	$183	92	C3M0032120J1	C4D15120H	LAM 5 50 12	20	0.9	1.5	36	130
20 kW	0.688	$193	382	C3M0032120J1	STPSC20H12C	LA V 6 150 12	20	0.9	1.5	25	130
	0.688	$495	211	CAB011M12FM3	C4D40120D	LA V 6 150 12	20	0.9	1.5	25	130
	0.459	$252	299	C3M0032120J1	C4D15120H	LA 6 100 12	20	0.9	1.5	25	130

4. Discussion

The results confirm correctness of the developed analytical model, both by simulation and by laboratory experiments. The automated design procedure based on this model provides the much-needed accuracy with regard to the design of high-power high-voltage converters based on the PSFB topology. This is a great alternative to conducting simulations at multiple parameter values and using many different semiconductor and heatsink models. Aside from a much higher speed of calculation of hundreds of variants, the MATLAB-based approach allows one to keep track of any desired value in any considered variant. This enables not only the selection of the lowest losses, or the smallest heatsink, but also the optimization of the design with regard to any other factor, such as cost or junction temperature. The developed design methodology can find application in all fields where a high-power, high-voltage, isolated topology such as PSFB can be used. Furthermore, not only AC–DC applications such as EV chargers can benefit from it—it can also be applied in DC–AC converters such as solar inverters with a DC–DC stage. In these cases, it is enough to keep in mind that parameter V_o, as referred to in this work, becomes the DC-link voltage, and parameter V_{dc} becomes the output voltage of the photovoltaic array. Proper definition of the transformer turns ratio should also be assumed, as shown in Figure 1b. In future work, magnetic design procedure could be incorporated into this method, including losses in those components. This would enable prediction of total volume of the converter in the same automated fashion. Nevertheless, the main point is that without an accurate

and verified formula such as (37), this sort of optimization of converters based on PSFB topology would not be possible.

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Appendix A

The expression (37) consists of one of the main design parameters, V_{dc}, and nine other parameters that are defined here: m, p, c, d, e, h, g, b, and z. As will be shown in the formulas below, all these parameters consist only of the remaining design parameters: R_o, φ, f_s, n, L_m, L_l, and L_o. As a result, the expression (37) is shown to consist exclusively of the main set of design parameters. First, let us define two auxiliary parameters: k_1 and k_2.

$$k_1 = 2 \cdot L_m \cdot n \tag{A1}$$

$$k_2 = \frac{R_o}{f_s} \tag{A2}$$

Based on (A1) and (A2), as well as on the design parameters, m_1–m_5 can be obtained, which leads to a simple calculation of m.

$$m_1 = {k_1}^4 \cdot n^4 \cdot \left(L_o \cdot (L_o + k_2 \cdot (\varphi \cdot (2 \cdot \varphi - 3) + 1)) + {k_2}^2 \cdot \varphi^2 \cdot (\varphi \cdot (\varphi - 1) + \frac{1}{4}) \right) \tag{A3}$$

$$m_2 = {k_1}^3 \cdot n^3 \cdot L_o \cdot \left(4 \cdot L_o \cdot (L_o + k_2 \cdot (\varphi \cdot (\varphi - 3) + \frac{5}{4})) + 2 \cdot {k_2}^2 \cdot \varphi \cdot (\varphi \cdot (1 - \varphi) - \frac{1}{4}) \right) \tag{A4}$$

$$m_3 = {k_1}^2 \cdot n^2 \cdot {L_o}^2 \cdot \left(4 \cdot L_o \cdot (L_o + 2 \cdot k_2 \cdot (1 - \frac{3}{2} \cdot \varphi)) + 3 \cdot {k_2}^2 \cdot (\varphi \cdot (\varphi - \frac{2}{3}) + \frac{1}{12}) \right) \tag{A5}$$

$$m_4 = k_1 \cdot n \cdot {L_o}^3 \cdot k_2 \cdot (4 \cdot L_o + k_2 \cdot (1 - 2 \cdot \varphi)) \tag{A6}$$

$$m_5 = {L_o}^4 \cdot {k_2}^2 \tag{A7}$$

$$m = (m_1 + m_2 + m_3 + m_4 + m_5) \cdot {L_l}^4 \tag{A8}$$

Using (A1)–(A2), a couple of design parameters and auxiliary parameters, p_1–p_4, p, is calculated in a straightforward manner.

$$p_1 = {k_1}^4 \cdot n^2 \cdot L_o \cdot \left(L_o \cdot (2 \cdot L_o + k_2 \cdot (2 \cdot \varphi \cdot (\varphi - 3) + \frac{5}{2})) - {k_2}^2 \cdot \varphi \cdot (\varphi \cdot (\varphi - 1) + \frac{1}{4}) \right) \tag{A9}$$

$$p_2 = {k_1}^3 \cdot n \cdot {L_o}^2 \cdot \left(4 \cdot L_o \cdot (L_o + k_2 \cdot (2 - 3 \cdot \varphi)) + {k_2}^2 \cdot (\varphi \cdot (3 \cdot \varphi - 2) + \frac{1}{4}) \right) \tag{A10}$$

$$p_3 = 3 \cdot {k_1}^2 \cdot {L_o}^3 \cdot k_2 \cdot \left(2 \cdot L_o + k_2 \cdot \left(\frac{1}{2} - \varphi \right) \right) \tag{A11}$$

$$p_4 = \frac{k_1 \cdot 2 \cdot {L_o}^4 \cdot {k_2}^2}{n} \tag{A12}$$

$$p = (p_1 + p_2 + p_3 + p_4) \cdot {L_l}^3 \tag{A13}$$

Parameter c can be obtained using three auxiliary parameters, c_1–c_3, the design parameters, and (A1)–(A2).

$$c_1 = {k_1}^4 \cdot {L_o}^2 \cdot \left(L_o \cdot (L_o + k_2 \cdot (2 - 3 \cdot \varphi)) + \frac{1}{2} \cdot {k_2}^2 \cdot (\varphi \cdot (\frac{3}{2} \cdot \varphi - 1) + \frac{1}{8}) \right) \tag{A14}$$

$$c_2 = 3 \cdot {k_1}^3 \cdot {L_o}^3 \cdot k_2 \cdot \frac{L_o + \frac{1}{2} \cdot k_2 \cdot \left(\frac{1}{2} - \varphi\right)}{n} \tag{A15}$$

$$c_3 = \frac{{k_1}^2 \cdot \frac{3}{2} \cdot {L_o}^4 \cdot {k_2}^2}{n^2} \tag{A16}$$

$$c = (c_1 + c_2 + c_3) \cdot {L_l}^2 \tag{A17}$$

Parameter d, required for the Formula (37), can be calculated based on two auxiliary parameters, d_1 and d_2, the design parameters, and (A1)–(A2).

$$d_1 = {k_1}^4 \cdot {L_o}^3 \cdot k_2 \cdot \frac{L_o + \frac{1}{2} \cdot k_2 \cdot \left(\frac{1}{2} - \varphi\right)}{2 \cdot n^2} \tag{A18}$$

$$d_2 = \frac{{k_1}^3 \cdot {L_o}^4 \cdot {k_2}^2}{2 \cdot n^3} \tag{A19}$$

$$d = (d_1 + d_2) \cdot L_l \tag{A20}$$

The final parameter inside of the square root of (37) is e, which can be calculated using two design parameters, (A1), and (A2).

$$e = \frac{{k_1}^4 \cdot {L_o}^4 \cdot {k_2}^2}{16 \cdot n^4} \tag{A21}$$

The first parameter outside of the square root of the Formula (37) is h, which can be obtained using auxiliary parameters h_1–h_3, the design parameters, and (A1)–(A2).

$$h_1 = {k_1}^2 \cdot n^2 \cdot \left(L_o + k_2 \cdot \varphi \cdot \left(\varphi - \frac{1}{2}\right)\right) \tag{A22}$$

$$h_2 = k_1 \cdot n \cdot L_o \cdot \left(2 \cdot L_o + k_2 \cdot \left(\frac{1}{2} - \varphi\right)\right) \tag{A23}$$

$$h_3 = {L_o}^2 \cdot k_2 \tag{A24}$$

$$h = (h_1 + h_2 + h_3) \cdot {L_l}^2 \tag{A25}$$

To obtain g, the penultimate parameter in the numerator of the Formula (37), the use of design parameters (A1), (A2) and two auxiliary parameters g_1 and g_2 is required.

$$g_1 = {k_1}^2 \cdot L_o \cdot \left(L_o + \frac{1}{2} \cdot k_2 \cdot \left(\frac{1}{2} - \varphi\right)\right) \tag{A26}$$

$$g_2 = \frac{k_1 \cdot {L_o}^2 \cdot k_2}{n} \tag{A27}$$

$$g = (g_1 + g_2) \cdot L_l \tag{A28}$$

Parameter b is the final one in the numerator of (37). It can be obtained simply by using (A1), (A2), and two of the design parameters.

$$b = \frac{{k_1}^2 \cdot {L_o}^2 \cdot k_2}{4 \cdot n^2} \tag{A29}$$

Parameter z belongs in the denominator of the Formula (37) and can be obtained based on (A1) and the design parameters, using auxiliary parameters z_1–z_3.

$$z_1 = \frac{L_l \cdot k_1 \cdot n}{2} \tag{A30}$$

$$z_2 = L_l \cdot L_o \tag{A31}$$

$$z_3 = \frac{k_1 \cdot L_o}{2 \cdot n} \tag{A32}$$

$$z = (z_1 + z_2 + z_3) \cdot 4 \cdot {L_l}^2 \cdot k_1 \cdot n^2 \tag{A33}$$

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