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Three-Level Unidirectional Rectifiers under Non-Unity Power Factor Operation and Unbalanced Split DC-Link Loading: Analytical and Experimental Assessment

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Abstract: Three-phase three-level unidirectional rectifiers are among the most adopted topologies for general active rectification, achieving an excellent compromise between cost, complexity and overall performance. The unidirectional nature of these rectifiers negatively affects their operation, e.g., distorting the input currents around the zero-crossings, limiting the maximum converter-side displacement power factor, reducing the split DC-link mid-point current capability and limiting the converter ability to compensate the low-frequency DC-link mid-point voltage oscillation. In particular, the rectifier operation under non-unity power factor and/or under constant zero-sequence voltage injection (i.e., when unbalanced split DC-link loading occurs) typically yields large and uncontrolled input current distortion, effectively limiting the acceptable operating region of the converter. Although high bandwidth current control loops and enhanced phase current sampling strategies may improve the rectifier input current distortion, especially at light load, these approaches lose effectiveness when significant phase-shift between voltage and current is required and/or a constant zero-sequence voltage must be injected. Therefore, this paper proposes a complete analysis and performance assessment of three-level unidirectional rectifiers under non-unity power factor operation and unbalanced split DC-link loading. First, the theoretical operating limits of the converter in terms of zero-sequence voltage, modulation index, power factor angle, maximum DC-link mid-point current and minimum DC-link mid-point charge ripple are derived. Leveraging the derived zero-sequence voltage limits, a unified carrier-based pulse-width modulation (PWM) approach enabling the undistorted operation of the rectifier in all feasible operating conditions is thus proposed. Moreover, novel analytical expressions defining the maximum rectifier mid-point current capability and the minimum peak-to-peak DC-link mid-point charge ripple as functions of both modulation index and power factor angle are derived, the latter enabling a straightforward sizing of the split DC-link capacitors. The theoretical analysis is verified on a 30 kW, 20 kHz T-type rectifier prototype, designed for electric vehicle ultra-fast battery charging. The input phase current distortion, the maximum mid-point current capability and the minimum mid-point charge ripple are experimentally assessed across all rectifier operating points, showing excellent performance and accurate agreement with the analytical predictions.

Keywords: grid-connected converter; three-level unidirectional rectifier; active front-end (AFE); power factor corrector (PFC); zero-sequence voltage; mid-point current; DC-link capacitor

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1. Introduction

Pulse-width modulated (PWM) active rectification is a fundamental requirement for the supply of modern high-power electrical systems, as it ensures lower distortion, higher performance and wider regulation capability with respect to passive and/or hybrid rectification solutions [1,2]. Typically, the supply of high-power loads from the three-phase grid is performed in two stages, as illustrated in Figure 1, the first being the rectifier or active front-end (AFE). The second conversion stage depends on the electrical system

being supplied, such as three-phase DC/AC inverters for variable-speed drives (VSDs) or uninterruptible power supplies (UPSs) (Figure 1a), isolated DC/DC converters for electric vehicle DC fast charging, telecommunication and data center power supplies, lighting systems or induction heating (Figure 1b), and non-isolated DC/DC converters for DC distribution systems, high-power DC loads or DC microgrids (Figure 1c).

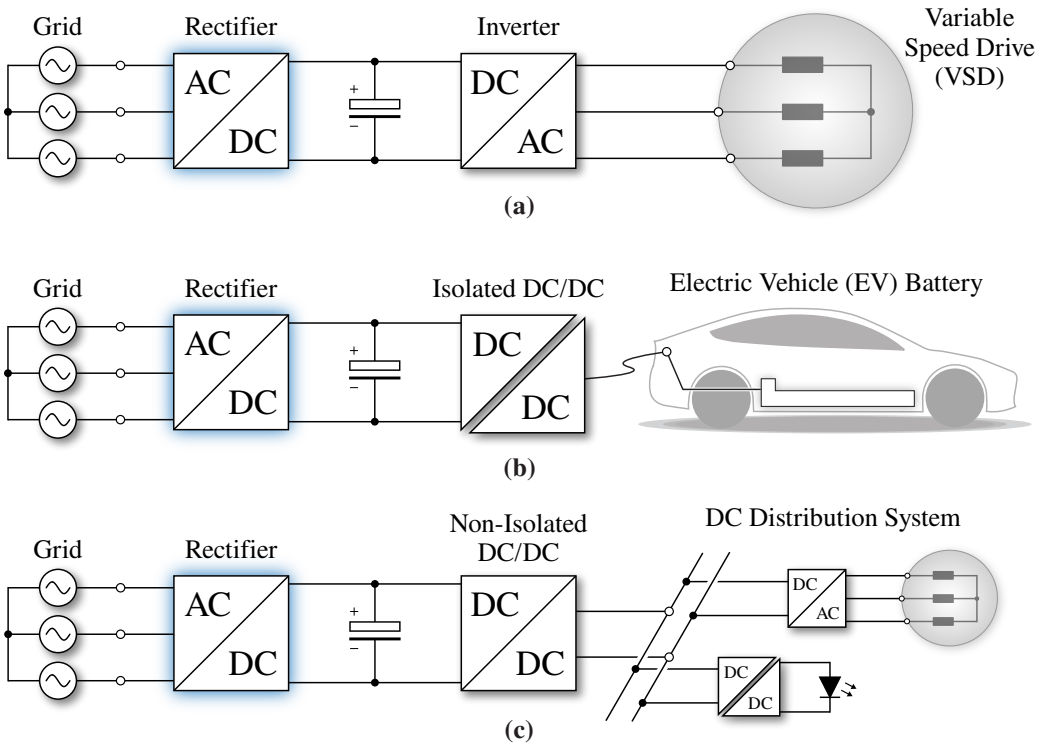

Figure 1. Schematic overview of typical grid-connected three-phase rectifier configurations supplying electrical loads such as (**a**) three-phase DC/AC inverters for variable-speed drives (VSDs) or uninterruptible power supplies (UPSs), (**b**) isolated DC/DC converters for electric vehicle DC fast charging, telecommunication and data center power supplies, lighting systems or induction heating, and (**c**) non-isolated DC/DC converters for DC distribution systems, high-power DC loads or DC microgrids.

General active rectification is typically performed by means of a conventional two-level inverter, due to its simplicity, robustness and intrinsic bidirectional capabilities. However, this topology has two major drawbacks, as it features a two-level output voltage waveform and requires semiconductor devices with relatively high voltage rating, both negatively affecting the converter losses and the grid-side filter size. Even though modern semiconductor technologies (e.g., high-voltage SiC MOSFETs) can substantially improve the two-level inverter performance by reducing losses and allowing for higher operating frequencies, multi-level converter solutions have demonstrated higher achievable performance, both in terms of efficiency and power density [3–5]. In fact, these topologies simultaneously reduce the stress on the AC-side filter components and allow the employment of semiconductor devices with lower voltage rating and thus better figures of merit [6].

When the power is only required to flow from the grid to the load, three-level unidirectional rectifiers represent perfect candidates for general active rectification [7–9]. In particular, these converter topologies trade higher efficiency and power density for a slight complexity increase, thus achieving improved performance with respect to conventional two-level inverters [3–5].

Besides high efficiency and high power density, the key requirements of a three-level rectifier can be summarized in (1) sinusoidal input current shaping, featuring low distortion and harmonics; (2) DC-link voltage regulation according to the desired reference value; and

(3) control of the DC-link mid-point voltage deviation under normal operating conditions (i.e., balanced split DC-link loading). Other desired features include, but are not limited to, (4) minimization of the DC-link mid-point third-harmonic voltage oscillation [8,10], which directly affects the size of the DC-link capacitors and may be hard to reject by the subsequent conversion stage [11]; (5) full control of the DC-link mid-point voltage deviation under unbalanced split DC-link loading [7], which may occur when separate DC/DC units are connected to the two DC-link halves (e.g., in DC fast chargers [12]); and (6) operation under non-unity power factor, to support the reactive energy flows in distribution grids [13]. All the aforementioned required and desired features can be addressed either with a proper converter control strategy (1)–(6) [14–16], with an accurate AC-side filter design (1) [17,18], or with an appropriate selection of the converter modulation strategy (4) [8,19]. In particular, (6) has not been explored in the literature and is increasingly becoming a desired feature of modern rectifiers, as distribution system operators (DSOs) are starting to charge end consumers for the injection/withdrawal of reactive energy into/from the grid [20]. If properly controlled, existing unidirectional rectifiers could in fact actively compensate this reactive power excess and/or substitute traditional power factor correction capacitor banks, benefiting the DSO and improving the system power quality.

The main challenges in achieving (1)–(6) are strictly related to the unidirectional nature of three-level rectifiers. One major issue is the discontinuous conduction mode (DCM) operation of the converter around the current zero-crossings, which, if not correctly addressed, can lead to unacceptable phase current distortion in light load conditions [21]. Moreover, unidirectional rectifiers are characterized by narrower operating limits with respect to their two-level and three-level bidirectional counterparts, mainly affecting the operation under non-unity power factor, the maximum DC-link mid-point current capability and the converter ability to compensate the low-frequency DC-link mid-point voltage oscillation. In particular, the rectifier operation under non-unity power factor and/or under constant zero-sequence voltage injection (i.e., when unbalanced split DC-link loading occurs) typically yields large and uncontrolled input current distortion, as reported in several previous works [22–27], practically limiting the acceptable operating region of the converter. Although high current control loop bandwidth and enhanced phase current sampling strategies may improve the rectifier input current distortion [16], especially in light load conditions, these approaches lose effectiveness when significant voltage-to-current phase-shift and/or zero-sequence voltage injection are required.

Mainly because of the aforementioned reason, several papers dealing with the analysis and the control of three-level unidirectional rectifiers under diverse operating conditions have been published in the literature [7–9,14,15,22–29].

In particular, [7–9] are the first papers analyzing the operational limits and the DC-link mid-point current capability of unidirectional three-level rectifiers, identifying a direct relation between the allocation of the converter redundant switching states (i.e., strictly related to the zero-sequence voltage injection) and the mid-point current generation process. Moreover, a preliminary attempt to control the DC-link mid-point voltage deviation is proposed in [9], acting on the zero-sequence current reference of a hysteresis current controller. However, no details on the operation of the rectifier with non-unity power factor are provided.

A detailed small-signal analysis of unidirectional three-level rectifiers is described in [14] and a complete multi-loop control strategy is proposed, enabling the accurate regulation of the DC-link mid-point voltage deviation. The same authors develop in [28] a carrier-based modulation strategy for three-level rectifiers based on the translation of conventional space vector dwell times into an equivalent zero-sequence duty-cycle injection. With this approach, the zero-sequence voltage limits of the converter are correctly taken into account, resulting in undistorted input currents under non-unity power factor operation and when a constant zero-sequence voltage is injected (i.e., to regulate the mid-point current). Nevertheless, the proposed implementation is quite complex, and no current distortion assessment is performed.

A direct carrier-based approach for undistorted operation under non-unity power factor is first proposed in [22]. This method is based on the addition of a zero-sequence voltage component to all bridge-leg voltage references, to make sure that the sign of the reference voltages is always equal to their respective phase currents. In fact, the unidirectional nature of the rectifier does not allow for the generation of a bridge-leg voltage with different sign as the current flowing in it. This approach, however, only solves the distortion issue for non-unity power factor operation (i.e., it has no general validity) and does not ensure sinusoidal operation when a constant zero-sequence voltage is injected.

In a similar way, [23–27,29] try to address the input phase current distortion deriving from non-unity power factor operation either by injecting a suitable zero-sequence voltage component for carrier-based approaches, or by correctly allocating the redundant switching states in space vector-based implementations. Nevertheless, none of these papers proposes a general and/or unified approach to ensure undistorted operation also under constant zero-sequence voltage injection.

Finally, a general methodology ensuring that the sign of the rectifier bridge-leg voltages remains equal to their respective phase currents in every operating condition is identified in [15]. This approach is based on the saturation of the reference zero-sequence voltage according to straightforward analytical relations and is theoretically able to ensure undistorted input current for both non-unity power factor operation and constant zero-sequence voltage injection. However, the converter distortion performances are not assessed and the effects of the zero-sequence voltage saturation on the DC-link mid-point current are not investigated.

As a further note, several considerations and analysis methods that have been specifically developed for three-level bidirectional inverters (e.g., to estimate and/or minimize the DC-link mid-point current and voltage oscillation [10,30–34], to control the DC-link mid-point voltage deviation with/without load unbalance [33,34], etc.) or the addition of an independent neutral module in four wire systems (i.e., to independently control the DC-link mid-point current in every operating condition [35,36]) have general validity and could thus be as well applied to three-level unidirectional rectifiers with minor modifications. Nevertheless, no additional and/or relevant elements with respect to the presented literature survey on unidirectional topologies has been identified.

Even though the operation and the control of three-level rectifiers have been thoroughly analyzed in the literature, according to the authors' best knowledge, a clear and complete analysis of the effects of non-unity power factor operation and constant zero-sequence voltage injection (i.e., operation under unbalanced split DC-link loading), has yet to be provided. In particular, no simple and unified carrier-based PWM approach ensuring undistorted operation of unidirectional rectifiers across their entire operating region has been proposed and verified experimentally. Moreover, no analytical expressions for the converter maximum DC-link mid-point current capability and minimum DC-link mid-point charge ripple for variable modulation index and power factor angle have been identified, forcing converter designers to make use of numerical and/or circuit simulations.

Therefore, this paper proposes a complete analysis of three-level unidirectional rectifiers under non-unity power factor operation and zero-sequence voltage injection, with the main goal of providing a simple and comprehensive overview of the rectifier limits and performance. The major contributions of this work are: (1) the adoption of a unified carrier-based PWM approach ensuring undistorted operation of the rectifier in every feasible operating condition (i.e., for variable power factor and variable zero-sequence voltage injection), based on the saturation of the zero-sequence voltage reference; (2) the analytical derivation of the DC-link mid-point current limits over the complete operating range of the rectifier; and (3) the analytical derivation of the minimum low-frequency (i.e., third-harmonic) mid-point peak-to-peak charge ripple for all feasible modulation index and power factor angle values. In particular, (3) allows the sizing of the split DC-link capacitors of three-level rectifiers with a straightforward analytical formula.

This paper is structured as follows. In Section 2 the operational basics of three-level unidirectional rectifiers are described and the converter limits in terms of zero-sequence voltage, modulation index, power factor angle, maximum DC-link mid-point current and minimum mid-point charge ripple are derived, leveraging the analytical approaches reported in Appendices A and B. In Section 3 the proposed analysis is verified experimentally on a digitally controlled 30 kW T-type converter prototype, assessing the input phase current distortion, the maximum mid-point current capability and the minimum mid-point charge ripple across all rectifier operating points. Finally, Section 4 summarizes and concludes this work.

2. Converter Operation and Limits

The structure of a three-level rectifier is schematically represented in Figure 2. The three-phase AC inputs are passively connected to the upper and lower DC-link rails through diodes (i.e., unidirectionally), while three bipolar/bidirectional 4-quadrant (4Q) switches actively connect them to the DC-link mid-point. In practice, the 4Q switch may be realized in different ways that are highlighted in Figure 2a–c [37], where switch implementations (b) and (c) may be also integrated within the diode bridge, thus requiring diodes with lower blocking voltage capability [1].

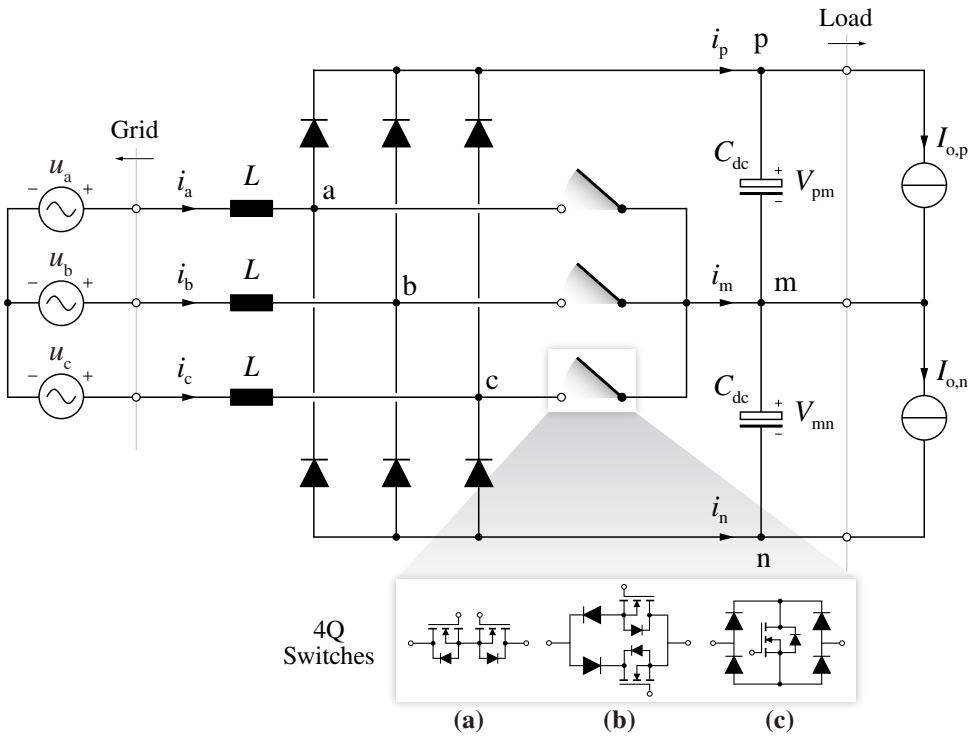

Figure 2. Schematic overview of a three-level rectifier connected to the three-phase grid. The mid-point switches must be bipolar and bidirectional, i.e., 4-quadrant (4Q). A highlight of the possible 4Q switch topologies is provided, namely (**a**) the T-type, (**b**) the NPC-type, and (**c**) the VIENNA-type: switches (**b**,**c**) can also be integrated inside the input diode bridge (see [9,37]).

To simplify the following analysis, the DC-side loads connected to the upper and lower DC-link halves are assumed as ideal current-sources, while no inner grid impedance and no AC-side filter are considered. It is worth noting that these simplifying assumptions do not affect the general validity of the following analysis.

2.1. Basics of Operation

The system state variables defining the converter operation are the boost inductor currents i_a, i_b, i_c and the DC-link capacitor voltages V_{pm}, V_{mn} (see Figure 2). Due to the three-phase three-wire nature of the system (i.e., $i_a + i_b + i_c = 0$), the total number of state

variables is reduced to four [16]. Moreover, the DC-link capacitor voltages V_{pm} and V_{mn} can be rearranged to define the DC-link voltage V_{dc} and the mid-point voltage deviation V_m, respectively

$$V_{dc} = V_{pm} + V_{mn}, \tag{1}$$

$$V_m = V_{pm} - V_{mn}. \tag{2}$$

It is worth noting that in normal operating conditions $V_m = 0$, assuming balanced split DC-link voltages $V_{pm} = V_{mn} = V_{dc}/2$.

Disregarding the voltage drop at fundamental frequency across the boost inductance L (i.e., negligible for converters with high pulse ratios [8]), the phase voltage local averages applied by the rectifier can be expressed as

$$\begin{cases} v_a \approx u_a = M \dfrac{V_{dc}}{2} \cos(\vartheta) \\ v_b \approx u_b = M \dfrac{V_{dc}}{2} \cos(\vartheta - \frac{2}{3}\pi) \\ v_c \approx u_c = M \dfrac{V_{dc}}{2} \cos(\vartheta - \frac{4}{3}\pi) \end{cases}, \tag{3}$$

where $\vartheta = \omega t = 2\pi f t$ is the phase angle, f is the grid frequency, $M = 2V/V_{dc}$ is the modulation index of the rectifier and V is the phase voltage peak value. For the sake of completeness, the phase voltages v_a, v_b, v_c can be represented with a space vector approach as

$$\vec{V} = \frac{2}{3}\left(v_a\, e^{j0} + v_b\, e^{j2\pi/3} + v_c\, e^{j4\pi/3}\right), \tag{4}$$

where j is the imaginary unit.

Neglecting the switching ripple, the controlled phase currents are sinusoidal and are therefore expressed by

$$\begin{cases} i_a = I \cos(\vartheta - \varphi) \\ i_b = I \cos(\vartheta - \frac{2}{3}\pi - \varphi) \\ i_c = I \cos(\vartheta - \frac{4}{3}\pi - \varphi) \end{cases}, \tag{5}$$

where I is the phase current peak value and φ is the converter-side power factor angle (i.e., $\varphi = \angle v_x - \angle i_x$ with x = a, b, c). As with the phase voltages, i_a, i_b, i_c can be expressed with an equivalent space vector representation as

$$\vec{I} = \frac{2}{3}\left(i_a\, e^{j0} + i_b\, e^{j2\pi/3} + i_c\, e^{j4\pi/3}\right). \tag{6}$$

Due to the structure of a three-level unidirectional rectifier, the AC terminal of each bridge-leg may be actively connected to the DC-link mid-point (switch in the ON state) or, depending on the phase current direction, passively connected to either the positive or negative DC-link rails (switch in the OFF state). Consequently, the voltage applied by each bridge-leg with respect to the DC-link mid-point can assume three different values (i.e., 0, $+V_{dc}/2$, $-V_{dc}/2$), which correspond to three separate switching states. Overall, the total number of switching state combinations of a three-phase three-level rectifier is theoretically $3^3 = 27$; however all three bridge-legs cannot be connected to the positive or negative DC-link rails at the same time due to the bridge diodes (i.e., $i_a + i_b + i_c = 0$), therefore the total number of states is reduced to 25. The total number of space vectors can be derived by observing that six space vectors are redundant, leading to total space vector number of $25 - 6 = 19$. An overview of the space vector diagram of a three-level rectifier is provided in Figure 3a.

Due to their unidirectional nature, three-level rectifiers cannot apply all 19 space vectors at any given time, as the feasible bridge-leg voltage values depend on the direction

of the phase currents. The 6 different phase current direction combinations (i.e., $2^3 - 2$, being $i_a + i_b + i_c = 0$) define 6 separate regions in the space vector diagram, referred to as current sectors in the following. When the current vector $\vec{I}$ transits through these regions, each bridge-leg can only apply two out of the three possible states, leading to a total of $2^3 = 8$ switching combinations. Therefore, the total number of allowed space vectors becomes 7, being 1 switching combination redundant. The 7 available voltage space vectors when $\vec{I}$ is located within current sector Ⓘ (i.e., $i_a > 0$, $i_b < 0$, $i_c < 0$) are illustrated in Figure 3b. The highlighted hexagon indicates that whatever voltage space vector $\vec{V}$ located inside the hexagon itself may be generated with a suitable combination of the 7 available space vectors.

It is worth noting that the required continuity of the voltage vector $\vec{V}$ when transitioning between neighboring sectors enforces a maximum angle between $\vec{V}$ and $\vec{I}$, depending on the modulation index M value. For instance, it is clear that $|\varphi| > \pi/6$ cannot be realized for any value of M, as the voltage vector $\vec{V}$ would temporarily fall out of the available space vector hexagon.

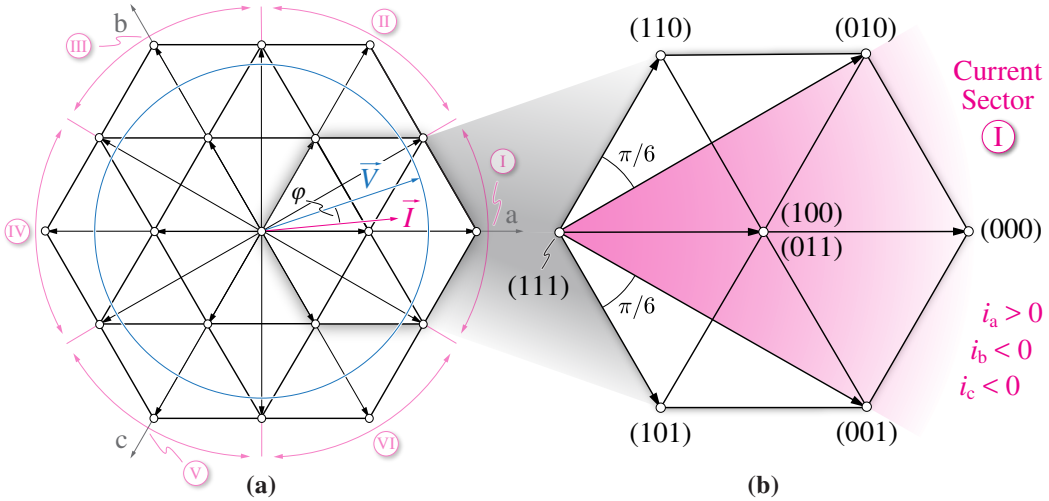

Figure 3. Complete space vector diagram of a three-phase three-level unidirectional rectifier. An overview of the 19 available space vectors, the 6 separate current sectors, the phase voltage vector $\vec{V}$, the phase current vector $\vec{I}$ and the converter-side power factor angle φ is shown in (**a**). A focus on the voltage space vector hexagon available when $\vec{I}$ is transiting inside current sector Ⓘ is provided in (**b**): the switching states are defined by the combination of the bridge-leg states, i.e., 0 when the 4Q switch is OFF and 1 when the 4Q switch is ON.

Even though the space vector representation allows identification of the three-level rectifier limits in terms of modulation index M and power factor angle φ by means of geometrical relations, a different approach based on the analysis of the time-domain waveforms is pursued in the following, achieving the same results as the space vector approach reported in [15].

2.1.1. AC-Side Voltage Formation

The local average of the bridge-leg voltages applied by the rectifier can be expressed as the sum of two contributions, namely the phase voltage component v_x and the zero-sequence voltage component v_o, as

$$v_{xm} = v_x + v_o \qquad x = a, b, c. \tag{7}$$

The phase voltages v_a, v_b, v_c are controlled to regulate the converter input currents i_a, i_b, i_c according to their reference sinusoidal values, being

$$\frac{di_x}{dt} = \frac{u_x - v_x}{L} \quad x = a, b, c. \tag{8}$$

As previously explained, because of the relatively low value of L in systems with high pulse ratio, the low-frequency voltage drop across the boost inductor can typically be neglected [8], such that $v_x \approx u_x$.

The zero-sequence component v_o is defined as the average of the three bridge-leg voltages, i.e.,

$$v_o = \frac{v_{am} + v_{bm} + v_{cm}}{3}. \tag{9}$$

Even though v_o has no effects on the phase current generation process in a three-phase three-wire system, it defines the modulation strategy of the rectifier [19] and may be leveraged to regulate the DC-link mid-point current [16], as demonstrated in Section 2.1.2.

2.1.2. DC-Side Current Generation

The three DC-link rail currents i_p, i_m, i_n indicated in Figure 2 are bounded by the following relation:

$$i_p + i_m + i_n = 0, \tag{10}$$

due to the three-wire nature of the DC-link.

In particular, i_p and i_n are linked to the total power transfer of the rectifier, being

$$P = v_a\, i_a + v_b\, i_b + v_c\, i_c = V_{pm}\, i_p - V_{mn}\, i_n \approx \frac{1}{2}\, V_{dc}\, (i_p - i_n), \tag{11}$$

where balanced split DC-link voltages (i.e., $V_{pm} = V_{mn} = V_{dc}/2$) have been assumed.

The generation process of the DC-link mid-point current i_m is slightly more complicated and has been investigated in several past works [7,10,14]. The main driver of i_m is the zero-sequence voltage component v_o injected by the converter. Even though this component does not affect the phase currents, it modifies the duty cycles τ_a, τ_b, τ_c of the mid-point 4Q switches, which in turn affect the mid-point current local average value, namely

$$i_m = \tau_a\, i_a + \tau_b\, i_b + \tau_c\, i_c. \tag{12}$$

The values of τ_a, τ_b, τ_c are determined by the ratio between their respective reference bridge-leg voltages v_{xm} and the DC-link voltage V_{dc} as

$$\tau_x = 1 - \frac{2}{V_{dc}}\, |v_{xm}| = 1 - \frac{2}{V_{dc}}\, |v_x + v_o| \qquad x = a, b, c. \tag{13}$$

Leveraging the three-phase three-wire nature of the system (i.e., $i_a + i_b + i_c = 0$) and substituting (13) into (12), the expression of the mid-point current local average becomes

$$i_m = \sum_{x\,=\,a,\,b,\,c} \left(i_x - \frac{2}{V_{dc}} |v_x + v_o|\, i_x \right) = \sum_{x\,=\,a,\,b,\,c} -\frac{2}{V_{dc}} |v_x + v_o|\, i_x. \tag{14}$$

A simplified version of (14) can be obtained by recalling that the bridge-leg voltages applied by a three-level unidirectional rectifier can only have the same sign as their respective phase currents (i.e., $v_{xm} \geq 0$ when $i_x > 0$ and $v_{xm} \leq 0$ when $i_x < 0$). Therefore, the following relation can be derived:

$$|v_{xm}|\, i_x = |v_x + v_o|\, i_x = (v_x + v_o)\, |i_x| \quad x = a, b, c, \tag{15}$$

which is then substituted into (14) obtaining

$$i_{\mathrm{m}} = \sum_{\mathrm{x=a,b,c}} -\frac{2}{V_{\mathrm{dc}}}(v_{\mathrm{x}} + v_{\mathrm{o}})\,|i_{\mathrm{x}}| = -\frac{2}{V_{\mathrm{dc}}}\left[\sum_{\mathrm{x=a,b,c}} v_{\mathrm{x}}\,|i_{\mathrm{x}}| + v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}|\right]. \tag{16}$$

To assess the ability of the rectifier to work with unbalanced split DC-link loading (i.e., $I_{\mathrm{o,p}} \neq I_{\mathrm{o,n}}$ in Figure 2), the expression of the mid-point current periodical average I_{m} is of particular interest. This is obtained by averaging the value of i_{m} over $2\pi/3$ (i.e., the DC-side current periodicity), as

$$I_{\mathrm{m}} = \frac{3}{2\pi}\int_0^{2\pi/3} i_{\mathrm{m}}\,\mathrm{d}\vartheta = -\frac{3}{\pi\,V_{\mathrm{dc}}}\int_0^{2\pi/3}\left[\sum_{\mathrm{x=a,b,c}} v_{\mathrm{x}}\,|i_{\mathrm{x}}| + v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}|\right]\mathrm{d}\vartheta. \tag{17}$$

Since the first term to be integrated is characterized by $2\pi/3$ periodicity, its integral is null, therefore (17) becomes

$$I_{\mathrm{m}} = -\frac{3}{\pi\,V_{\mathrm{dc}}}\int_0^{2\pi/3} v_{\mathrm{o}} \sum_{\mathrm{x=a,b,c}} |i_{\mathrm{x}}|\,\mathrm{d}\vartheta. \tag{18}$$

2.2. Zero-Sequence Voltage (v_{o}) Limits

The instantaneous zero-sequence voltage which can be applied by a three-level unidirectional rectifier is dynamically limited by the feasible three-phase bridge-leg voltage values, which depend on the signs of the respective phase currents [15], as

$$\begin{cases} 0 \leq v_{\mathrm{xm}} \leq +V_{\mathrm{pm}} & i_{\mathrm{x}} > 0 \\ -V_{\mathrm{mn}} \leq v_{\mathrm{xm}} \leq 0 & i_{\mathrm{x}} < 0 \end{cases} \qquad \mathrm{x = a,\ b,\ c.} \tag{19}$$

Assuming balanced split DC-link voltages, namely $V_{\mathrm{pm}} = V_{\mathrm{mn}} = V_{\mathrm{dc}}/2$, (19) can be rewritten as

$$\begin{cases} v_{\mathrm{xm}} \leq \dfrac{\mathrm{sign}(i_{\mathrm{x}}) + 1}{2}\,\dfrac{V_{\mathrm{dc}}}{2} \\ v_{\mathrm{xm}} \geq \dfrac{\mathrm{sign}(i_{\mathrm{x}}) - 1}{2}\,\dfrac{V_{\mathrm{dc}}}{2} \end{cases} \qquad \mathrm{x = a,\ b,\ c.} \tag{20}$$

Leveraging the bridge-leg voltage definition (7), the maximum and minimum zero-sequence voltage limits are obtained:

$$\begin{cases} v_{\mathrm{o,max}} = \min\left[\dfrac{V_{\mathrm{dc}}}{4}(\mathrm{sign}(i_{\mathrm{x}}) + 1) - v_{\mathrm{x}}\right] \\ v_{\mathrm{o,min}} = \max\left[\dfrac{V_{\mathrm{dc}}}{4}(\mathrm{sign}(i_{\mathrm{x}}) - 1) - v_{\mathrm{x}}\right] \end{cases} \qquad \mathrm{x = a,\ b,\ c,} \tag{21}$$

which are characterized by a $2\pi/3$ periodicity. A graphical representation of (21) is shown in Figure 4 for different values of M, and in Figure 5 for different values of φ. It is primarily observed that a reduction of M widens the feasible zero-sequence injection region, while $\varphi \neq 0$ determines the impossibility to apply $v_{\mathrm{o}} = 0$ around the phase current zero-crossings. In particular, this last feature affects the ability of the converter to eliminate the low-frequency mid-point voltage oscillation, as demonstrated in Section 2.5.

It is worth noting that to ensure that only feasible bridge-leg voltages are applied, the zero-sequence voltage limits (21) must be enforced within the rectifier control structure by means of a saturation action (i.e., $v_{\mathrm{o}} = v_{\mathrm{o,max}}$ if $v_{\mathrm{o}} > v_{\mathrm{o,max}}$ and $v_{\mathrm{o}} = v_{\mathrm{o,min}}$ if $v_{\mathrm{o}} < v_{\mathrm{o,min}}$). This saturation process is in fact necessary to avoid potentially large and uncontrolled phase current distortion [16].

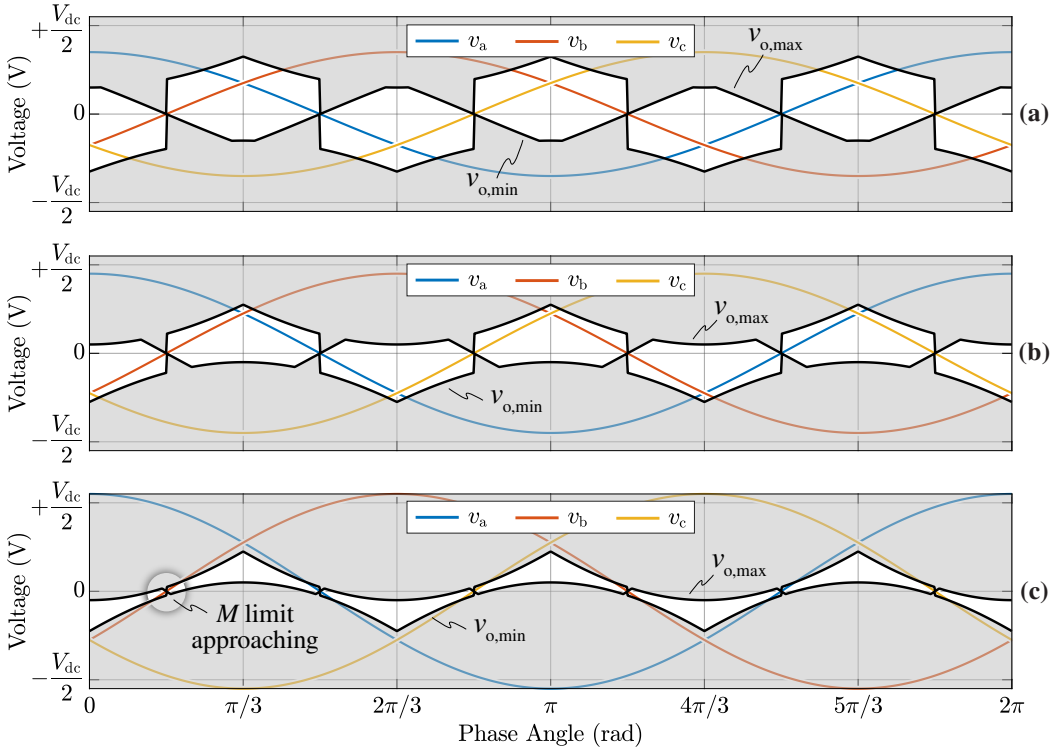

Figure 4. Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ for $M = 0.7$ (**a**), $M = 0.9$ (**b**) and $M = 1.1$ (**c**) assuming unity power factor operation ($\varphi = 0$, i.e., $\text{sign}(i_x) = \text{sign}(v_x)$).

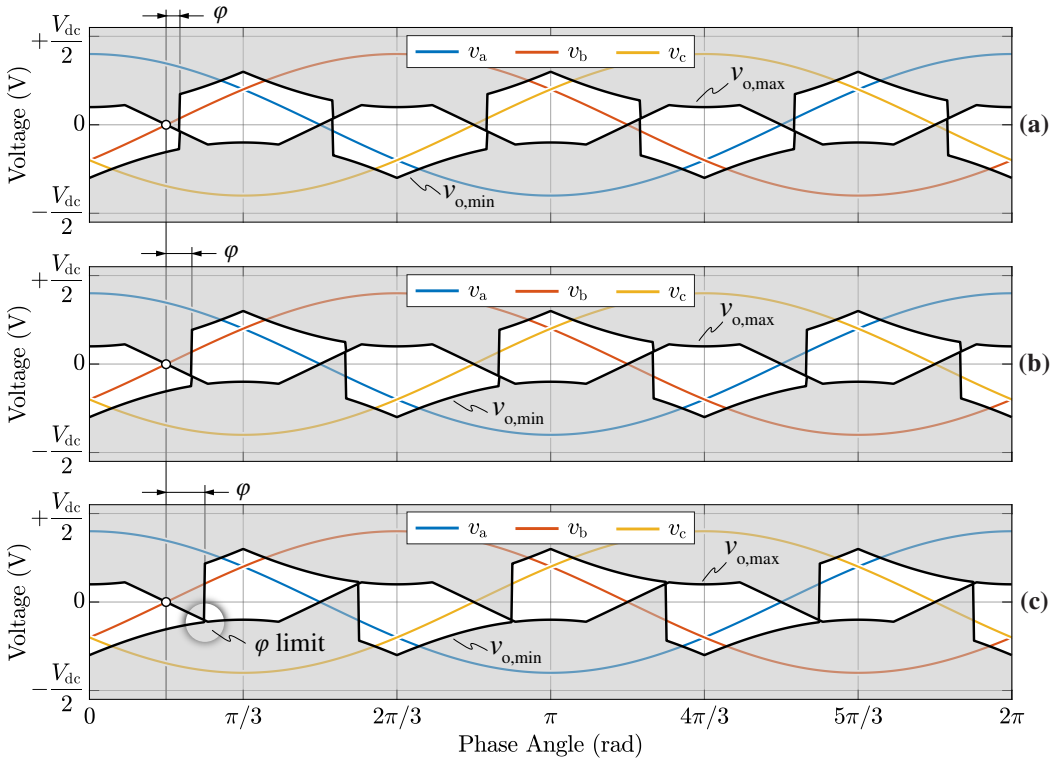

Figure 5. Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ for $\varphi = 5°$ (**a**), $\varphi = 10°$ (**b**) and $\varphi = 15°$ (**c**) assuming $M = 0.8$.

2.3. Modulation Index (M) Limits

The modulation index limits of a three-level rectifier can be easily derived from the zero-sequence voltage limits reported in (21). It is observed from Figure 4 that increasing values of M reduce the feasible zero-sequence injection region. Therefore, the maximum modulation index value in linearity (i.e., ensuring no low-frequency AC voltage distortion) is found from the intersection of $v_{o,max}$ and $v_{o,min}$, as shown in Figure 4c. Focusing on $\vartheta \in [0, \pi/3]$, this intersection corresponds to setting $V_{dc}/2 - v_a = -V_{dc}/2 - v_c$ with $\vartheta = \pi/6$. By leveraging the phase voltage definitions in (3), the maximum modulation index is obtained as

$$M_{max} = \frac{2}{\sqrt{3}} \approx 1.15, \tag{22}$$

which corresponds to the limit of conventional three-phase bidirectional two-level and three-level converters. The same results can be obtained by geometrical considerations on the space vector diagram reported in Figure 3 [9,15].

2.4. Power Factor Angle (φ) Limits

Even though three-level rectifiers can operate with non-unity power factor, their reactive power capabilities are limited by their unidirectional nature, as the AC-side voltage formation depends on the phase current sign. The converter φ limits can be derived from the instantaneous zero-sequence limits reported in (21). In particular, the maximum allowed φ at a certain modulation index value M is found from the intersection between $v_{o,max}$ and $v_{o,min}$, as illustrated in Figure 5c. Focusing on $\vartheta \in [0, \pi/3]$, this intersection corresponds to setting $v_b = v_c + V_{dc}/2$. By leveraging the phase voltage definitions in (3), the following expression of the converter-side power factor angle limits is obtained:

$$\varphi_{max} = -\varphi_{min} = \sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) - \frac{\pi}{6} \qquad M \geq \frac{2}{3}, \tag{23}$$

which is valid for $2/3 \leq M \leq 2/\sqrt{3}$. With a similar procedure, it can be demonstrated that for lower values of M (i.e., not typical in rectifier applications) the power factor angle is limited within $\varphi \in [-\pi/6, +\pi/6]$. Additionally in this case, the same results can be obtained by geometrical considerations on the space vector diagram reported in Figure 3 [9,15].

2.5. Mid-Point Current (i_m) Limits

Since the generation process of the DC-link mid-point current i_m depends on the zero-sequence voltage injection (see Section 2.1.2), it is straightforward to understand that $v_{o,max}$ and $v_{o,min}$ directly limit the feasible values of the mid-point current local average. The upper and lower i_m limits can therefore be derived substituting (21) into (16), obtaining

$$\begin{cases} i_{m,max} = -\dfrac{2}{V_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,min}\sum_{x=a,b,c}|i_x|\right] \\ i_{m,min} = -\dfrac{2}{V_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,max}\sum_{x=a,b,c}|i_x|\right] \end{cases}. \tag{24}$$

A graphical representation of (24) is shown in Figure 6 for different values of M, and in Figure 7 for different values of φ. It is worth noting that a reduction of M increases the mid-point current generation capability of the converter, while $\varphi \neq 0$ forces $i_{m,max}$ and $i_{m,min}$ to cross the line defined by $i_m = 0$, thus preventing to achieve a zero mid-point current local average over the complete fundamental period.

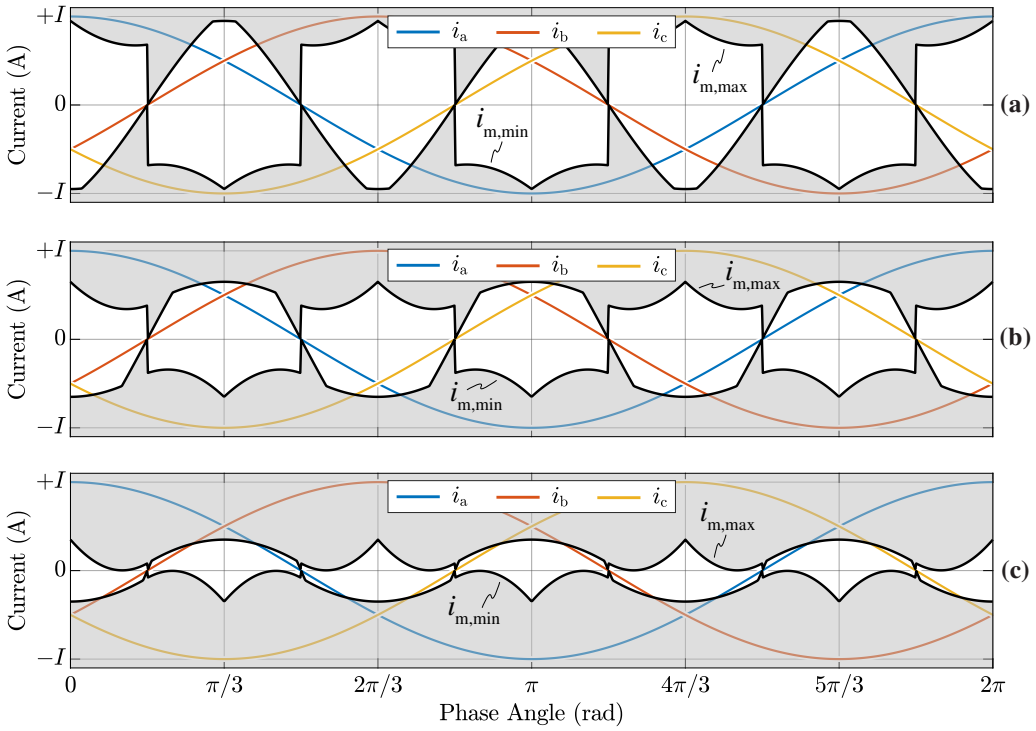

Figure 6. Mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for $M = 0.7$ (**a**), $M = 0.9$ (**b**) and $M = 1.1$ (**c**) assuming unity power factor operation ($\varphi = 0$, i.e., $\text{sign}(i_x) = \text{sign}(v_x)$).

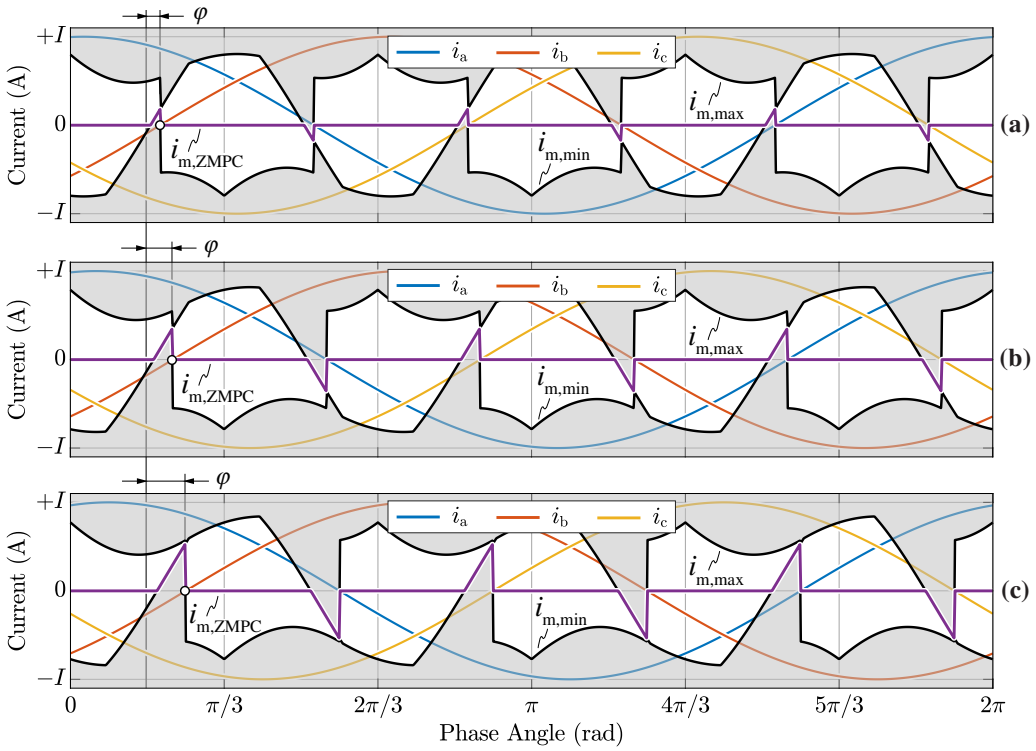

Figure 7. Mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for $\varphi = 5°$ (**a**), $\varphi = 10°$ (**b**) and $\varphi = 15°$ (**c**) assuming $M = 0.8$. The mid-point current local average waveform obtained with zero mid-point current modulation (ZMPCPWM) is superimposed (i.e., $i_{m,ZMPC}$).

By averaging $i_{m,max}$ and $i_{m,min}$ over their $2\pi/3$ periodicity, the mid-point current periodical average I_m limits can be calculated. The results of this averaging process are provided in Appendix A, where the analytical expressions of $I_{m,max} = -I_{m,min}$ are derived for the complete converter operating range. In particular, (A9) defines the limits of the mid-point current periodical average within the typical rectifier operating range (i.e., $2/3 \leq M \leq 2/\sqrt{3}$ and $-\pi/6 \leq \varphi \leq \pi/6$). These limits identify the ability of the rectifier to operate under unbalanced split DC-link loading (i.e., being $I_m = I_{o,n} - I_{o,p}$) and are illustrated in normalized form in Figure 8, where the analytical results are compared to the experimental measurements (see Section 3.2.3), showing excellent agreement.

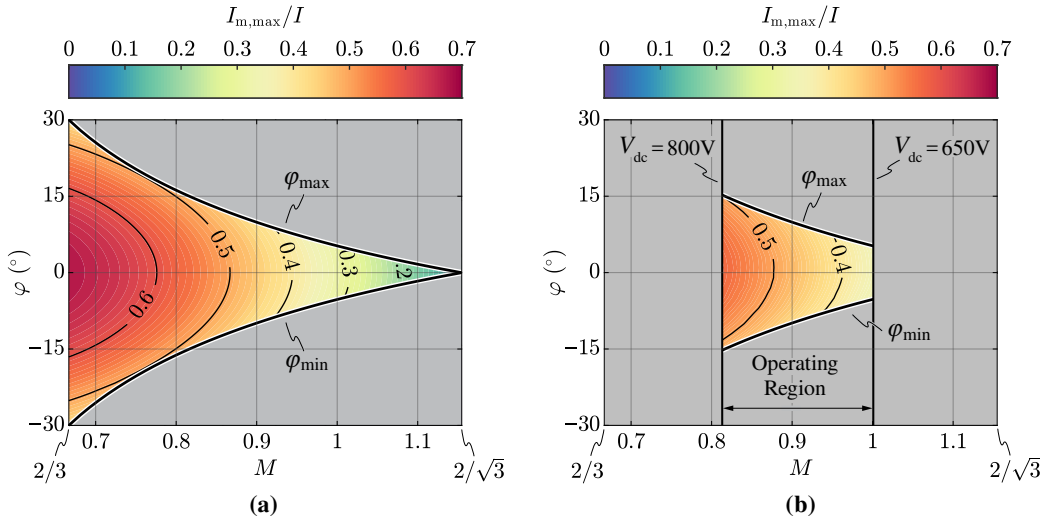

Figure 8. Mid-point current periodical average limits $I_{m,max} = -I_{m,min}$ (i.e., normalized with respect to the peak phase current I) for $2/3 \leq M \leq 2/\sqrt{3}$. (**a**) analytical results and (**b**) experimental results, limited to the operating region of the rectifier prototype (see Section 3).

2.6. Minimum Mid-Point Charge Ripple ($\Delta Q_{m,pp,min}$)

The DC-link mid-point peak-to-peak charge ripple $\Delta Q_{m,pp}$ is defined as the difference between the maximum and the minimum values achieved by the time-integral of the mid-point current local average i_m over $\pi/3$ (i.e., half of the zero-sequence voltage periodicity):

$$\Delta Q_{m,pp} = \frac{1}{2\pi f}\left(\max\left[\int_0^{\vartheta} i_m \, d\vartheta'\right]_{\vartheta=0}^{\vartheta=\pi/3} - \min\left[\int_0^{\vartheta} i_m \, d\vartheta'\right]_{\vartheta=0}^{\vartheta=\pi/3}\right), \tag{25}$$

where f is the grid frequency. It is worth noting that the definition in (25) only considers the low-frequency charge ripple contribution (i.e., defined by the mid-point current local average), since the high-frequency contribution directly depends on the rectifier switching frequency f_{sw} and is typically negligible in systems with high pulse ratios [8].

Expression (25) shows that the only way to achieve $\Delta Q_{m,pp} = 0$ is by enforcing $i_m = 0$ over the complete period. This can be achieved by adding to the phase voltage reference signals a proper zero-sequence third-harmonic component $v_{o,3}$, which may be derived by setting $i_m = 0$ and $v_o = v_{o,3}$ in (16), obtaining

$$v_{o,3} = \frac{\sum_{x=a,b,c} v_x |i_x|}{\sum_{x=a,b,c} |i_x|} = \frac{v_a |i_a| + v_b |i_b| + v_c |i_c|}{|i_a| + |i_b| + |i_c|}. \tag{26}$$

A graphical illustration of $v_{o,3}$ is reported in Figure 9 for $M = 0.9$ and $\varphi = 0$, together with the phase and bridge-leg voltage waveforms. The injection of (26) is typically referred

to as zero mid-point current modulation (ZMPCPWM) and ensures the converter operation with ideally zero low-frequency charge ripple [8,15,19].

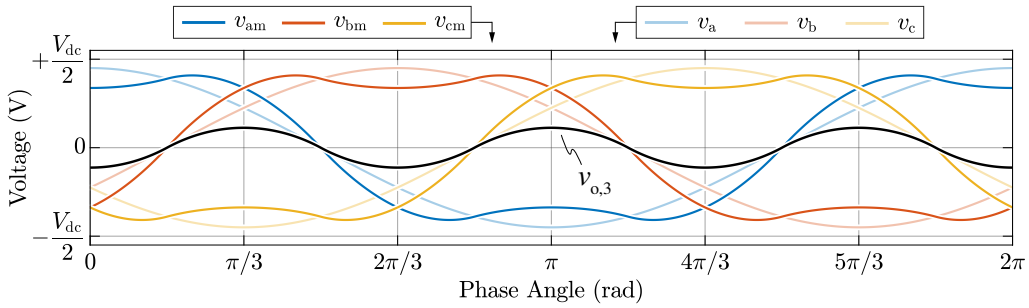

Figure 9. Zero-sequence voltage injection $v_{o,3}$ according to the zero mid-point current modulation (ZMPCPWM) with $M = 0.9$ and $\varphi = 0$. The reference phase voltages v_a, v_b, v_c and the resulting bridge-leg voltages v_{am}, v_{bm}, v_{cm} are shown for completeness.

Unfortunately, the adoption of ZMPCPWM cannot ensure $i_m = 0$ over the complete period when $\varphi \neq 0$, as pointed out in Section 2.5, since $i_{m,max}$ and $i_{m,min}$ cross the line defined by $i_m = 0$ (see Figure 7). In fact, $v_{o,3}$ encounters the zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ as soon as $\varphi \neq 0$ (see Figure A4 in Appendix B). Nevertheless, the injection of (26) ensures the minimum possible value of $\Delta Q_{m,pp} = \Delta Q_{m,pp,min}$ for a given power factor angle φ, since the saturated v_o is as near as possible to the desired $v_{o,3}$ value. Therefore, the adoption of ZMPCPWM allows the minimization of the size of the split DC-link capacitors for a given mid-point voltage ripple requirement and is therefore particularly beneficial in three-level rectifiers.

Figure 7 shows the mid-point current local average obtained with ZMPCPWM (i.e., $i_{m,ZMPC}$) for different values of φ. It is directly observed that higher absolute values of φ increase the minimum mid-point charge ripple.

The exact analytical expression of $\Delta Q_{m,pp,min}(M, \varphi)$ is derived in Appendix B for the complete operating region of the converter (i.e., $0 \leq M \leq 2/\sqrt{3}$ and $-\pi/6 \leq \varphi \leq \pi/6$). These results are illustrated in normalized form in Figure 10, where the analytical expression (A13) is compared to experimental measurements (see Section 3.2.4), showing excellent agreement.

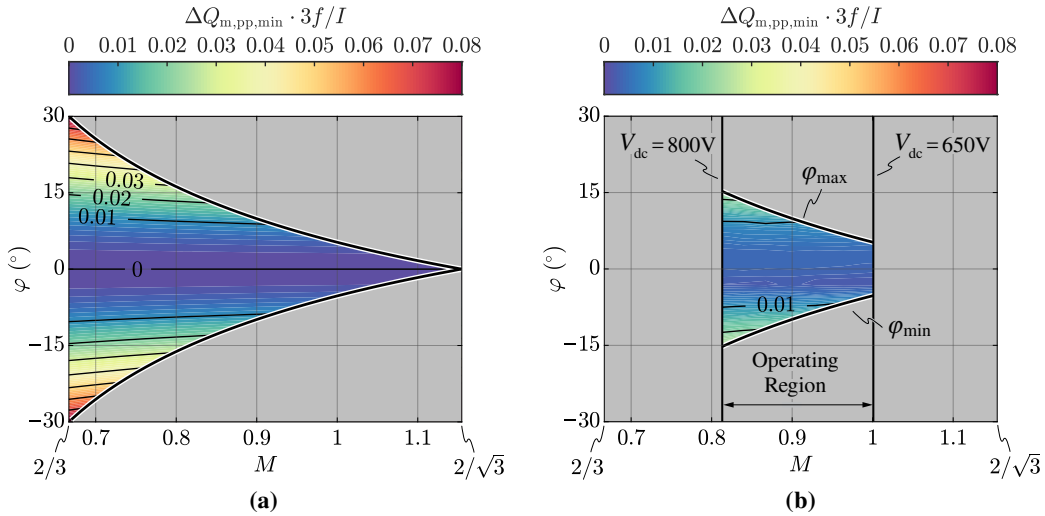

Figure 10. Minimum DC-link mid-point charge ripple $\Delta Q_{m,pp,min}$ (i.e., normalized with respect to the peak phase current I and three-times the grid frequency $3f$) for $2/3 \leq M \leq 2/\sqrt{3}$. (**a**) Analytical results and (**b**) experimental results, limited to the operating region of the rectifier prototype (see Section 3).

It is worth noting that (A13) provides a straightforward approach to size the three-level rectifier DC-link capacitors according to a maximum mid-point voltage ripple $\Delta V_{\mathrm{m,pp,max}}$ criterion, as

$$C_{\mathrm{dc}} \geq \frac{\Delta Q_{\mathrm{m,pp,min}}(M, \varphi)}{2\,\Delta V_{\mathrm{m,pp,max}}}, \tag{27}$$

where M and φ must be selected as the worst-case values within the operating range of the considered application. However, since (27) tends to 0 for $\varphi = 0$ (i.e., the analytical approach neglects the switching-frequency charge ripple), if the rectifier is exclusively operated under unity power factor, C_{dc} can be sized with conventional approaches derived for two-level inverters [38].

3. Experimental Results

In this section, the rectifier limits and performance in terms of displacement power factor (DPF), current total harmonic distortion (THD), maximum mid-point current capability and minimum mid-point charge ripple are experimentally assessed on a digitally controlled T-type converter prototype, supporting the theoretical analysis provided in Section 2, Appendices A and B. For reasons of conciseness, the converter performances are here evaluated only in steady-state conditions, nevertheless a complete assessment of the dynamical behavior of the considered rectifier prototype is provided in [16].

The specifications and the nominal operating conditions of the three-level T-type unidirectional rectifier exploited for the experimental validation are reported in Table 1. It is worth noting that this converter has been designed as the active front-end stage of an electric vehicle ultra-fast battery charger [16,39]. The rectifier prototype is illustrated in Figure 11 and consists of two paralleled three-phase 30 kW units, realized for modularity reasons. Nevertheless, only one converter unit is used in the experimental tests, due to the maximum power limitation of the available equipment.

Table 1. Three-level unidirectional T-type rectifier specifications and nominal operating conditions.

Parameter	Description	Value
f	grid frequency	50 Hz
P	nominal active power	30 kW
S	nominal apparent power	30 kVA
V	peak phase voltage	325 V
I	peak phase current	61.5 A
V_{dc}	DC-link voltage	650–800 V
L	boost inductance	150–190 µH
C_{dc}	DC-link capacitance	4080 µF
$f_{\mathrm{sw}}, f_{\mathrm{s}}$	switching, control frequency	20 kHz

Each converter bridge-leg employs two 650 V Si MOSFETs connected in anti-series (i.e., as 4Q switch) operating at 20 kHz and two 1200 V Si fast-recovery diodes. Furthermore, the converter boost inductors employ XFlux 60µ powder cores from Magnetics [40], which are characterized by a soft-saturating B–H characteristic. This feature leads to a current-dependent variable inductance value (see Table 1), which must be taken into account in the control tuning [16]. The detailed characteristics of the inductor design are reported in [39], obtained as a result of the optimization procedure described in [41].

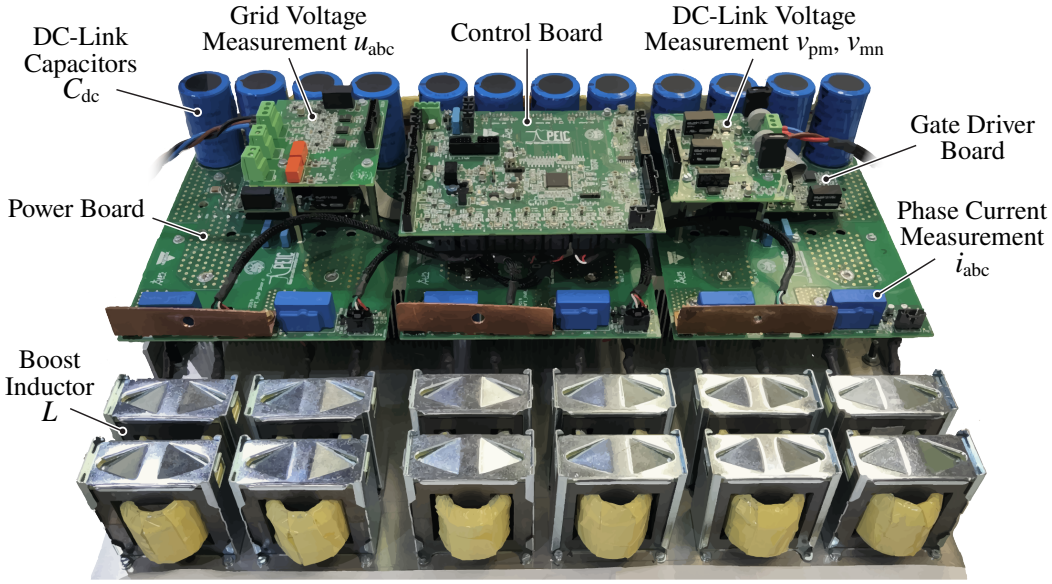

Figure 11. Overview of the three-level unidirectional T-type rectifier prototype used for the experimental tests. The converter consists of two paralleled 30 kW units: only one unit is exploited for the experimental verification, due to the maximum power limitation of the available equipment.

Figure 12 shows a schematic diagram of the adopted experimental setup. The T-type rectifier is connected to a grid emulator (i.e., emulating the 50 Hz, 400 V European low-voltage grid) by means of an *LCL* filter, consisting of the converter boost inductors (L), filter capacitors ($C_f = 15\,\mu F$) equipped with series damping resistors ($R_f = 0.8\,\Omega$), and grid-side inductors ($L_g = 100\,\mu H$). The main scope of the *LCL* filter is to eliminate the switching-frequency harmonic content from the grid currents $i_{g,abc}$ [17,42], so that a lower current total harmonic distortion (THD) is achieved and the converter may comply with grid-code standards [43,44]. Furthermore, the presence of the *LCL* filter allows isolation of the low-frequency component of the distortion, which depends on the control strategy, from the switching-frequency one, which only depends on the selected modulation scheme, allowing for a proper assessment of the converter closed-loop control performance. In the present case, the values of C_f and R_f are selected according to [39], and the value of L_g is representative of an equivalent inner grid impedance of ≈0.02 pu. On the DC-side, the converter is connected to two independent electronic loads, which emulate the rectifier split DC-link loads. The measurements are performed both with a Teledyne LeCroy 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope (i.e., employing isolated high-voltage differential probes for voltage measurements and standard current probes for current measurements), and with an HBM GEN4tB 2 MS/s data acquisition system, leveraging current and voltage sensors with high rated accuracy (i.e., <0.1 %). In particular, the latter approach has been exploited to automatically map the rectifier performance over its complete operating region.

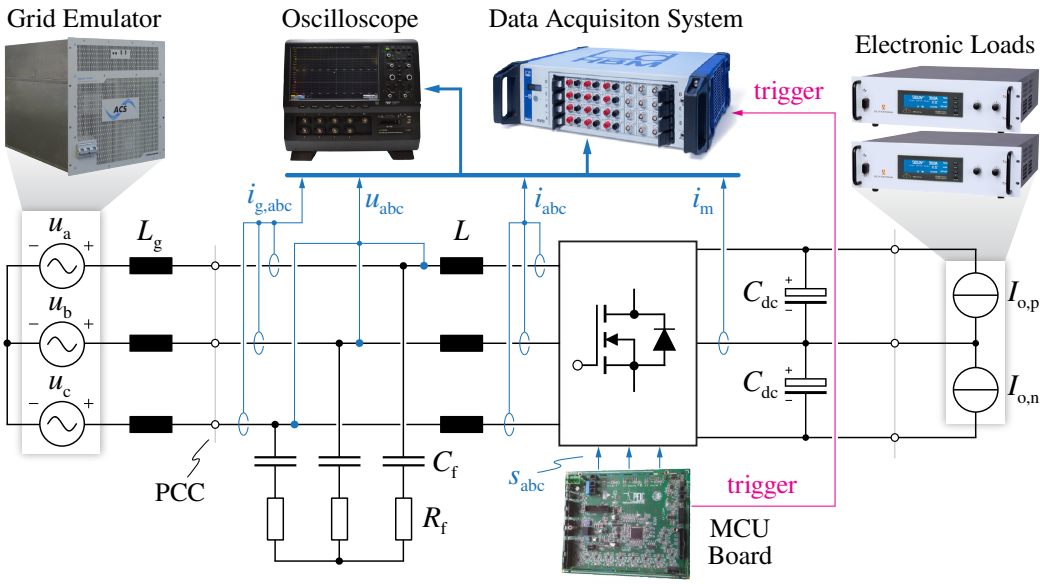

Figure 12. Simplified schematic diagram of the experimental setup.

3.1. Multi-Loop Control Scheme

The rectifier is controlled with the full-digital multi-loop control strategy reported in [16], where the detailed description and tuning of all loops is provided. A conventional voltage-oriented dq current control scheme is adopted [17,45–47], complemented by a DC-link voltage loop, tracking the desired DC-link voltage value V_{dc}, and a DC-link mid-point voltage balancing loop, ensuring limited steady-state and dynamical V_m voltage deviation. A simplified block diagram of the complete system and the adopted control strategy is provided in Figure 13.

The voltages at the point of common coupling (PCC) are measured to achieve the reference frame synchronization with the grid by means of a phase locked loop (PLL) [48,49]. The measured grid voltages are then fed forward in the current control loop, to unburden the integral part of the PI regulator. Even though the digital sampling and update process is performed once per switching/control period, the i_{abc} current feedback values are obtained by means of oversampling (32 samples per control period) and averaging, to enhance the measurement quality around the current zero-crossings. In fact, traditional synchronous/asynchronous sampling approaches do not provide the correct average current value when discontinuous conduction mode (DCM) takes place [21,50], thus affecting the current control accuracy and leading to increased low-frequency distortion. The DC-link voltage loop controls the active power transfer of the rectifier and therefore provides the reference to the d-axis current control loop. The q-axis current i_q, instead, is typically controlled to compensate the reactive power injected by the filter capacitors C_f (i.e., to ensure unity power factor operation at the PCC), nevertheless it can be set to any value that complies with the converter-side power factor angle limitations of the rectifier (see Section 2.4), being $\varphi = \tan^{-1}(i_q/i_d)$. Finally, the DC-link mid-point voltage balancing loop ensures $V_{pm} \approx V_{mn}$ at all times, acting on the zero-sequence voltage v_o injection [9,14–16,51]. In particular, this control loop theoretically does not interfere with the others, as v_o affects neither the active power transfer nor the phase current formation process (see Section 2.1.1). Furthermore, the measured V_m is passed through a moving average filter operated at $3f$, so that the control loop does not react to the possibly occurring low-frequency mid-point voltage oscillation.

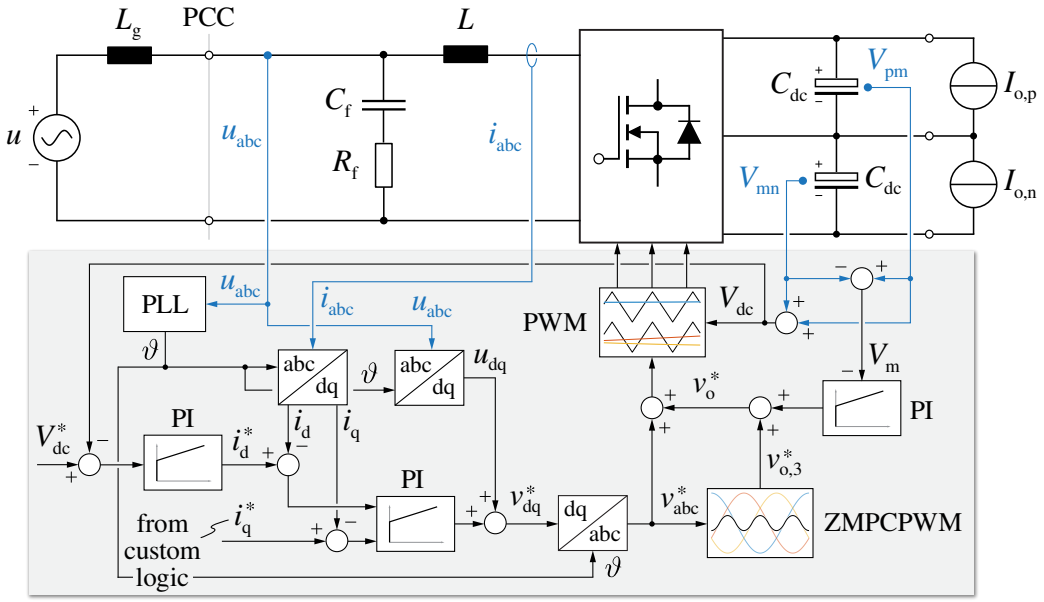

Figure 13. Simplified single-phase equivalent circuit of the considered system and overview of the adopted digital multi-loop control strategy [16].

In practice, the complete converter multi-loop control strategy is implemented on a STM32G474VE MCU from ST Microelectronics [52] with an interrupt service routine running at $f_s = 20\,\text{kHz}$.

3.2. Steady-State Performance Evaluation

The most significant rectifier waveforms in steady-state operation are illustrated in Figure 14, where the grid voltages u_{abc}, the converter-side currents i_{abc} and the grid-side (i.e., filtered) currents $i_{g,abc}$ are shown for $V_{dc} = 800\,\text{V}$, $\varphi = 0$ and different values of transferred power. It is observed that the grid-side current quality improves with the rectifier loading. For instance, at 10% of the rated power (see Figure 14b) the converter-side current ripple amplitude becomes comparable to the current peak value, therefore leading to marked low-frequency zero-crossing distortion that bypasses the filter capacitor and appears in the grid-side currents. Even though the distortion at light load may seem large, the pronounced DCM operation of unidirectional rectifiers typically leads to much higher distortion levels [21]. In the present case, the pseudo-sinusoidal shape of the currents is maintained thanks to the adopted current oversampling and averaging strategy, the high current control loop bandwidth and the feed-forward contributions reported in Figure 13 [16]. At 50% and 100% of the rated power (see Figure 14c,d the quality of both converter-side and grid-side currents improves substantially, as the relative amplitude of the current ripple decreases and the zero-crossing distortion related to DCM operation is mostly eliminated by the current control loop [16].

Both instantaneous and local average values of the DC-link mid-point current i_m for $V_{dc} = 800\,\text{V}$ ($M \approx 0.81$), $\varphi = 0$ and $P = 30\,\text{kW}$ are illustrated in Figure 15, where a focus is also provided in (b). Although the instantaneous value of i_m jumps between the converter-side phase current values $\pm i_a$, $\pm i_b$, $\pm i_c$ and 0 (i.e., visible from the current envelopes), the local average value of i_m remains approximately 0 along the complete grid period, due to the adopted zero-mid-point current modulation (ZMPCPWM) strategy. A focus of the instantaneous values of i_a, i_b, i_c and i_m towards the end of current sector ① is provided in Figure 15b, where the mid-point current is shown to jump between $+i_a$ (state 100), $-i_a$ (state 011), $+i_b$ (state 010) and $-i_c$ (state 110), as expected from space vector theory (see Figure 3b).

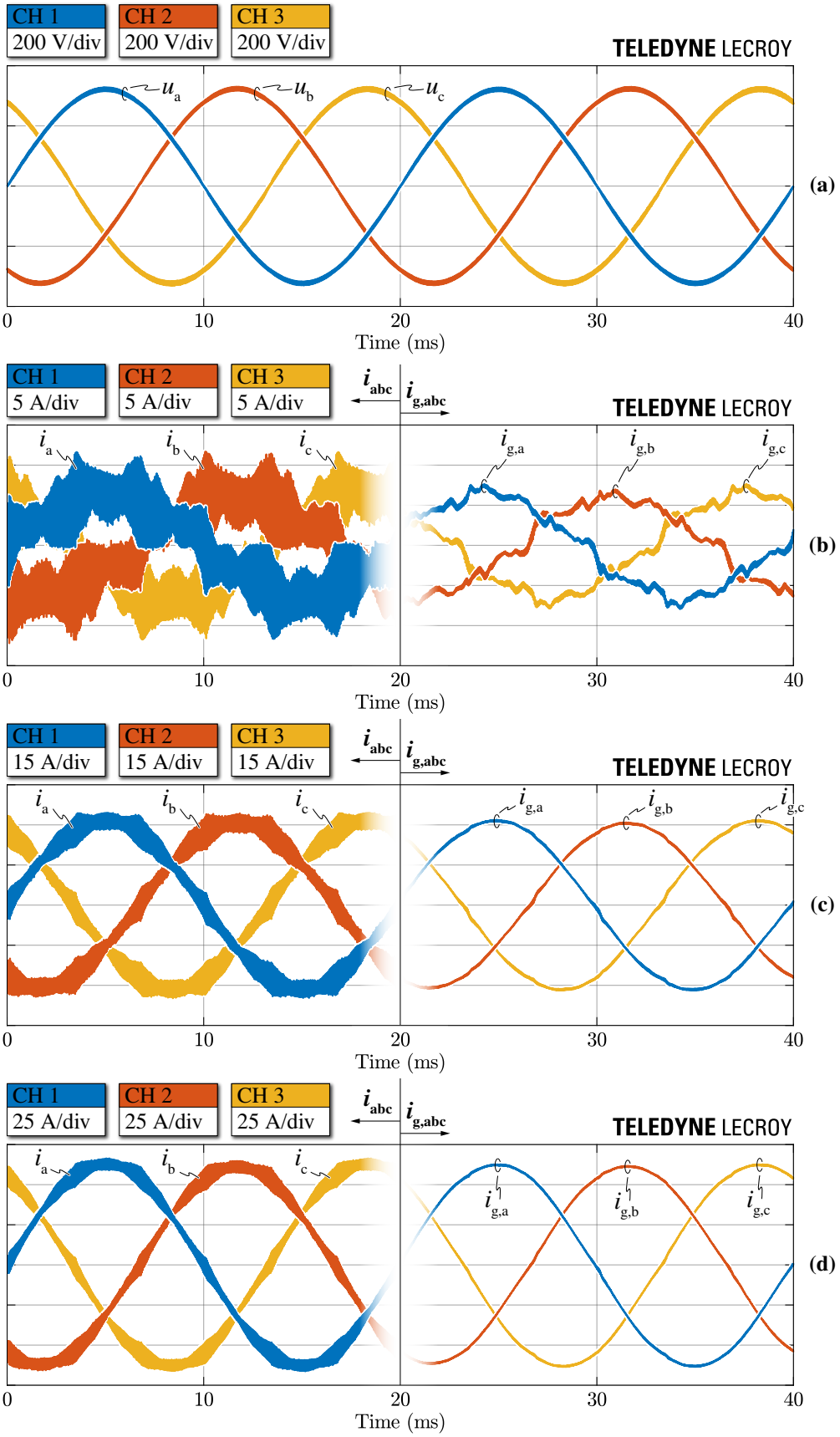

Figure 14. Experimental waveforms in steady-state conditions with $V_{dc} = 800\,V$ and $\varphi = 0$. Measured grid voltages u_{abc} (**a**) and both converter-side currents i_{abc} and grid-side currents $i_{g,abc}$ at (**b**) 10%, (**c**) 50%, and (**d**) 100% of the nominal power (i.e., $P = 30\,kW$).

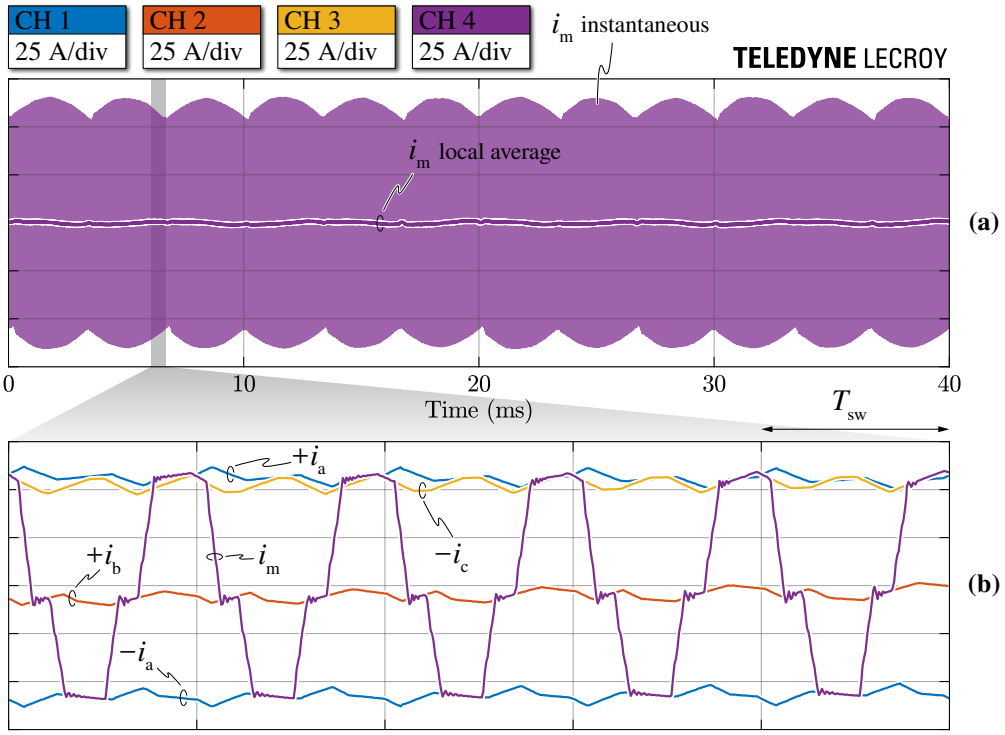

Figure 15. Experimental waveforms of the mid-point current i_m instantaneous and local average values in steady-state conditions with $V_{dc} = 800\,V$, $\varphi = 0$ and $P = 30\,kW$ (**a**). Focus of the instantaneous mid-point current towards the end of current sector Ⓘ (see Figure 3) and converter-side phase current values $\pm i_a$, $+i_b$, $-i_c$ (**b**).

It is worth noting that the measurement of the instantaneous mid-point current value is not common in the literature (i.e., the only case known to the authors is [53]), as it represents a challenging task to achieve. In practice, the current measurement must be placed within the commutation loop of all bridge-legs, thus negatively affecting the switching performance of the rectifier. In the present case, the measurement of i_m has been achieved by placing the current probe between the bridge-leg decoupling capacitors (i.e., 220 nF ceramic capacitors) and the DC-link capacitors (i.e., 4080 µF electrolytic capacitors), as schematically illustrated in Figure 16. Even though the decoupling capacitors are placed in parallel to the DC-link capacitors, their small capacitance value does not substantially affect the mid-point current, especially considering the relatively low switching frequency of the rectifier.

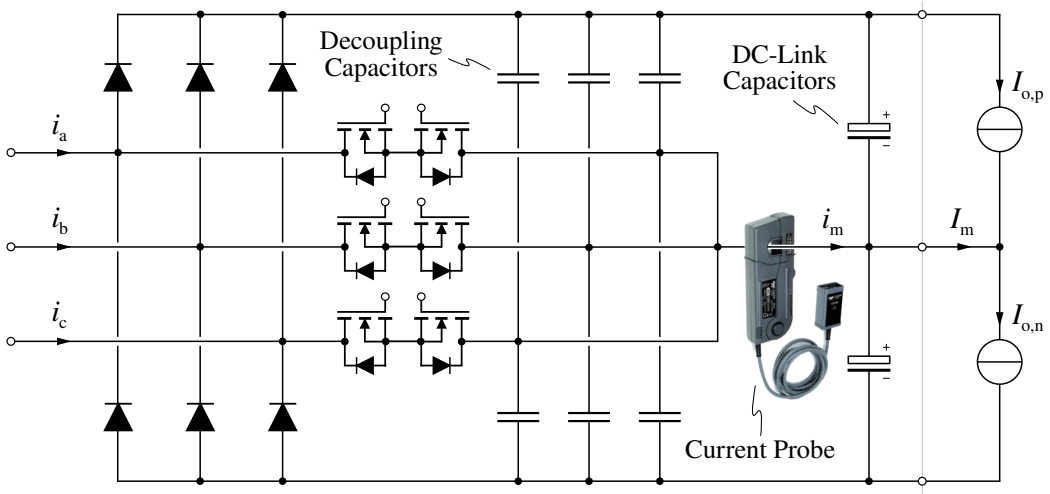

Figure 16. Schematic overview of the DC-link mid-point current i_m measurement setup. The current probe is placed between the bridge-leg decoupling capacitors and the DC-link capacitors.

Figures 17 and 18 show the most relevant rectifier waveforms under non-unity power factor operation and constant zero-sequence voltage injection, respectively. In particular, the reference bridge-leg voltages v_{am}, v_{bm}, v_{cm}, the reference zero-sequence voltage v_o, the converter-side currents i_{abc}, the grid-side currents $i_{g,abc}$ and the DC-link mid-point current i_m are shown for $V_{dc} = 800\,V$ and $S = 15\,kVA$. Furthermore, the effect of the zero-sequence voltage saturation $v_{o,max/min}$ on all measured quantities is highlighted by comparing the results with a conventional control implementation (i.e., with no saturation acting on v_o). It is worth noting that v_{am}, v_{bm}, v_{cm} and v_o are obtained from separate digital-to-analog converters (DACs) of the MCU (i.e., with a 0–3.3 V scale) and are thus rescaled in Figures 17a and 18a.

Figure 17 shows the operation of the rectifier with $\varphi = 15°$. In particular, Figure 17c highlights that non-unity power factor operation generates a large zero-crossing distortion if no zero-sequence voltage saturation is implemented. The enforcement of $v_{o,max/min}$, in fact, allows the rectifier to correctly apply the desired bridge-leg voltage values even when the phase currents are phase-shifted with respect to the reference voltages, as described in Section 2. Consequently, undistorted operation under non-unity power factor is achieved. Furthermore, Figure 17d shows that by saturating the zero-sequence voltage, a larger mid-point current local average i_m and thus a higher DC-link mid-point peak-to-peak charge ripple $\Delta Q_{m,pp}$ are obtained. This is because, to ensure the undistorted operation of the rectifier, the applied zero-sequence voltage v_o departs from the ideal $v_{o,3}$ value introduced by the ZMPCPWM (see Figure 17a). It is also worth observing that the local average of i_m obtained experimentally is in good agreement with the simulated waveforms reported in Figures 7 and A4b.

The rectifier waveforms with a constant zero-sequence voltage $v_o = 0.15\,V_{dc}/2$ added to $v_{o,3}$ (i.e., ZMPCPWM injection) are shown in Figure 18. This injection emulates the converter performance under unbalanced split DC-link loading, i.e., when a constant mid-point current periodical average $I_m = I_{o,n} - I_{o,p}$ is required. This is highlighted in Figure 18d, where the injection of a positive zero-sequence voltage is shown to generate a negative value of mid-point periodical average I_m, as expected from theoretical considerations. Additionally in this case larger i_m and $\Delta Q_{m,pp}$ ripple values are obtained when the $v_{o,max/min}$ saturation is enabled. Figure 18c shows that the zero-sequence voltage saturation $v_{o,max/min}$ allows substantial improvement of the phase current waveforms. Nevertheless, in this case the zero-crossing distortion cannot be completely avoided, since the injection of the constant zero-sequence voltage contribution increases the amplitude of the converter-side current ripple (see Figure 14c for comparison), which widens the DCM window around the current zero-crossings and leads to higher distortion. It is worth noting that this issue can be greatly reduced in practice by independently controlling the two anti-series mid-point switches, such that the free-wheeling of the current through the mid-point is always possible [26]. In fact, even though in the present case the two anti-series switches are supplied by independent gate drivers, they receive equal PWM signals, greatly simplifying the modulation and the control of the rectifier. It should be pointed out that the low-frequency distortion would mostly disappear at full load (i.e., $P = 30\,kW$), due to the lower ratio between the current ripple and the current peak. However, this condition could not be tested, due to the power limitations of the adopted electronic loads.

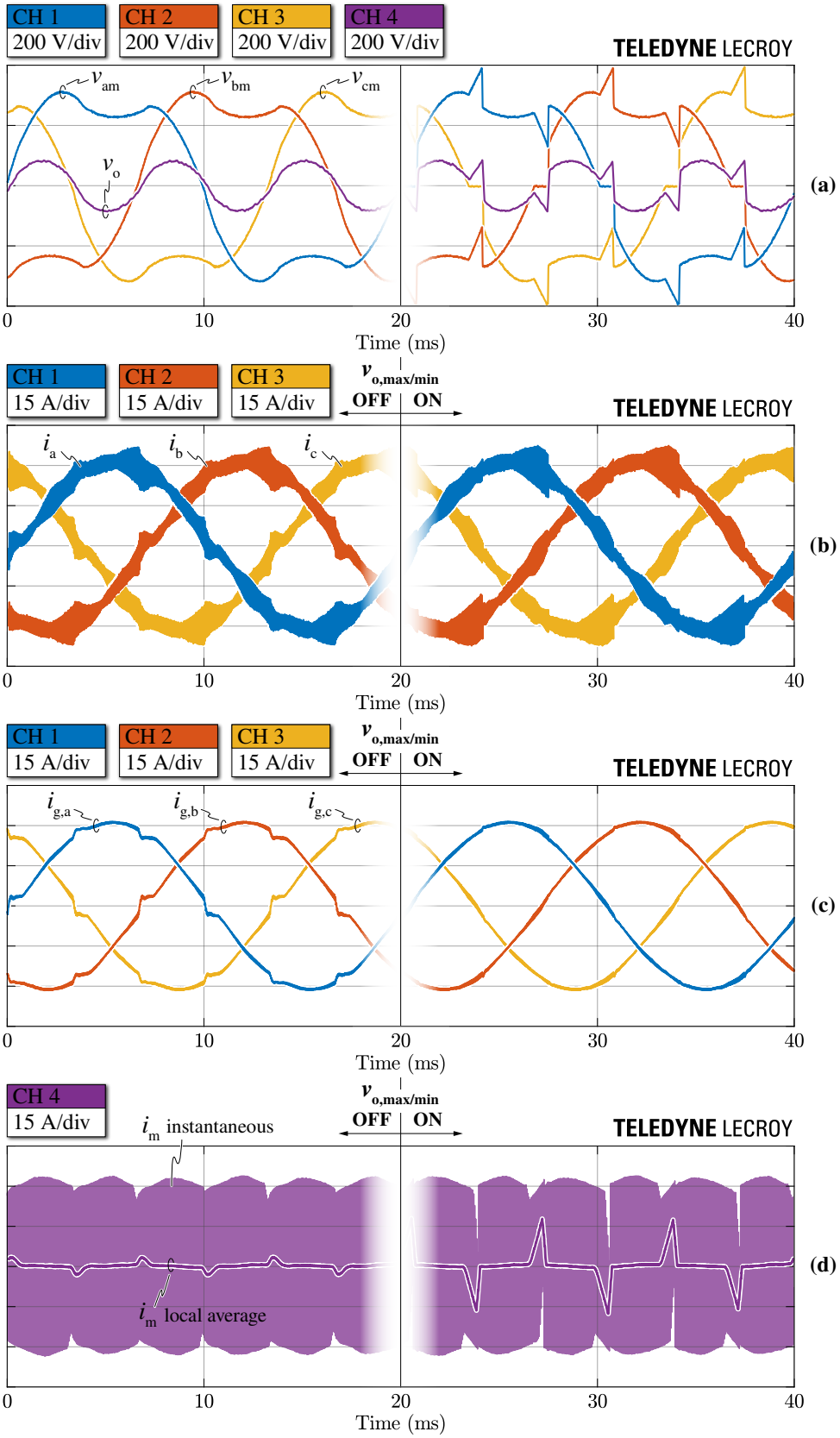

Figure 17. Experimental waveforms in steady-state conditions with $V_{dc} = 800\,V$, $\varphi = 15°$ and $S = 15\,kVA$. From top to bottom: (**a**) reference bridge-leg voltages v_{am}, v_{bm}, v_{cm} and zero-sequence voltage v_o (from DAC of the MCU), (**b**) converter-side currents i_{abc}, (**c**) grid-side currents $i_{g,abc}$, (**d**) and mid-point current i_m, with and without the zero-sequence voltage saturation $v_{o,max/min}$.

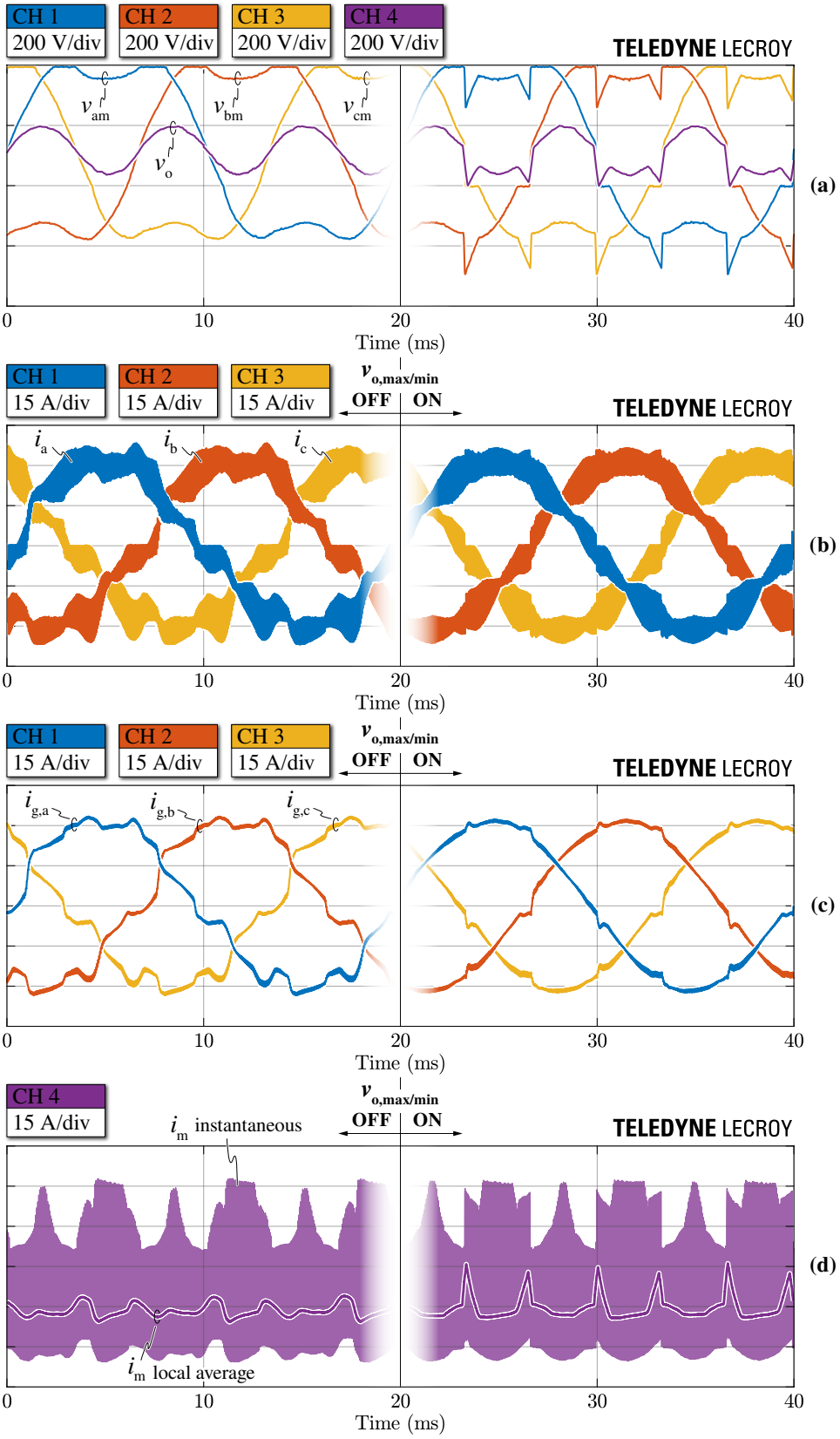

Figure 18. Experimental waveforms in steady-state conditions with $V_{dc} = 800\,V$, $\varphi = 0$ and $P = 15\,kW$. A constant zero-sequence voltage component $v_o = 0.15\,V_{dc}/2$ is added to $v_{o,3}$ (ZM-PCPWM). From top to bottom: (**a**) reference bridge-leg voltages v_{am}, v_{bm}, v_{cm} and zero-sequence voltage v_o (from DAC of the MCU), (**b**) converter-side currents i_{abc}, (**c**) grid-side currents $i_{g,abc}$, (**d**) and mid-point current i_m, with and without the zero-sequence voltage saturation $v_{o,max/min}$.

3.2.1. Total Harmonic Distortion (THD)

The grid-side current total harmonic distortion (THD) is defined as

$$\mathrm{THD} = \frac{\sqrt{I_{\mathrm{g,RMS}}^2 - I_{\mathrm{g,1,RMS}}^2}}{I_{\mathrm{g,1,RMS}}} \tag{28}$$

where $I_{\mathrm{g,RMS}}$ is the total RMS value of the grid-side current and $I_{\mathrm{g,1,RMS}}$ is the RMS value of the grid current first harmonic.

The rectifier performance is mapped over the complete modulation index M and converter-side power factor angle φ operating region, both at 50% and 100% of the nominal apparent power (i.e., $S = 30\,\mathrm{kVA}$). The results are shown in Figure 19, where the THD performance obtained with and without $v_{\mathrm{o,max/min}}$ saturation are compared. As expected from Figure 14, the quality of the grid-side current improves at higher load levels, as the zero-crossing distortion is reduced. Moreover, by enforcing the zero-sequence voltage saturation, the THD lies below the conventional 5% limit (i.e., required by grid standards [44]) for all operating points, which is not the case when $v_{\mathrm{o,max/min}}$ is disabled. Finally, it is observed that the THD values are not symmetrical with respect to φ, resulting in worse distortion for $\varphi < 0$ (i.e., capacitive operation). The main explanation resides in the fact that the zero-sequence voltage saturation modifies the current ripple shape and amplitude, leading to a wider DCM operation around the zero-crossings for negative values of φ.

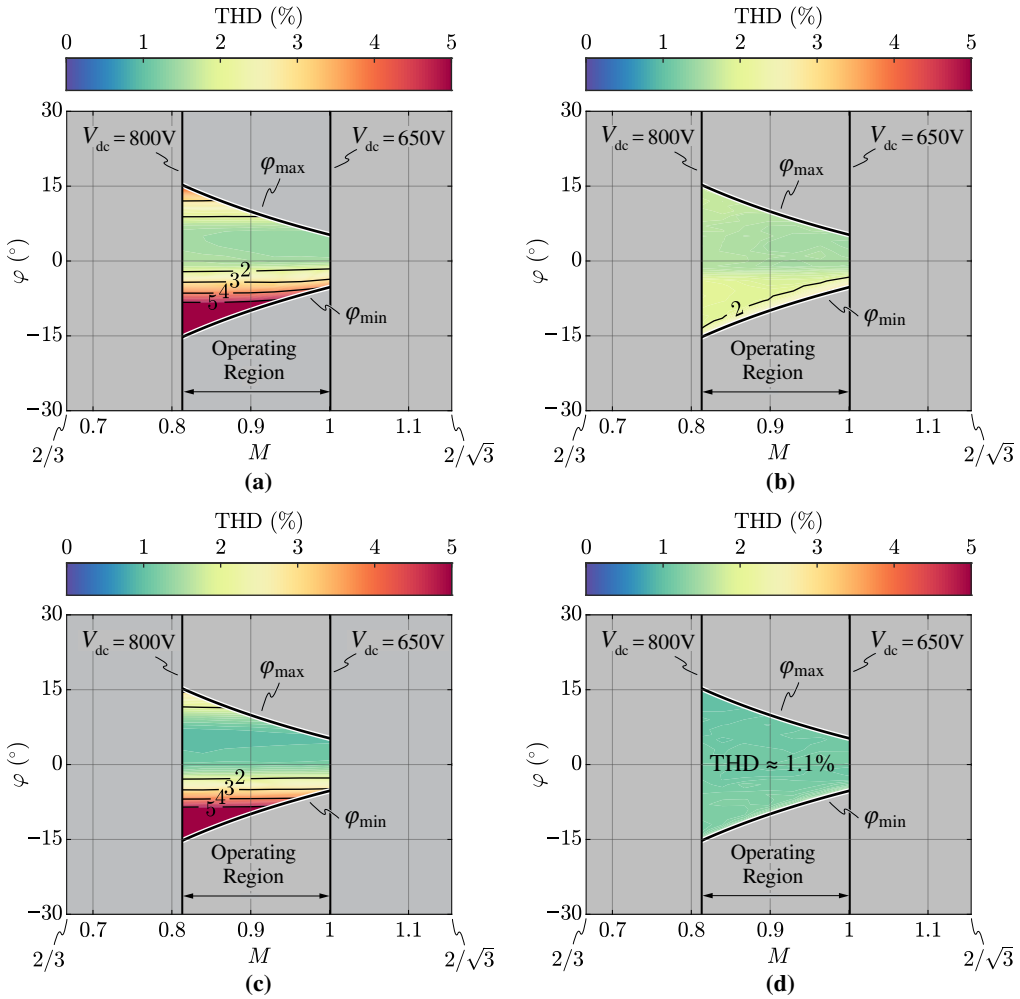

Figure 19. Experimental grid-side current total harmonic distortion (THD) for $S = 15\,\mathrm{kVA}$ (**a**,**b**) and $S = 30\,\mathrm{kVA}$ (**c**,**d**). Results without zero-sequence voltage saturation (**a**,**c**) and with zero-sequence voltage saturation (**b**,**d**).

3.2.2. Displacement Power Factor (DPF)

The displacement power factor (DPF) of the rectifier is defined as

$$\mathrm{DPF} = \cos\left(\angle\vec{U} - \angle\vec{I}_{\mathrm{g}}\right) = \frac{P}{S} \tag{29}$$

where $\angle\vec{U}$ and $\angle\vec{I}_{\mathrm{g}}$ are the phase angles of the grid voltage vector (i.e., measured at the PCC) and the grid current vector, respectively. It is worth noting that DPF $\neq \varphi$, as the grid-side converter current also includes the filter capacitor current contribution. The experimental DPF is illustrated in Figure 20a,c for 50% and 100% of the nominal apparent power (i.e., $S = 30\,\mathrm{kVA}$). In both cases, the zero-sequence voltage saturation is enabled.

For a better understanding of the phase-shift between $\vec{U}$ and $\vec{I}_{\mathrm{g}}$, the DPF angle (i.e., $\cos^{-1}(\mathrm{DPF})$) is shown in Figure 20b,d, where a positive value indicates a lagging power factor (i.e., inductive behavior) and a negative value indicates a leading power factor (i.e., capacitive behavior). It can be observed that the current flowing into the filter capacitor C_{f} is completely compensated for $\varphi \approx 4.2°$ at 50% of the rated power and $\varphi \approx 3°$ at 100% of the rated power, as expected from basic theoretical considerations.

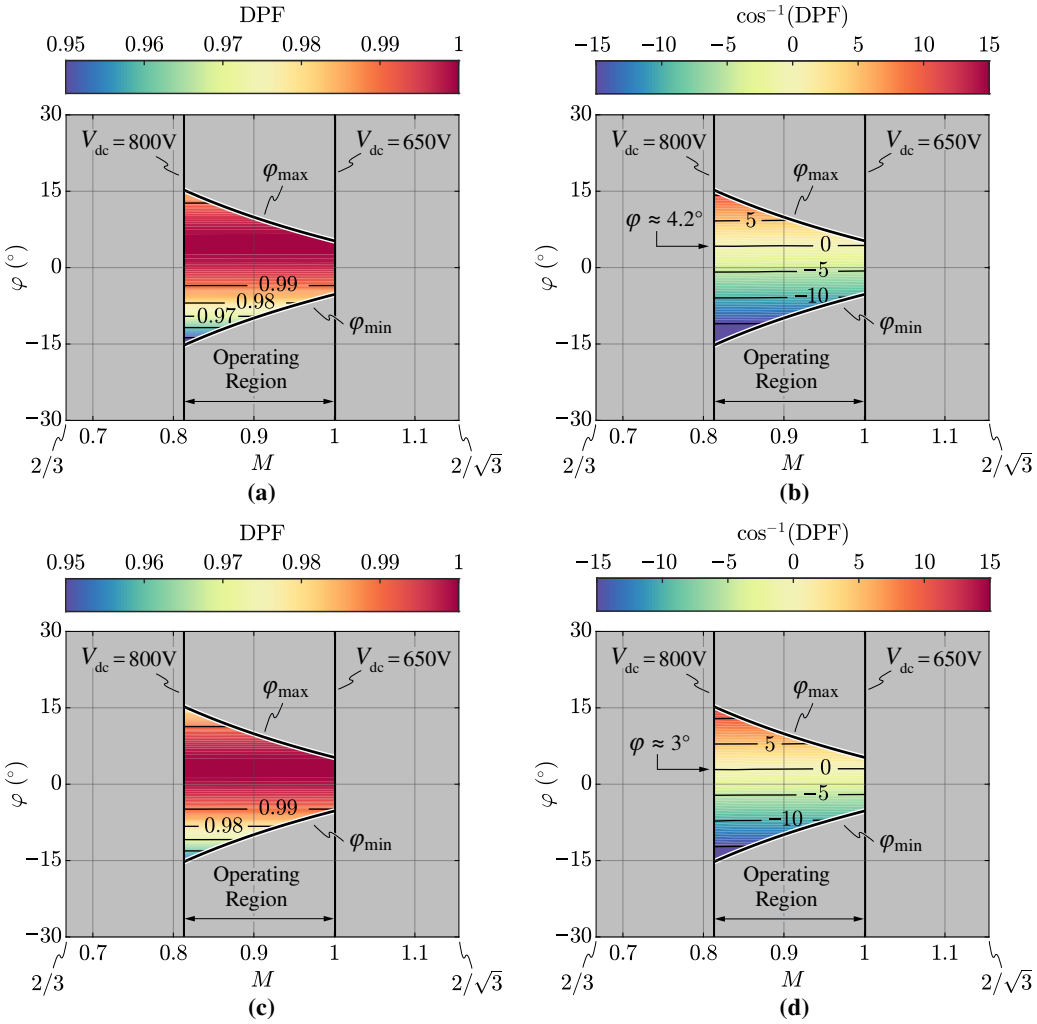

Figure 20. Experimental displacement power factor (DPF) (**a**,**c**) and DPF angle (**b**,**d**) for $S = 15\,\mathrm{kVA}$ (**a**,**b**) and $S = 30\,\mathrm{kVA}$ (**c**,**d**). The current flowing into the filter capacitor C_{f} is completely compensated for $\varphi \approx 4.2°$ in (**b**) and $\varphi \approx 3°$ in (**d**).

3.2.3. Maximum Mid-Point Current ($I_{m,max}$)

The maximum DC-link mid-point current capability of the rectifier ($I_{m,max}$) is assessed experimentally by operating the converter at 50% of the rated apparent power (i.e., $S = 15\,kVA$) and injecting a zero-sequence voltage equal to $v_{o,min}$. The results are illustrated in Figure 8b in Section 2.5, where they are normalized with respect to the converter-side peak current value I. It is observed that the theoretical and the experimental results are in close agreement, achieving a maximum deviation of 5% over the complete operating range of the rectifier. Therefore, the analytical $I_{m,max}$ formulas derived in Appendix A can be considered successfully verified.

3.2.4. Minimum Mid-Point Charge Ripple ($\Delta Q_{m,pp,min}$)

The minimum DC-link mid-point peak-to-peak charge ripple $\Delta Q_{m,pp,min}$ is assessed experimentally by operating the converter at 100% of the rated apparent power (i.e., $S = 30\,kVA$), injecting the zero-sequence voltage component $v_{o,3}$ defined by ZMPCPWM and saturating it according to the $v_{o,max/min}$ limits. In particular, the mid-point charge is obtained in post-processing as the integral of the measured mid-point current i_m. The results are illustrated in Figure 10b in Section 2.6, where they are normalized with respect to the converter-side peak phase current I and three-times the grid frequency $3f$. Additionally in this case, the theoretical and the experimental results are in close agreement; however, the value $\Delta Q_{m,pp,min}$ obtained experimentally does not reach 0 for $\varphi = 0$. This is mainly due to the converter-side current not being perfectly sinusoidal, as it features a slight zero-crossing distortion that yields a non-zero mid-point current local average (see Figure 15). Nevertheless, $\Delta Q_{m,pp,min} = 0$ can never be achieved in practice, as the switching-frequency mid-point current ripple (i.e., neglected in the theoretical model) yields a non-zero charge ripple: theoretical and experimental results at $\varphi = 0$ would only coincide for $f_{sw} = \infty$. Overall, the analytical $\Delta Q_{m,pp,min}$ formula derived in Appendix B can be considered successfully verified, achieving best estimation accuracy for systems with $f_{sw} \gg f$ (i.e., with high pulse ratios).

4. Conclusions

This paper has presented a comprehensive analysis and performance assessment of three-phase three-level unidirectional rectifiers under non-unity power factor operation and unbalanced split DC-link loading.

The complete analysis applies to all three-level unidirectional rectifiers and thus features a wide range of applications, e.g., active front ends for the supply of variable-speed drives, uninterruptible power supply systems, battery chargers, data centers and high-power DC loads. In particular, the ability to operate under non-unity power factor is becoming a desired feature of modern rectifiers, as distribution system operators worldwide are starting to charge end consumers for the excess reactive energy injected/withdrawn into/from the grid. In this scenario, properly controlled unidirectional rectifiers could support the reactive energy flows and potentially substitute traditional power factor correction capacitor banks, without requiring new or additional hardware. Furthermore, the ability to operate under unbalanced split DC-link loading is necessary when separate loads are connected to the rectifier DC-link halves, which is typically the case for modular high-power converters (e.g., the DC/DC stage of electric vehicle DC fast chargers).

Therefore, this paper has focused on analyzing, improving and extending the operation of three-phase three-level unidirectional rectifiers. First, the operational basics of three-level rectifiers have been recalled and the theoretical operating limits of the converter in terms of zero-sequence voltage, modulation index, power factor angle, DC-link mid-point current and minimum DC-link mid-point charge ripple have been derived. A unified carrier-based pulse-width modulation (PWM) approach aiming for the undistorted operation of the rectifier across all feasible operating conditions has been proposed, de facto enabling the converter operation under non-unity power factor and unbalanced split-DC-link loading. This approach, uniquely based on restraining (i.e., saturating) the zero-sequence voltage within its feasible limits, has been described in detail and its effects

on the DC-link mid-point current generation have been investigated. Furthermore, novel analytical expressions have been derived in the Appendix, defining the rectifier maximum mid-point current capability (i.e., directly linked to the converter DC-link load unbalance) and the minimum peak-to-peak DC-link mid-point charge ripple (i.e., allowing for the straightforward sizing of the DC-link capacitance value) over the complete converter operating region. Finally, the theoretical analysis has been successfully verified on a digitally controlled 30 kW T-type rectifier prototype operating at 20 kHz. The input phase current total harmonic distortion (THD), the maximum mid-point current capability and the minimum mid-point peak-to-peak charge ripple have been experimentally assessed across all rectifier operating points, demonstrating excellent performance and a high-level of agreement with the analytical predictions.

Author Contributions: Conceptualization, D.C.; methodology, D.C.; software, M.G., E.B.; validation, D.C., M.G., E.B. and F.M.; formal analysis, D.C.; investigation, D.C.; resources, F.M and R.B.; data curation, D.C., M.G., E.B. and F.M.; writing–original draft preparation, D.C.; writing–review and editing, D.C., M.G., E.B., F.M. and R.B; visualization, D.C.; supervision, F.M. and R.B; project administration, F.M. and R.B.; funding acquisition, R.B. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. Analytical Derivation of the Mid-Point Current Limits

The boundaries of the mid-point current periodical average I_m can be derived averaging the maximum and minimum feasible envelopes of i_m along the grid period, i.e., integrating (24) over $2\pi/3$. In particular, being the integrals of $i_{m,max}$ and $i_{m,min}$ identical but with opposite sign, the I_m limits are symmetrical:

$$I_{m,max} = -I_{m,min} = -\frac{3}{\pi V_{dc}} \int_0^{2\pi/3} \left[\sum_{x=a,b,c} v_x |i_x| + v_{o,min} \sum_{x=a,b,c} |i_x| \right] d\vartheta. \tag{A1}$$

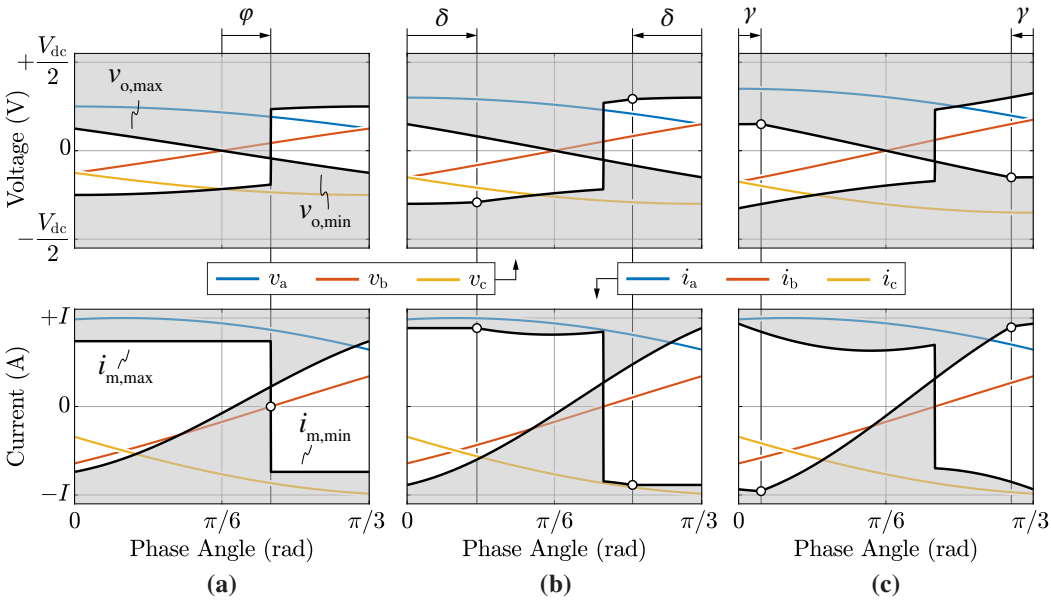

Figure A1. Zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ and mid-point current local average limits $i_{m,max}$, $i_{m,min}$ for **(a)** $M = 0.5$ (region ①), **(b)** $M = 0.6$ (region ②) and **(c)** $M = 0.7$ (region ③) assuming $\varphi = 10°$. The focus is on $0 \leq \vartheta \leq \pi/3$ to highlight the most relevant angle definitions for the analytical calculations (i.e., φ, δ, γ).

Due to the $2\pi/3$ periodicity of the first term, its integral is null, thus resulting in

$$I_{\mathrm{m,max}} = -\frac{3}{\pi V_{\mathrm{dc}}} \int_0^{2\pi/3} v_{\mathrm{o,min}} \left(|i_{\mathrm{a}}| + |i_{\mathrm{b}}| + |i_{\mathrm{c}}|\right) \mathrm{d}\vartheta. \tag{A2}$$

To ease the solution of (A2), it is worth observing that $i_{\mathrm{m,max}}$ for $0 \leq \vartheta \leq \pi/3$ is equal to $-i_{\mathrm{min}}$ for $\pi/3 \leq \vartheta \leq 2\pi/3$ (see Figures 6 and 7). Therefore, the integration interval may be restricted to $\vartheta \in [0, \pi/3]$ by considering both maximum and minimum i_{m} envelopes. A highlight of the waveforms within the selected integration interval is provided in Figure A1.

Therefore, leveraging the $v_{\mathrm{o,min}}$ definition and the signs of i_{a}, i_{b}, i_{c} inside the considered averaging window, different $I_{\mathrm{m,max}}$ expressions are obtained depending on the value of the modulation index. In particular, three main regions can be defined, as illustrated in Figure A2: region ① with $M < 1/\sqrt{3}$, region ② with $1/\sqrt{3} \leq M \leq 2/3$ (i.e., the transition region) and region ③ with $M > 2/3$. The current and voltage waveforms for regions ①, ② and ③ are reported in Figure A1a–c, respectively.

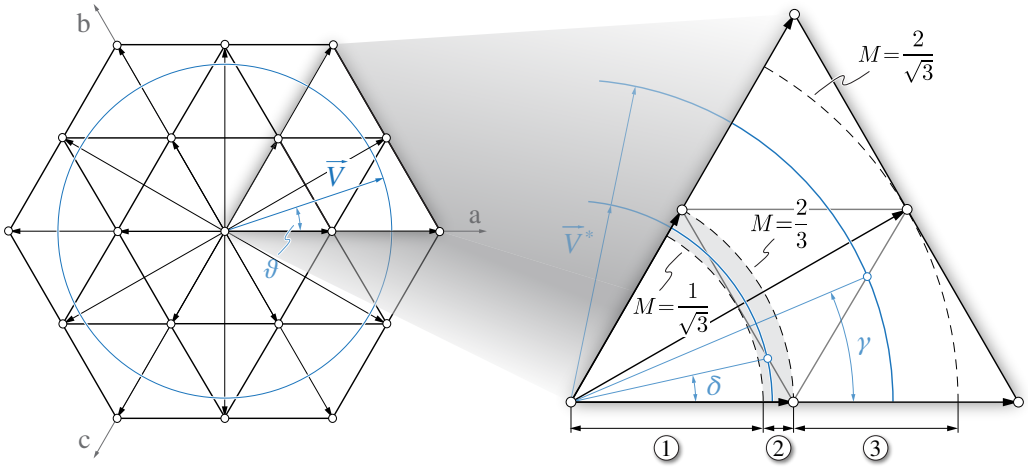

Figure A2. Overview of the modulation index regions ①, ② and ③ on the space vector diagram, focusing on $0 \leq \vartheta \leq \pi/3$. The transition region ② is highlighted in grey and the most significant angle definitions for the analytical calculations are indicated (i.e., ϑ, δ, γ).

The expressions of $I_{\mathrm{m,max}}$ are therefore:

$$I_{\mathrm{m,max,①}} = \frac{6}{\pi V_{\mathrm{dc}}} \left[\int_0^{\pi/6+\varphi} i_{\mathrm{a}} v_{\mathrm{a}} \, \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3} i_{\mathrm{c}} v_{\mathrm{b}} \, \mathrm{d}\vartheta - \int_0^{\pi/6+\varphi} i_{\mathrm{a}} v_{\mathrm{b}} \, \mathrm{d}\vartheta + \int_{\pi/6+\varphi}^{\pi/3} i_{\mathrm{c}} v_{\mathrm{c}} \, \mathrm{d}\vartheta \right], \tag{A3}$$

valid for $M < 1/\sqrt{3}$,

$$I_{\mathrm{m,max,②}} = \frac{6}{\pi V_{\mathrm{dc}}} \left[- \int_0^{\pi/6+\varphi} i_{\mathrm{a}} v_{\mathrm{b}} \, \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3-\delta} i_{\mathrm{c}} \left(\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{a}} \right) \mathrm{d}\vartheta + \int_{\pi/3-\delta}^{\pi/3} i_{\mathrm{c}} v_{\mathrm{c}} \, \mathrm{d}\vartheta + \right.$$
$$\left. + \int_0^{\delta} i_{\mathrm{a}} v_{\mathrm{a}} \, \mathrm{d}\vartheta + \int_{\delta}^{\pi/6+\varphi} i_{\mathrm{a}} \left(\frac{V_{\mathrm{dc}}}{2} + v_{\mathrm{c}} \right) \mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3} i_{\mathrm{c}} v_{\mathrm{b}} \, \mathrm{d}\vartheta \right], \tag{A4}$$

valid for $1/\sqrt{3} \leq M \leq 2/3$, and

$$I_{\mathrm{m,max,③}} = \frac{6}{\pi\, V_{\mathrm{dc}}}\left[\int_0^{\pi/6+\varphi} i_{\mathrm{a}}\left(\frac{V_{\mathrm{dc}}}{2}+v_{\mathrm{c}}\right)\mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3-\gamma} i_{\mathrm{c}}\, v_{\mathrm{b}}\,\mathrm{d}\vartheta - \int_{\pi/3-\gamma}^{\pi/3} i_{\mathrm{c}}\left(\frac{V_{\mathrm{dc}}}{2}+v_{\mathrm{c}}\right)\mathrm{d}\vartheta + \right.$$
$$\left. + \int_0^{\gamma} i_{\mathrm{a}}\left(\frac{V_{\mathrm{dc}}}{2}-v_{\mathrm{a}}\right)\mathrm{d}\vartheta - \int_{\gamma}^{\pi/6+\varphi} i_{\mathrm{a}}\, v_{\mathrm{b}}\,\mathrm{d}\vartheta - \int_{\pi/6+\varphi}^{\pi/3} i_{\mathrm{c}}\left(\frac{V_{\mathrm{dc}}}{2}-v_{\mathrm{a}}\right)\mathrm{d}\vartheta\right], \quad \text{(A5)}$$

valid for $M > 2/3$. The angles δ, γ are graphically illustrated in Figures A1 and A2, and their expression is obtained by setting $v_{\mathrm{a}} = v_{\mathrm{c}} + V_{\mathrm{dc}}/2$ and $v_{\mathrm{a}} - V_{\mathrm{dc}}/2 = v_{\mathrm{b}}$, respectively, as

$$\delta = \frac{\pi}{6} - \cos^{-1}\left(\frac{1}{\sqrt{3}M}\right) \qquad \frac{1}{\sqrt{3}} \leq M \leq \frac{2}{3}, \quad \text{(A6)}$$

$$\gamma = \frac{\pi}{3} - \sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) \qquad M \geq \frac{2}{3}. \quad \text{(A7)}$$

Finally, substituting (3), (5), (A6), (A7) into (A3)–(A5) and solving the integral terms, the following analytical expressions are obtained:

$$I_{\mathrm{m,max,①}} = \frac{3}{\pi}\, I\, \frac{M}{4}\cos\varphi\left(\pi + \sqrt{3} - 2\sqrt{3}\,\varphi\,\tan\varphi\right) \quad \text{(A8)}$$

valid for $M < 1/\sqrt{3}$ and

$$I_{\mathrm{m,max,②}} = I_{\mathrm{m,max,③}} = \frac{3}{\pi}\, I\left[1 + \frac{1}{2M}\cos\varphi\left(\sqrt{3M^2-1} - \frac{1}{\sqrt{3}}\right) + \right.$$
$$\left. + \frac{M}{2}\cos\varphi\left(3\,\sin^{-1}\left(\frac{1}{\sqrt{3}M}\right) - \pi - \frac{\sqrt{3}}{2} - 2\sqrt{3}\,\varphi\,\tan\varphi\right)\right] \quad \text{(A9)}$$

valid for $M > 1/\sqrt{3}$. Expressions (A8) and (A9) are graphically illustrated in Figure A3, where the modulation index regions ①, ② and ③ are also indicated.

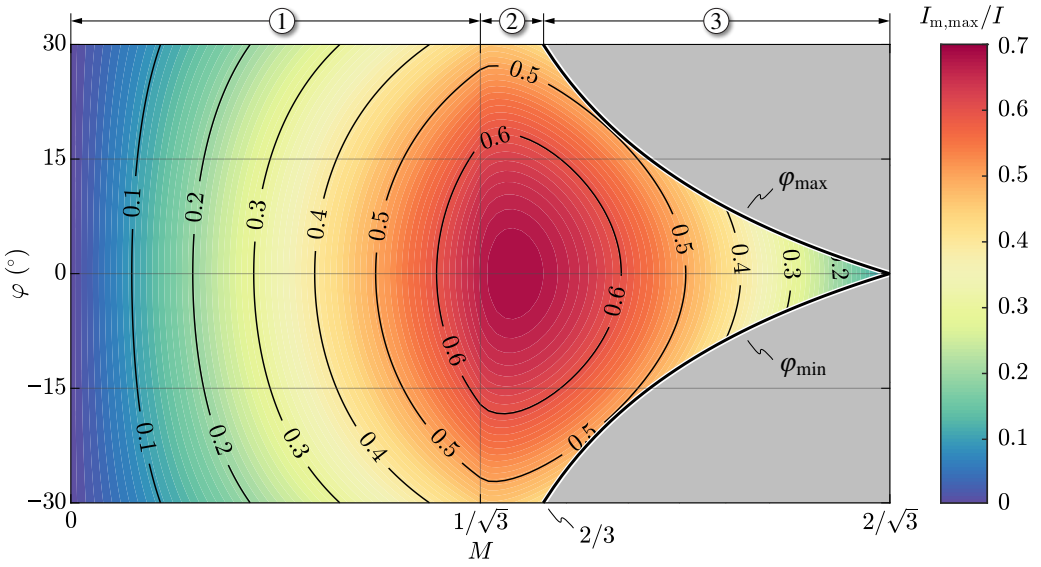

Figure A3. Maximum mid-point current periodical average $I_{\mathrm{m,max}}$ (i.e., normalized with respect to the peak phase current I) as a function of the modulation index M and the converter-side power factor angle φ. The three modulation index regions ①, ② and ③ are indicated.

It is worth noting that this analytical derivation extends the approach reported in [16], where the mid-point current periodical average limits are derived uniquely for $\varphi = 0$.

Appendix B. Analytical Derivation of the Minimum Mid-Point Charge Ripple

To identify the minimum value of DC-link mid-point peak-to-peak charge ripple $\Delta Q_{m,pp}$, the zero mid-point current modulation (ZMPCPWM) is considered, therefore the third-harmonic zero-sequence voltage reported in (26) is added to the phase voltage references. Figure A4 shows the zero-sequence voltage v_o waveform and the mid-point current local average i_m waveform for $M = 0.8$ and $\varphi = 15°$. In particular, it is observed that the zero-sequence voltage saturation occurring for $\varphi \neq 0$ causes a deviation of the mid-point current average, which in turn leads to a non-zero $\Delta Q_{m,pp}$.

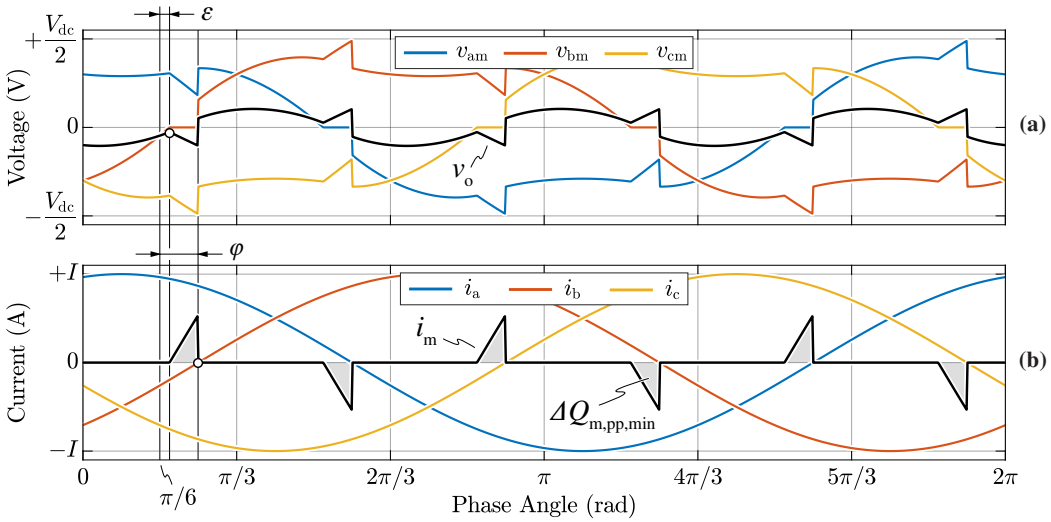

Figure A4. Zero-sequence voltage v_o (**a**) and mid-point current local average i_m (**b**) for $M = 0.8$ (region ③) and $\varphi = 15°$. Zero mid-point modulation (ZMPCPWM) is adopted. The most relevant angle definitions for the analytical calculations (i.e., φ, ε) are indicated.

Figure A4 also shows that when ZMPCPWM is adopted, $i_m \geq 0$ within $0 \leq \vartheta \leq \pi/3$, thus leading to a simplified expression of the mid-point charge ripple:

$$\Delta Q_{m,pp} = \frac{1}{2\pi f} \int_0^{\pi/3} i_m \, d\vartheta, \tag{A10}$$

Therefore, due to i_m being null for most of the period, the minimum $\Delta Q_{m,pp}$ can be calculated by restricting the integration interval to

$$\Delta Q_{m,pp,min} = \frac{1}{2\pi f} \int_{\pi/6+\varepsilon}^{\pi/6+\varphi} i_m \, d\vartheta = -\frac{1}{\pi f V_{dc}} \int_{\pi/6+\varepsilon}^{\pi/6+\varphi} \left[\sum_{x=a,b,c} v_x |i_x| + v_{o,min} \sum_{x=a,b,c} |i_x| \right] d\vartheta, \tag{A11}$$

where i_m has been substituted with (16), $v_o = v_{o,min}$ within $\pi/6 + \varepsilon \leq \vartheta \leq \pi/6 + \varphi$, and ε is obtained by setting $v_{o,3} = -v_b$, as

$$\varepsilon = \frac{1}{2}\left[\varphi - \frac{\pi}{2} + \cos^{-1}\left(\frac{1}{2}\sin\varphi\right)\right]. \tag{A12}$$

Finally, substituting (3), (5), (A12) into (A11) and solving the integral terms, the following analytical expression is obtained:

$$\Delta Q_{\mathrm{m,pp,min}} = \frac{\sqrt{3}}{8\pi f} IM \left[\sqrt{4 - \sin^2\varphi} - 2\cos\varphi - \sin\varphi \left(\cos^{-1}\left(\frac{\sin\varphi}{2} \right) - \frac{\pi}{2} - \varphi \right) \right], \quad \text{(A13)}$$

valid for the complete modulation index range $0 \leq M \leq 2/\sqrt{3}$. Expression (A13) is illustrated in normalized form in Figure A5, where the modulation index regions ①, ② and ③ are also indicated.

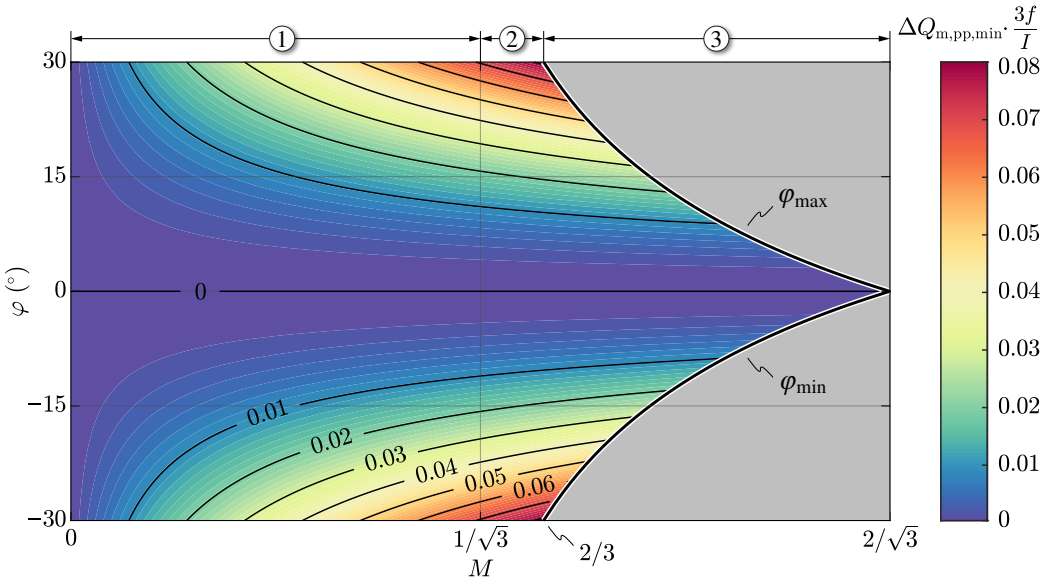

Figure A5. Minimum DC-link mid-point charge ripple $\Delta Q_{\mathrm{m,pp}}$ (i.e., normalized with respect to the peak phase current I and three-times the grid frequency $3f$) as a function of the modulation index M and the converter-side power factor angle φ. The three modulation index regions ①, ② and ③ are indicated.

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