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Application of Scattering Parameters to DPL Time-Lag Parameter Estimation at Nanoscale in Modern Integration Circuit Structures

Mariusz Zubert *, Zbigniew Kulesza, Mariusz Jankowski and Andrzej Napieralski

Department of Microelectronics and Computer Science—DMCS, Lodz University of Technology, 90-924 Lodz, Poland; zbigniew.kulesza@p.lodz.pl (Z.K.); mariusz.jankowski@p.lodz.pl (M.J.); andrzej.napieralski@p.lodz.pl (A.N.)

* Correspondence: mariusz.zubert@p.lodz.pl

Abstract: This paper presents the methodology of material parameters' estimation for the dual-phase-lag (DPL) model at the nanoscale in modern integration circuit (IC) structures. The analyses and measurements performed were used in the unique dedicated micro-electro-mechanical system (MEMS) test structure. The electric and thermal domain of this structure was analysed. Finally, the silicon dioxide (SiO_2) temperature time-lag estimation procedure is presented based on the scattering parameters measured by a vector network analyser for the considered MEMS structure together with the 2-omega method. The proposed methodology has the ability to estimate the time-lag parameter with high accuracy and is also suitable for the temperature time-lag estimation for other manufacturing process technologies of ICs and other insulation materials used for integrated circuits such as silicon nitride (Si_3N_4), titanium nitride (TiN), and hafnium dioxide (HfO_2).

Keywords: dual-phase-lag heat transfer model; no-mesh FDM; *S*-parameters measurements; scattering parameters; DPL time lag estimation; multi-domain modelling; material parameter estimation; heat transfer at the nanoscale

Citation: Zubert, M.; Kulesza, Z.; Jankowski, M.; Napieralski, A. Application of Scattering Parameters to DPL Time-Lag Parameter Estimation at Nanoscale in Modern Integration Circuit Structures. *Energies* **2021**, *14*, 4425. https://doi.org/10.3390/en14154425

Academic Editor: Andras Poppe

Received: 15 June 2021
Accepted: 20 July 2021
Published: 22 July 2021

1. Introduction

The modelling and analysis of thermal and electromagnetic phenomena in integrated circuits (ICs) have great significance for the reliable design of modern nanoscale electronic structures and micro-electro-mechanical systems (MEMSs). It is also highly recommended to use this approach during various design-related activities. The most important of them are as follows: continuous decrease of semiconductor technology nodes, design cost reduction of microelectronic systems, and application of modern transistors in ICs (e.g., a fin field-effect transistor—FinFET [1,2], a gate-all-around field-effect transistor—GAAFET [3], and a vertical-slit field-effect transistor—VeSFET [4]).

Therefore, the presented work focuses on the following issues:

- The effective modelling and simulation methods of electromagnetic (EM) and thermal phenomena of integration circuits, micro-electro-mechanical systems (MEMSs), and 3D integrated systems (see [1,5]).
- The design of an equivalent electric circuit extractor and electrical simulation tools, e.g., [2,6,7].
- The verification of new simulation tools dedicated for the design of experimental application specific integrated circuits (ASICs).
- Estimation of IC material parameters for the nanometric technologies.

The first and last issues will be presented in the paper and are performed on scattering parameters measurements of a designed MEMS test structure with a printed circuit board (PCB) test board.

2. Heat Transfer at the Nanoscale

The heat transfer problems in solids can be described using Fourier's theory [8,9]. The mathematical description is based on Fourier's law and the Fourier–Kirchhoff (FK) equation and can be expressed as follows:

$$\begin{cases} c_v \frac{\partial T(\mathbf{x},t)}{\partial t} = -\nabla \cdot \mathbf{q}(\mathbf{x},t) + q_v(\mathbf{x},t) \\ \mathbf{q}(\mathbf{x},t) = -k \cdot \nabla T(\mathbf{x},t) \end{cases} \quad \text{for } x \in R^n, n \in N, t \in R_+ \cup \{0\} \tag{1}$$

where $\mathbf{q}$ is heat flux vector; k is material thermal conductivity; T is distributed temperature; and c_v and q_V are volumetric heat capacity and value of internally generated heat, respectively. The FK equation has been commonly used to describe heat flow for over two centuries. However, the application of the FK equation has some significant limitations at the nanoscale [10].

The main limitation is related to the assumption of the infinite heat flow velocity in the semiconductor structure, which is very important in the case of nanostructures with a Knudsen number of Kn < 0.1 (where the characteristic length of IC is ca. ten times longer than the heat carrier mean free path 41.8 nm at 300 K [8]). Furthermore, the simultaneous change of temperature gradient and heat flux is a non-physical behaviour [9–13]; these phenomena have been presented in the case of nanosized structures in [8]. The second problem is associated with the radiative heat transfer and the Casimir effect (i.e., photons tunnelling) [14,15]; these phenomena occur in MEMSs [16] at small distances between surfaces (or particles). Both phenomena cause more dynamic and intense heat transfer than the classical Fourier–Kirchhoff and radiation models.

The new and more general dual-phase-lag (DPL) model of heat flow in solids at the nanoscale was introduced by Tzou [17,18] and is described with the following equations:

$$\begin{cases} c_v \frac{\partial T(\mathbf{x},t)}{\partial t} = -\nabla \cdot \mathbf{q}(\mathbf{x},t) + q_v(\mathbf{x},t) \\ \mathbf{q}(\mathbf{x},t) + \tau_q \frac{\partial \mathbf{q}(\mathbf{x},t)}{\partial t} = -k \nabla T(\mathbf{x},t) - \tau_T k \nabla \frac{\partial T(\mathbf{x},t)}{\partial t} \end{cases} \tag{2}$$

or

$$\tau_q c_v \frac{\partial^2 T(\mathbf{x},t)}{\partial t^2} + c_v \frac{\partial T(\mathbf{x},t)}{\partial t} = k \Delta T(\mathbf{x},t) + \tau_T k \frac{\partial \Delta T(\mathbf{x},t)}{\partial t} + q_v(\mathbf{x},t) + \tau_q \frac{\partial q_v(\mathbf{x},t)}{\partial t} \tag{3}$$

where τ_T and τ_q are temperature time-lag and heat flux time-lag, respectively. The simplified version of the DPL heat transfer model can be obtained for one time-lag parameter τ_q for $\tau_q > 0$ and $\tau_T = 0$. This equation was proposed by Cattaneo and Vernotte (CV) in [19–26] and is also used to eliminate the paradox of the heat-flux infinite velocity transfer.

The comprehensive presentation of the DPL model aspects is included in the following published sources:

- Modified boundary conditions, the DPL model simplification, and numerically effective 3D harmonic temperature models' representation were presented in [1];
- Internal heat generation source analysis and its realistic approximation were presented in Appendix A and [19] (pp. 12–13 in Appendix A);
- Detailed analysis of anomalies and intriguing behaviours of the CV, DPL, and FK models were discussed by Vermeersch and De Mey, as well as Kovács and Ván, in [1,27–29] and [25];
- Material parameters are collected in [1,30];
- Detailed description of the most commonly used heat transfer models at the nanoscale was presented in [16] (pp. 1–4) [22–24,30].

The DPL model can be used to describe heat transfer behaviour in various solid materials (e.g., metals, bulk crystals, dielectrics, and amorphous materials). For most of them, indicative dual-phase time-lag parameters values (τ_T, τ_q) can be approximated using theoretical formulas [1]. Unfortunately, these parameters are strictly dependent on material

density, fractal dimensions of material structure [30], and so on. Therefore, the values of the time-lag parameters should be empirically and independently characterised for each IC and MEMS technology process types. It is possible to perform empirical measurements of their values using a unique tool based on the femtosecond pulse laser with reflection mirrors for the following:

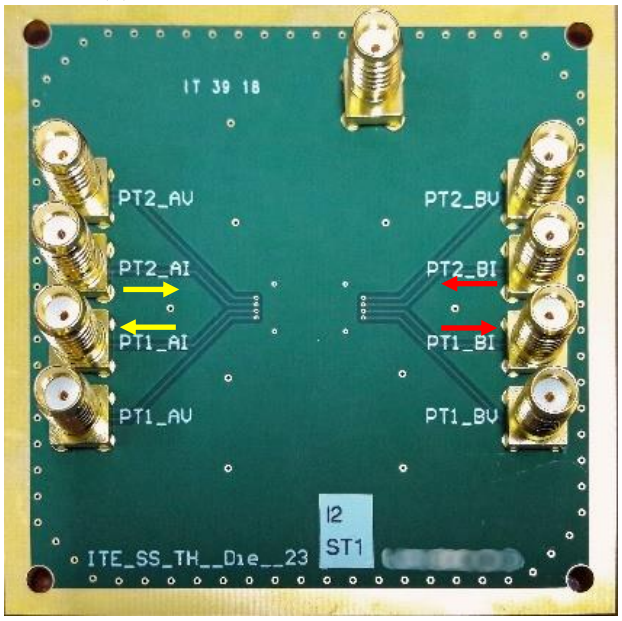
- Thin metals (Brorson et al. [31,32]; Elsayed-Ali [33]; and Qiu et al. [34–37]);
- No crystalline and amorphous materials (Fournier and Boccara [38]).

However, the test probes used for this purpose should be prepared not exactly like real structures in ICs and MEMSs. The first investigation of the dual-phase time-lag parameters estimation using dedicated MEMS structures with a measurement system implemented on a PCB was depicted in [39–43]. The authors of this paper propose the scattering wave parameters presented in [2] to extract the value of the dual-phase time-lag parameter τ_T.

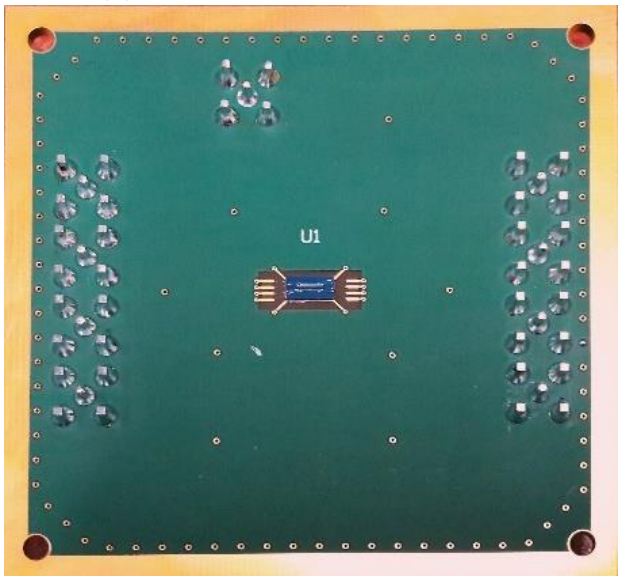
3. Test Structure

The DPL model was verified using a dedicated test structure containing a 104 nm thin silicon oxide layer (SiO_2: ε_r = 3.9 [44,45], we assume a constant value up-to 13.5 GHz based on [46]; tan δ = 0.0002 [47]) placed between two platinum resistors (the top resistor: Pt: W_{top} = 2.75 µm, thickness h = 150 nm, length L = 460 µm, resistance R_{top} = 155 Ω at 20 °C [39,48,49]; the bottom resistor: Pt, W_{bottom} = 4.96 µm, thickness h = 150 nm, length L = 460 µm, resistance R_{bottom} = 262.3 Ω at 20 °C [39,48,49]). Generally, each resistor could be used either as a heat source line or a temperature sensor. The bottom resistor is treated as a heater, and the upper resistor is a temperature sensor. Each resistor has a four-wire connection for independent measurements of voltage and current. These elements are placed on a 100 nm wide silicon dioxide (SiO_2) layer stacked on a 400 µm thick silicon layer. The test structure presented in Figure 1c was manufactured in MEMS technology by the Institute of Electron Technology (ITE) in Warsaw, Poland [39–45]. The bottom and upper resistor dependence on temperature and their temperature rise dependence on heating power were measured and characterised in [39,40]. The entire structure is bonded to a metal copper foil on a PCB test board (Figure 1a,b).

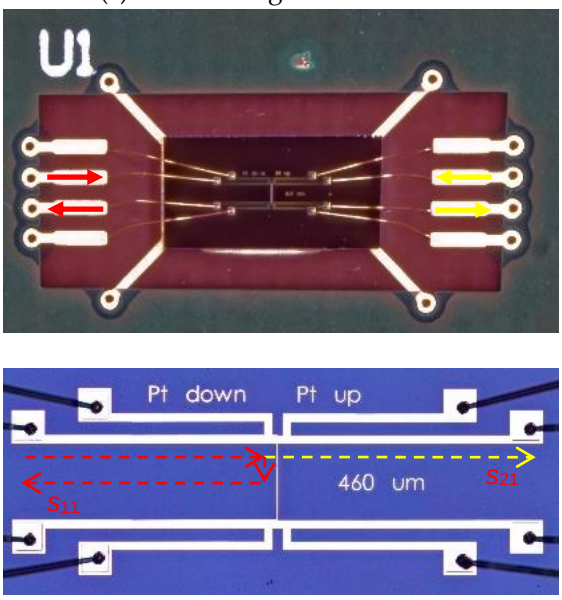
(**a**) PCB front side



(**b**) PCB back-side



(**c**) MEMS integrated structure



(**d**) The cross-section of MEMS structure (not to scale)

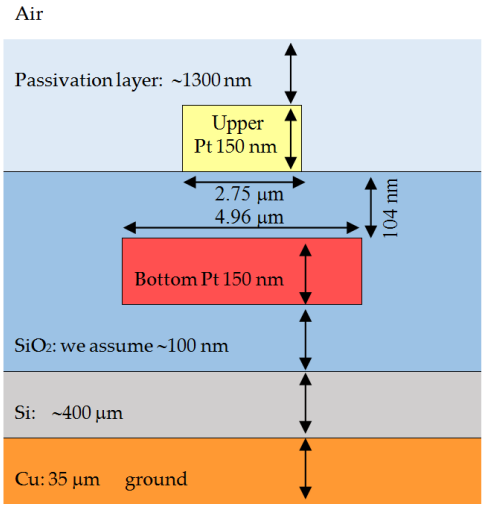


Figure 1. The micro-electro-mechanical systems (MEMS) test structure (**c**) is bonded to the test boards (**a**,**b**). The simplified cross-section of the MEMS structure is presented in (**d**). PCB, printed circuit board.

4. Test Structure Models and Measurement Process

4.1. Thermal Model

The 2D DPL thermal model of the MEMS test structure is described with the application of the harmonic temperature models proposed in [1]:

$$\begin{cases} k\beta\,\Delta T_r - k\gamma\,\Delta T_i + \frac{g_0}{\sqrt{2}} = -\omega c_v T_i \\ k\beta\,\Delta T_i + k\gamma\,\Delta T_r = \omega c_v T_r \end{cases} \quad (4)$$

$$\beta = \frac{1+\tau_T\tau_q\omega^2}{1+\tau_q^2\omega^2};\ \gamma = \frac{(\tau_T-\tau_q)\omega}{1+\tau_q^2\omega^2} \quad (5)$$

where $\underline{T} = \underline{T}(x,y,z) = T_r + jT_i \in Z$ is harmonic temperature field distribution for angular frequency $\omega = 2\pi f$, associated with the temperature in the following way:

$$T(x,y,z,t) = T_m(x,y,z)\ \sin(\omega t + \varphi(x,y,z)) = \mathrm{Im}\left[\sqrt{2}\,\underline{T}(x,y,z)\ \exp(j\omega t)\right] \quad (6)$$

$$\sqrt{2}\,\underline{T}(x,y,z) = T_m(x,y,z)\ \exp(j\varphi(x,y,z)) \quad (7)$$

Moreover, T_m and φ are amplitude and phase-shift for a given angular frequency, respectively. Please note that the maximal complex values of the harmonic temperature field are taken into consideration; thus, the coefficient $\sqrt{2}$ is introduced in Equations (4)–(7). The dissipated heat power generation per unit volume in the bottom resistor ($g_0 > 0$) is described in Appendix A. The heat power generation outside the bottom resistor is equal to zero $g_0 = 0$ W/m^3. The following boundary conditions were applied:

- The upper side of the structure—the heat-free convection is encoded using Neumann boundary condition with a heat transfer coefficient equal to 658.763 W/(m^{2}K).
- The left and right side of the structure—the symmetry is applied using Neumann boundary conditions.
- The Dirichlet boundary condition for the bottom side of the structure $T_r = T_{ambient}$, $T_i = 0$.

The material parameters are included in Table 1. In addition, calculated temperature distributions for 10 Hz, 1 kHz, 100 kHz, and 1 GHz are presented in Table 2.

Table 1. Considered material parameter values based on [1,30].

Material Name	k [$\frac{W}{m \cdot K}$]	c_v[$\frac{kg}{m^3 K}$]	τ_q [ns]	τ_T [ns]
Silicon (Si)	160	1.78×10^6	3	120
Silicon dioxide (SiO_2)	1.38	1.65×10^6	3	predicted: 50–120
Platinum (Pt)	71.6	2.85×10^6	0.0916	2.6×10^{-12}

Table 2. The equivalent resistance and inductance of transmission line for low frequencies up to 1 MHz.

Conductor	Equivalent Resistance	Equivalent Inductance
Top resistor (Pt, W_{top} = 2.75 µm., h = 150 nm, L = 460 µm)	155 Ω at 20 °C 0.3045 T_{top} + 147.4524 Ω [44]	6.91443×10^{-10} H
Bottom resistor (Pt, W_{bottom} = 4.96 mm., h = 150 nm, L = 460 µm)	262.3 Ω at 20 °C 0.5064 T_{bottom} + 249.6276 Ω [44]	5.81732×10^{-10} H
PCB ground (Cu, W_{ground} = 200 µm, h = 35 µm, L = 460 µm, $\rho_{Cu} = 1.72 \cdot 10^{-8}$ Ωm^{-1})	1.13 mΩ	2.62057×10^{-10} H
Equivalent capacitances and mutually coupled inductances: $L_{top\text{-}bottom} = 5.25685 \times 10^{-10}$ H, $L_{top\text{-}ground} = 1.90503 \times 10^{-10}$ H, $L_{bottom\text{-}ground} = 1.90799 \times 10^{-10}$ H, $C_{top\text{-}bottom} \approx 0.56405 \times 10^{-12}$ F, $C_{bottom\text{-}ground} \approx 0.631304 \times 10^{-15}$ F.		

As can be observed in Figure 2, the changes of temperature amplitude $|\underline{T}(x,y,f)|$ in SiO_2 are located around the bottom heating resistor at f = 100 MHz and higher frequencies. Therefore, SiO_2 thermal characterisation should be performed for $f \geq 100$ MHz. Consequently, the simulations were carried out for the frequency in the range f = 200–900 MHz.

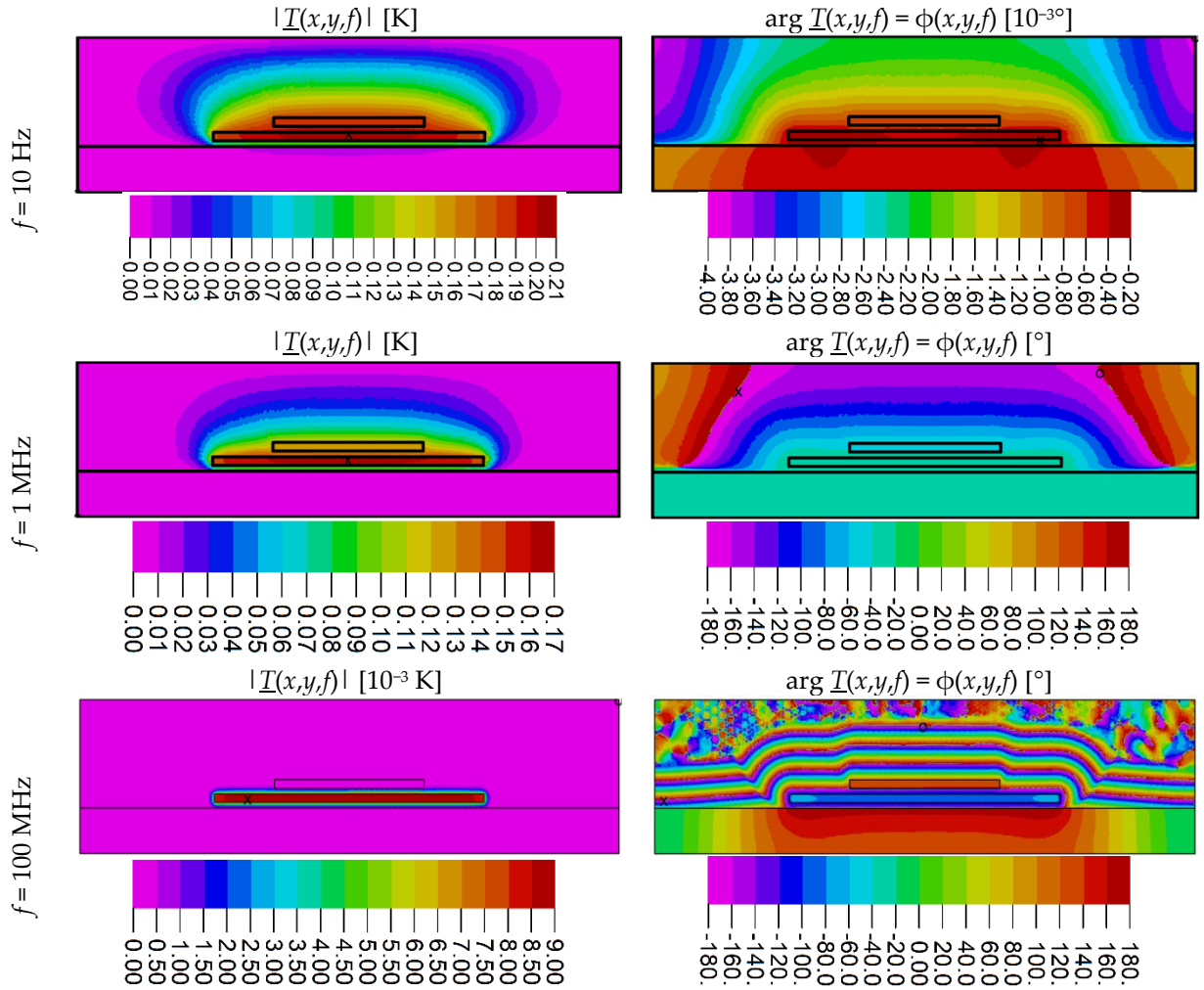


Figure 2. The amplitude of the harmonic temperature field obtained for $g_{bottom}/2^{1/2}$ = 262.3 Ω·(5 mA)^2/($2^{1/2}W_{bottom}$ t_{bottom} L), τ_T = 60 ns, τ_q = 3 ns, and f ∈ {10 Hz, 1 MHz, 100 MHz}, mesh nodes: 12,807.

Values of a temperature time-lag and a heat flux time-lag for bulk SiO_2 material have been proposed in the literature equal to $\tau_T \approx 60$ ns and $\tau_q \approx 3$ ns, respectively (see [1,30]). Nevertheless, we also have to determine this value for the ITE process technologies. We want to propose a methodology of the DPL time lag estimation for other insulation materials applied in the integrated circuits, such as silicon nitride (Si_3N_4), titanium nitride (TiN), hafnium dioxide (HfO_2), and others. Thus, numerous simulations were carried out for the temperature time-lag-delay parameter in the range τ_T = 50–120 ns to find the estimated value.

The experiments and analyses carried out by Tomasz Raszkowski in his PhD thesis [50,51], concerning the transformation of the DPL equation into the Grünwald–Letnikov fractional space-derivative dual-phase-lag equation [16,46,47], indicate a lower influence of the heat flux time lag parameter τ_q for the whole thermal system response than for the temperature time lag parameter τ_T.

The analysis of the influence of time lag differences τ_T-τ_q [1] (pp. 140—Figure 2, pp. 143—Figures 5 and 6, pp. 142—Table 2) as well as the total thermal delay of complex IC thermal system [1] (pp. 151, see Table 6) show that the heat-flux time lag parameter is less critical than the temperature-time lag for final thermal system response. Therefore, we adopted its value equal to $\tau_q \approx 3$ ns, as proposed in the literature. Simulations were carried out and are presented in Figure 3. It can be noticed that the most significant change in the phase of temperature depending on the time-lags is recognised at the frequency range

near 300 MHz and 500 MHz. However, the most significant amplitude of temperature changes on the upper resistor is observed close to the lower frequency $f \approx 300$ MHz (see Figure 3a). Therefore, the highest sensitivity of time-lag estimation is at $f \approx 300$ MHz. Finally, $f \approx 300$ MHz frequency neighbourhood, in the range of τ_T = 50–120 ns and $\tau_q \approx 3$ ns, was selected as the best parameter value set for further investigation (Figure 4b).

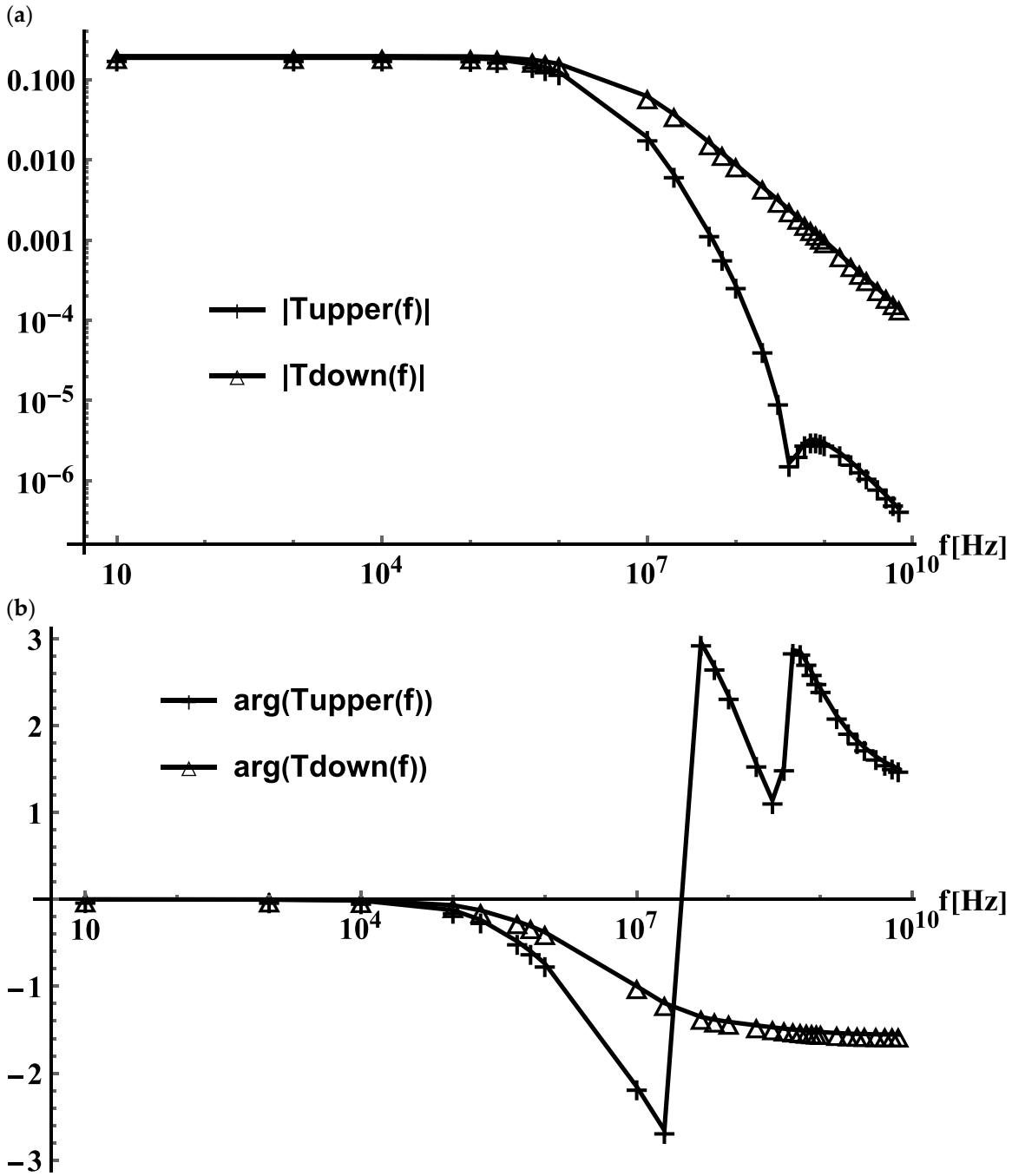


Figure 3. (**a**) The average value of | T(x,y,f) | in the upper and bottom resistor. (**b**) The average value of arg T(x,y,f) in the upper and bottom resistor.

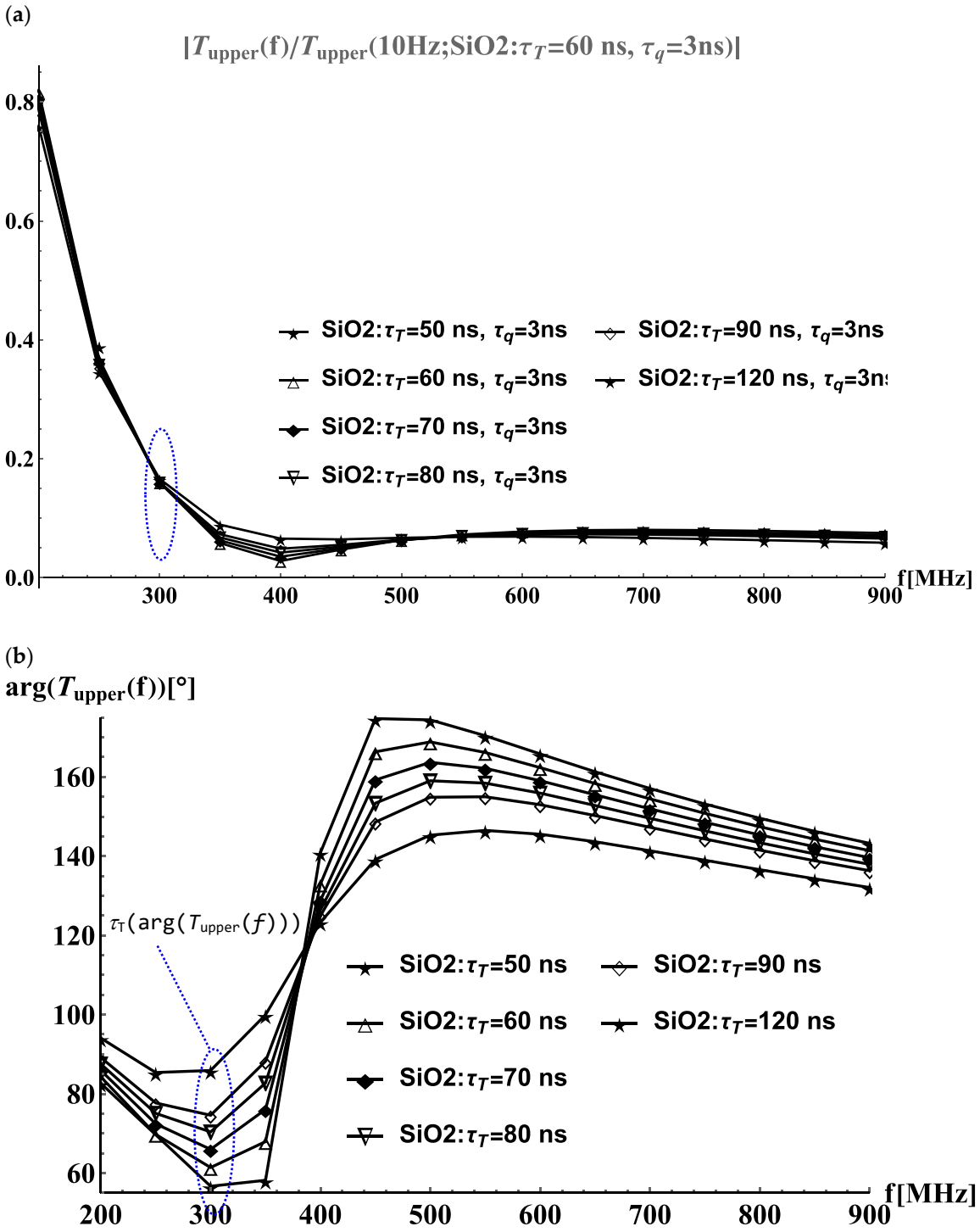


Figure 4. (**a**) The variation in mean temperature across the upper resistor normalised to its temperature at f = 10 MHz. (**b**) The variation in phase-shift of temperature across the upper resistor relative to temperature time-lag of SiO_2.

Next, based on the collected simulation results, the linear regression was used to model the relationship between the temperature time-lag τ_T and the averaged phase-shift of the upper resistor temperature arg $\underline{T}(x,y,f)$. The function

$$\tau_T|_{f\,=\,300\text{MHz}} \;=\; 2.391746\;(\pm 0.064775)\cdot\arg\left(T_{\text{upper}}\right) - 87.07922(\pm 4.52158)\;[\text{ns},^\circ] \qquad (8)$$

is used for the analysed MEMS test structure, which is presented in Figure 1c ($\tau_T \in$ (50 ns, 120 ns) and τ_q = 3 ns) with R^2 = 0.999774.

4.2. Electrical Analysis and Final Measurement Procedure

The electrical behaviour or the MEMS test structure (Figure 1c) was determined using the Vector Network Analyzer PNA-X Microwave Agilent N5242A after application of the de-embedding procedure [2]. The electrical reference planes were set to the test board SMA (SubMiniature version A) connectors using Agilent N4691B Electronic Calibration Module. All non-utilised connectors were terminated. The complex scattering parameters (s_{11}, s_{12}, s_{21}, s_{22}) have to be measured at 32,000 spot frequency points in the range 10 kHz–15 GHz using 50 Ω characteristic impedance of the measurement equipment.

The analysis of the electric behaviour of the MEMS test structure (Figure 1d) and the PCB test board is based on the previous study about transmission lines presented in [2]. Therefore, the following conclusions were derived for the chosen frequency close to $f \approx 300$ MHz:

- The upper and lower resistor lengths are very short compared with the wavelength at $f \approx 300$ MHz. Therefore, the distributed character of both resistors shall be taken into account for $f > c/(20\ L\ \varepsilon_r{}^{-1/2}) \approx 64$ GHz, where c is the speed of the light in the vacuum, and the relative electric permittivity of SiO_2 is equal to $\varepsilon_r \approx 3.9$. Consequently, only a de-embedded procedure for a PCB is required for the PCB transmission lines' elimination [2].
- The investigation presented in [2] shows that the eddy-current losses (and skin effect) in a conductor and dielectric losses can be neglected with a 1.4% error up to 10 GHz and an error lower than 0.3% up to 2 GHz.
- The extracted parasitic parameters in Table 2 show that inductance and capacitance can be neglected for $f \approx 300$ MHz.
- It should also be noted the self-heating can be neglected for a small current flowing through the platinum resistor (e.g., $I_{bottom} \leq 5$ mA [44]).
- As can be noticed, the application of the network analyser allows for the direct measurement of the power wave transmitted through the MEMS test structure $s_{12} = s_{21}$, which represents the insertion loss of the analysed network. To determine the temperature time-lag delay, we used the s_{21} measurements for a frequency close to $f = 150$ MHz ($n = 21$ spot frequency points in the range 145 MHz $\leq f \leq$ 155 MHz) and determined the averaged value and standard deviation of this parameter $\arg(s_{21}) = 62.3219\ (\pm 0.676051)^\circ$ at $f = 150$ MHz, with the sum of error squares (SS) = 9.01973 and degrees of freedom (DOFs) = 21 (see Figure 5). Finally, the temperature time-lag delay can be calculated from Equation (8):

$$\tau_T = 61.9791(\pm 1.61694)\ \text{ns at } f = 300\ \text{MHz} \quad (9)$$

4.3. Results and Discussions

As can be observed in Figure 2, the changes of temperature amplitude $|\underline{T}(x,y,f)|$ in SiO_2 are localised around the bottom heating resistor at $f = 100$ MHz and higher frequencies. Therefore, SiO_2 thermal characterisation should be performed for $f \geq 100$ MHz.

Based on the simulation, it can be noticed that the best scopes for which we obtain the highest sensitivity of the measurement method are the frequency range near 300 MHz to 500 MHz (see Figure 4). However, the most significant amplitude of temperature changes on the upper resistor is observed close to the lower frequency $f \approx 300$ MHz (Figure 3a).

Next, based on the collected simulation results, the linear regression was used to model the relationship between the temperature time-lag τ_T and the averaged phase-shift of the upper resistor temperature $\arg \underline{T}(x,y,f)$ in the form of a function:

$$\tau_T|_{f\,=\,300\text{MHz}} = 2.391746\ (\pm 0.064775)\cdot\arg\left(T_{\text{upper}}\right) - 87.07922(\pm 4.52158)\ [\text{ns}, ^\circ] \quad (10)$$

for the analysed MEMS test structure, which is presented in Figure 1c ($\tau_T \in$ (50 ns, 120 ns) and $\tau_q = 3$ ns) with $R^2 = 0.999774$.

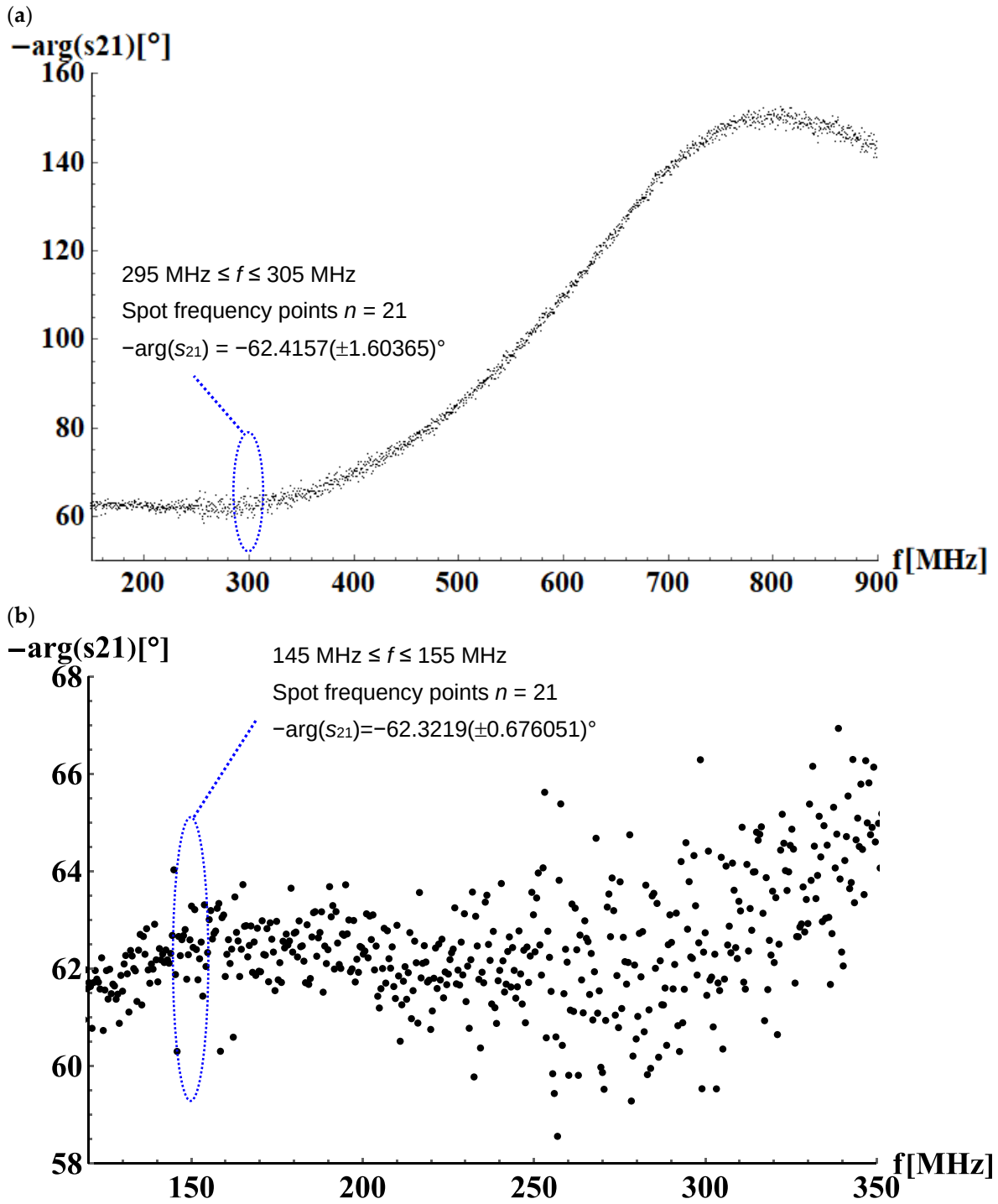


Figure 5. The direct measurement of the wave transmission through the MEMS test structure (s_{21}) for (**a**) 150 MHz ≤ f ≤ 900 MHz and (**b**) 150 MHz ≤ f ≤ 900 MHz.

To determine the temperature time-lag delay, we used the s_{21} measurements for a frequency close to f = 150 MHz and determined the averaged value and standard deviation of this parameter arg(s_{21}) = 62.3219 (±0.676051)° at f = 150 MHz (see Figure 4). Finally, the temperature time-lag delay can be calculated from Equations (8) and (10) using scattering parameters arg(s_{21}):

$$\tau_T = 61.9791(\pm 1.61694) \text{ ns at } f = 300 \text{ MHz} \quad (11)$$

for $I_{top} \leq 5$ mA and $I_{bottom} \leq 5$ mA [44].

5. Conclusions

This paper includes electromagnetic and thermal analyses of the MEMS test structure developed to validate the DPL model based on the methodology and tools presented in [2] for electric and thermal domains [1], respectively. The detailed analysis allows determining the best measurement frequency as well as electric and thermal model simplifications. Moreover, the new approach is associated with conducting measurements of electromagnetic scattering parameters together with simplification of the EM and thermal models of the MEMS test structure.

As a final result, we used a network analyser to determine the temperature time-lag delay in SiO_2 τ_T = 61.9791 ($\pm$1.61694) ns for assumed heat flux time-lag delay τ_q = 3ns, which is a big challenge in the case of ICs and MEMSs. The final time-lag delay values are applicable for the devices manufactured in the technology process developed by the Institute of Electron Technology in Warsaw, Poland.

The proposed method is suitable for determining the time-lag delay parameters of other materials and other technological processes of ICs, which can be very important during thermal and electro-thermal investigations of advanced electronic nano structures. The ability of high accuracy estimation of temperature distribution in the newest electronic devices is very significant for the real thermal model analysis. As a result, it is crucial for the reliability of whole nanoscale appliances in modern semiconductor structures.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10.3390/en14154425/s1.

Author Contributions: Conceptualization and methodology, M.Z.; investigation, all authors; resources, M.J. and Z.K.; writing—original draft preparation, M.Z.; writing—review and editing, M.J., Z.K. and A.N.; supervision, A.N. All authors have read and agreed to the published version of the manuscript.

Funding: The research presented in this paper was supported by both the project OPUS No 2013/11/B/ST7/01742 funded by the National Science Centre in Poland and by the internal university grant of the Lodz University of Technology.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are openly available in supplementary materials.

Acknowledgments: The authors would like to express their special thanks to M. Janicki and J. Topilko for sharing papers [39,40] and [43–45].

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. Analysis of Dissipated Power and Internal Heat Generation Source in MEMS Test Structure

With a limited error, we can assume that the bottom resistor of the considered MEMS test structure is a lamped resistive element for the electric domain ($L << \lambda/20$, see Section 4.2 and Table 2). The power dissipated in this resistor is equal to $p(t) = u_{bottom}(t) \cdot i_{bottom}(t)$, where $i_{bottom}(t) = A \cdot \sin(2\pi f_E\, t)$ is a current flowing through this resistor; A is the amplitude of current, e.g., $A = (5/\sqrt{2})$mA; $u_{bottom}(t) = |Z_{bottom}| \cdot \sin(2\pi f_E\, t + \phi)$ is a voltage drop on the resistor, $\phi = \arg Z_{bottom} \approx 0.12^\circ$ at 150 MHz, $|Z_{bottom}| \approx R_{bottom}$ at 150 MHz; and f_E is a frequency in the electric domain (e.g., 150 MHz).

In this appendix, we will use the Fourier transform of $x(t)$ in the limit sense defined according to the following equation [1]:

$$X(\omega) \;=\; 2\pi \sum_{k\,=\,-\infty}^{+\infty} X_k \delta(\omega - k\omega_0) \tag{A1}$$

where $\delta(t)$ is the Dirac delta function; $\omega_0 = 2\pi f_{\mathrm{E}}$ is pulsation, $T = 1/f_{\mathrm{E}}$; and X_k is a set of complex Fourier coefficients given by

$$X_k \;=\; \frac{1}{T} \int_{-T/2}^{T/2} x(t)\ \exp(-j\omega_0 k t) dt \tag{A2}$$

The series of expansion coefficients of the periodic function $x(t)$ into the complex series $\{Xn\}$ will be defined as $x(t) \leftrightarrow \{X_k\}$ for $k = -\infty, \ldots, 0, \ldots, +\infty$. The current flowing through the resistor has two complex coefficients associated with two alternating currents (ACs) $\pm f_{\mathrm{E}}$ in the electric frequency domain for $k = \pm 1$.

$$\begin{array}{rccccccccc} k = & -\infty, & \ldots, & -2, & -1, & 0, & 1, & 2, & \ldots, & +\infty \\ i_{\mathrm{bottom}}(t) \leftrightarrow \left\{I_{\mathrm{bottom},k}\right\} \;=\; & 0 & \ldots, & 0, & \frac{jA}{2}e^{-j\varphi}, & 0, & \frac{-jA}{2}e^{j\varphi}, & 0, & \ldots, & 0 \end{array} \tag{A3}$$

The active power dissipation is equal to $p(t) \leftrightarrow \left\{P_{\mathrm{bottom},k}\right\}$, where

$$\begin{array}{rccccccc} k = & -\infty, \ldots, 3 & -2, & -1, & 0, & 1, & 2, & 3, \ldots, +\infty \\ \left\{P_{\mathrm{bottom},k}\right\} = & 0 & -\frac{|Z_{bottom}|}{4}A^2\mathrm{Re}\left(e^{-j2\varphi}\right), & 0, & |Z_{bottom}|\cdot\left(\frac{A}{\sqrt{2}}\right)^2, & 0, & -\frac{|Z_{bottom}|}{4}A^2\mathrm{Re}\left(e^{j2\varphi}\right), & 0 \end{array} \tag{A4}$$

Therefore, the heat generated per unit volume in the bottom resistor is equal to

$$\begin{array}{rccccccc} k = & -\infty, \ldots, 3 & -2, & -1, & 0, & 1, & 2, & 3, \ldots, +\infty \\ \left\{g_{\mathrm{bottom},k}\right\} \approx & 0, & -\frac{R_{bottom}A^2}{4V_{bottom}}\cos(2\varphi), & 0, & \frac{R_{bottom}}{V_{bottom}}\cdot\left(\frac{A}{\sqrt{2}}\right)^2, & 0, & -\frac{R_{bottom}A^2}{4V_{bottom}}\cos(2\varphi), & 0 \end{array} \tag{A5}$$

where $V_{\mathrm{bottom}} = L{\cdot}W_{\mathrm{bottom}}{\cdot}t_{\mathrm{bottom}}$; $|Z_{\mathrm{bottom}}| \approx R_{\mathrm{bottom}}$ and $\mathrm{Re}(\mathrm{e}^{\pm \mathrm{j}2\phi}) = \cos(2\phi) \approx 1$ for $\phi \approx 0.12^\circ$ at 150 MHz; the expression $g_{\mathrm{bottom},k}/\sqrt{2}$ is used as the last left term in Equation (4). It should be underlined that the heat generated per unit in the bottom resistor is associated with the direct current (DC, for $k = 0$) and two alternating currents $\pm 2f_{\mathrm{E}}$ in the thermal frequency domain for $k = \pm 2$. This is why the harmonic temperature field distribution (4) is performed at a frequency of, e.g., 300 MHz, while scattering parameters measurements (s_{21}) are determined at half the frequency of 150 MHz. It should also be noted that detailed information on the operational principles of the vector network analyser can be found in [52]. The application of $\pm f_{\mathrm{E}}$ in the electric domain and $\pm 2f_{\mathrm{E}}$ in the thermal domain was presented for the first time in [53].

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