Article

Efficiency Enhancement of Non-Isolated DC-DC Interleaved Buck Converter for Renewable Energy Sources

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Abstract: The article describes the principles based on which it is possible to obtain energy from renewable sources more efficiently. The principles use the conventional DC-DC interleaved buck converter based on the common electronic component types and the control strategy. A novelty of such a proposed solution lies in the methods which are not new, but with the right combination, better results can be achieved. The resulting method can be implemented into various topologies where the highest efficiency for wide input power is required. In case of the renewable energy sources where the power can vary hugely during the day, the proposed method can be implemented. Therefore, the article provides several steps, from calculation through simulation to experimental results that brings reader close to understanding of a such proposed solution.

Keywords: buck converter; DC-DC converter; interleaved converter; non-isolated DC-DC converter; renewable energy sources

Citation: Bereš, M.; Kováč, D.; Vince, T.; Kováčová, I.; Molnár, J.; Tomčíková, I.; Dziak, J.; Jacko, P.; Fecko, B.; Gans, Š. Efficiency Enhancement of Non-Isolated DC-DC Interleaved Buck Converter for Renewable Energy Sources. *Energies* **2021**, *14*, 4127. <https://doi.org/10.3390/en14144127>

Received: 16 June 2021

Accepted: 6 July 2021

Published: 8 July 2021

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1. Introduction

DC-DC converters play a very important role in drawing energy from the renewable energy sources. The main reason is that the renewable energy sources do not produce constant power during the day. Therefore, they cannot be connected to the constant load, or to the load directly. This main drawback has a solution in implementing the DC-DC converter which, with an appropriate control strategy, can change the load factor to draw maximum energy as possible, or create a desired voltage level for connected load [1].

Currently, there are many solutions for how to create a more effective control strategy, to find the maximum power point more accurately, and much quicker [2]. In this case, the article will be describing the power-related aspect of the interleaved DC-DC converters and a solution which can be used to enhance their efficiency.

Interleaved DC-DC converters provide several advantages against non-interleaved versions. For instance, the interleaved converter produces lower current ripple [3] for the same switching frequency, working in a narrower area of discontinuous current, and providing a higher efficiency of power conversion.

To achieve smaller size of input and output filters, and lighter weights of the converters, it is necessary to operate converters at the highest possible switching frequency. However, high-switching devices for high power are expensive compared to low-switching devices with low power. Therefore, using several DC-DC converters working in an interleaved mode creates a high-frequency output with current sharing between each individual leg. Therefore, the soft switching technique can be omitted due to its low switching frequency in each individual converter's leg, and the expensive switching components can be replaced for inexpensive versions.

Interleaved DC-DC converters in various converter topologies can be found in many applications. In some cases, the interleaved mode can be implemented in novel topologies, or basic topologies with novel electrical components [4,5], and many other applications. For example, to enhance the output voltage ratio of boost converters [6–8], or for use in bidirectional connection [9,10], or for achieving better efficiency on passive components [11]. The interleaved connection finds its way in renewable energy sources [12–14], electrical vehicles [15], in isolated power sources [16,17], and many others. In all mentioned cases of DC-DC converters, the proposed solution can enhance their efficiency.

All of them use interleaved, multiphase or multi-leg connection, but none of the above-mentioned explain why the specific converter leg number is used. Therefore, it is difficult to find similar comparable results in the literature. For instance, the references [18,19] describe the impact of number of phases in interleaved converters in different way that can be used for achieving more efficiency. Due to the lack of contribution numbers in the interleaved converter effective leg number field, the article in addition provides a simple solution to achieve better efficiency, which will be described later.

Due to the huge number of advantages in using interleaved DC-DC converters, their application for renewable energy sources is widely used. However, the number of converter legs that should be used with specific electrical components in specific range of input power is still an open question. If the control algorithm allows a converter leg number change, then, with the right implementation, it also could contribute to the enhancement of converter efficiency. The solution provided in this paper can be used to determine converters optimum leg number based on used electrical components, and input power to achieve better efficiency.

Therefore, the optimal number of legs in the interleaved buck converter with specific electrical components remains an open question. To answer that question, an analysis should be made from the perspective of achieving maximum efficiency. For that reason, the paper is further structured in the following way:

In the beginning, the paper describes the calculations used to obtain the final mathematical form. With such a mathematical form, the right interleaved converter legs number can be determined. Based on the expressed mathematical form, the control unit can select the optimum interleaved converter legs number to achieve better efficiency in various input power.

At the end of the paper, the simulation and experimental results on a four-leg DC-DC interleaved converter validate the proposed final mathematical form.

2. Interleaved DC-DC Converter Analysis

The schematic connection of the interleaved converter with n legs number is shown in Figure 1. The figure shows the basic scheme (see Figure 1a) and the scheme with parasitic electrical components of the converter (see Figure 1b). As the converter topology is a cascaded DC-DC Buck-Boost converter in this case, only work carried out in buck mode where the second transistor is omitted is considered [20]. However, the diodes D12 to Dn2 should be included for efficiency determination. Boost mode analysis is out of scope of this article. As will be described later, the calculation can be easily modified to achieve final mathematical form for any topology the application required. Because the simulations and the experimental results consist of the mentioned diodes, the analysis will also consider these diodes. The presence of the diodes does not invalidate following proposed analysis, the simulation or the validity of the experimental results.

Figure 1. Schematic connection of n legs number of DC-DC converter (a) basic scheme (b) scheme with parasitic electrical components.

All electrical components which contain index P represent the parasitic components of a real model of the converter. For electrical current, the first Kirchhoff law is applied (1).

$$i = \sum_{j=1}^n i_j \quad (1)$$

Each converter leg works with the same switching frequency and duty cycle as the other converter legs. The control signals are time shifted based on T/n , where T is switching period and the n is a quantity of converter legs. With such phase-shifted control signals, the interleaved mode will be achieved for every leg number change.

2.1. The First Time Period Analysis–Energy Accumulation

In this working period, the switching device in this case a MOSFET transistor is closed, which will cause the energy accumulation in the main induction element of the circuit. The described situation can be seen in Figure 2.

Figure 2. Substitute scheme for the first working period of the converter.

To the n conductive converter leg, the second Kirchhoff law can be applied (2).

$$\begin{aligned} -V + R_{Pn1} \cdot i_n + L_{Pn1} \cdot \frac{di_n}{dt} + r_{DS(on)n} \cdot i_n \\ + R_{Ln} \cdot i_n + L_n \cdot \frac{di_n}{dt} + V_F + R_{Pn2} \cdot i_n \\ + L_{Pn2} \cdot \frac{di_n}{dt} + V_Z = 0 \end{aligned} \quad (2)$$

where V is an input voltage, R_{pn1} and L_{pn1} is a parasitic resistance and a parasitic inductance, respectively, of the input wire. $r_{DS(on)}$ is a MOSFET transistor resistance when it is turned on, R_{Ln} and L_n is a resistance and inductance of the main inductor, respectively. V_F is a voltage drop on a diode, R_{pn2} is an output wire resistance leaded to load and the V_Z is a voltage load.

Due of resistive and inductive load, the current waveform in continuous conduction mode (CCM) will have a shape according to Figure 3.

Figure 3. Current waveform in CCM of converters n leg.

According to Figure 2, the loop circuit can be simplified by the parameter's concentration (3)–(6).

$$V_Z = Z \cdot I = Z \cdot \sum_{i=1}^n i_i \approx Z \cdot n \cdot i_n \quad (3)$$

$$V_F = V_{TO} + r_F \cdot i_n \quad (4)$$

$$R_{n1} = R_{pn1} + r_{DS(on)} + R_{Ln} + R_{pn2} + r_F \quad (5)$$

$$L_{n1} = L_{pn1} + L_n + L_{pn2} \quad (6)$$

where V_{TO} is a threshold voltage of the diode, R_{n1} is a n -th leg resistance of the first time period, r_F is a diode resistance in the forward direction and L_{n1} is an induction of n -th leg converter in the first time period.

Based on (3) to (6), the (2) can be modified as follows (7):

$$V_{TO} - V + Z \cdot n \cdot i_n + R_{n1} \cdot i_n + L_{n1} \cdot \frac{di_n}{dt} = 0 \quad (7)$$

Rewriting (7) with shape operator, the equation will obtain the following format:

$$V_{TO} - V + Z \cdot n \cdot \hat{i}_n + R_{n1} \cdot \hat{i}_n + pL_{n1} \cdot \hat{i}_n - pL_{n1} \cdot I_1 = 0 \quad (8)$$

Now, from (8) the current can be expressed as follows:

$$\hat{i}_n = \frac{V - V_{TO}}{(R_{n1} + n \cdot Z)} \cdot \frac{\frac{(R_{n1} + n \cdot Z)}{L_{n1}}}{\frac{(R_{n1} + n \cdot Z)}{L_{n1}} + p} + I_1 \cdot \frac{p}{\frac{(R_{n1} + n \cdot Z)}{L_{n1}} + p} \quad (9)$$

By completing a back transformation of (9) to the time domain, we obtain (10).

$$i_n = \frac{V - V_{TO}}{(R_{n1} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot t} \right) + I_1 \cdot e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot t} \quad (10)$$

If, in this time domain, the expression of the current we substitute $t = t_{on} = D/f$, then at a given moment in time, it obtains a current I_2 , according to Figure 3. The resulting equation for the current I_2 takes a following form:

$$I_2 = \frac{V - V_{TO}}{(R_{n1} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \right) + I_1 \cdot e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \quad (11)$$

where D is a duty cycle, and f is a switching frequency.

To obtain the current value I_1 , the second time period of the converter will be described.

2.2. The Second Time Period Analysis—Energy Transferred to the Load

In the second working period of the converter, the switching device will turn off and an accumulated energy in the main inductor will be transferred to the load through diodes Dn1 and Dn2, as seen in Figure 4.

Figure 4. Substitute scheme for the second working period of the converter.

For the n conductive converter leg, the second Kirchhoff law can be applied as follows (12).

$$V_Z + V_F + R_{Ln} \cdot i_n + L_n \cdot \frac{di_n}{dt} + V_F + R_{Pn2} \cdot i_n + L_{Pn2} \cdot \frac{di_n}{dt} = 0 \quad (12)$$

where (3) can be applied as well as the following equations to simplified loop circuit by parameter concentration:

$$R_{n2} = R_{Ln} + 2 \cdot r_F + R_{Pn2} \quad (13)$$

$$L_{n2} = L_n + L_{Pn2} \quad (14)$$

Applying equations for parameter concentration, the modified (12) will get the following form:

$$n \cdot Z \cdot i_n + 2 \cdot V_{TO} + R_{n2} \cdot i_n + L_{n2} \cdot \frac{di_n}{dt} = 0 \quad (15)$$

Rewriting (15) with shape operator, the equation will obtain the following format:

$$n \cdot Z \cdot \hat{i}_n + 2 \cdot V_{TO} + R_{n2} \cdot \hat{i}_n + pL_{n2} \cdot \hat{i}_n - pL_{n2} \cdot I_2 = 0 \quad (16)$$

Now, from (16), the current can be expressed as follows:

$$\hat{i}_n = \frac{-2 \cdot U_{TO}}{(R_{n2} + n \cdot Z)} \cdot \frac{\frac{(R_{n2} + n \cdot Z)}{L_{n2}}}{\frac{(R_{n2} + n \cdot Z)}{L_{n2}} + p} + I_2 \cdot \frac{p}{\frac{(R_{n2} + n \cdot Z)}{L_{n2}} + p} \quad (17)$$

By completing a back transformation of (17) to the time domain, we obtain (18).

$$i_n = \frac{-2 \cdot V_{TO}}{(R_{n2} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot t} \right) + I_2 \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot t} \quad (18)$$

If in this time domain expression of the current we substitute $t = t_{off} = (1 - D)/f$, then at a given moment in time, it obtains a current I_1 , according to Figure 3. The resulting equation for the current I_1 takes a following form:

$$I_1 = \frac{-2 \cdot V_{TO}}{(R_{n2} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right) + I_2 \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \quad (19)$$

2.3. Total Power Loss Calculation

Based on (11) and (19), it is possible to obtain current values of the I_1 and the I_2 at the beginning of each time period.

Next, the current value of I_2 from (11) is substituted into (19), which results in:

$$I_1 = \frac{-2 \cdot V_{TO}}{(R_{n2} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right) + \left(\frac{V - V_{TO}}{(R_{n1} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \right) + I_1 \cdot e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \right) \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \quad (20)$$

The final expression of the I_1 current value is obtained after adjusting (20) to the form:

$$I_1 = \frac{\frac{-2 \cdot V_{TO}}{(R_{n2} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right) + \left(\frac{(V - V_{TO})}{(R_{n1} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \right) \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right)}{\left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right)} \quad (21)$$

The current value expression of I_2 can be achieved by substitution of (21) into (11), which results in:

$$I_2 = \frac{V - V_{TO}}{(R_{n1} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \right) + \left(\frac{-2 \cdot V_{TO}}{(R_{n2} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right) + \left(\frac{V - V_{TO}}{(R_{n1} + n \cdot Z)} \cdot \left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \right) \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right) \right) \cdot e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} + \left(\frac{\left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right)}{\left(1 - e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \cdot e^{-\frac{(R_{n2} + n \cdot Z)}{L_{n2}} \cdot \frac{(1-D)}{f}} \right)} \right) \cdot e^{-\frac{(R_{n1} + n \cdot Z)}{L_{n1}} \cdot \frac{D}{f}} \quad (22)$$

Based on (10), (18), (21) and (22), the current waveform can be determined for any leg of the converter.

To determine the optimum legs number of the converter, the power losses based on leg number were determined. The power losses occur in conduction losses with static (quiescent) losses for both, time periods as well as for switching losses of the power converter. The considered losses in a power converter are the losses produced by the semiconductor switches (MOSFETs and diodes) and the passive components (inductors). Their losses can be expressed as follows:

Conduction losses:

$-P_{RPn1}$ —Power losses due to current flowing through input wire resistance of the converter n leg;

$-P_{MF}$ —Power losses in the MOSFET transistor in conductive state;

$-P_{MR}$ —Power losses in the MOSFET in non-conductive state (quiescent losses);

$-P_{RLn}$ —Power losses due to current flowing through inductor wire resistance of the converter n leg;

$-P_{DF}$ —Power losses in diode in conductive state;

$-P_{DR}$ —Power losses in the diode in non-conductive state (quiescent losses);

$-P_{RPn2}$ —Power losses due to current flowing through output wire resistance of the converter n leg.

Switching losses:

$-P_{Mon}$ —Power losses in the MOSFET during the time it takes to turn on;

$-P_{Moff}$ —Power losses in the MOSFET during the time it takes to turn off;

$-P_{Doff}$ —Power losses in the diode during the time it takes to turn off;

$-P_{Don}$ —Power losses in the diode during the time it takes to turn on.

Considering the standard waveforms and the time taken by the semiconductors to turn on and off, and the (1), the total power losses P_W can be determined as follows:

$$P_W = P_{RPn1} + P_{MF} + P_{MR} + P_{RLn} + P_{DF} + P_{DR} + P_{RPn2} + P_{Mon} + P_{Moff} + P_{Doff} + P_{Don} \quad (23)$$

An average current value of n leg of the converter can be determined as follows:

$$I_{n(AV)} = \frac{I_1 + I_2}{2} = \frac{I}{n} \quad (24)$$

where the I is the average current value of the converter. Based on (24), the total power losses of the converter can be determined as follows:

$$\begin{aligned} P_W = & n \cdot R_{Pn1} \cdot \left(I_{n(AV)}\right)^2 \cdot D + n \cdot r_{DS(on)} \cdot \left(I_{n(AV)}\right)^2 \cdot D + n \cdot V \cdot I_{DS(off)} \cdot (1 - D) + n \cdot R_{Ln} \cdot \left(I_{n(AV)}\right)^2 \\ & + n \cdot 2 \cdot \left(V_{TO} + r_F \cdot \left(I_{n(AV)}\right)\right) \cdot I_{n(AV)} \cdot (1 - D) + n \cdot \left(V_{TO} + r_F \cdot \left(I_{n(AV)}\right)\right) \cdot I_{n(AV)} \cdot D + n \cdot V \cdot I_R \cdot D \\ & + n \cdot R_{Pn2} \cdot \left(I_{n(AV)}\right)^2 + n \cdot 0.5 \cdot V \cdot I_1 \cdot t_{on} \cdot f + n \cdot 0.5 \cdot V \cdot I_2 \cdot t_{off} \cdot f \\ & + n \cdot 0.5 \cdot Q_{rr} \cdot V \cdot f + n \cdot 0.5 \cdot V_{FP} \cdot I_2 \cdot t_{fr} \cdot f \end{aligned} \quad (25)$$

where the $r_{DS(on)}$ is an MOSFET channel (drain to source) resistance in time when it is turned on, $r_{DS(off)}$ is an MOSFET channel resistance in time when it is turned off, I_R is the current flowing through diode in reverse direction, t_{on} is the time when the MOSFET transistor takes to turn on, t_{off} is the time when the MOSFET transistor takes to turn off, Q_{rr} is a commutation charge of the diode and V_{FP} is the voltage drop on diode during time t_{fr} the diode takes to turn on.

By substituting (24) into (25), the total power losses can be expressed in simpler and final form, as follows:

$$\begin{aligned} P_W = & \left(\frac{I^2}{n}\right) \cdot \left(R_{Pn1} \cdot D + r_{DS(on)} \cdot D + R_{Ln} + 2 \cdot r_F \cdot (1 - D) + r_F \cdot D + R_{Pn2}\right) + n \cdot V \cdot I_{DS} \cdot (1 - D) \\ & + 2 \cdot V_{TO} \cdot I \cdot (1 - D) + V_{TO} \cdot I \cdot D + n \cdot V \cdot I_R \cdot D + n \cdot 0.5 \cdot V \cdot I_1 \cdot t_{on} \cdot f \\ & + n \cdot 0.5 \cdot V \cdot I_2 \cdot t_{off} \cdot f + n \cdot 0.5 \cdot Q_{rr} \cdot V \cdot f + n \cdot 0.5 \cdot V_{FP} \cdot I_2 \cdot t_{fr} \cdot f \end{aligned} \quad (26)$$

The converter efficiency can be determined as follows:

$$\eta = \frac{P_{output}}{P_{input}} = \frac{P_{input} - P_W}{P_{input}} = 1 - \frac{P_W}{P_{input}} = 1 - \frac{P_W}{U \cdot I} \quad (27)$$

From (27) the efficiency is most influenced by the total power loss. The amount of total power loss highly depends on individual structural elements. In addition, it is possible to influence the total power losses by the number of converter legs connected in parallel, because in this way the input current is divided linearly between the legs, but the losses produced by parasitic resistance in each converter leg decrease quadratically. Thus, the total losses may be smaller for several legs than for one leg. However, due to the additional losses in the parallel legs, the statement that the larger the number of legs, the smaller the losses does not apply. As a result, it is possible to search for the optimal leg number for the required size of input power (at a constant input voltage, for the required size of input current, and thus the selected duty cycle). It is, therefore, possible to control the converter by changing the topology, so the highest possible efficiency is achieved at each value of the input power—of course, with fixed design components of the converter and their properties.

Equation (26) must be differentiated to determine the optimal legs number. By deriving this according to n , it is possible to obtain the result of the local extreme, thus, the expression of the number of legs for the minimum power loss.

$$\begin{aligned} P'_W = & -\left(\frac{I^2}{n^2}\right) \cdot \left(R_{Pn1} \cdot D + r_{DS(on)} \cdot D + R_{Ln} + 2 \cdot r_F \cdot (1 - D) + r_F \cdot D + R_{Pn2}\right) \\ & + V \cdot I_{DS} \cdot (1 - D) + V \cdot I_R \cdot D + 0.5 \cdot V \cdot I_1 \cdot t_{on} \cdot f \\ & + 0.5 \cdot V \cdot I_2 \cdot t_{off} \cdot f + 0.5 \cdot Q_{rr} \cdot V \cdot f + 0.5 \cdot V_{FP} \cdot I_2 \cdot t_{fr} \cdot f \end{aligned} \quad (28)$$

If the result of the derivative is equal to zero, and n is expressed, (28) takes the following form:

$$n = I \cdot \sqrt{\frac{(R_{pn1} \cdot D + r_{DS(on)} \cdot D + R_{Ln} + 2 \cdot r_F \cdot (1-D) + r_F \cdot D + R_{pn2})}{V \cdot I_{DS} \cdot (1-D) + V \cdot I_R \cdot D + 0.5 \cdot V \cdot I_1 \cdot t_{on} \cdot f + 0.5 \cdot V \cdot I_2 \cdot t_{off} \cdot f + 0.5 \cdot Q_{rr} \cdot V \cdot f + 0.5 \cdot V_{FP} \cdot I_2 \cdot t_{FR} \cdot f}} \quad (29)$$

It follows that, based on (29), it is possible to determine the most suitable number of legs using the design and operation parameters of the converter in the buck mode so that the converter delivers the greatest possible power to the load under all operation conditions [21]. To validate that statement, the simulations, as well as experimental results are provided later in this paper.

3. Calculated Efficiency Results Based on Legs Number and Input Power

For efficiency calculation, the four input power values were considered (3 W, 10 W, 40 W and 100 W). For such input power values, the result—showing how different leg numbers for converters impacts performance and, thus, how many should be used—was achieved. As an example, the four-leg converter was considered. For each input power the various legs number were used to calculate efficiency. The parameter values of the electrical components are in Table 1.

Table 1. Electrical components parameters values.

Parameter	Description	Value
n	Number of legs	1–4
R_{pn1}	Input wire resistance	0.2 [Ω]
R_{pn2}	Output wire resistance	0.2 [Ω]
V	Input voltage	30 [V]
$R_{DS(on)}$	MOSFET drain source electric resistance when it is turned on	0.07 [Ω]
R_{Ln}	electric resistance of main inductor	0.044 [Ω]
r_F	Diode resistance in forward direction	0.02 [Ω]
$I_{DS(off)}$	Leakage current of MOSFET	250 [μ A]
V_{TO}	Threshold voltage of diodes	0.77 [V]
I_R	Current through diode in reverse direction	2 [mA]
t_{on}	Time which transistor takes to turn on	55 [ns]
t_{off}	Time which transistor takes to turn off	96 [ns]
Q_{rr}	Commutation charge of diode	120 [nC]
V_{FP}	the voltage drop on diode during time t_{fr} the diode takes to turn on	2 [V]
f	frequency	200 [kHz]
t_{fr}	Time duration of voltage drop on diode which takes to turn it on	2 [ns]
D	Duty cycle	0–1
Z	Resistive load	4.7 [Ω]

–The MOSFET transistor type the IRF540N was used.

Based on provided parameters and (27), the calculated efficiency results were obtained. The input voltage was always the same. Thus, the input power (current) was controlled by duty cycle parameter. The Equation (29) takes into an account not only the current, but also the voltage changes.

Obtained results of the calculations are illustrated in Figure 5. For achieving such results, two steps of the same calculated value of input power, output power and efficiency were implemented. With such illustrated results the difference in efficiency values for different input powers as well as for different converter legs number can be easily spotted.

“L” means legs number and “Steps” means the number of calculation results, where, for the one leg, the calculation result is implemented two times. That creates a stair effect. It is not a time step. Therefore, for four different input power and four converter legs the sixteen calculations results were made and implemented into graph two times each.

Figure 5. Efficiency results achieved by proposed equations for various converter legs number and input powers.

From such proposed and illustrated calculated results as it can be seen in Figure 5, for different input power value, the different leg numbers of the converter should be used to make sure that the converter is working with maximum efficiency. As mentioned in the introduction, if the control algorithm allows the converter leg number to be changed, it can enhance the efficiency in wider input power area.

4. Simulated Efficiency Results Based on Legs Number and Input Power

To validate calculations a simulation model was created. The simulation model illustrated in Figure 6 was created with the help of a Proteus simulation environment. The 8.9 SP2 version of the Proteus was used. The Proteus simulation environment uses a PSpice as a simulation core.

Figure 6. Simulation model of the four-leg buck converter with the parasitic resistance.

The main advantage of using this simulation environment is in a capability to mixed digital devices such as microcontrollers with the analog devices. The microcontrollers can be programmed in their own programming environment. Then, the binary file can be directly used in the simulation environment.

The challenge was in creating the similar waveforms as for calculated one. Therefore, instead of the microcontroller unit, the VHDL script was used to achieve dynamic control signals. Signal upgrading and creating was much easier to do with VHDL than with the microcontroller, where every change in control signals, the whole control program must be compiled and uploaded into simulation program. The dynamic control signals, in the sense that the duty cycle of the control signals, even for the same input power, but for different

converter leg numbers, can vary, and, therefore, it must be changed. The converter leg numbers are, in this case, changed every 2.5 ms. Thus, duty cycle, as well as the phase shift of control signals, must be changed. The VHDL script also changes duty cycle value to draw more current from the power source every 10 ms. Every 10 ms, the input power will increase due to duty cycle change in following steps: 3 W, 10 W, 40 W and 100 W. After that, the VHDL script started generating signals from the beginning (3 W . . .)—see Figure 7. In such a way of controlling the similar waveform results, an arrangement can be achieved, as shown in the case of calculation results—see Figure 5.

```

Generator Name: HDL_Vg2
Assigned Script: <LOCAL>
Local Script:
TIME OFFSET = 0
FLOAT phase = 0
FLOAT v, t
FLOAT period = 5u
FLOAT t_delay = period/2
FLOAT t_rise = 80n
FLOAT duty = 0
FLOAT t_fall = duty + 80n
FLOAT Voltage = 0
DATA t_rise, Voltage
DATA duty, Voltage
DATA t_fall, 0
DATA 0, 0
TIME CHANGETM = 0
INT step = 0
IF EVTIME > CHANGETM
SWITCH krok
CASE 0: Voltage = 0 :BREAK //1v3W
CASE 1: duty= 0.56u :Voltage = 15: BREAK //2v3W
CASE 2: duty= 0.51u :phase = -period/2 + period*1/3: BREAK //3v3W
CASE 3: duty= 0.45u :phase = -period/3 + period*1/4: BREAK //4v3W
CASE 4: Voltage = 0 :BREAK //1v3W
CASE 5: duty= 1.1395u :phase = - period*1/4 + period/2: Voltage = 15: BREAK //2v3W
CASE 6: duty= 1.11u :phase = -period/2 + period*1/3: BREAK //3v3W
CASE 7: duty= 1.08u :phase = -period*1/3 + period*1/4: BREAK //4v3W
CASE 8: Voltage = 0 :BREAK //1v3W
CASE 9: duty= 2.3055u :phase = - period*1/4 + period/2: Voltage = 15: BREAK //2v3W
CASE 10: duty= 2.29u :phase = -period/2 + period*1/3: BREAK //3v3W
CASE 11: duty= 2.27u :phase = -period*1/3 + period*1/4: BREAK //4v3W
CASE 12: Voltage = 0 :BREAK //1v3W
CASE 13: duty= 3.6475u :phase = - period*1/4 + period/2: Voltage = 15: BREAK //2v3W
CASE 14: duty= 3.62889u :phase = -period/2 + period*1/3: BREAK //3v3W
CASE 15: duty= 3.61u :phase = -period*1/3 + period*1/4: BREAK //4v3W
ENDSW
CHANGETM = CHANGETM + 2.5m
step = step + 1
IF step > 15
step = 0
ENDIF
ENDIF
ON TIMER AT period+t_delay EVERY period + phase
RESTORE
OFFSET=EVTIME
phase=0
ENDON
ON EVENT
READ t, v
IF t > 0
t = t + OFFSET
OUT= v AT t
CALLBACK AT t
ENDIF
ENDON
Debug this generator?
OK Cancel

```

Figure 7. VHDL script for creating dynamic control signals for second leg.

In the simulation program, the input, and the output power are calculated with the help of current controlled voltage source, voltage control voltage source, and an ideal four-quadrant multiplier. The results from the multipliers are in the next filtered by a Laplace first-order low-pass filter transfer function—see Figure 8. The value τ is set to 4 μ s.

After the input and the output power determination, the efficiency can be easily calculated (see, Figure 9). The calculated efficiency result is in the next same as in the case of the input, and the output power filtered by Laplace first-order low-pass filter transfer function.

Figure 8. The input and the output power determination using ideal current control voltage sources, voltage control voltage sources, voltage multipliers and the Laplace first-order low-pass filter transfer functions.

Figure 9. Efficiency determination using divider function, arbitrary voltage control voltage source and the Laplace first-order low-pass filter transfer function.

In the simulation, the same electrical components were used as for the calculation. However, after the simulation model was completed, the difference in calculation and simulation results occurred. The main difference was efficiency value. The difference could be in parameters values which in case of calculation were subtracted from manufacturer datasheets, and not from the real measured values. However, for the same four different input powers, the results show that even in the simulation model the different legs number should be used to achieve maximum efficiency, as seen in Figure 10. From the achieved results using the Proteus simulation environment, the efficiency can be easily determined.

Figure 10. Simulation results achieved by a simulation model of the converter and the help of VHDL script in a Proteus simulation environment.

5. Experimental Validation

To validate the mathematical and the simulation results, the experimental model was created. The block scheme of the experimental test is illustrated in the following Figure 11.

Figure 11. The block scheme of the experimental test.

As a control unit to generate control signals a microcontroller STM32F446RET was used, which is a 32-bit microcontroller with a maximum CPU clock of 160 MHz. The microcontroller is sufficiently fast and can handle all four converter legs. To avoid converter damaging microcontroller in any way, the control signals are galvanically isolated through an optocoupler and isolated DC-DC converters on power side. Controlling signals for each converter leg uses a different timer of microcontroller. The reason is that each converter leg should be phase shifted to ensure interleave operation. The phase shift between the control signals is handled by another timer. The frequency of this timer varies based on the converter legs number and control signal switching frequency. This timer runs only once every leg number change.

The duty cycle changing was as same as in case of the simulations to achieve same input power for different converter legs number. The duty cycle also changes when the different input power should be drawn. In the results, the converter leg number is changing every 9 ms. At the start, the one converter leg is working. After 9 ms, two converter legs work with phase shifted control signals. After another 9 ms, the three converter legs work, etc. When the four converter legs work for a 9 ms duration for a specific input power, the next stage will begin. In the next stage, the duty cycle changes much more to draw more current from the power source. After each stage of drawing specific input power, the controller will start from beginning, from lower power to higher power at four stages. Each stage the converter draws different power from the power source. The input power values are the same as in case of simulation (3 W, 10 W, 40 W and 100 W).

The power switch of MOSFET IRF540N was utilized together with the power diode of MBR20100CT. The main inductor value of each converter legs was 106 μ H. The switching frequency of each converter leg is 200 kHz. The experimental setup is illustrated in Figure 12.

The experimental waveform results are illustrated in Figure 13.

After using a math function in the oscilloscope (Tektronix DPO 7354) to determine the input and the output power, the filter functions were also implemented. Without them, the waveforms were unreadable. From achieved results by the experimental test, it can clearly be seen that the different converter legs number should be considered in different input power. For such presented results, it is not necessary the make separate measurements for different input power. All cases are illustrated in one figure. That was the reason why the control signal changes were made in the mentioned way.

Figure 12. Experimental setup illustration.

Figure 13. The achieved efficiency waveform from experimental results for different input power values as well as different converter legs number. The input power (darker blue) and the output power (green) waveforms have 12 W/div and the efficiency waveform (light blue) has 10%/div. The time base is 20 ms/div.

6. Discussion

Based on (29) with the result in Figure 5 as well as the waveforms shown in Figures 10 and 13, it is possible to obtain several important facts influencing the design and operation of interleaved multi leg converters. The first fact is that, in low-power inputs of the converter, the connection of a single leg converter is more effective in terms of higher efficiency compared to more active legs of the converter. However, this is no longer the case for higher input power, and more converter legs are more effective. The second fact that can be obtained from the analysis is the fact that the amount of power at which the single converter leg connection is effective in favor of multi-leg converter connection is influenced by both design and operating parameters of the converter, so it is more parametric. The third acquired knowledge is the fact that the principle that the more legs the converter has, the higher its efficiency, does not apply to larger power inputs, but it is true that for individual power values it is always possible to determine the final optimal converter legs

number. The fourth important finding is the fact that the optimal design and operation of the buck mode of the DC-DC converter is such that from a design point of view, it is implemented as multi leg, but is operated with variable topology, depending on input power value, either as single leg, double leg or multi leg, so that the optimal number of legs is always selected.

7. Conclusions

It should be noted that the described procedure for determining the optimal converter legs number can be applied not only to the buck converter connection, but also to any type of DC-DC converter. With changing converters legs number to achieve better efficiency could be very useful for renewable energy sources, where the power can vary in a wider range.

The main drawback of the proposed solution is in the application difficulties. Because with the different electrical components, the calculation results will change as well as the efficiency for the same input power. Therefore, if the control algorithm does not consider the electrical components change, the whole system will be working in no sufficient way. The solution may be in the measuring input, and the output power continuously, which can contribute to higher price of the system.

In the future, a control strategy that consider a converter legs number change could bring a new idea with interesting results. Of course, with main drawback consideration.

Author Contributions: Conceptualization, B.F.; methodology, D.K.; software, T.V.; validation, D.K. and I.K.; formal analysis, J.D.; investigation, Š.G.; resources, J.M.; data curation, I.T.; writing—original draft preparation, M.B.; visualization, P.J. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available as the data also forms part of an ongoing study.

Conflicts of Interest: The authors declare no conflict of interest.

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