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Starter for Voltage Boost Converter to Harvest Thermoelectric Energy for Body-Worn Sensors

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Abstract: This paper examines the suitability of selected configurations of ultra-low voltage (ULV) oscillators as starters for a voltage boost converter to harvest energy from a thermoelectric generator (TEG). Important properties of particularly promising configurations, suitable for on-chip implementation are compared. On this basis, an improved oscillator with a low startup voltage and a high output voltage swing is proposed. The applicability of n-channel native MOS transistors with negative or near-zero threshold voltage in ULV oscillators is analyzed. The results demonstrate that a near-zero threshold voltage transistor operating in the weak inversion region is most advantageous for the considered application. The obtained results were used as a reference for design of a boost converter starter intended for integration in 180-nm CMOS X-FAB technology. In the selected technology, the most suitable transistor available with a negative threshold voltage was used. Despite using a transistor with a negative threshold voltage, a low startup voltage of 29 mV, a power consumption of 70 µW, and power conversion efficiency of about 1.5% were achieved. A great advantage of the proposed starter is that it eliminates a multistage charge pump necessary to obtain a voltage of sufficient value to supply the boost converter control circuit.

Keywords: CMOS; low voltage; low power; starter; boost DC-DC converter; energy harvesting; Colpitts oscillator

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1. Introduction

Rapid development of body-worn sensors systems integrated on a chip imposes a significant demand on small and efficient power supply circuits. Batteries are avoided in these types of applications because of their relatively large size and limited life span. Among alternative energy sources such as photovoltaic cells [1], vibration transducers [2], or the thermoelectric generators (TEGs) [3–5], the latter ones are widely used due to their small size, portability and suitability for on-body applications. TEGs exploit temperature gradient between the human skin and the ambient environment in practical situations. Small TEG size and low temperature difference (typically 1–2 °C) limit the upper voltage bound below 100 mV. Such a low voltage can be applied to slow circuits based on MOS transistors operating in the subthreshold region. However, many systems-on-chip implementing sophisticated functions require MOS transistors operating in the strong inversion region, which involves the use of supply voltages of around 1 V. Although boost converters can be used to raise voltages as low as 20–40 mV [6–11] to the required supply level, they also need a voltage within 1 V for efficient energy conversion. For this reason, an additional starter is used to allow "cold start" of the converter at low voltages. Such a circuit is turned on for a short time needed to start the converter, and then turned off once the converter supplies sufficient voltage to its own control circuits. In practical implementations of ULV boost converters, very significant difficulties are associated with realization of their starters.

Starter solutions designed to initialize the operation of on-chip boost converters are described in the literature [7–10,12–17]. The solutions can be classified into two major

groups: starters based on classic ring oscillators using only transistors [12,16,17], and starters based on oscillators with inductors or transformers [7,9,10,12–14]. In ring oscillators, each stage must have a gain greater than one in order to start and sustain oscillations. Satisfying this condition at very low supply voltages is very difficult, where all transistors have relatively low transconductance and drain-source resistance [18–21]. The lowest supply voltage reported for this type of starter is 60 mV [13]. This level was achieved by applying a mechanism for technology corner detection and automatic reconfiguration of the ring oscillator to achieve almost optimal operating conditions. The ring oscillator using only transistors generates output voltages that are limited by the supply voltage, therefore, they need an additional multistage (in some solutions up to 40 stages [13]) charge pump to obtain a sufficiently high voltage. As a result, ring-oscillator-based starters are fairly complicated and have a relatively low efficiency. On the other hand, they can be fully integrated on a chip.

Inductor or transformer-based starters support much lower supply voltages. In these circuits, a transformer or inductor acts as a load for a MOS transistor, allowing for voltage swing greater than the supply voltage and eliminating the inevitable voltage drop across the active load as in the case of a transistor-only ring oscillator. Consequently, they are capable of self-starting at supply voltages as low as 25–40 mV [7,9]. Moreover, an output voltage within 1 V can be achieved without additional charge-pump-based voltage multipliers owing to boosting voltage in a transformer or a LC resonant tank. In this regard, such starters are preferable over ones based on ring oscillators owing to their reliability, even with the supply voltages of only 25–40 mV. The disadvantage of these solutions is the need for inductors, which often have to be implemented as off-chip components to meet the high quality factor requirement.

In terms of the feasibility of reducing the startup voltage, the starters based on the Colpitts oscillator are particularly promising [12,14,18,19]. The paper [19] gives an example implementation of a low-voltage Colpitts oscillator that operates even at 3.5 mV supply voltage. This circuit has indeed a very low inrush voltage but reveals a limitation of the output voltage swing. As a result, the circuit requires an additional multi-stage voltage multiplier to achieve a voltage close to 1 V.

This paper describes a low voltage starter based on an improved Colpitts oscillator featuring a high output voltage swing, which allows using only a few stages of a charge pump.

2. Ultra-Low-Voltage Oscillators

Three configurations of ULV oscillator potentially suitable as a boost converter starter are depicted in Figure 1.

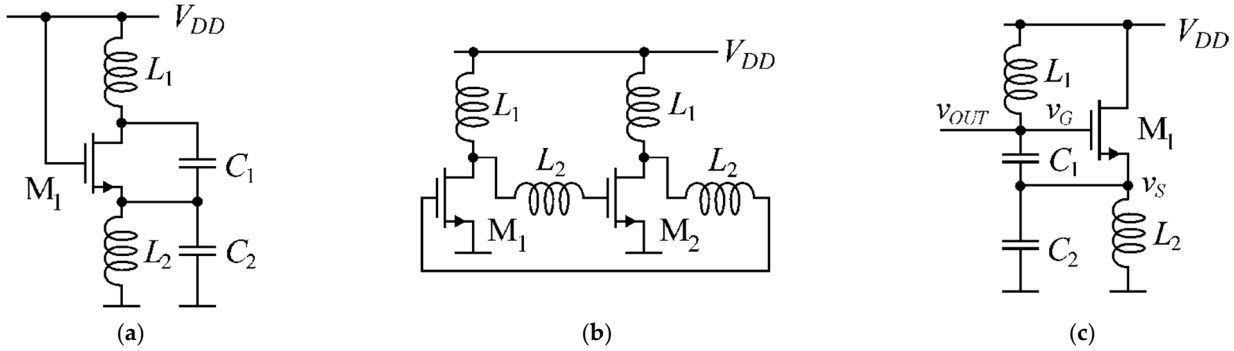

Figure 1. Ultra-low-voltage oscillators: (**a**) ESCO; (**b**) ESILRO; (**c**) proposed HSCO.

The oscillators in Figure 1a,b are ULV solutions discussed in [18,19], referred to as enhanced swing Colpitts oscillator (ESCO) and inductive-load enhanced swing ring oscillator (ESILRO). The circuit in Figure 1c is a proposed high swing Colpitts oscillator

(HSCO). The common feature of all the ULV circuits is the application of the full supply voltage (V_{DD}) to bias the transistor gate and drain. In this way, a sufficiently high intrinsic gain of the transistor can be achieved at a relatively low supply voltage. For this reason, two inductors are necessary to avoid voltage drop between the V_{DD} rail, drain and gate of the transistor. An unavoidable disadvantage of ESCO and ESILRO is limited voltage swing at the drains of the transistors. The reason for this effect is the pn junction between the drain and the substrate, which is forward biased during the negative halves of the generated periodic voltage waveform.

This undesirable effect is avoided in HSCO by connecting the resonant tank with the inductor L_1 to the transistor gate and design the feedback loop (C_1, C_2) so that the voltage scaling factor v_G/v_S is much larger than unity. Under such conditions, the voltage swing on the resonant tank is virtually unlimited. At the same time, voltage across the pn junction formed between the source and the substrate is highly reduced, which prevents it from forward bias. In the small-signal model of the circuit, shown in Figure 2, the biasing inductor L_2 is represented by its dynamic resistance R_{L2} at oscillation frequency ω_0.

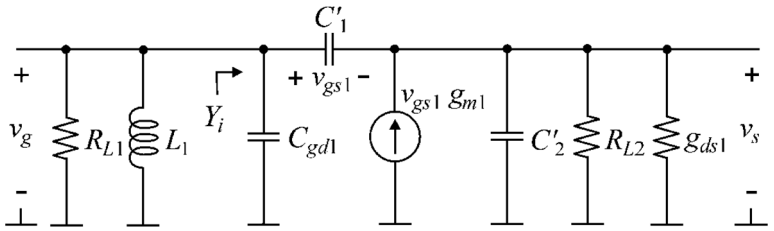

Figure 2. Small-signal model of HSCO shown in Figure 1c.

In Figure 2, the transistor M_1, represented by g_{m1} and g_{ds1}, together with the capacitors C'_1, C'_2 and the dynamic resistance R_{L2} form a circuit that implements the admittance Y_i with negative real part (conductance). The negative conductance allows compensation for the losses of inductor L_1, represented by R_{L1}. The real and imaginary parts of the admittance $Y_i(\omega)$ seen from the gate of M_1 are

$$\mathrm{Re}\{Y_i(\omega)\} = \frac{\omega^2 C'^2_1 R_0 \left[1 - g_{m1} R_0 \frac{C'_2}{C'_1}\right]}{(1 + g_{m1} R_0)^2 + \omega^2 (C'_1 + C'_2)^2 R_0^2} \tag{1}$$

$$\mathrm{Im}\{Y_i(\omega)\} = \omega C_{gd1} + \frac{\omega C'_1 \left[1 + g_{m1} R_0 + \omega^2 R_0^2 C'_2 \left(C'_1 + C'_2\right)\right]}{(1 + g_{m1} R_0)^2 + \omega^2 \left(C'_1 + C'_2\right)^2 R_0^2} \tag{2}$$

where: $C'_1 = C_1 + C_{gs1}$, $C'_2 = C_2 + C_{sb1} - 1/(\omega^2 L_2)$, $R_0 = 1/(g_{ds1} + 1/R_{L2})$. The negative real part of the admittance $Y_i(\omega)$ can be obtained when the following condition is satisfied

$$\frac{C'_2}{C'_1} > \frac{1}{R_0 g_{m1}} \tag{3}$$

For a transistor operating at low supply voltage, this condition also means that $C'_2 >> C'_1$, due to the fact that $1/R_0 >> g_{m1}$. Therefore, further considerations are restricted to such a case. The L_1 inductor losses will be compensated and oscillations with frequency ω_0 will start if the following conditions are met

$$\mathrm{Re}\{Y_i(\omega_0)\} < -1/R_{L1} \tag{4}$$

$$\mathrm{Im}\{Y_i(\omega_0)\} = -\frac{1}{\omega_0 L_1} \tag{5}$$

With the condition $C'_2 >> C'_1$, the Equation (1) can be simplified to

$$\mathrm{Re}\{Y_i(\omega)\} \cong \frac{\omega^2 C'^2_1 R_0 \left(1 - g_m R_0 \frac{C'_2}{C'_1}\right)}{1 + \omega^2 C'^2_2 R_0^2} \tag{6}$$

The simplified Equation (6) was derived under assumption that $g_{ds1} >> g_{m1}$ which is satisfied when M_1 operates at very low supply voltages. To satisfy the Equation (4), transconductance of M_1 must fulfill

$$g_{m1} > \left(\frac{C'_1}{C'_2}\right)\frac{1}{R_0} + \left(\frac{C'_2}{C'_1}\right)\frac{1}{R_{L1}} + \frac{1}{\omega_0^2 C'_1 C'_2 R_0^2 R_{L1}} \tag{7}$$

The absolute minimum transconductance g_{m1} can be achieved when both inductors are lossless (R_{L1}, $R_{L2} \to \infty$). In such a case, oscillations will start when the transconductance of M_1 meets the condition

$$g_{m1} > \left(\frac{C'_1}{C'_2}\right)\frac{1}{R_0} \overset{g_{ds1} \gg 1/R_{L2}}{\to} \left(\frac{C'_1}{C'_2}\right) g_{ds1} \tag{8}$$

It is worth noting that in theory by minimization of C'_1/C'_2 ratio an arbitrarily small value of g_{m1} can be achieved, and thus an arbitrarily low supply voltage can be obtained. In practice the inductors are lossy, therefore g_{m1} can be reduced by minimizing the last component of Equation (7) and by selecting the optimal value of the C'_2/C'_1 ratio. Reduction of the last component in Equation (7) requires that

$$\omega_0^2 C'_1 C'_2 R_0^2 \overset{g_{ds1} \gg 1/R_{L2}}{\to} \frac{\omega_0^2 C'_1 C'_2}{g_{ds1}^2} >> 1 \tag{9}$$

Under the assumption that Equation (9) is fulfilled, the optimal value of the capacitance ratio is given as

$$\frac{C'_2}{C'_1} = \sqrt{\frac{R_{L1}}{R_0}} \overset{g_{ds1} \gg 1/R_{L2}}{\to} \sqrt{g_{ds1} R_{L1}} \tag{10}$$

and the minimum transconductance required to start the oscillations is

$$g_{m1,min} > \frac{2}{\sqrt{R_{L1} R_0}} > 2\sqrt{\frac{1 + g_{ds1} R_{L2}}{R_{L1} R_{L2}}} \overset{g_{ds1} \gg 1/R_{L2}}{\to} 2\sqrt{\frac{g_{ds1}}{R_{L1}}} \tag{11}$$

Note that according to Equation (9), it is advantageous to choose the highest possible oscillation frequency (ω_0) and the largest capacitances C'_1, C'_2. Thus, in order to minimize the transconductance required to start oscillations in Equation (7), small inductances L_1 and L_2 and large capacitances C'_1, C'_2 are advantageous, which is also very beneficial for integration of the oscillator.

3. Minimum Supply Voltage Required to Start ULV Oscillators

Low supply voltage and high output swing are important criteria for choosing an oscillator as a starter for ULV boost converter. To identify which of the configurations shown in Figure 1 is best suited as a starter, the minimum supply voltages of these circuits were determined and compared. In further considerations ESILRO is omitted due to the need for four inductors, which is difficult to integrate. N-channel MOS transistors with near-zero threshold voltage as well as negative threshold voltage are good candidates for implementing ULV oscillators because they provide relatively high drain current at supply voltages below a few tens of mV [18,19,21]. Therefore, the minimum supply voltages of ESCO and HSCO were determined for the transistor operating in the weak and strong inversion regions.

For the sake of simplicity, in the compared oscillators it was assumed that both inductances as well as their losses are identical ($L_1 = L_2$, $G_{L1} = G_{L2}$). According to the analysis presented in [19], oscillations will start in ESCO if the following condition holds

$$\frac{g_{ms1}}{g_{md1}} > a + \frac{a^2+1}{a-1}\frac{G_{L1}}{g_{md1}} \tag{12}$$

where

$$a = 1 + \sqrt{\frac{2G_{L1}/g_{md1}}{G_{L1}/g_{md1}+1}} \tag{13}$$

where g_{ms1} and g_{md1} are the source and drain transconductances [19,20]. The ratio of these conductances for strong and weak inversion regions can be approximated [19,20] by

$$\frac{g_{ms1}}{g_{md1}} = \frac{V_{DS}V_{T0}}{V_{DS}(1-n)-V_{T0}} \tag{14}$$

$$\frac{g_{ms1}}{g_{md1}} = \exp\left(\frac{V_{DS}}{U_T}\right) \tag{15}$$

where V_{T0} is the threshold voltage, n is the slope factor of the current-voltage characteristic in the weak inversion region, U_T is the thermal voltage, and V_{DS} is the drain-source voltage.

The minimum supply voltage necessary to start oscillations in ESCO can be determined from Equations (12)–(15) for the strong and weak inversion regions, respectively [19]

$$V_{DD,min} > \frac{\left(1-\frac{G_{L1}}{g_{md1}}\right)V_{T0}}{1-(1-n)\frac{G_{L1}}{g_{md1}}} \tag{16}$$

$$V_{DD,min} > U_T \ln\left(a + \frac{a^2+1}{a-1}\frac{G_{L1}}{g_{md1}}\right) \tag{17}$$

In HSCO, oscillations start when Equation (11) is satisfied. Based on this equation, the minimum ratio of the gate transconductance (g_{m1}) to the output conductance (g_{ds1}) of the transistor can be determined as

$$\frac{g_{m1,min}}{g_{ds1}} > 2\sqrt{\frac{G_{L1}}{g_{ds1}}} \tag{18}$$

where G_{L1}/g_{ds1} represents the ratio of L_1 losses, modeled by $G_{L1} = 1/R_{L1}$, to the transistor output conductance. The ratio of the transistor transconductance to its output conductance for the strong and weak inversion regions can be defined [19,20] as

$$\frac{g_{m1}}{g_{ds1}} = \frac{nV_{DS}}{V_{DS}(1-n)-V_{T0}} \tag{19}$$

$$\frac{g_{m1}}{g_{ds1}} = \frac{1}{n}\left(\exp\left(\frac{V_{DS}}{U_T}\right)-1\right) \tag{20}$$

The minimum supply voltage for HSCO, $V_{DD,min}$, determined based on Equations (18)–(20), is for the strong and weak inversion regions, respectively

$$V_{DD,min} > \frac{-2V_{T0}\sqrt{G_{L1}/g_{ds1}}}{n-2(1-n)\sqrt{G_{L1}/g_{ds1}}} \tag{21}$$

$$V_{DD,min} > U_T \ln\left(1+n\sqrt{G_{L1}/g_{ds1}}\right) \tag{22}$$

The comparison of the minimum supply voltage, $V_{DD,min}$, defined by Equations (16), (17), (21) and (22), for ESCO and HSCO is plotted in Figure 3a,b, for the strong and weak inversion regions, respectively. The calculations for the strong inversion region are based on extracted values of V_{T0} and n for particular $V_{GS} = V_{DS} = V_{DD}$ voltage values for a native n-channel MOS transistor (W/L = 2500 µm/1 µm) in X-FAB 180-nm CMOS technology. The plots for the weak inversion were made for U_T = 26 mV and similar values of the parameter n.

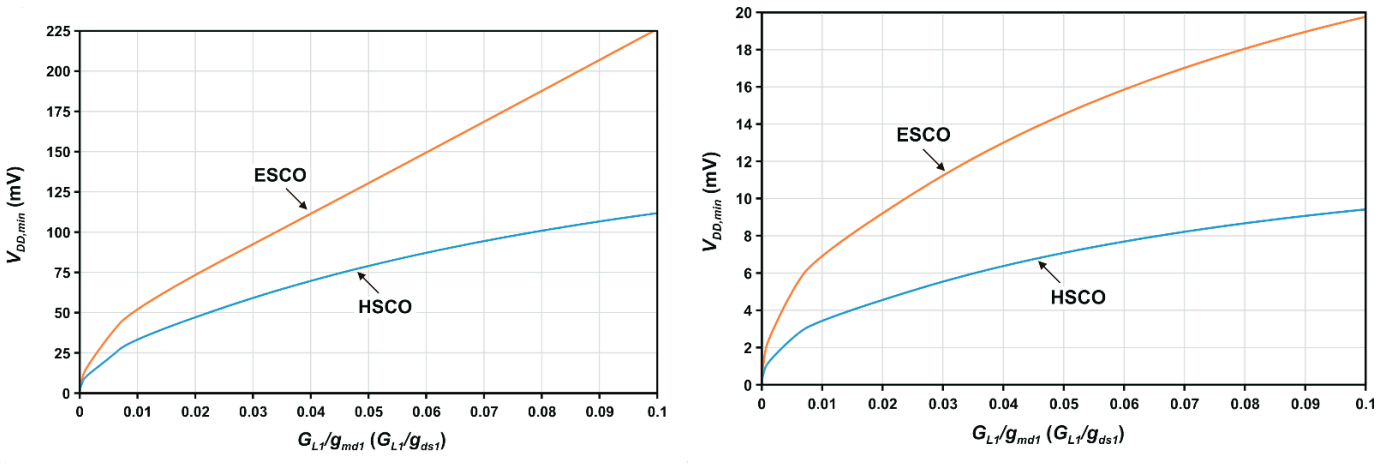

Figure 3. The minimum supply voltage, $V_{DD,min}$, required to start oscillations in ESCO and HSCO as a function of G_{L1}/g_{md1} (G_{L1}/g_{ds1}), for the transistor operating in: (**a**) the strong inversion region; (**b**) the weak inversion region.

The results in Figure 3a,b show that HSCO requires significantly lower supply voltage compared to ESCO. This feature is particularly evident for high values of G_{L1}/g_{ds1}, which corresponds to use of low quality factor inductors. The general Equations (16), (17), (21) and (22), defining the minimum startup voltage, were derived based on a simplified linear model. To provide more in-depth investigation of the considered oscillators properties, number of HSCO and ESCO oscillator designs using native n-channel MOS transistors with negative threshold voltage were prepared for a 180-nm X-FAB technology. For each oscillator design, the component parameters were optimized to obtain the minimum startup voltage, $V_{DD,min}$, for selected values of: G_{L1}/g_{md1} (G_{L1}/g_{ds1}), inductances $L_1 = L_2$, and inductor quality factors Q_L. A summary of the oscillators parameters is shown in Table 1.

Table 1. Summary of parameters of ULV oscillators.

G_{L1}/g_{ds1}	$V_{DD,min}$	C_1	C_2	L_1	L_2	Q_L	$f_0 = \omega_0/(2\pi)$
			HSCO				
0.001	10 mV	3.8 nF	120 nF	10 µH	10 µH	255	820 kHz
0.005	24 mV	4 nF	60 nF	10 µH	10 µH	51	826 kHz
0.01	37 mV	4.2 nF	50 nF	10 µH	10 µH	26	806 kHz
			ESCO				
0.001	20 mV	73 nF	9 nF	10 µH	10 µH	275	770 kHz
0.005	37 mV	45 nF	9 nF	10 µH	10 µH	55	758 kHz
0.01	54 mV	45 nF	11 nF	10 µH	10 µH	29	715 kHz

Based on the data from Table 1, one can see that HSCO oscillator, compared to the ESCO, exhibits lower inrush voltage for similar values of G_{L1}/g_{ds1} and inductor quality factor Q_L. For the variants G_{L1}/g_{ds1} = 0.001, Q_L = 255, and G_{L1}/g_{ds1} = 0.005, Q_L = 51 a series of simulations for HSCO and ESCO were performed showing the peak-to-peak value

of the output voltage, $v_{OUT\text{-}PP}$, as a function of the supply voltage V_{DD} (Figure 4). For the high inductor quality factor case, a noticeable limitation of the output voltage is observed as the ESCO supply voltage increases. This effect is caused by forward biasing of the pn junction between the transistor drain and substrate.

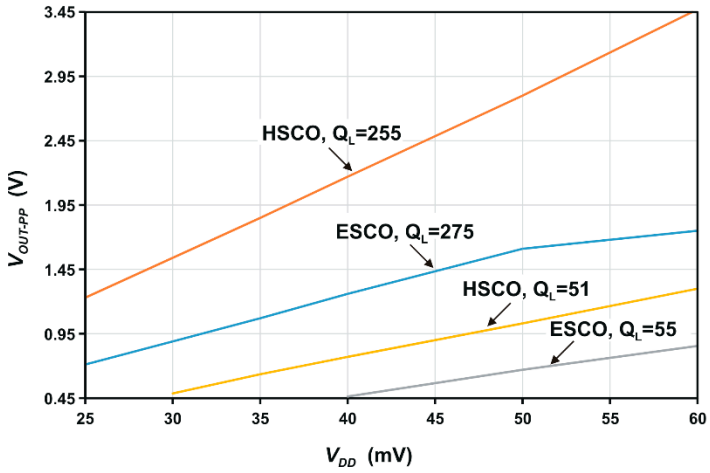

Figure 4. Peak-to-peak values of the output voltage, $v_{OUT\text{-}PP}$, as a function of the supply voltage, V_{DD}, for HSCO and ESCO.

For all the considered ULV oscillators, the main factor limiting amplitude of the output voltage is a relatively large drain to source conductance of a transistor. Due to this fact, the transistor internal gain is relatively small, especially in HSCO. The gain in this configuration can be increased by increasing the supply voltage V_{DD}, but this is unfavorable because ULV oscillators should operate for the lowest possible supply voltage. To overcome this limitation, an improved version of HSCO was developed, as shown in Figure 5.

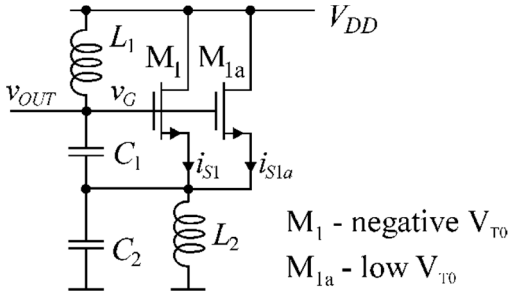

Figure 5. Improved version of HSCO.

In this oscillator, two transistors connected in parallel are used. M_1 is a transistor with negative or near-zero threshold voltage, whereas M_{1a} is a low-threshold-voltage transistor. The transistor M_1 plays the same role as in the circuit of Figure 1c and serves mainly to initiate the oscillation, while M_{1a} acts as an additional booster which is activated when the output voltage v_{OUT} reaches a sufficient amplitude. Notice that introduction of M_{1a} does not lead to noticeable increase of the output conductance of the composite transistor (M_1 + M_{1a}), because it is switched off for most of the time of the periodic waveform. This transistor is only turned on for short periods of time when the voltage at its gate exceeds a threshold value. Time waveforms illustrating operation of the circuit are shown in Figure 6.

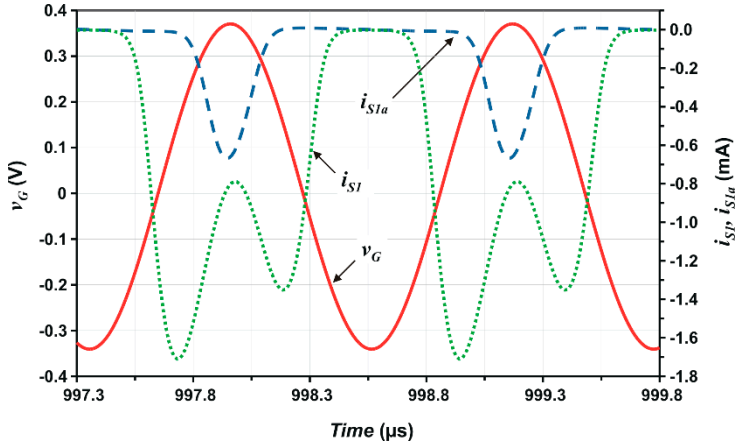

Figure 6. Time waveforms of the signals in the improved HSCO.

To demonstrate the advantage of the improved oscillator, the peak-to-peak values of the output voltage as a function of the supply voltage for ESCO, HSCO and improved HSCO are plotted in Figure 7.

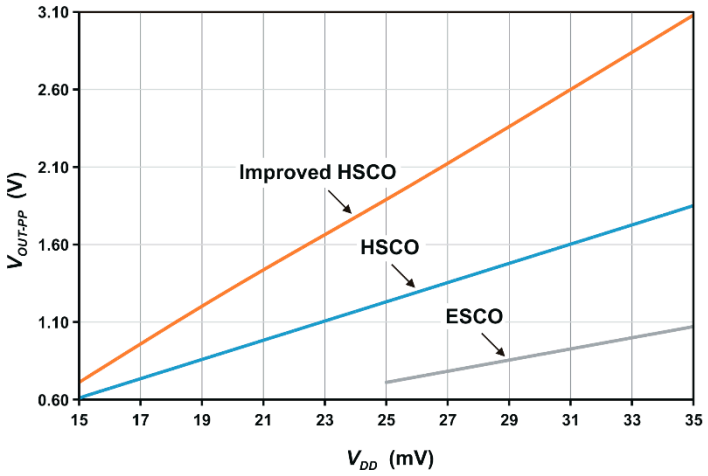

Figure 7. Peak-to-peak values of the output voltage, $v_{OUT\text{-}PP}$, as a function of the supply voltage, V_{DD}, for ESCO, HSCO and improved HSCO ($G_{L1}/g_{ds1} = G_{L1}/g_{dm1} = 0.0025$, $Q_L = 100$).

4. Starter Based on the Improved HSCO

The key component of the proposed starter is the improved HSCO oscillator (Figure 5) which is capable of generating the highest output voltage at low supply voltages (Figure 7). As the plots in Figure 3 show, the most advantageous is to use a transistor with a near-zero threshold voltage that operates in the weak inversion region. In the chosen X-FAB 180 nm CMOS technology a zero-threshold-voltage transistor is not available. Thus, the most suitable transistor available was used, namely a n-channel native MOS transistor with a negative threshold voltage of approximately −180 mV. The starter consists of the improved HSCO and a 3-stage voltage multiplier, as shown in Figure 8.

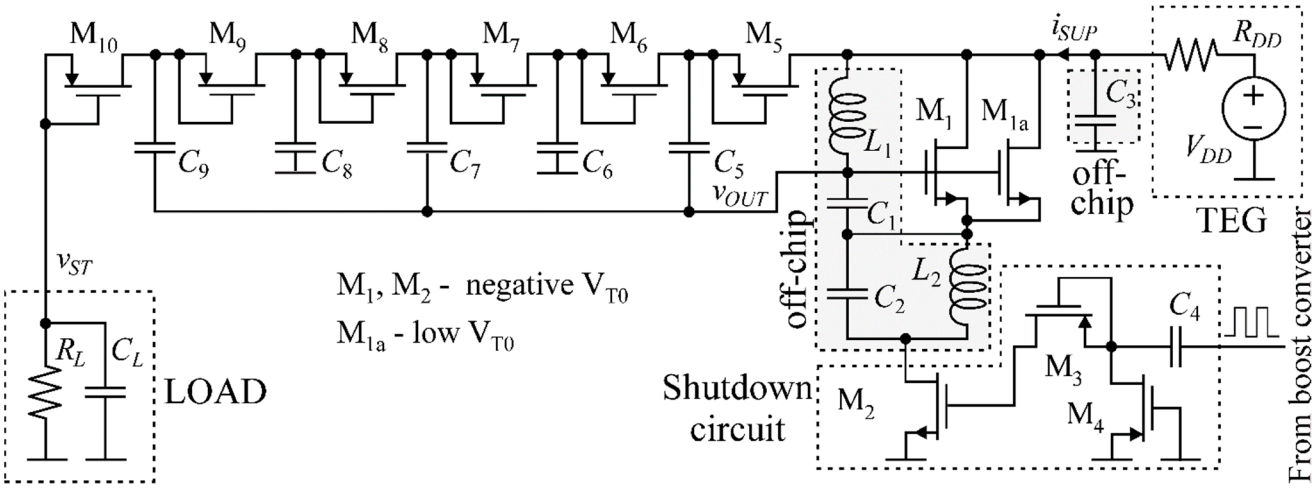

Figure 8. Starter based on the improved HSCO.

This solution is additionally equipped with a shutdown circuit which allows its disabling when the main boost converter starts running. The shutdown circuit, consisting of M_2, M_3, M_4, and C_4 is placed in the main current path and allows for complete cutoff of the supplying current. With this solution, when the main boost converter is running, the starter does not increase power consumed from the supply source. M_2 in the shutdown circuit requires a negative voltage to be turned off. This voltage is obtained through rectification (by means of M_3, M_4, and C_4) the square wave voltage applied to control the boost converter switches. The parameters of the starter components are given in Table 2.

Table 2. Parameters of the starter components.

M_1	M_{1a}	M_2	M_3, M_4	M_5–M_{10}
1500 µm/1 µm	75 mm/0.22 µm	30 mm/1 µm	0.22 µm/0.22 µm	50 µm/0.22 µm
C_1 2.9 nF	C_2 100 nF	C_3 10 µF	C_4 0.5 pF	C_5–C_9 15 pF
C_L 25 pF	R_L 1 MΩ	L_1, L_2 10 µH	Q_{L1}, Q_{L2} 100	R_{DD} 5 Ω

The HSCO startup process is illustrated in Figure 9 showing the oscillator output voltage, v_{OUT}, waveform. Two phases of startup can be clearly observed in this plot. The first one, covering the time interval up to about 1.4 ms, is mainly related to operation of the transistor M_1. The second phase begins when the voltage amplitude exceeds the threshold voltage of M_{1a}. During this time interval, additional current pulses are generated to further increase the amplitude of v_{OUT}. The plot also illustrates the shutdown moment, which occurs at 2 ms.

The voltage waveform at the output of the starter, v_{ST}, is shown in Figure 10. It can be seen that obtaining v_{ST} above 1 V became possible only after boosting the oscillator by the transistor M_{1a}. The effectiveness of the shutdown circuit can be determined based on the waveform of the current i_{SUP} sourced from the supply V_{DD}. In shutdown state, i_{SUP} decreases to a few tens of nA.

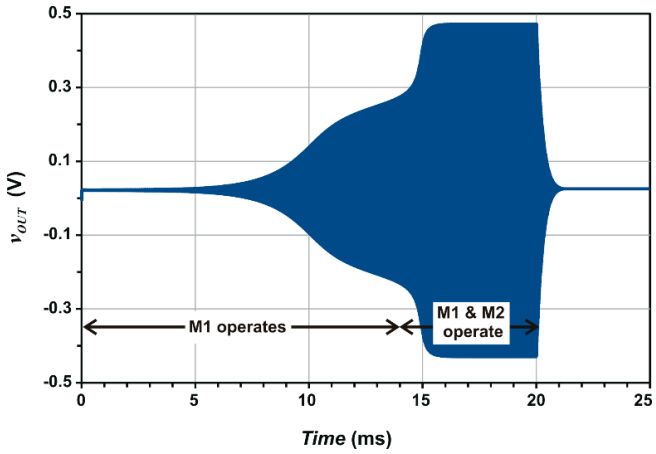

Figure 9. The output voltage, v_{OUT}, waveform in HSCO illustrating the startup process.

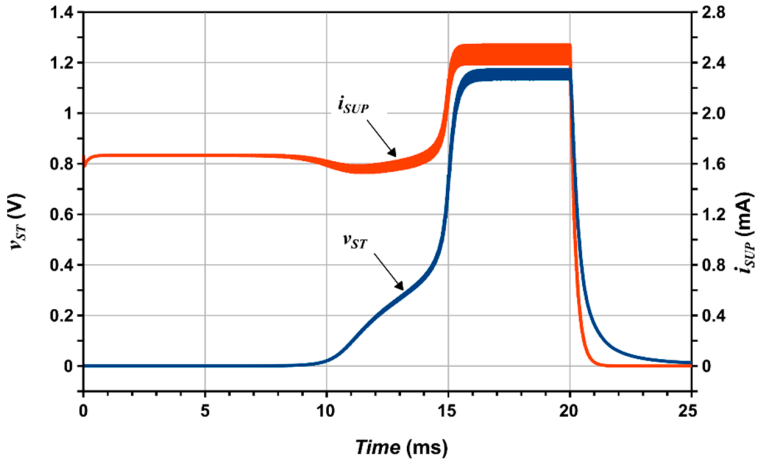

Figure 10. Waveforms of the output voltage (v_{ST}) and current (i_{SUP}) sourced from supply in the starter.

The effect of temperature changes and variations of technology parameters, represented by corners, on the startup voltage is shown in Figure 11. The worst case startup voltage is 29 mV at 50 °C under worst-speed (WS—slow NMOS, slow PMOS) and worst-zero (WZ—slow PMOS, fast PMOS) corners. Therefore, the proposed starter enables reliable start at supply voltages greater than 29 mV.

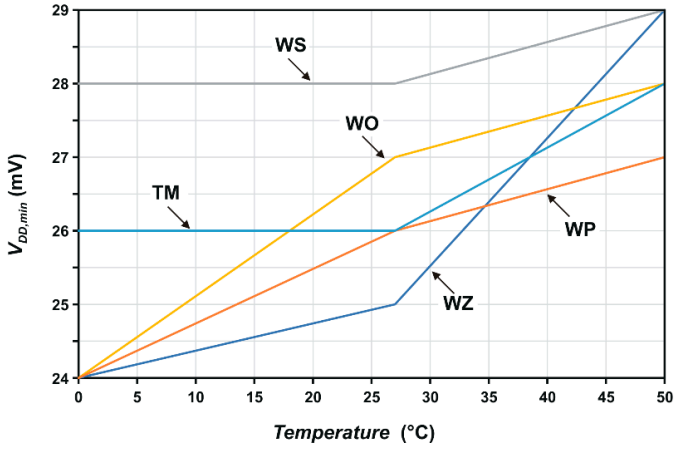

Figure 11. Minimal startup voltage, $V_{DD,min}$, as a function of temperature and variations of technology parameters, represented by corners.

A comparison of the main features of the developed starter with solutions reported in the literature is given in Table 3. The developed starter has a startup voltage which is within the lower range of voltages generated by TEGs. It should be emphasized that the startup voltage can be further reduced for CMOS technologies where zero threshold voltage transistors are available. The developed starter needs two external inductors (L_1, L_2), where L_2 can be of low quality, and two external capacitors (C_1, C_2). In the presented solution, the oscillation frequency is about 1 MHz, but can be increased to more than 10 MHz, allowing further reduction of external inductors and capacitors leading to a higher degree of miniaturization. The power efficiency of the proposed starter is approximately 1.5%. However, it should be emphasized that such low efficiency is not important since the starter operates only in the initial phase of the converter start-up and then is immediately turned off.

Table 3. Comparison of starters.

Parameters	[7]	[9]	[10]	[12]	This Work [1]
CMOS technology	130 nm	130 nm	65 nm	130 nm	180 nm
Minimal startup voltage	21 mV	40 mV	50 mV	11 mV	29 mV
Output voltage	1 V	2 V	1.2 V	1 V	>1 V
Power consumption/conversion efficiency	N/A N/A	N/A N/A	N/A N/A	N/A N/A	70 µW 1.5%
External components	Transformer 2 capacitors 1 diode	Transformer 3 capacitors 1 diode	2 inductors 2 capacitors	4 inductors 4 capacitors	2 inductors 3 capacitors

[1] Results of simulations.

5. Conclusions

A comparison of ULV oscillators, suitable for on-chip implementation, in terms of critical features for their use as starters in boost converters was presented. Based on the analysis, the improved oscillator configuration featuring a small startup voltage and a large output voltage swing was proposed. These features allow for simplification of the starter design. With the developed oscillator, a starter for on-chip implementation was designed that meets the requirements for using TEG as a power source. Compared to known solutions, the proposed starter offers greater miniaturization owing to the possibility of using smaller inductors with lower quality.

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References

1. Prabha, R.D.; Rincon-Mora, G.A. CMOS photovoltaic-cell layout configurations for harvesting microsystems. In Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus, OH, USA, 4–7 August 2013; pp. 368–371. [CrossRef]
2. Ramadass, Y.; Chandrakasan, A. An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor. *IEEE J. Solid State Circ.* **2010**, *45*, 189–204. [CrossRef]

3. Leonov, V.; Torfs, T.; Fiorini, P.; Van Hoof, C. Thermoelectric converters of human warmth for self-powered wireless sensor nodes. *IEEE Sens. J.* **2007**, *5*, 650–657. [CrossRef]
4. Yang, Y.; Wei, X.-J.; Liu, J. Suitability of a thermoelectric power generator for implantable medical electronic devices. *J. Phys. D Appl. Phys.* **2007**, *40*, 5790–5800. [CrossRef]
5. Morais, F.; Carvalhaes-Dias, P.; Duarte, L.; Spengler, A.; de Paiva, K.; Martins, T.; Cabot, A.; Siqueira Dias, J. Optimization of the TEGs Configuration (Series/Parallel) in Energy Harvesting Systems with Low-Voltage Thermoelectric Generators Connected to Ultra-Low Voltage DC–DC Converters. *Energies* **2020**, *13*, 2297. [CrossRef]
6. Carlson, E.; Strunz, K.; Otis, B. A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting. *IEEE J. Solid State Circ.* **2010**, *45*, 741–750. [CrossRef]
7. The, Y.-K.; Mok, P.K.T. Design of Transformer-Based Boost Converter for High Internal Resistance Energy Harvesting Sources with 21 mV Self-Startup Voltage and 74% Power Efficiency. *IEEE J. Solid State Circ.* **2014**, *49*, 2694–2704. [CrossRef]
8. Ramadass, Y.; Chandrakasan, A. A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage. *IEEE J. Solid State Circ.* **2011**, *46*, 333–341. [CrossRef]
9. Im, J.-P.; Wang, S.-W.; Ryu, S.-T.; Cho, G.-H. A 40 mV Transformer-Reuse Self-Startup Boost Converter with MPPT Control for Thermoelectric Energy Harvesting. *IEEE J. Solid State Circ.* **2012**, *47*, 3055–3067. [CrossRef]
10. Weng, P.-S.; Tang, H.-Y.; Ku, P.-C.; Lu, L.-H. 50 mV-input batteryless boost converter for thermal energy harvesting. *IEEE J. Solid State Circ.* **2013**, *48*, 1031–1041. [CrossRef]
11. Katic, J.; Rodriguez, S.; Rusu, A. A Dual-Output Thermoelectric Energy Harvesting Interface with 86.6% Peak Efficiency at 30 μW and Total Control Power of 160 nW. *IEEE J. Solid State Circ.* **2016**, *51*, 189–204. [CrossRef]
12. Radin, R.L.; Sawan, M.; Galup-Montoro, C.; Cherem Schneider, M. A 7.5-mV-Input Boost Converter for Thermal Energy Harvesting with 11-mV Self-Startup. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2020**, *67*, 1379–1383. [CrossRef]
13. Dezyani, M.; Ghafoorifard, H.; Sheikhaei, S.; Serdijn, W.A. A 60 mV Input Voltage, Process Tolerant Start-Up System for Thermoelectric Energy Harvesting. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2018**, *65*, 3568–3577. [CrossRef]
14. Lim, B.-M.; Seo, J.-I.; Lee, S.-G. A Colpitts Oscillator-Based Self-Starting Boost Converter for Thermoelectric Energy Harvesting with 40-mV Startup Voltage and 75% Maximum Efficiency. *IEEE J. Solid State Circ.* **2018**, *53*, 3293–3302. [CrossRef]
15. Blakiewicz, G.; Jakusz, J.; Kłosowski, M.; Jendernalik, W.; Szczepański, S. Light-Powered Starter for Micro Power Boost DC-DC Converter for CMOS Image Sensors. *Circuits Syst. Signal Process.* **2020**, *39*, 1195–1212. [CrossRef]
16. Goeppert, J.; Manoli, Y. Fully Integrated Startup at 70 mV of Boost Converters for Thermoelectric Energy Harvesting. *IEEE J. Solid State Circ.* **2016**, *51*, 1716–1726. [CrossRef]
17. Yi, H.; Yin, J.; Mak, P.-I.; Martins, R.P. A 0.032-mm^2 0.15-V Three-Stage Charge-Pump Scheme Using a Differential Bootstrapped Ring-VCO for Energy-Harvesting Applications. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2018**, *65*, 146–150. [CrossRef]
18. Galup-Montoro, C.; Schneider, M.C.; Machado, M.B. Ultra-Low-Voltage Operation of CMOS Analog Circuits: Amplifiers, Oscillators, and Rectifiers. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2012**, *59*, 932–936. [CrossRef]
19. Machado, M.B.; Schneider, M.C.; Galup-Montoro, C. On the Minimum Supply Voltage for MOSFET Oscillators. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2014**, *61*, 347–357. [CrossRef]
20. Enz, C.; Krummenacher, F.; Vittoz, E.A. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. *J. Anal. Integr. Circuits Signal Process.* **1995**, *8*, 83–114. [CrossRef]
21. Alioto, M. Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2012**, *59*, 3–29. [CrossRef]