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A Novel Predictive Control Method with Optimal Switching Sequence and Filter Resonance Suppression for Two-Stage Matrix Converter

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Abstract: This paper proposes a vector modulation-based model predictive current control strategy for a two-stage matrix converter. The switching frequency is kept constant by fixing the switching instantly. The control scheme controls the source reactive power on the input side and output currents on the output side. Besides, the advantage of the proposed strategy compared with conventional model predictive control is firstly proved using the principle of vector synthesis and the law of sines in the vector distribution area. Moreover, to ensure zero-current switching operations and reduce the switching losses, an optimal switching sequence is proposed and implemented. Furthermore, considering that the input filter resonance is easier to be inspired by the model predictive control, compared with conventional linear control strategies, an innovative active damping technique is proposed to suppress the input filter resonance. To assess the performance of the proposed method, simulation and experimental results are demonstrated, showing that the control system features both good steady-state and transient performance.

Keywords: two-stage matrix converter; model predictive control; vector modulation; optimal switching strategy; input filter resonance suppression



Citation: Di, Z.; Xu, D.; Tarisciotti, L.; Wheeler, P. A Novel Predictive Control Method with Optimal Switching Sequence and Filter Resonance Suppression for Two-Stage Matrix Converter. *Energies* **2021**, *14*, 3652. <https://doi.org/10.3390/en14123652>

Academic Editors:

Mariusz Malinowski, Steffen Bernet, Marcelo A. Perez and Sebastian Styński

Received: 29 May 2021

Accepted: 16 June 2021

Published: 19 June 2021

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1. Introduction

A matrix converter is a compact ac-ac power converter, in which dc-link capacitors are not used [1]. A matrix converter is commonly divided into a one-stage matrix converter (OSMC) and two-stage matrix converter (TSMC) with the same transfer function, and the TSMC is divided into the rectifier stage and the inverter stage, where the rectifier stage is based on a conventional three-phase full-bridge [2,3]. In recent years, this converter family has been globally studied in power topologies, control schemes, and trends [4–7]. Because of the absence of dc-link capacitors, the input side of the matrix converter directly connects the output side, coupling the input and output currents and voltages [4,5]. Compared with the traditional control schemes of the matrix converter, like the Venturini method [4,6], direct power control [7], and so on, the space vector modulation (SVM) method has been proved as a suitable control strategy [8,9]. In SVM, the input and output voltages and currents are considered using space vectors [10,11]. However, model predictive control defies SVM with the emergence of developing digital processors and power devices [12–14]. In this control scheme, the matrix converter's future behaviors are predicted and optimized by minimizing a user-defined and model-based cost function, featuring many advantages such as simpler modifications, easier implementations in modern digital control platforms, and so on [15–17].

However, model predictive control (MPC) defies SVM with the emergence of developing digital processors and power devices [12–14]. In this control scheme, the matrix

converter's future behaviors are predicted and optimized by minimizing a user-defined and model-based cost function, featuring many advantages such as simpler modifications, easier implementations in modern digital control platforms, and so on [15–17]. In [15], a simple digital predictive current control strategy without the modulation stage was proposed for the two-level four-leg inverters, where both balanced and unbalanced loading conditions were considered. In [16], a new speed finite control set model predictive control (FCS-MPC) algorithm was proposed and applied for a permanent-magnet synchronous motor driven by a matrix converter, in which the comparison between classical modulation methods and the FCS-MPC was carried out with the simulation and the experiment. In [17], a simplified FCS-MPC method was proposed to reduce the calculation efforts for the application in matrix converter-fed permanent magnet synchronous motors, including a new cost function controlling currents during both speed transient and steady-state conditions and an input filter observer increasing the system reliability. However, the major weakness of the FCS-MPC is the lack of modulation, where only one optimal switching state is determined and applied in one sampling period. Owing to this weakness, variable switching frequency and a broad harmonic spectrum are produced, which lead to unexpected ripples in the system and affect the system's power-quality performance [18]. To overcome these problems, the modulated model predictive control (MMPC) strategy is introduced [19–23], where the switching frequency is kept constant and more than one switching states are determined and applied by the two independent cost functions of the rectifier and the inverter in an appropriately fixed switching instant. In [19], the MMPC strategy was proposed for shunt active filters, where a cost function ratio for output vectors-based modulation algorithm was included in the MPC. In [20], a three-vector-based low-complexity model predictive direct power control scheme was proposed and applied for doubly fed induction generators, aiming to eliminate the steady-state errors and reduce the current ripples. In [21], the MMPC was proposed and applied for the modular multilevel converters in voltage source converter-high voltage dc systems, where modulated switching signals with a fixed switching frequency were applied to minimize the ac line current ripples. In [22], a continuous control set model predictive control (CCS-MPC) scheme was proposed for the constant voltage constant frequency inverters, in which a fuzzy logic approach corrected the input voltage commands to obtain a faster transient response and smaller steady-state error. In [23], a comparative study of the FCS-MPC and the CCS-MPC for induction machine in terms of their design and performance was conducted, in which the behaviors were assessed by applying reference and disturbance steps to the system in different operational modes. The CCS-MPC was proved to feature smaller current ripples and could cope with a less powerful DSP than the FCS-MPC.

Besides, some research work has been done about the optimal pulse patterns [24,25]. In [24], an optimal six vector switching pattern based on the SVM has been proposed for matrix converters to reduce harmonics and switching losses, in which a faster response, lower harmonics, and lower losses have been obtained than those using the five vector pattern. The weaknesses of this method are larger $1/2$ and $3/2$ sampling frequency harmonics and increased complexity. In [25], an offline computed optimal pulse pattern has been proposed based on modulated model predictive control for a delta-connected modular multilevel converter, which facilitates the shaping of the grid current spectrum at low switching frequencies.

For matrix converters, an input filter is usually employed to prevent the line-current ripples. However, the converter itself and the potential harmonics in the ac source usually excite the series resonance and the parallel resonance of the input filter, leading to highly distorted line-side currents, which can also transfer to the load side because of the direct topology [26–30]. To solve this problem, several damping methods have been proposed. In [26], the researcher proposed a passive damping method by placing a damping resistor in parallel with the filter inductor, which can mitigate the resonance but draw more power losses and less attenuation around switching frequency. Besides, as discussed in [27], this method is not suitable for some specific applications, such as a generator source where

stator inductance acts as the filter inductor. To improve this, some active damping methods have been proposed, where physical resistors are not used [28–30]. In [28], the filtered capacitor voltages were added into the input current references in the active damping method, which can suppress the oscillations effectively but only work for the independent control of input currents. In [29], an iterative design method in consideration of the most significant grid-current harmonics is proposed to decide the filter parameters, using a PWM strategy. In [30], another active damping method is proposed by modifying the input current reference, using the SVM strategy. This method is not applicable to the predictive control where the input current reference is not required. Most of these schemes include complex control methods.

To solve these problems above, this paper proposes a novel predictive control method with optimal switching sequence (OSS) and input filter resonance suppression (IFRS) for the TSMC. The main contributions of this paper are as follows:

1. A vector modulation-based model predictive control (VMMPC) strategy is proposed, which features the controllable source reactive power and the controllable output currents with fixed switching frequency output waveforms.
2. In this paper, the advantage of the VMMPC strategy compared with the conventional MPC (CMPC) is firstly proved using the principle of vector synthesis and the law of sines in the vector distribution area.
3. An optimal switching sequence is proposed, which can ensure safe zero-current switching operations and reduce the switching losses. This pattern can simplify the commutation of the TSMC and avoid complex commutation strategies (e.g., four-step commutation) in traditional control methods;
4. A novel input filter resonance suppression method is proposed and implemented in the VMMPC for the TSMC, which shows good damping performance and easy implementation.

The paper is organized as follows: In Section 1, an introduction to the research problem is carried out. Section 2 describes the TSMC mathematical system model. Section 3 presents the proposed VMMPC with the OSS and the IFRS and validates the advantage of the VMMPC over the CMPC in theory. Section 4 shows the simulation results and discussion. Section 5 demonstrates the experimental results and discussion. Section 6 is the conclusion.

2. TSMC System Model

The TSMC system is composed of the rectifier stage and the inverter stage, whose topology is shown in Figure 1 [13]. This configuration can simplify the commutation strategy.

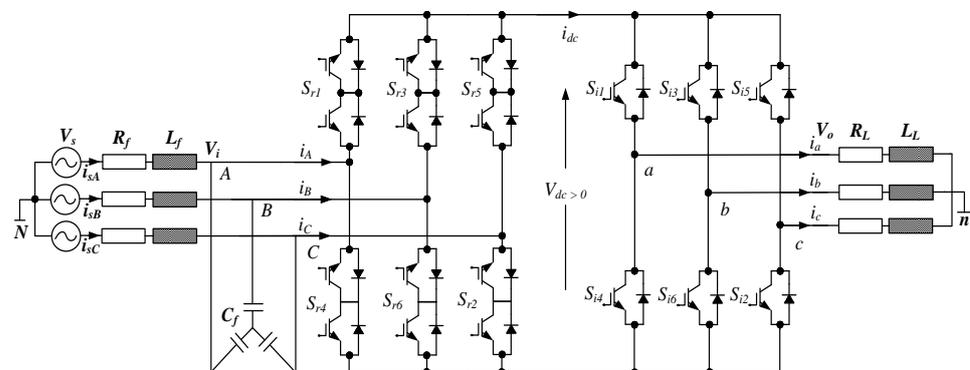


Figure 1. Power circuit of the two-stage matrix converter (TSMC) system.

For the rectifier stage, V_{dc} can be calculated with V_i and S_{r_i} as:

$$V_{dc} = [S_{r1} - S_{r4} \quad S_{r3} - S_{r6} \quad S_{r5} - S_{r2}] V_i \quad (1)$$

$$S_{ri} = \begin{cases} 0, \text{open state} \\ 1, \text{closed state} \end{cases} \quad (2)$$

where $S_{ri} \{i \in (1, 2, 3, 4, 5, 6)\}$ are the switching functions, V_{dc} is the DC-link voltage and V_i is the input voltage. Besides, i_i are calculated with S_{ri} and i_{dc} as:

$$i_i = \begin{bmatrix} S_{r1} - S_{r4} \\ S_{r3} - S_{r6} \\ S_{r5} - S_{r2} \end{bmatrix} i_{dc} \quad (3)$$

For the inverter stage, the DC-link current i_{dc} is calculated with the inverter switching functions S_{ix} and the output current i_o :

$$i_{dc} = [S_{i1} - S_{i4} \quad S_{i3} - S_{i6} \quad S_{i5} - S_{i2}] i_o \quad (4)$$

$$S_{ix} = \begin{cases} 0, \text{open state} \\ 1, \text{closed state} \end{cases} \quad (5)$$

where $S_{ix} \{x \in (1, 2, 3, 4, 5, 6)\}$ are the switching functions for the inverter stage. Moreover, the output voltage V_o is calculated with S_{ix} and V_{dc} :

$$V_o = \begin{bmatrix} S_{i1} - S_{i4} \\ S_{i3} - S_{i6} \\ S_{i5} - S_{i2} \end{bmatrix} V_{dc} \quad (6)$$

In the TSMC system, only six switching states for the rectifier stage and eight switching states for the inverter stage are valid as shown in Tables 1 and 2.

Table 1. Valid switching states of the rectifier.

V_{dc}	i_A	i_B	i_C	S_{r1}	S_{r2}	S_{r3}	S_{r4}	S_{r5}	S_{r6}
V_{AC}	i_{dc}	0	$-i_{dc}$	1	1	0	0	0	0
V_{BC}	0	i_{dc}	$-i_{dc}$	0	1	1	0	0	0
$-V_{AB}$	$-i_{dc}$	i_{dc}	0	0	0	1	1	0	0
$-V_{AC}$	$-i_{dc}$	0	i_{dc}	0	0	0	1	1	0
$-V_{BC}$	0	$-i_{dc}$	i_{dc}	0	0	0	0	1	1
V_{AB}	i_{dc}	$-i_{dc}$	0	1	0	0	0	0	1

Table 2. Valid switching states of the inverter.

i_{dc}	V_{ab}	V_{bc}	V_{ca}	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}
i_a	V_{dc}	0	$-V_{dc}$	1	1	0	0	0	1
$i_a + i_b$	0	V_{dc}	$-V_{dc}$	1	1	1	0	0	0
i_b	$-V_{dc}$	V_{dc}	0	0	1	1	1	0	0
$i_b + i_c$	$-V_{dc}$	0	V_{dc}	0	0	1	1	1	0
i_c	0	$-V_{dc}$	V_{dc}	0	0	0	1	1	1
$i_a + i_c$	V_{dc}	$-V_{dc}$	0	1	0	0	0	1	1
0	0	0	0	1	0	1	0	1	0
0	0	0	0	0	1	0	1	0	1

As seen in Figure 1, Tables 1 and 2, i_A , i_B , i_C are the three-phase input currents, V_{AB} , V_{AC} , V_{BC} are the three-phase input line voltages, V_{ab} , V_{bc} , V_{ca} are the three-phase output line voltages, and i_a , i_b , i_c are the three-phase output currents.

In addition, in order to avoid over-voltages and harmonics distortions, an input filter is implemented with its model described as follows [7]:

$$\begin{cases} \frac{di_s}{dt} = \frac{1}{L_f}(V_s - V_i) - \frac{R_f}{L_f}i_s \\ \frac{dV_i}{dt} = \frac{1}{C_f}(i_s - i_i) \end{cases} \quad (7)$$

where L_f and C_f represent the input filter inductance and capacitance, and R_f is the resistance of L_f .

Moreover, the load model can be described as follows [7]:

$$V_o = L_L \frac{di_o}{dt} + R_L i_o \quad (8)$$

where R_L and L_L are the load resistance and inductance.

3. Vector Modulation-Based Model Predictive Control Strategy with Optimal Switching Sequence and Input Filter Resonance Suppression

The proposed control strategy for the TSMC system is shown in Figure 2, which consists of source reactive power prediction, output current prediction, cost function optimization, the OSS, and the IFRS.

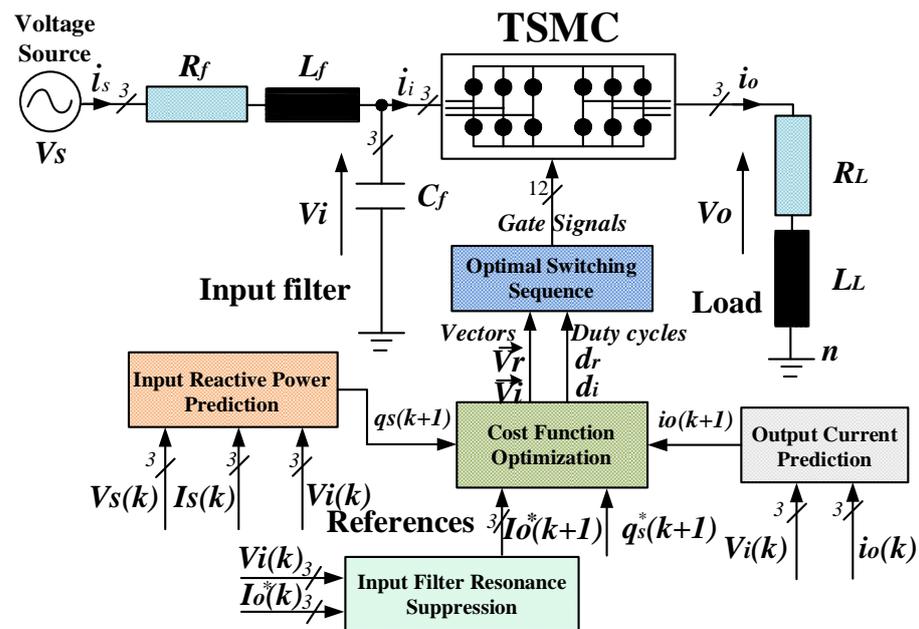


Figure 2. Block diagram of the vector modulation-based model predictive control (VMMPC) with the optimal switching sequence (OSS) and the input filter resonance suppression (IFRS).

Firstly, the IFRS generates the updated output-current reference $i_o^*(k + 1)$, then $i_o(k + 1)$ and $q_s(k + 1)$ are calculated with the output current prediction and the source reactive power prediction, which are the predicted values at the $(k + 1)^{th}$ sampling instant.

Thus, with the references $i_o^*(k + 1)$ and $q_s^*(k + 1)$, the optimal switching states are selected by the cost functions, which approach $i_o^*(k + 1)$ and $q_s^*(k + 1)$ at the end of the $(k + 1)^{th}$ sampling instant.

Finally, the OSS scheme is employed to ensure zero-current switching operations, where the vectors are symmetrically arranged.

3.1. Source Reactive Power Prediction and Output Current Prediction

For the input side, the discrete state-space model can be obtained as follows:

$$\begin{bmatrix} i_s(k+1) \\ V_i(k+1) \end{bmatrix} = \Phi_i \begin{bmatrix} i_s(k) \\ V_i(k) \end{bmatrix} + \Gamma_i \begin{bmatrix} V_s(k) \\ i_i(k) \end{bmatrix} \tag{9}$$

$$A_i = \begin{bmatrix} -R_f/L_f & -1/L_f \\ 1/C_f & 0 \end{bmatrix}, B_i = \begin{bmatrix} 1/L_f & 0 \\ 0 & -1/C_f \end{bmatrix}$$

where T_s represents the sampling time, $\Phi_i = e^{A_i T_s}$, $\Gamma_i = A_i^{-1}(\Phi_i - I)B_i$, R_f , L_f and C_f represent the input filter resistance, inductance, and capacitance. Thus, the predicted source reactive power $q_s(k+1)$ can be calculated as:

$$q_s(k+1) = v_{s\alpha}(k+1)i_{s\beta}(k+1) - v_{s\beta}(k+1)i_{s\alpha}(k+1) \tag{10}$$

where $v_{s\alpha}(k+1)$, $v_{s\beta}(k+1)$ represent the source voltage and $i_{s\alpha}(k+1)$, $i_{s\beta}(k+1)$ are the predicted source current in $\alpha\beta$ reference frame.

In the same way, the discrete state-space model of the output stage is obtained as follows:

$$i_o(k+1) = \Phi_o i_o(k) + \Gamma_o V_o(k) \tag{11}$$

where $\Phi_o = e^{-\frac{R_L}{L_L} T_s}$, $\Gamma_o = -\frac{1}{R_L}(\Phi_o - 1)$, R_L and L_L are the load resistance and inductance.

3.2. Cost Function Optimization

For the inverter stage, eight voltage space vectors are valid (six active vectors and two zero vectors) as shown in Figure 3a, and associated with switching states in Table 2. The proposed VMMPC strategy employs two valid adjacent vectors V_{i1} , V_{i2} and one zero vector V_{i0} or two zero vectors (if necessary).

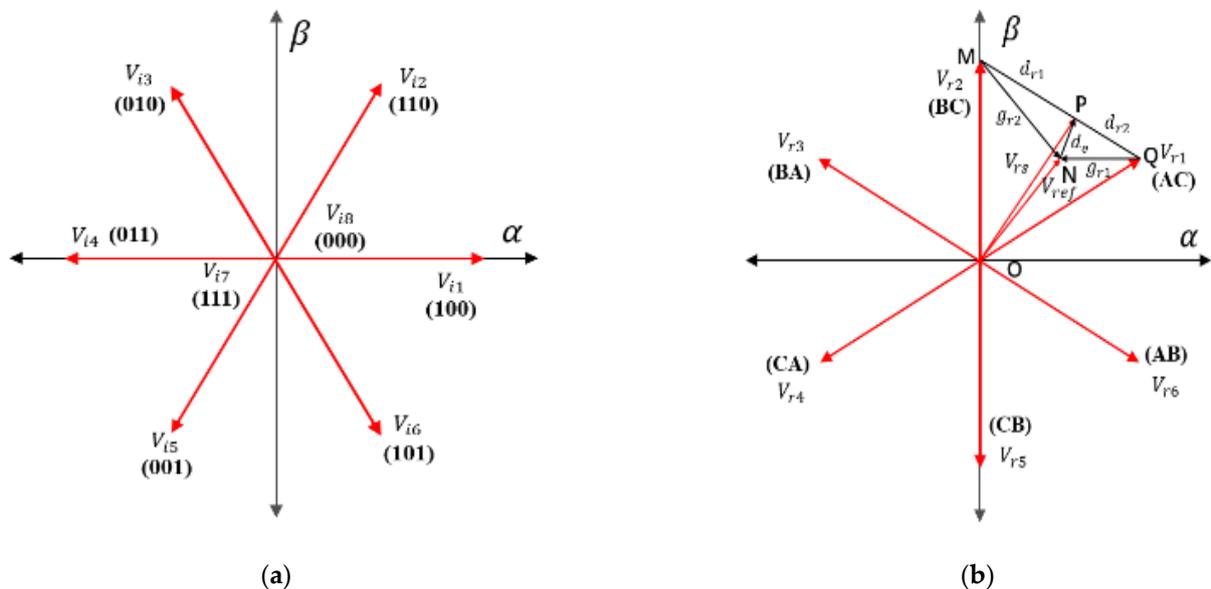


Figure 3. Space vectors of the TSMC [10]: (a) Voltage space vectors for the inverter. (b) Current space vectors for the rectifier.

It should be noticed that the sampling frequency is much higher than the fundamental frequency, and thus, the control objective error e_i can be approximated by using a time-weighted value $d_{ij}e_{ij}$ [22,23].

$$e_i = \sum_{j=0}^2 d_{ij}e_{ij} \tag{12}$$

where e_{ij} represents the error when only one vector $V_{ij}\{j \in (0,1,2)\}$ is applied for the whole sampling period T_s and d_{ij} is the duty cycle of V_{ij} .

Define e_{iRMS} as the root mean square (RMS) value of all the weighted errors, which can be calculated as

$$e_{iRMS} = \sqrt{\frac{\sum_{j=0}^2 (d_{ij}e_{ij})^2}{3}} = \bar{e}_i + e_{i\sigma}^2 \quad (13)$$

In Equation (13), \bar{e}_i represents the mean value of the weighted errors and $e_{i\sigma}$ is the variance of the weighted error as

$$\begin{cases} \bar{e}_i = \frac{1}{3} \sum_{j=0}^2 d_{ij}e_{ij} \\ e_{i\sigma}^2 = \frac{1}{3} \sum_{j=0}^2 (d_{ij}e_{ij} - \bar{e}_i)^2 \end{cases} \quad (14)$$

Considering that $d_{ij}e_{ij} \geq 0$, minimizing e_{iRMS} yields minimum values of \bar{e}_i and $e_{i\sigma}$. Thus, the duty cycles used by the proposed VMPC strategy can be obtained based on minimizing (13). That is

$$\min_{d_i} G_i = \frac{1}{3} \sum_{j=0}^2 (d_{ij}e_{ij})^2 = \frac{1}{3} \sum_{j=0}^2 g_{ij} (d_{ij})^2 \quad (15)$$

$$\sum_{j=0}^2 d_{ij} = 1, (0 \leq d_{ij} \leq 1) \quad (16)$$

Here, this optimization problem could be solved by the Lagrange multipliers method. In order to find the stationary points of a function $f(x, y)$ subject to the constraint $g(x, y) = 0$, define the Lagrangian function as

$$L(x, y, \lambda) = f(x, y) + \lambda g(x, y) \quad (17)$$

Therefore, the optimization problem yields minimization of the following function:

$$f(d_{i0}, d_{i1}, d_{i2}) = \frac{1}{3}g_0d_{i0}^2 + \frac{1}{3}g_1d_{i1}^2 + \frac{1}{3}g_2d_{i2}^2 \quad (18)$$

$$g_i = (i_o^*(k+1) - i_o(k+1))^2 \quad (19)$$

where g_0, g_1, g_2 are the cost function values for three active vectors V_{i0}, V_{i1}, V_{i2} and d_{i0}, d_{i1}, d_{i2} are the duty cycles respectively. In the Lagrange multipliers method, the constraint is

$$g(d_{i0}, d_{i1}, d_{i2}) = d_{i0} + d_{i1} + d_{i2} - 1 \quad (20)$$

Substituting (18) and (20) into (17), the Lagrangian function yields

$$L(d_{i0}, d_{i1}, d_{i2}, \lambda) = \frac{1}{3}g_0d_{i0}^2 + \frac{1}{3}g_1d_{i1}^2 + \frac{1}{3}g_2d_{i2}^2 + \lambda(d_{i0} + d_{i1} + d_{i2} - 1) \quad (21)$$

The gradient of $L(d_{i0}, d_{i1}, d_{i2}, \lambda)$ can be calculated as

$$\nabla_{d_{i0}, d_{i1}, d_{i2}, \lambda} L(d_{i0}, d_{i1}, d_{i2}, \lambda) = \left(\frac{\partial L}{\partial d_{i0}}, \frac{\partial L}{\partial d_{i1}}, \frac{\partial L}{\partial d_{i2}}, \frac{\partial L}{\partial \lambda} \right) \quad (22)$$

Substituting (21) into (22) yields

$$\nabla_{d_{i0}, d_{i1}, d_{i2}, \lambda} L(d_{i0}, d_{i1}, d_{i2}, \lambda) = \left(\frac{2}{3}g_0d_{i0} + \lambda, \frac{2}{3}g_1d_{i1} + \lambda, \frac{2}{3}g_2d_{i2} + \lambda, d_{i0} + d_{i1} + d_{i2} - 1 \right) \quad (23)$$

Considering the minimization condition

$$\nabla_{d_{i0}, d_{i1}, d_{i2}, \lambda} L(d_{i0}, d_{i1}, d_{i2}, \lambda) = 0 \quad (24)$$

Using (23) and (24), the duty cycles can be calculated as

$$\begin{cases} d_{i0} = \frac{g_1 g_2}{g_0 g_1 + g_0 g_2 + g_1 g_2} \\ d_{i1} = \frac{g_0 g_2}{g_0 g_1 + g_0 g_2 + g_1 g_2} \\ d_{i2} = \frac{g_0 g_1}{g_0 g_1 + g_0 g_2 + g_1 g_2} \end{cases} \quad (25)$$

$$\lambda = -\frac{2}{3} \frac{g_0 g_1 g_2}{g_0 g_1 + g_0 g_2 + g_1 g_2} \quad (26)$$

Thus, the synthesized vector V_{is} and the total cost function g_i can be obtained as follows:

$$g_i = d_{i0} g_{i0} + d_{i1} g_{i1} + d_{i2} g_{i2} \quad (27)$$

$$V_{is} = d_{i0} V_{i0} + d_{i1} V_{i1} + d_{i2} V_{i2} \quad (28)$$

Similarly, for the rectifier stage, there are six active current space vectors, as shown in Figure 3b, associated with switching states in Table 1. The proposed VMMPC scheme employs two valid adjacent vectors V_{r1} , V_{r2} and assesses two respective cost functions g_{r1} , g_{r2} . The duty cycles d_{r1} , d_{r2} can be obtained as:

$$\begin{cases} d_{r1} = g_{r2} / (g_{r1} + g_{r2}) \\ d_{r2} = g_{r1} / (g_{r1} + g_{r2}) \\ d_{r1} + d_{r2} = 1 \end{cases} \quad (29)$$

$$g_r = (q_s^* - q_s(k+1))^2 \quad (30)$$

With d_{r1} , d_{r2} , the total cost function g_r and the synthesized vector V_{rs} can be evaluated at every sampling period as:

$$g_r = d_{r1} g_{r1} + d_{r2} g_{r2} \quad (31)$$

$$V_{rs} = d_{r1} V_{r1} + d_{r2} V_{r2} \quad (32)$$

3.3. Comparison between the Proposed VMMPC and the CMPC

From Figure 3b, it is obvious that the length of the segment NQ is g_{r1} , which is defined as the error when only the vector V_{r1} is applied, and the length of the segment MN is g_{r2} , which is defined as the error when only the vector V_{r2} is applied respectively.

From Equations (29) and (32)–(34), it can be obtained that:

$$V_{rs} = V_{r2} + d_{r1}(V_{r1} - V_{r2}) \quad (33)$$

$$V_{rs} = V_{r1} + d_{r2}(V_{r2} - V_{r1}) \quad (34)$$

From Equations (33) and (34), obviously that the end-point of the synthesized vector V_{rs} (tagged as P) should be located on the segment MQ, and the length of the segment MQ is d_{MQ} . Besides, the length of the segment MP is $d_{r1} d_{MQ}$, and the length of the segment MP is $d_{r2} d_{MQ}$, respectively.

Considering Equations (29), (33), and (34) and the law of sines, (35) can be obtained:

$$\frac{\sin(\angle MNP)}{\sin(\angle MPN)} = \frac{d_{r1} d_{MQ}}{g_{r2}} = \frac{d_{r2} d_{MQ}}{g_{r1}} = \frac{\sin(\angle PNQ)}{\sin(\angle NPQ)} \quad (35)$$

Moreover, since $\angle MPN + \angle NPQ = \pi$, thus $\sin(\angle MPN) = \sin(\angle NPQ)$, (36) can be obtained as:

$$\sin(\angle MNP) = \sin(\angle PNQ) \quad (36)$$

In this scenario, two conditions are always fulfilled:

1. $\angle MNP + \angle PNQ = \pi$; This means that the endpoints P and Q are the same points and the error d_e between the synthesized vector V_{rs} and the reference vector V_{ref} (equal to the length of the segment PN) is equal to zero;
2. $\angle MNP = \angle PNQ$. In fact, since:

$$\begin{cases} \angle NOP < \angle OQM = \pi/3 \\ \angle NPQ = \angle MNP + \angle NMP > \angle PNQ \\ \angle PNQ + \angle NPQ = \pi - \angle NQP > 2\pi/3 \end{cases} \quad (37)$$

It can be inferred that $\angle NPQ > \pi/3 > \angle NQP$. Considering the law of sine, $d_e < g_{r1}$ is obtained. Similarly, $d_e < g_{r2}$ is deduced. Both these two conditions can prove the advantages of the VMMPC strategy when compared with CMPC in which only one switching state is selected and applied for the whole sampling instant.

3.4. Zero-Current Switching Sequence

Since no dc-link capacitors are used in the TSMC topology, the rectifier stage connects the inverter stage directly. In this paper, a zero-current switching sequence is proposed, in which the switching sequences of the rectifier and the inverter are strictly coupled. The OSS proposed is shown in Figure 4.

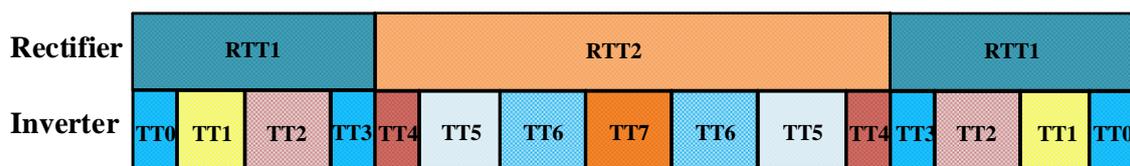


Figure 4. Zero-current switching sequence.

The duty cycles $TT0 \sim TT7$ for the inverter are calculated as:

$$\begin{cases} TT0 = TT3 = \frac{d_{i0}d_{r1}}{4} \\ TT1 = \frac{d_{i1}d_{r1}}{2} \\ TT2 = \frac{d_{i2}d_{r1}}{2} \\ TT4 = \frac{d_{i0}d_{r2}}{4} \\ TT5 = \frac{d_{i2}d_{r2}}{2} \\ TT6 = \frac{d_{i1}d_{r2}}{2} \\ TT7 = \frac{d_{i0}d_{r2}}{2} \end{cases} \quad (38)$$

Moreover, the duty cycles $RTT1 \sim RTT2$ for the rectifier stage are

$$\begin{cases} RTT1 = TT0 + TT1 + TT2 + TT3 \\ RTT2 = 2(TT4 + TT5 + TT6) + TT7 \end{cases} \quad (39)$$

From Equations (38) and (39), it is obvious that the rectifier state commutation always occurs, when zero voltage vector is implemented for the inverter and $i_{dc} = 0$. In such a way, zero-current switching operations and reduction of the switching losses of the TSMC are achieved, simplifying the commutation strategy of the TSMC.

3.5. Input Filter Resonance Suppression

As mentioned before, the input filter resonance is easier to be inspired by the model predictive control. The OSS is proposed as shown in Figure 5.

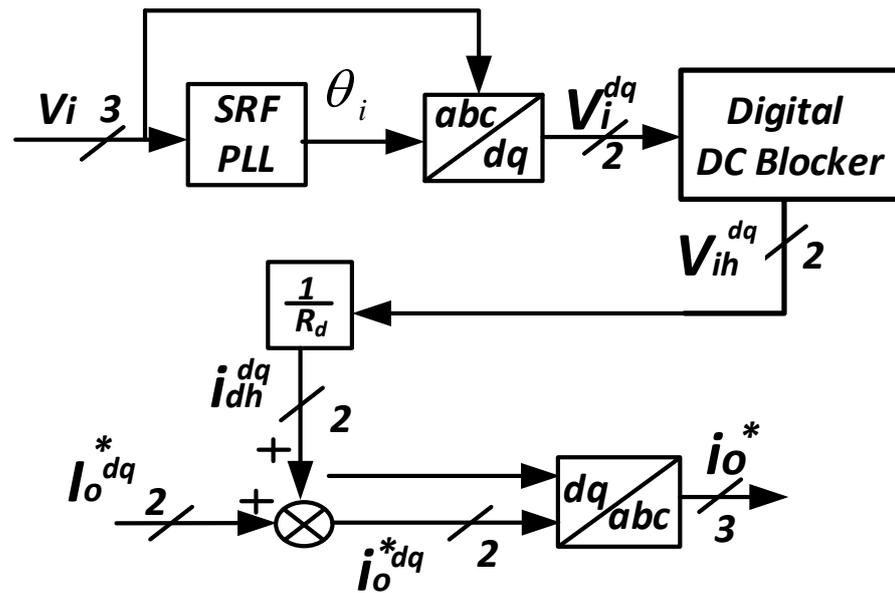


Figure 5. Input filter resonance suppression.

Initially, the scheme considers V_i in a dq reference frame based on the abc/dq transformation, which is realized by the synchronous-reference frame phase-locked loop (SRF-PLL). Then, the harmonic components V_{ih}^{dq} in the dq reference frame can be obtained by passing through a digital DC-blocker filter, which blocks the fundamental component of the voltage. Finally, the damping harmonic currents i_{ih}^{dq} can be calculated as:

$$\begin{bmatrix} i_{dh}^d \\ i_{dh}^q \end{bmatrix} = \frac{1}{R_d} \begin{bmatrix} V_{ih}^d \\ V_{ih}^q \end{bmatrix} \tag{40}$$

where $V_{ih}^{dq} = [V_{ih}^d \ V_{ih}^q]^T$ denotes all the input voltage harmonic components in V_i , and $i_{ih}^{dq} = [i_{ih}^d \ i_{ih}^q]^T$ denotes the damping harmonic currents, R_d is a virtual resistive damper placed in parallel with the input filter capacitor C_f . Then, the modified output-current reference is obtained as follows:

$$\begin{bmatrix} i_o^{*d} \\ i_o^{*q} \end{bmatrix} = \begin{bmatrix} I_o^{*d} \\ I_o^{*q} \end{bmatrix} + \begin{bmatrix} i_{dh}^d \\ i_{dh}^q \end{bmatrix} \tag{41}$$

where $I_o^{*dq} = [I_o^{*d} \ I_o^{*q}]^T$ is the unchanged reference of output current in dq reference frame, and $i_o^{*dq} = [i_o^{*d} \ i_o^{*q}]^T$ is the updated output current reference in dq reference frame.

The transfer function of the input filter is

$$V_i(s) = \frac{L_f s + R_f}{L_f C_f s^2 + R_f C_f s + 1} I_i(s) \Big|_{V_s = 0} \tag{42}$$

Considering the damping current

$$I_d[k+2] \approx \frac{V_i[k+1]}{R_d} \tag{43}$$

It is clear that the damping current delay results from the dynamics of the digital dc blocker and the $(k + 1)^{\text{th}}$ variables. Then, this paper uses the following approximation:

$$I_d(s) = \frac{V_i(s)}{R_d} e^{-sT_s} \quad (44)$$

Besides, a low-pass filter is defined as:

$$h_f(z) = \frac{1 - z^{-1}}{1 - az^{-1}} \quad (45)$$

By using a bilinear transformation, (45) can be rewritten as:

$$h_f(s) = \frac{2sT_s}{sT_s(1+a) + 2(1-a)} \quad (46)$$

Thus, the harmonic current can be obtained as

$$I_{dh}(z) = h_f(z)I_d(z) \quad (47)$$

and

$$I_{dh}(s) = h_f(s)I_d(s) \quad (48)$$

Hence, the idealized open-loop active damping system is approximated by using the damping current gain $1/R_d$ and the parallel filter impedance as

$$\begin{aligned} L(s) &= \left. \frac{I_{dh}(s)}{I_i(s)} \right|_{V_s = 0} \\ &= \frac{L_f s + R_f}{L_f C_f s^2 + R_f C_f s + 1} \cdot \frac{e^{-sT_s}}{R_d} \cdot \frac{2sT_s}{sT_s(1+a) + 2(1-a)} \end{aligned} \quad (49)$$

where T_s is the sampling time, L_f and C_f are the input filter inductance and capacitance, R_f is the resistance of L_f . The parameter "a" in Equations (46) and (49) is set to 0.99999, which is the parameter of the digital DC blocker, R_d is the active damping resistor. From (49), based on the phase and gain margins of the open-loop gain, the minimum damping resistance for the approximated system stability can be determined. The idealized system becomes unstable when an active damping resistance is under 25Ω . In practical applications, a much larger resistance than the minimum necessary for the approximated system stability is used. Considering reasonable phase and gain margins, and the suppression of the load current distortions, the recommended resistance value of the active damping resistor is between 25 and 83Ω .

4. Simulation Results

In order to validate the performance of the proposed method, simulation results in Matlab/Simulink have been carried out and the parameters of the simulation model are shown in Table 3.

Table 3. System parameters.

V_s	AC-voltage amplitude	141 V
L_f	Input filter inductor	3 mH
R_f	Input filter resistor	0.5 Ω
C_f	Input filter capacitor	37 μF
L_L	Load inductor	10 mH
R_L	Load resistor	10 Ω
T_s	Sampling time	100 μs
f_s	Sampling frequency	10 kHz

The input filter resonance can be excited by the utility (series resonance) due to the potential fifth and seventh harmonics in the ac source (seen in Figure 6a), and also by the converter itself (parallel resonance seen in Figure 6b). The highly distorted line-side currents are also reflected in the load side because of the direct topology of the TSMC (seen in Figure 1). Normally, the filter resonant frequency should satisfy both one decade above the input supply frequency f_w and one decade below the switching frequency f_s to minimize the effect of the resonance introduced by the filter [31]. That is

$$10f_w < f_{res} = \frac{1}{2\pi\sqrt{LC}} < 10f_s \quad (50)$$

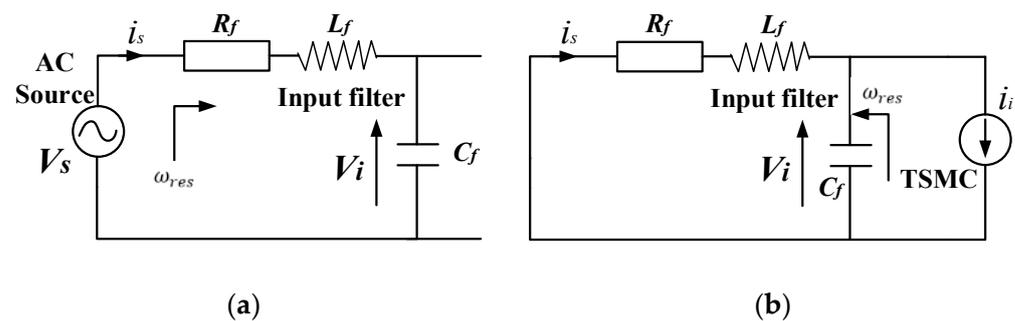


Figure 6. Possible input filter resonances. (a) Series resonance. (b) Parallel resonances.

In this paper, the resonant frequency is designed and situated nearly at the seventh harmonic of the source system to excite the resonant situation, in which the TSMC system performance can be compared with the IFRS and without the IFRS.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \approx 7(\text{pu}) \quad (51)$$

The source voltage and current, and the source-current reference of the input phase A are demonstrated in Figure 7a, and the output current and its reference of the output phase a are shown in Figure 7b. As can be seen from Figure 7, the IFRS is added at $t = 0.06$ s. Before that, the source current is highly distorted because of the resonance of the input filter. In contrast, the source current is greatly improved with an almost sinusoidal waveform after $t = 0.06$ s, achieving a very good tracking to its reference. At the same time, an almost sinusoidal waveform of the output current is obtained in Figure 7b, approaching its reference. Figure 8 shows the results of another simulation group, where the output-current frequency reference is set to 25 Hz and the other control parameters remain the same. As shown in Figures 7 and 8, the IFRS can greatly improve the quality of source current in spite of frequency variations. Besides, the source current is in phase with the source voltage, indicating that the source reactive power is minimized based on Equations (10) and (30).

To assess the dynamic performance of the proposed strategy for the TSMC with the IFRS, two groups of simulation results are shown in Figures 9 and 10, considering the conditions with the IFRS and without the IFRS. In Figure 9, the output-current frequency steps from 25 Hz to 50 Hz at $t = 0.06$ s, and the other control parameters remain the same. In Figure 10, the output-current reference amplitude steps from 4.3 A to 2.15 A at $t = 0.06$ s, and the other control parameters remain the same. As illustrated in Figures 9 and 10, the system resumes quickly after minute oscillations in a short time, when the output-current frequency or the output-current reference amplitude steps at $t = 0.06$ s. At the same time, almost sinusoidal waveforms of the source current and output current can be reached with a very good tracking to their references with the IFRS, and the source current is always in phase with the source voltage with the source reactive power minimization in both cases of output-current reference and output-current frequency changes. As expected, the control scheme presents a fast dynamic response on both the input and output sides.

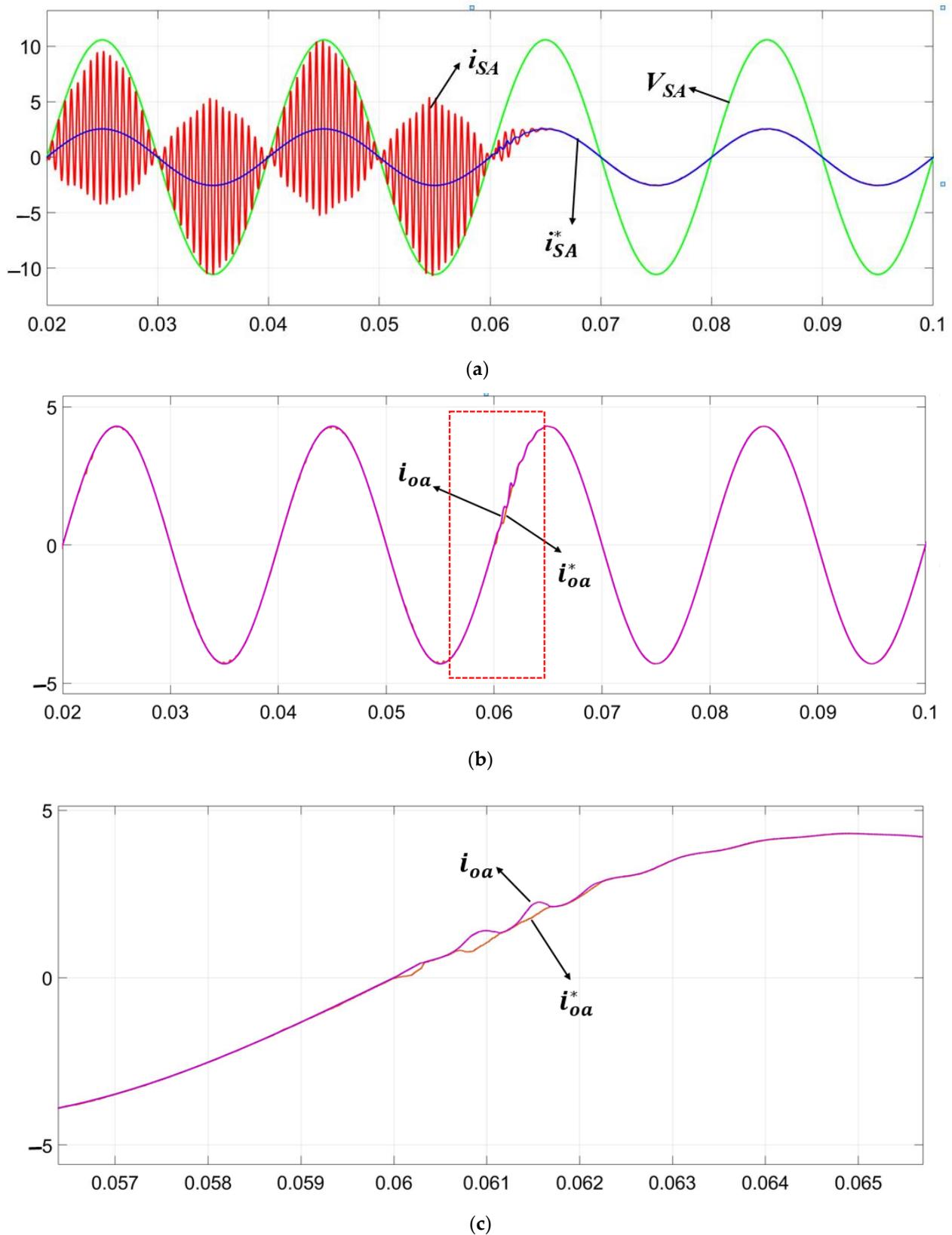
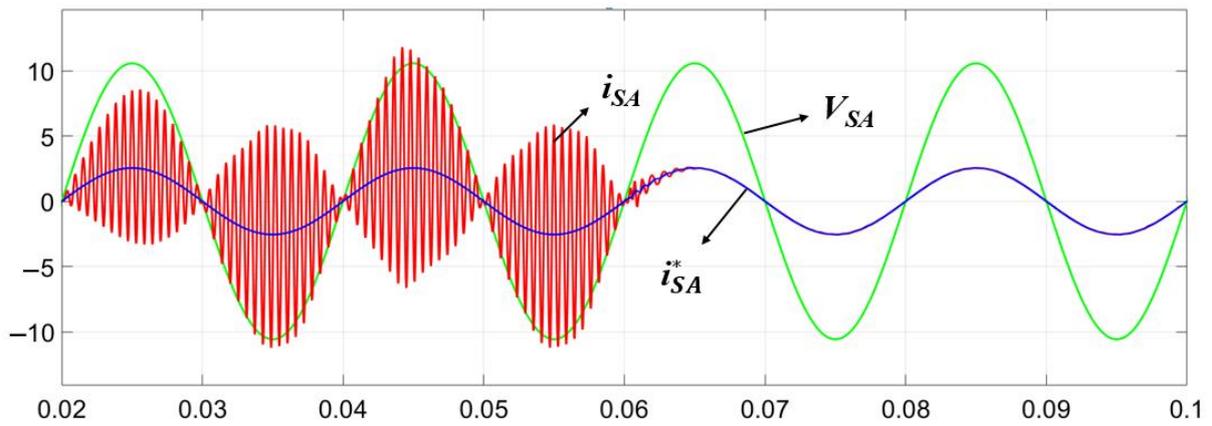
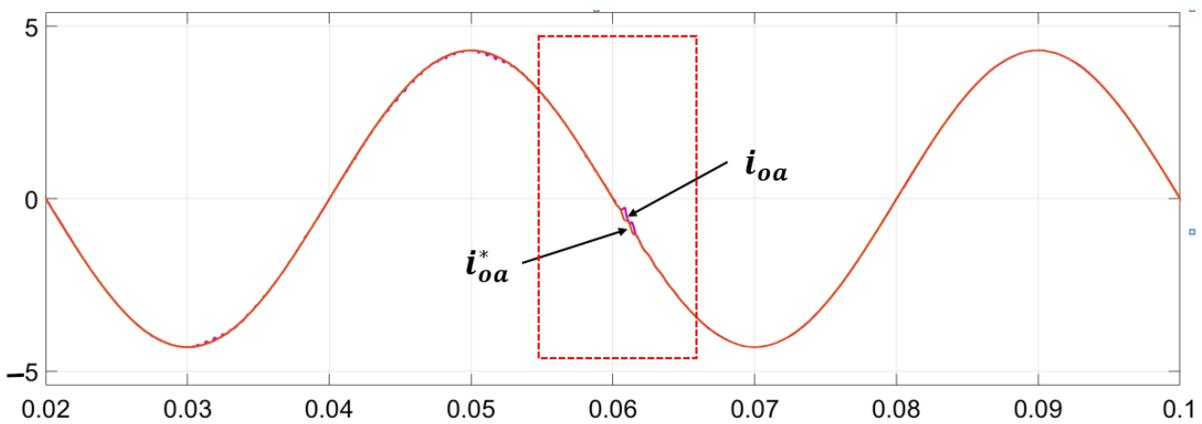


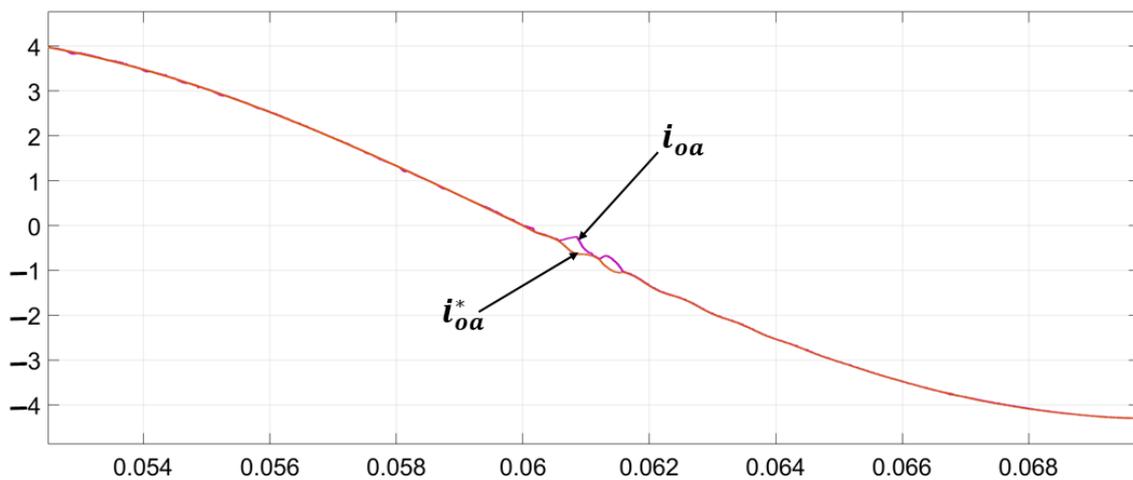
Figure 7. Simulation results of the VMMP for the TSMC, and output-current frequency reference is set to 50 Hz: The IFRS is added at $t = 0.06$ s, x-axis unit second: (a) source voltage $V_{sA}/13$ V, source current i_{sA} A and source-current reference i_{sA}^* A; (b) output current i_{oa} A and output-current reference i_{oa}^* A; (c) details of the box in Figure 7b.



(a)



(b)



(c)

Figure 8. Simulation results of the VMPC for the TSMC, and output-current frequency reference is set to 25 Hz: The IFRS is added at $t = 0.06$ s, x axis unit second: (a) source voltage $V_{sA}/13$ V, source current i_{sA} A and source-current reference i_{sA}^* A; (b) output current i_{oa} A and output-current reference i_{oa}^* A; (c) details of the box in Figure 8b.

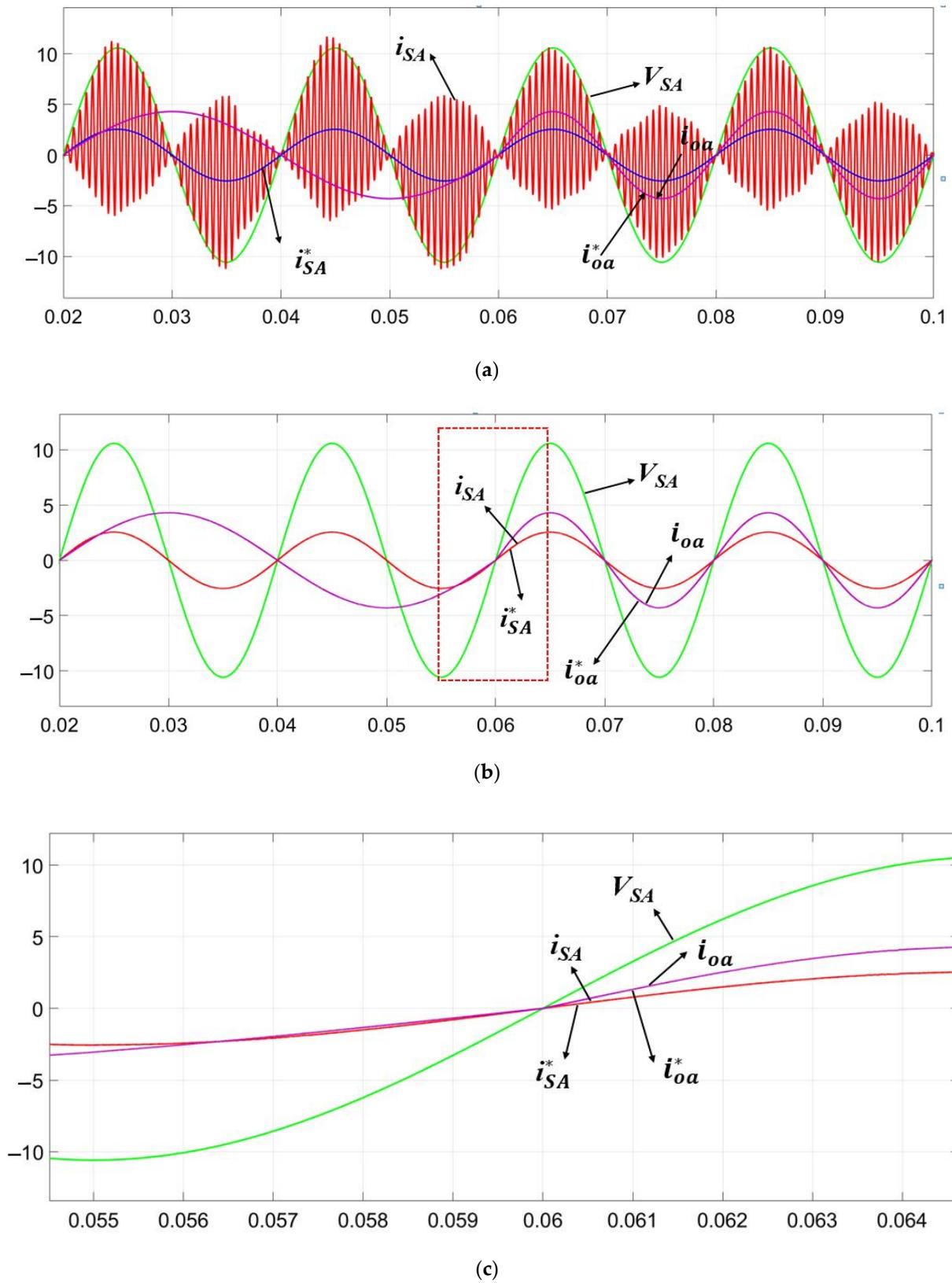


Figure 9. Simulation results of the VMPC for the TSMC, where output-current frequency reference steps from 25 Hz to 50 Hz at $t = 0.06$ s, source voltage $V_{sA} / 13$ V, source-current reference i_{sA}^* A, source current i_{sA} A, output current i_{oa} A, and output-current reference i_{oa}^* A, x-axis unit second: (a) without the IFRS; (b) with the IFRS; (c) details of the box in Figure 9b.

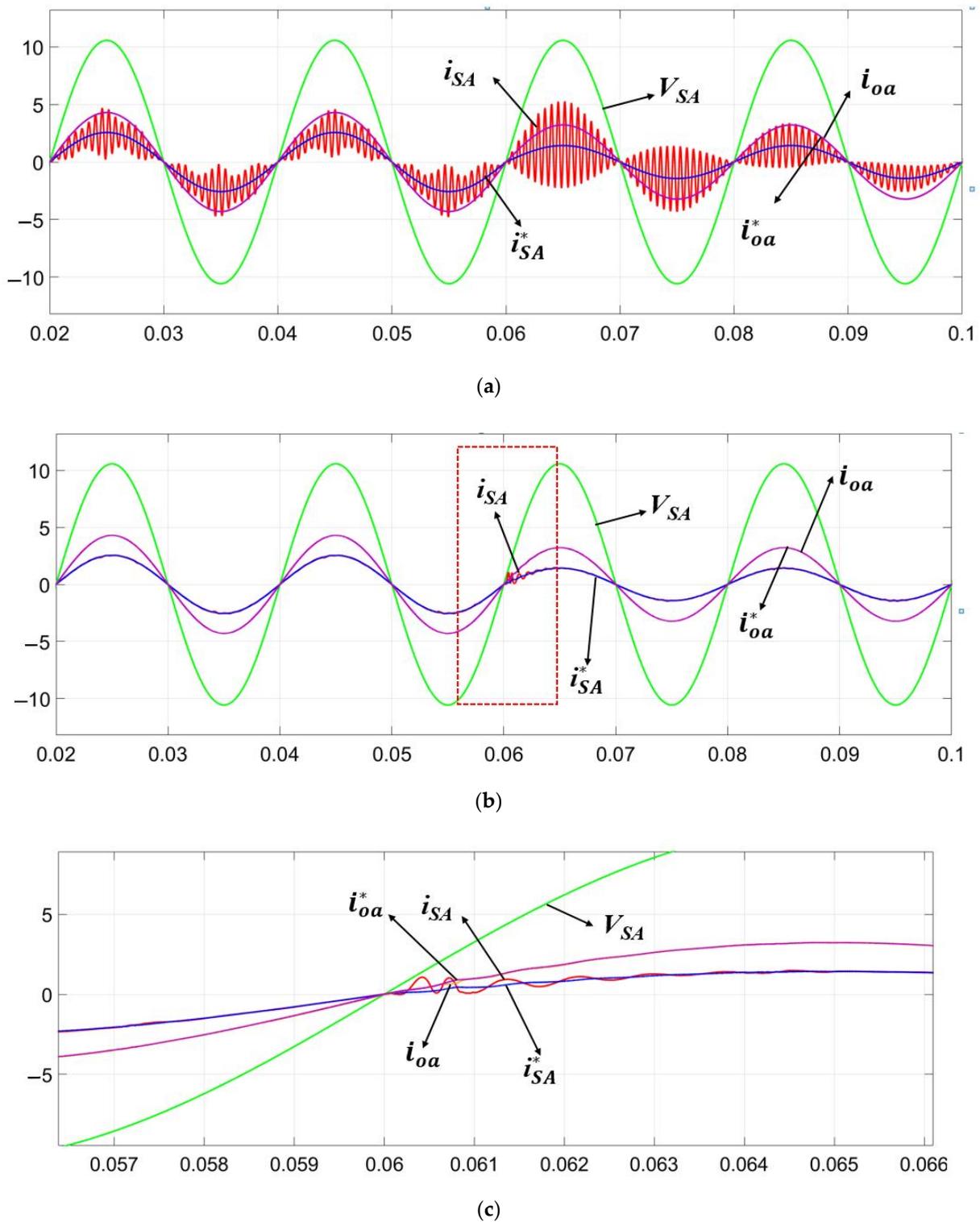


Figure 10. Simulation results of the VMMP for the TSMC, where output-current reference amplitude steps from 4.3 A to 2.15 A at $t = 0.06$ s, source voltage $V_{sA}/13$ V, source-current reference i_{sA}^* A, source current i_{sA} A, output current i_{oa} A, and output-current reference i_{oa}^* A, x-axis unit second: (a) without the IFRS; (b) with the IFRS; (c) details of the box in Figure 10b.

5. Experimental Results

A laboratory TSMC prototype designed and built by the University of Nottingham for experimental evaluation. The prototype is shown in Figure 11 and the relevant experimental parameters are shown in Table 3. The scheme is implemented in a spectrum digital control board integrating a Texas Instruments C6713 DSP and a ProASIC3 FPGA. Compared to the OSMC, the TSMC presents zero current switching for the rectifier and thus, can simplify the commutation of the bidirectional switches in the rectifier. While the inverter stage has no particular commutation schemes with hard switching operations. Owing to this, unlike the OSMC, where all 18 switches have to be realized using Silicon Carbide (SiC) MOSFETs, this experiment used 12 standard insulated gate bipolar transistors (IGBT, IKW15T120) for the rectifier and 6 SiC MOSFETs (C2M0080120D) for the inverter, considering the high switching frequencies and the switching losses. Besides, a radiator is used to dissipate the heat produced by the high-frequency switches. In addition to the input filter, an EMI filter capacitor is connected to the output of the AC source. More details about the EMI filter can be found in [32].



Figure 11. Laboratory TSMC system prototype for evaluation of the proposed control strategy.

Firstly, the conventional model predictive control strategy for the TSMC without the IFRS and the OSS is implemented, and the results are shown in Figure 12. From Figure 12a, the source current is highly distorted with a THD of 92.42%. As seen in Figure 12b, the main distortions are situated around the input filter resonance frequency calculated based on Equation (51). In addition, the waveforms of the source voltage and the output current are also affected by the large oscillations of i_s , due to the direct topology of the TSMC. From Figure 12, it is clear that the input filter resonance is necessary to be suppressed to improve the power-quality performance of the TSMC system.

Secondly, the IFRS is added to the CMPC for the TSMC and the results are shown in Figure 13. Compared with Figure 12, with the help of the IFRS, the quality of the source current is largely improved with the THD of 11.49%, and the THD of the output current is also improved from 10.23% to 8.25% respectively. From Figure 13b, the distortions around the input filter resonance frequency are significantly suppressed, the maximum amplitude is under 4%, while the maximum amplitude is over 60% without the IFRS in Figure 12b. Besides, the variable switching frequency and a broad harmonic spectrum phenomenon can be easily observed in Figure 13b,c. The source current is not always in phase with the source voltage in Figure 13a, which indicates that the minimization of the instantaneous source reactive power based on Equations (10) and (30) needs to be improved.

Thirdly, the proposed VMMPCC strategy with the IFRS and the OSS for the TSMC is evaluated, and the results are shown in Figure 14. Compared with Figure 13, the source current i_{sA} is improved with a THD from 11.49% to 7.35%. From Figure 14b, the distortions around the input filter resonance frequency are suppressed, the maximum amplitude is near 2% with the proposed VMMPCC strategy, while the maximum amplitude is 4% with the CMPC. The THD of the output current is also improved from 8.25% to 6.08% respectively.

Besides, from Figure 14b,c, it is clear that the harmonics are concentrated around the fundamental frequency and its multiples frequency, the fixed switching frequency phenomenon can be easily observed. The source current is always in phase with the source voltage in Figure 14a, which indicates the minimization of the instantaneous source reactive power based on Equations (10) and (30) is also improved compared with Figure 13a.

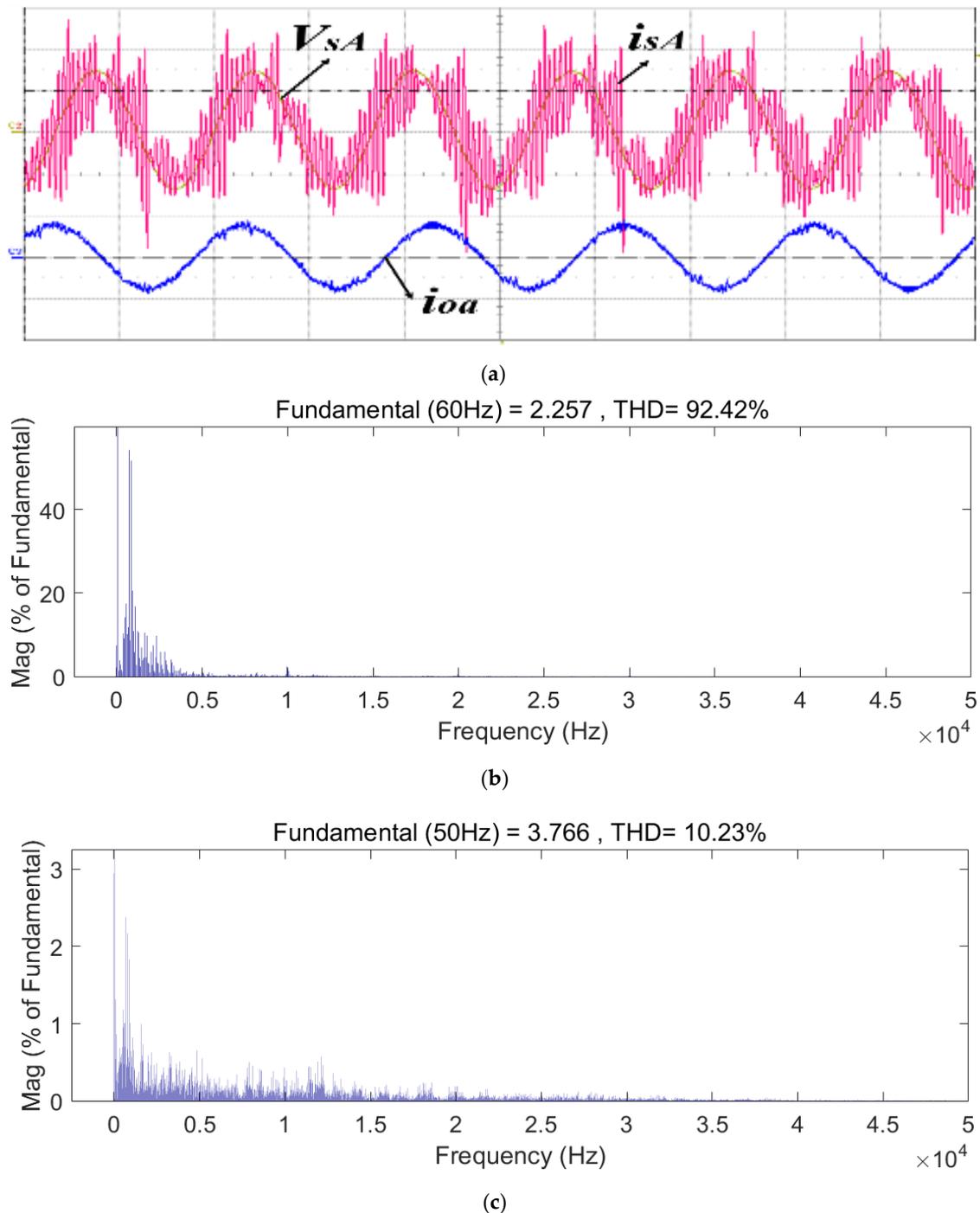


Figure 12. Experimental results of the CMPC strategy without the IFRS for the TSMC, where output-current reference amplitude is set to 4.3 A and output-current frequency is set to 50 Hz: (a) Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (5 A/div) and output current i_{oa} (5 A/div). (b) Spectrum distribution of i_{sA} . (c) Spectrum distribution of i_{oa} .

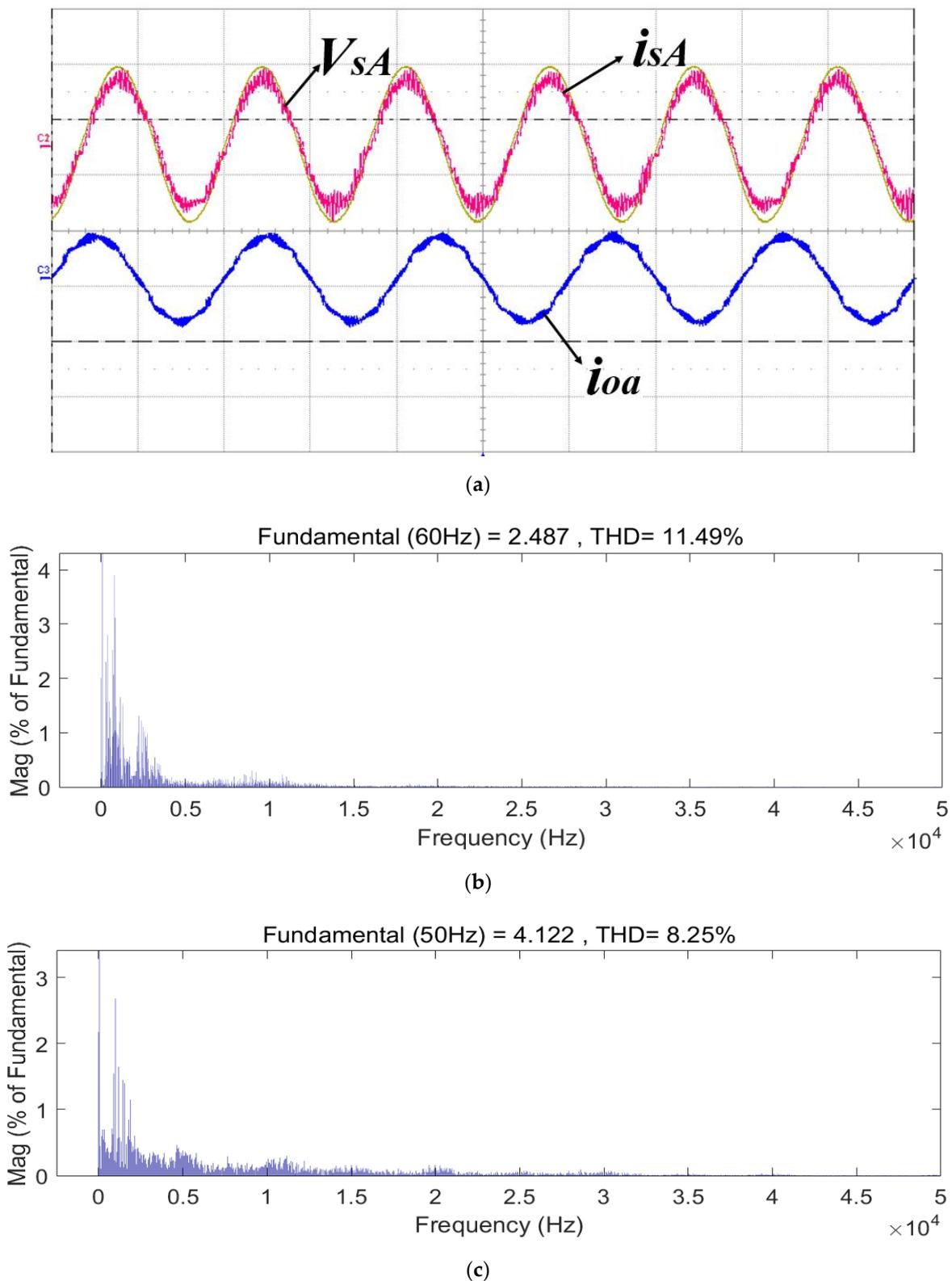
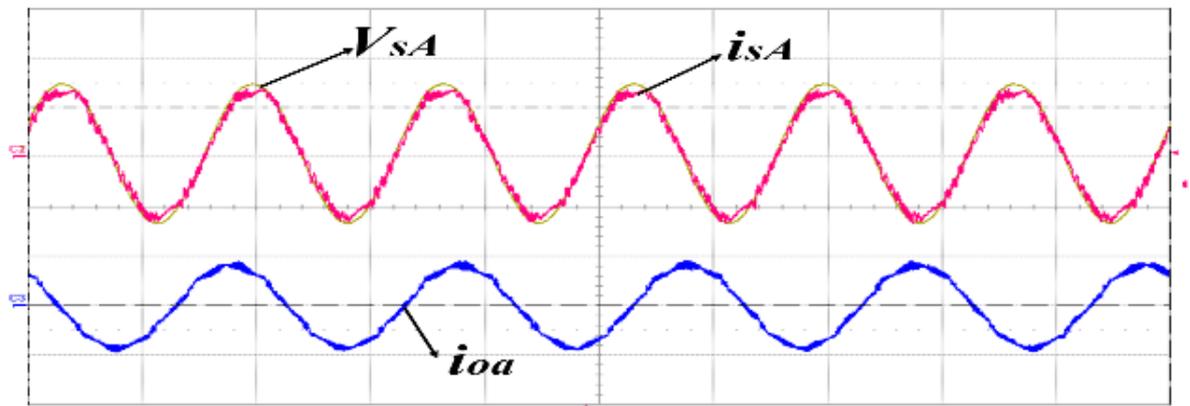
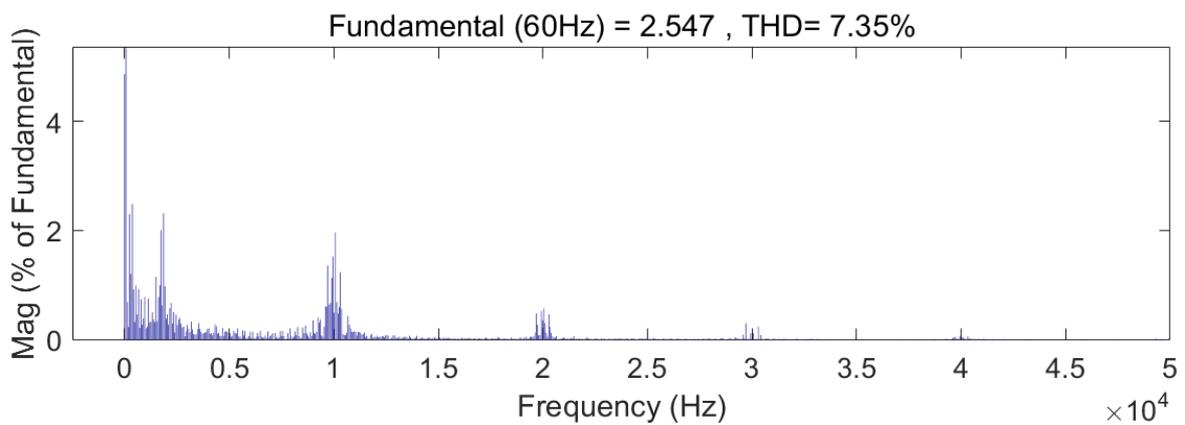


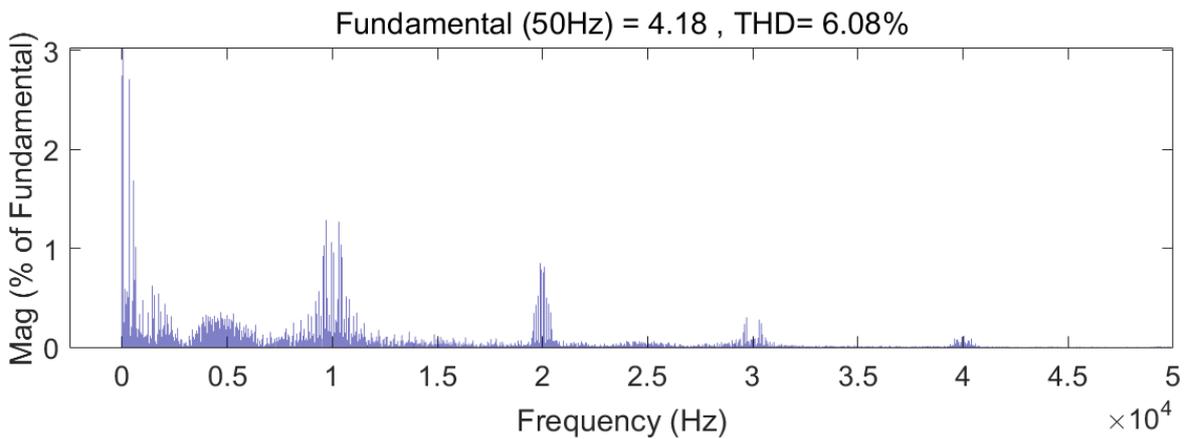
Figure 13. Experimental results of the CMPC strategy with the IFRS for the TSMC, where output-current reference amplitude is set to 4.3 A and output-current frequency is set to 50 Hz, x-axis 10 ms/div (a) Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (2 A/div) and output current i_{oa} (5 A/div). (b) Spectrum distribution of i_{sA} . (c) Spectrum distribution of i_{oa} .



(a)



(b)



(c)

Figure 14. Experimental results of the proposed VMPC strategy with the IFRS for the TSMC, where output-current reference amplitude is set to 4.3 A and output-current frequency is set to 50 Hz, x-axis 10 ms/div (a) Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (2 A/div) and output current i_{oa} (5 A/div). (b) Spectrum distribution of i_{sA} . (c) Spectrum distribution of i_{oa} .

In addition, since the proposed control strategy controls the instantaneous source reactive power on the input side, the parameter named as the mean power M_p is defined to assess the performance:

$$M_p = \frac{1}{m} \sum_{k=1}^m |p(k)| \quad (52)$$

where $p(k)$ is the actual value of power at the k^{th} sampling instant and m is set to 10,000.

The comparisons between the CMPC and the proposed VMMPC with the OSS are shown in Table 4.

Table 4. The assessment parameters of experimental results.

	M_{q_s} (Var)	THD of i_s	THD of i_a
CMPC	8.21	11.49%	8.25%
VMMPC	3.59	7.35%	6.08%

From Table 4, the proposed VMMPC with the OSS can obtain better performance in all aspects of the instantaneous source reactive power, the source current, and the output current, compared with the CMPC.

It should be stated that the CMPC may obtain a similar performance with the VMMPC in aspects of control objectives, by using a much higher sampling frequency than that in the VMMPC [18,22]. However, since predictive controllers are commonly demanding in terms of computational resources, it is not always possible to increase the sampling frequency in practical implementations. Besides, the variable switching frequency with the CMPC is a lurking peril for the control system [18].

Besides, the amplitude of the output current is 4.18 A, thus there exists a 2.8% steady-state error, because the reference of the output current is set to 4.3 A. In fact, a steady-state error between the measured current and its reference is normal in model-based control strategies, where a steady-state error on the controlled variables usually occurs from the system model inaccuracies. This can be usually compensated by external control loops (e.g., PI controller-based). Besides, in [33], a method aiming to improve the system parameter robustness with the CMPC has been proposed, which can also mitigate this problem.

Furthermore, the waveforms of the dc-link voltage u_{dc} and current i_{dc} with the CMPC and the VMMPC with the OSS are shown in Figure 15. The commutation of u_{dc} represents the switching state change of the rectifier stage. From Figure 15a, it is possible to change the switching state of the rectifier stage when i_{dc} is nonzero (blue line). This may increase the converter switching losses and require a more complex commutation strategy (e.g., four-step commutation) for the rectifier stage. On the contrary, in Figure 15b with the proposed control strategy, the commutation of u_{dc} always occurs when i_{dc} is zero (blue line), which guarantees the zero-current switching of the rectifier stage.

Finally, transient results are shown in Figures 16–19. The output-current frequency reference is changed between 25 Hz and 50 Hz in Figures 16 and 17, and its amplitude reference is changed between 2.15 A and 4.3 A in Figures 18 and 19. As indicated in Figures 16–19, almost sinusoidal waveforms of the source current and the output current are obtained, and the output current shows a good tracking to the reference. Besides, the source current is in phase with the source voltage, achieving the minimization of the instantaneous source reactive power, and the source and output currents show fast dynamic responses to the variations of the references. As expected, the proposed strategy demonstrates a fast dynamic response and a good performance in the transient state.

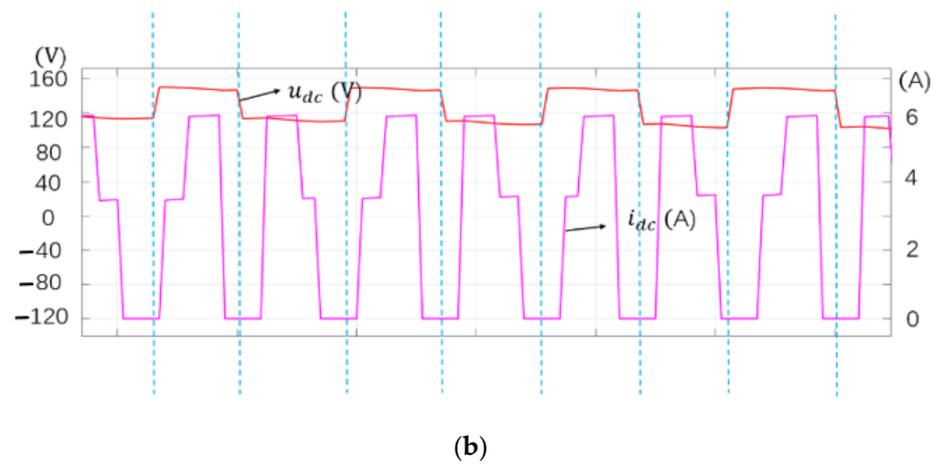
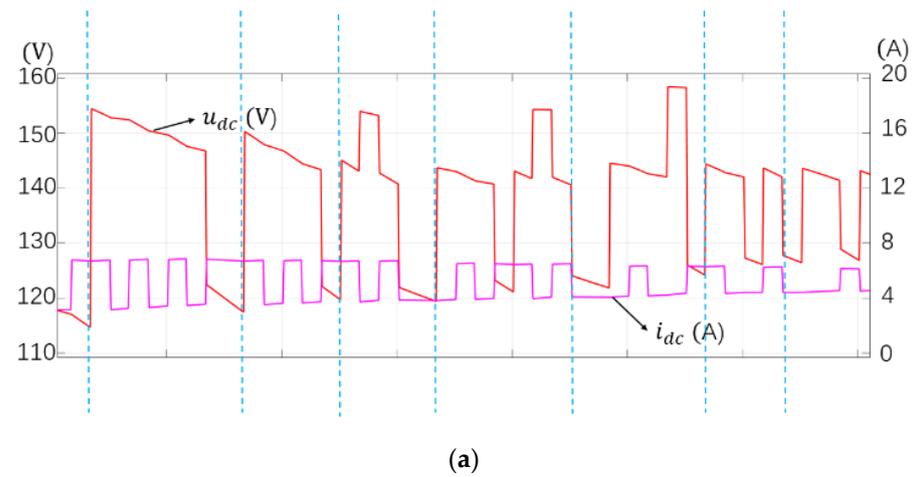


Figure 15. Waveforms of dc-link voltage u_{dc} and current i_{dc} : (a) with the CMPC; (b) with the VMMPC and the OSS.

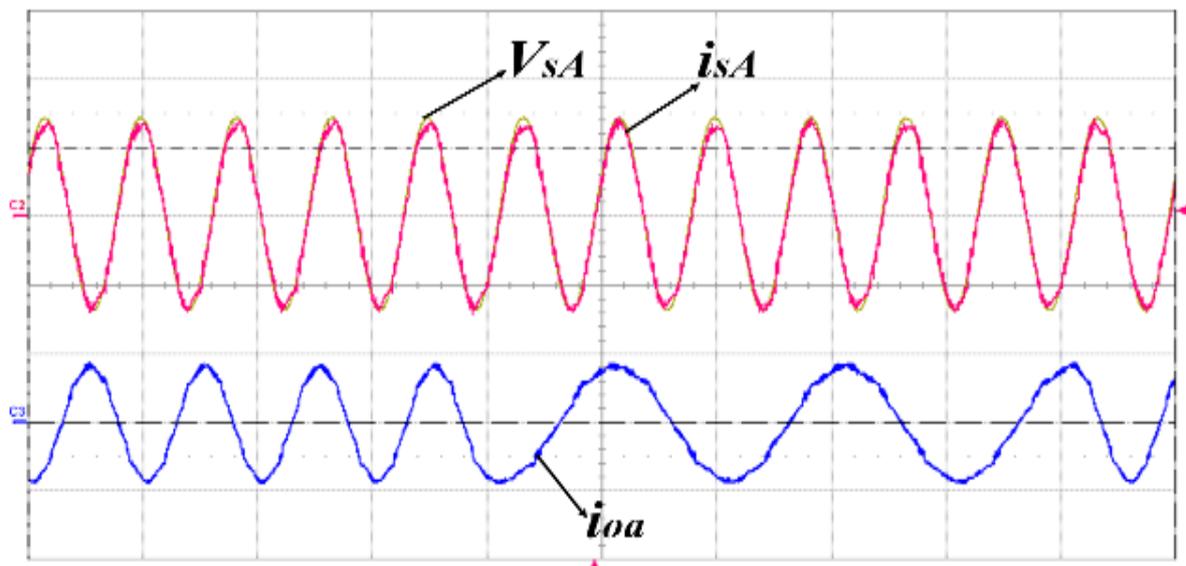


Figure 16. Experimental results of the proposed strategy with the IFRS, where output-current reference amplitude is set to 4.3 A and output-current frequency is changed from 50 Hz to 25 Hz, x-axis 20 ms/div. Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (2 A/div) and output current i_{oa} (5 A/div).

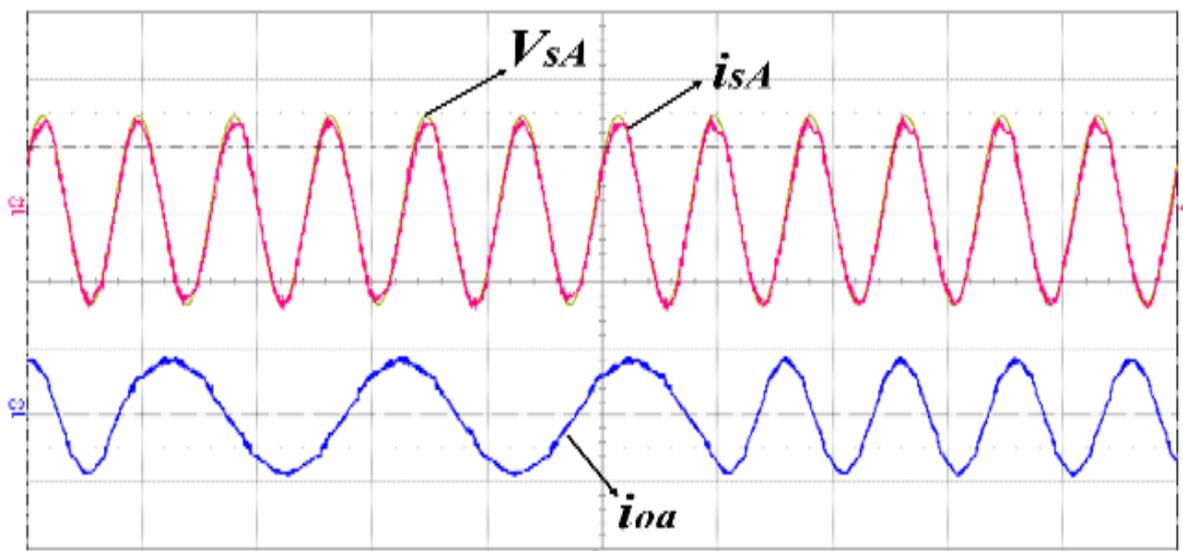


Figure 17. Experimental results of the proposed strategy with the IFRS, where output-current reference amplitude is set to 4.3 A and output-current frequency is changed from 25 Hz to 50 Hz, x-axis 20 ms/div. Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (2 A/div) and output current i_{oa} (5 A/div).

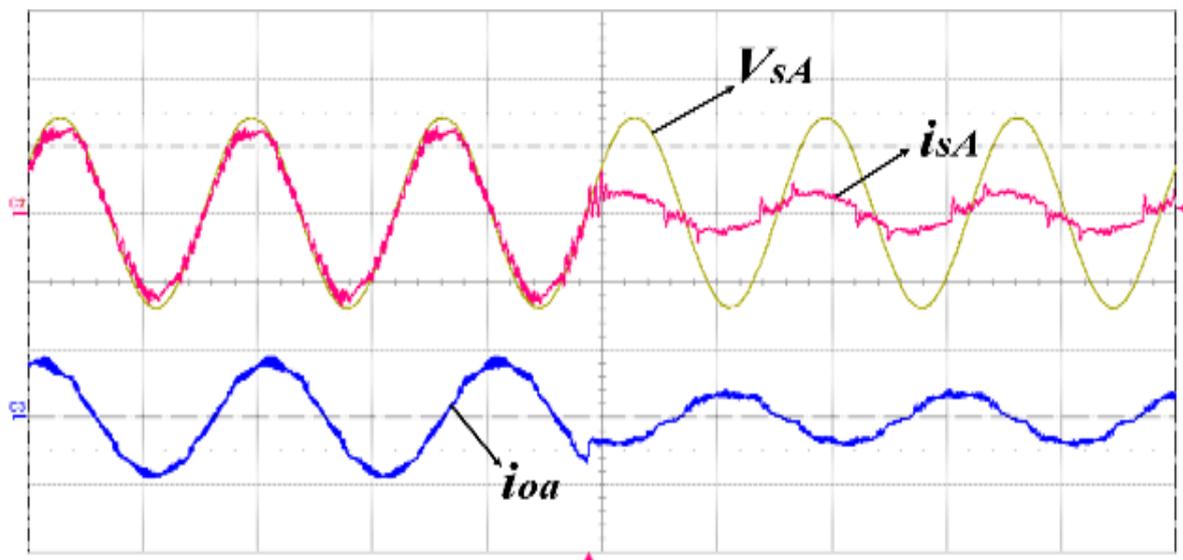


Figure 18. Experimental results of the proposed strategy with the IFRS, where output-current reference amplitude is changed from 4.3 A to 2.15 A and output-current frequency is set to 50 Hz, x-axis 10 ms/div. Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (2 A/div) and output current i_{oa} (5 A/div).

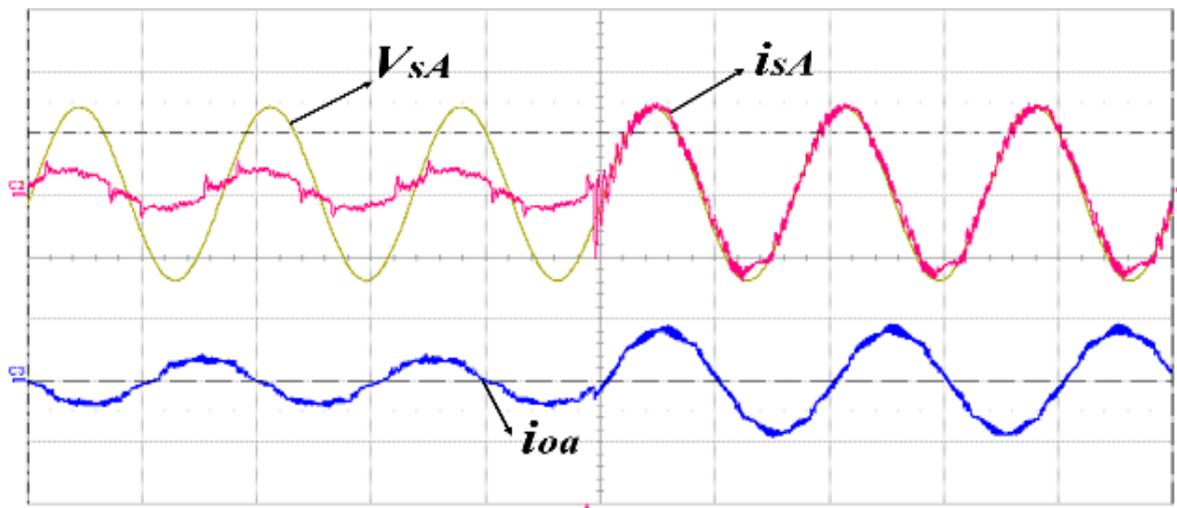


Figure 19. Experimental results of the proposed strategy with the IFRS, where output-current reference amplitude is changed from 2.15 A to 4.3 A and output-current frequency is set to 50 Hz, x-axis 10 ms/div. Waveforms of the source voltage V_{sA} (100 V/div), source current i_{sA} (2 A/div) and output current i_{oA} (5 A/div).

6. Conclusions

For matrix converters, an input filter is necessary for the commutation of switching devices and to mitigate against line-current harmonics. However, the filter configuration presents a resonance frequency and can be excited by the utility due to the potential fifth and seventh harmonics in the ac source (series resonance), and also by the converter itself (parallel resonance). Besides, the model predictive control strategy is more likely to excite the input filter resonance, when compared with traditional control methods, leading to additional harmonics in the AC source and distorted source current waveforms.

To solve these problems above, a vector modulation-based model predictive control strategy is proposed, which controls the source reactive power and the output currents with fixed switching frequency. The advantage of the proposed VMMPC strategy compared with the CMPC is firstly proven using the principle of vector synthesis and the law of sines in the vector distribution area. Besides, an optimal switching sequence is proposed, which can guarantee safe zero-current switching operations and reduce the switching losses. This pattern can simplify the commutation of TSMC and avoid complex commutation strategies (e.g., four-step commutation) in traditional control methods. Furthermore, a novel input filter resonance suppression method is proposed and implemented in the VMMPC for the TSMC, which shows good damping performance and easy implementation. In fact, the IFRS method proposed in this paper is not only suitable for the TSMC with the MPC scheme but also can be used for other power converters, i.e., current source rectifiers and inverters and other control techniques, i.e., the space vector pulse width modulation technique, where the reference amplitude of the load current or voltage can be modified.

Experimental results validate the performance of the proposed method, which features unity input displacement power factor, low source-current distortions, good sinusoidal waveforms of output currents, and zero-current switching operations, demonstrating that the proposed control technique poses an attractive alternative to classical control strategies for the TSMC.

Author Contributions: Conceptualization, methodology and validation, Z.D. and D.X.; formal analysis, investigation, resources and writing—original draft preparation, Z.D.; writing—review and editing, supervision and project administration, P.W.; funding acquisition, D.X. and L.T. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Natural Science Basic Research Plan in Shaanxi Province of China under Grant 2018JM5033 and in part by the China Scholarship Council under Grant 201606290180.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data available on request due to restrictions eg privacy or ethical The data presented in this study are available on request from the corresponding author. The data are not publicly available due to commercial sensitivity.

Acknowledgments: The authors thank the Natural Science Basic Research Plan in Shaanxi Province of China and the China Scholarship Council.

Conflicts of Interest: The authors declare no conflict of interest.

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