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A New Configuration of Three-Level ZSI Using Transistor Clamped Topology

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Abstract: In this paper, a three-level ZSI (impedance source inverter) based on transistor clamped theory is proposed. It uses the least number of switch counts and associated gate circuitry among all existing topologies of three-level ZSI without any performance degradation. The existing three-level ZSI topologies require three power switches to be turned ON for upper-lower shoot-through (ULST), and four power switches to be turned ON for full dc-link shoot-through (FST). However, with the proposed configuration, upper–lower shoot-through (ULST) and full dc-link shoot-through (FST) is inserted by turning ON only two power semiconductors. A comparison between diode clamped, transistor clamped, and t-type is presented. The proposed topology can realize any of the existing sine-triangle- or space vector-based PWM (pulse width modulation) schemes, and all existing configurations of three-level ZSI can merge into the proposed inverter configuration.

Keywords: three-level inverters; Z-source inverters; pulse width modulation; transistor clamped inverter

1. Introduction

The three most common multilevel configurations—diode clamped, capacitor clamped, and cascaded multilevel—are extensively studied in the literature. Since each of these three have their own merits and demerits, numerous branches of research areas emerged. Some of them found their applications in renewable energy, drives, and hybrid vehicles. Some other implementations are associated with control techniques like neutral point balance, reduced common-mode voltage, and topological developments, such as symmetrical/asymmetrical hybrid topologies and PWM technique developments like hybrid PWM techniques.

The main drawback of these three basic topologies is that only voltage buck operation is possible. So, to insert a voltage buck-boost feature in an existing voltage source inverter, a new class of inverters, namely Z-source inverters, is proposed in [1] with its two-level configurations. The other advantages offered by these (ZSI) inverters are: (i) no need for the time delay between the switches of the same leg, and (ii) better output voltage quality. Extensive research is present in the area of two-level ZSI, with the main focus on its topological improvements, PWM techniques, and its suitability for different applications.

However, the concept of ZSI in the area of multilevel inverters is less explored as compared to two-level ZSI- and VSI based multilevel inverters.

The first attempt to extend the ZSI concept in a three-level neutral point clamped (NPC) inverter was reported in [2], with a detailed explanation of the shoot-through addition procedure in the existing continuous and discontinuous PWM techniques. The presented circuit configuration in [2] requires two impedance networks for boosting output voltage, which increases the inverter complexity, control, and cost.

Two new three-level z source inverter topologies—NPC type and dc-link cascaded type—using a single impedance network were proposed in [3] with the alternate phase opposition disposition (APOD) PWM technique. However, output voltage quality degrades, as APOD does not use the nearest three vector switching. An attempt to use two separate dc sources and two impedance networks is reported [4]. To get a more theoretical insight of three-level ZSI, the effect of the modulation index ($M > 0.575$ and $M < 0.575$) on the shoot-through insertion and concept of reduced common-mode voltage is presented [5].

Another topological variation in the field of three-level ZSI is present in [6], named as "dual z-source inverter." It uses three single-phase transformers at its output terminal to supply the load, and offers bidirectional power flow and electrical isolation with an output transformer. A comparison between dual ZSI-based three-level and DC link cascaded type three-level ZSI is presented [7]. Advantages offered by dual ZSI—such as phase leg redundancy for equalizing switching losses among power devices, and the applicability of different PWM techniques for its control—makes it superior to the dc-link cascaded type topology. To achieve both, i.e., reduced element counts (one impedance network) and the nearest three vectors switching (PD carrier PWM), three operating modes for the adjustable drive system are presented [8]. However, for stable voltage boosting, a triple offset is required to make the duration of E-active and E-null states equal in the case of phase disposition carrier.

Loh et al. [9] presented a three-level z source converter with reduced switching commutations using carrier-based modulation techniques. Effah et al. [10] presented a three-level ZSI based on the SVPWM technique. Some other configurations are an extension of two-level ZSI into three-level are: trans and flipped trans ZSI type NPC [11], embedded Z source three-level and dc-link integrated Z source NPC inverter [12], and quasi ZSI-based three-level NPC [13]. McGrath et al. [14] achieve the same phase leg switching sequence using phase disposition and space vector modulation strategies applied to diode clamped and hybrid multilevel inverters.

The above configurations attempted to achieve better performance in terms of gain, small shoot-through for more significant boost, inrush current suppression capability, continuous input current, low total harmonic distortion of output voltage/current, and common ground for inverter and source. Nabae et al. [15] presented a neutral-point clamped inverter. Schweizer et al. [16] discussed the modified version of the neutral-point clamped T-Type inverter for low voltage application. In recent years, more works on multilevel ZSI are found in the literature based on topological and PWM technique developments. The common-mode voltage reduction, which is responsible for leakage current in the photovoltaic application, is discussed [17]. A three-level quasi –boost T-Type inverter with reduced inductor current ripple is presented in [18]. A switched-capacitor multilevel inverter with a single DC source is proposed [19]. A five-level inverter with a reduced passive component is successfully established [20]. It represented a single-stage quasi-cascaded H-bridge inverter. Roncero-Clemente et al. [21] discussed a modified carrier, level-shifted based a control method for a three-phase, three-level T-type quasi-impedance-source inverter. Here, a modulation method for a Z-source three-level T-type inverter is developed. It combines the merits of the Z-source two-level inverter and the advantages of the Z-source neutral-point-clamped inverter. Xing et al. [22], proposes an improved space vector based PWM technique to balance the neutral point potential of three-level T-type ZSI. [23] attempted to reduce the common-mode voltage by suitably placing the shoot-through states for the case of a quasi-Z-source three-level T-type inverter.

Section 2 of this paper discusses the main drawback of the diode clamped three-level VSI, and the main features of the transistor clamped VSI are presented in Section 3. The novelty of the paper is to utilize the advantages offered by the transistor clamped VSI in the field of ZSIs, which is discussed in Section 4. In transistor clamped topology, the number of switching components, and their associated gate driver requirement, is less compared to existing multilevel inverters. The ULST (upper–lower shoot-through) and FST (full shoot-through) schemes are analyzed, and the PWM technique for the insertion of shoot-through in a TC-ZSI (ransistor clamped impedance source inverter) is presented. This paper aims to achieve a three-level boosted output phase voltage employing transistor clamped

topology for the case of ZSI. Finally, simulation and experimental results are presented in Section 5. Section 6 concludes this paper.

2. Review of Existing Three-Level ZSI Configurations

The configuration of the existing three-level ZSI is shown in Figure 1, where one impedance network is used for voltage boosting [12]. One impedance network indicates two inductors and two capacitors.

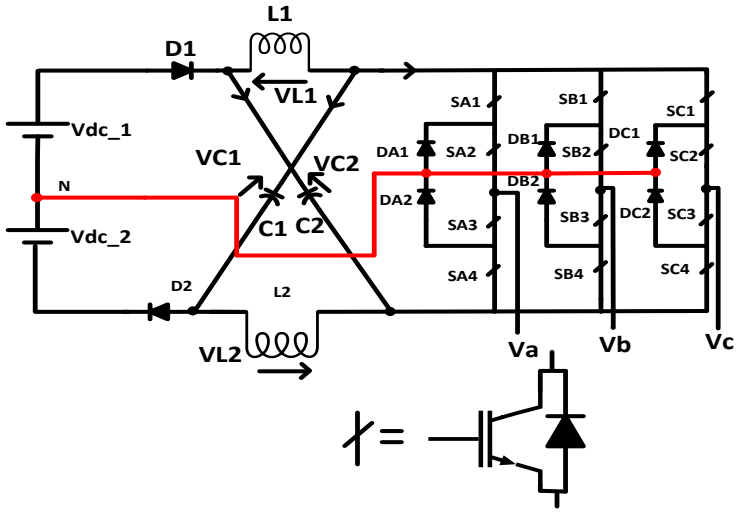

Figure 1. Existing three-level ZSI with one impedance network.

The two primary types of shoot-through techniques used for shoot-through insertion are full dc-link shoot-through (FST) and upper–lower shoot-through (ULST). The switching combinations to implement FST and ULST scheme in diode clamped configurations are as follows:

A. Full dc-link shoot-through (FST):

$$S_{x1} = S_{x2} = S_{x3} = S_{x4} = ON;\ DA1 = DA2 = OFF\ (\text{where } x = \text{A, B, C})$$

B. Upper shoot-through:

$$S_{x1} = S_{x2} = S_{x3} = ON;\ DA2 = ON,\ DA1 = OFF$$

C. Lower shoot-through:

$$S_{x2} = S_{x3} = S_{x4} = ON;\ DA1 = ON, DA2 = OFF$$

D. Non-shoot-through state:

$$S_{x1} \neq S_{x3},\ S_{x2} \neq S_{x4};\ DA1 = DA2 = ON.$$

In the FST scheme, full shoot-through states and non-shoot-through states are present, while in the ULST scheme, upper–lower shoot-through states and non-shoot-through states are present.

When upper and lower ST states use a single impedance network, the relation between M and ST duty ratio (d_{sh}) is written as:

$$d_{sh} = \frac{T_0}{\mathrm{T}} \tag{1}$$

where T_0 is the shoot-through duration in a sample period T.

With a single impedance network, d_{sh} offered by the ULST scheme is half in comparison to the FST scheme. This is written as:

$$(d_{sh})_{ULST} = \frac{1}{2}.(d_{sh})_{FST} \quad (2)$$

The relation between boost factor B and d_{sh} is:

$$B = \frac{1}{1 - 2.d_{sh}} \quad (3)$$

For a particular value of modulation index 'M', the value of boost factor 'B' offered by the ULST scheme is lower than the FST scheme. The value offered by the ULST scheme is lower than the FST scheme of 3L-ZSI using a single impedance network. Figure 2 represents the relation between 'B' and 'M' for ULST and FST schemes.

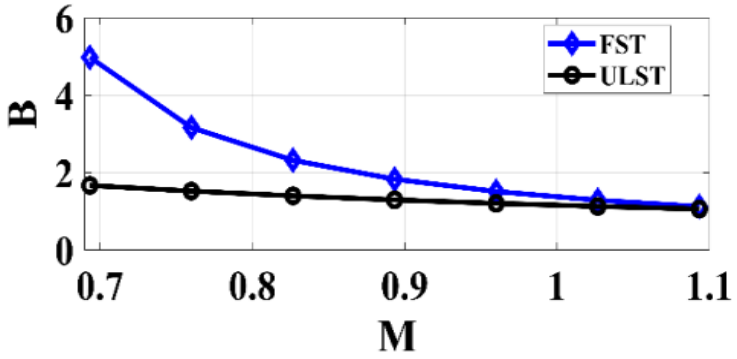

Figure 2. Graph of 'B' and 'M' for ULST and FST schemes using a single impedance network.

3. Operating Principal of the Three-Level Transistor Clamped Topology and Its Comparison with Other Existing Topologies

The diode clamped three-level voltage source inverter is shown in Figure 3. The main problems associated with these inverters are unequal device ratings of semiconductor switches, the need for diodes for dc voltage clamping, a high number of component counts at high levels, and neutral point potential unbalance. The above drawbacks limit their applications in real power conversion. Another alternative is presented in Figure 4, named as transistor clamped three-level inverter in this paper.

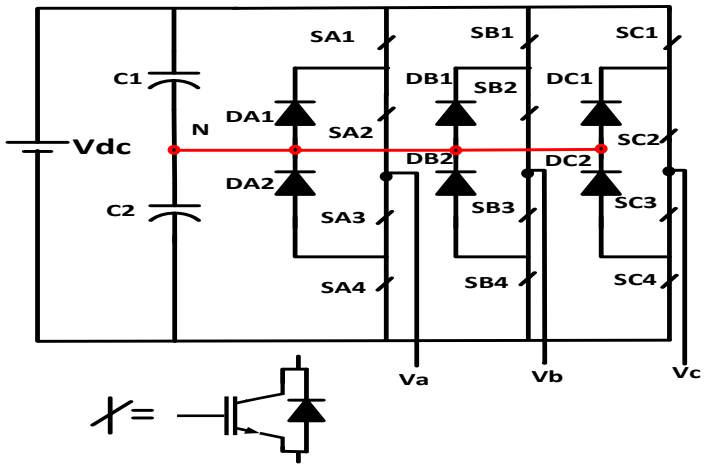

Figure 3. Topology of the diode clamped three-level inverter.

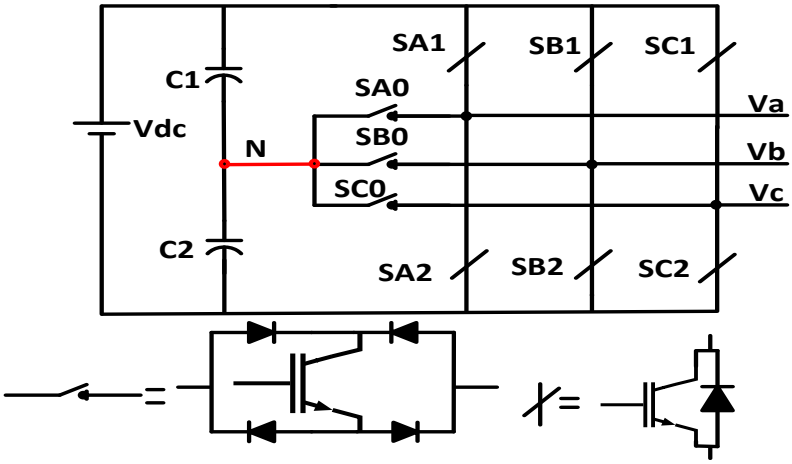

Figure 4. Topology of the transistor clamped three-level voltage source inverter.

This three-level topology has the two main power switches and one auxiliary switch in each leg. The auxiliary switch (a combination of one IGBT and four diodes to accomplish bidirectional power flow) clamps each phase leg voltage to the zero or neutral potential. Table 1 indicates the switch combination for each level of the output pole voltage. From Table 1, it can be seen that at each instant, only one switch from each leg is ON, and the other two (auxiliary and power switches) are off, to generate a three-level output voltage waveform.

Table 1. Transistor clamped three-level inverter voltage level and switching states

V_{YN} (Pole Voltages)	Switch States		
	*SX*1	*SX*0	*SX*2
$V_{dc}/2$	ON	OFF	OFF
0	OFF	ON	OFF
$-V_{dc}/2$	OFF	OFF	ON

Where X = (A, B, C) and Y = (a, b, c).

Main features of this topology are listed below:

- Total power switch count reduces to nine, as compared to twelve in the diode clamped, capacitor clamped, and cascaded for the same three-phase output voltage level.
- No unequal device rating problem, as in the diode clamped configuration. No need for clamping diodes/capacitors.
- Any conventional PWM techniques (sine-triangle/SVPWM) can be used with suitable modifications.
- Single-phase five-level configurations can be realized using only six power switches via appropriately modulating the two legs.

However, neutral point voltage unbalance and common-mode voltage elimination/reduction still require attention, and these issues are not discussed here.

Comparison of the Transistor Clamped, Diode Clamped and T-Type Inverter

The two other main three-level inverter configurations are diode clamped and T-type inverter. One phase leg of the diode clamped and T-type VSI is shown in Figure 5. The working principle of the diode clamped and T-type voltage source inverter can be understood from Table 2.

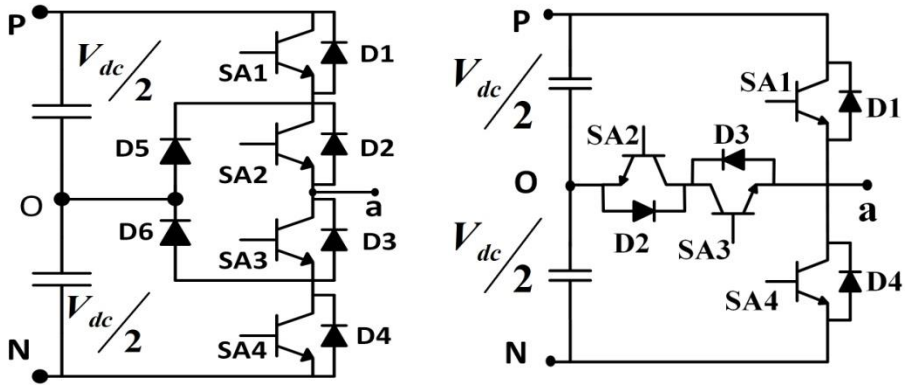

Figure 5. One phase leg of (**a**) the diode clamped VSI, and (**b**) the T-type VSI.

Table 2. Switching states of Diode clamped and T-Type VSI

V_{ao} (Pole Voltage)	Switching State/Position	Diode Clamped		T-Type	
		Gating Pulse	ON Switches/Diodes	Gating Pulse	ON Switches/Diodes
$\frac{V_{dc}}{2}$	P	SA1 and SA2	SA1 and SA2 Or D1 and D2	SA1 and SA3	SA1 or D1
0	O	SA2 and SA3	SA2 and D5 Or SA3 and D6	SA2 and SA3	SA2 and D3 Or SA3 and D2
$-\frac{V_{dc}}{2}$	N	SA3 and SA4	SA3 and SA4 Or D3 and D4	SA2 and SA4	SA4 Or D4

There are four power switches in each phase leg of the diode clamped and T-type VSI. Therefore, four gating pulses are required. Depending upon the direction of load current, various combinations of the ON switch and the ON diodes have been listed in Table 2. The comparison of the average switching frequency of each switch of the transistor clamped, diode clamped, and T-type VSI is presented in Table 3.

Table 3. Average switching frequency of the transistor clamped, diode clamped and T-type VSI.

Avg. Switching Frequency	Transistor Clamped VSI			Diode Clamped VSI				T-Type VSI			
	SX1	SX2	SX3	SX1	SX2	SX3	SX4	SX1	SX2	SX3	SX4
F_{sw}	$\frac{1}{4.T_s}$	$\frac{1}{2.T_s}$	$\frac{1}{4.T_s}$	$\frac{1}{4.T_s}$				$\frac{1}{4.T_s}$			

X = A, B, C, T_s is the duration of one sample period.

From Table 3, it is clear that the switching frequency of the bidirectional switch (SX2) of the transistor clamped VSI is twice that of the upper and lower switch of the same phase leg, and each switch of the diode clamped and T-type VSI. Considering the case of low voltage application (<= 1200 V), the transistor clamped configuration offers the following advantages:

- It provides reduced conduction and switching losses, as compared to the diode clamped VSI, since only one switch per phase leg is conducting at any instant in the transistor clamped VSI. On the other hand, in the diode clamped VSI, two switches per phase leg are in conduction during power flow to load (Table 2).
- It reduces one IGBT per phase leg and its associated gate driver ICs/circuit elements, as compared to the diode clamped and T-type VSI.

- Only one gating pulse is being generated and fed to the particular IGBT at a time to turn it ON in the transistor clamped VSI (Table 1). But there are always two gating pulses being generated in the diode clamped and T-type VSI (Table 2).

However, the following points can be considered as the drawbacks of the transistor clamped inverter configuration:

During the inverter operation in state '0' shown in Table 1, there are two diodes and one IGBT in the conduction path of the transistor clamped VSI. On the other hand, the diode clamped and T-type VSI have one diode and one IGBT in the conduction during state 'O', which can be seen from Table 2. Therefore, the power loss due to one extra diode in state 'O' can be seen as the drawback of the transistor clamped VSI.

The schematic of the gating pulse for the three power switches in the TC-VSI and the conventional VSI is shown in Figure 6. The gating signal of SA2 and SA3 of the existing three-level VSI are logically transformed into one signal for switch SA0 of TC-VSI.

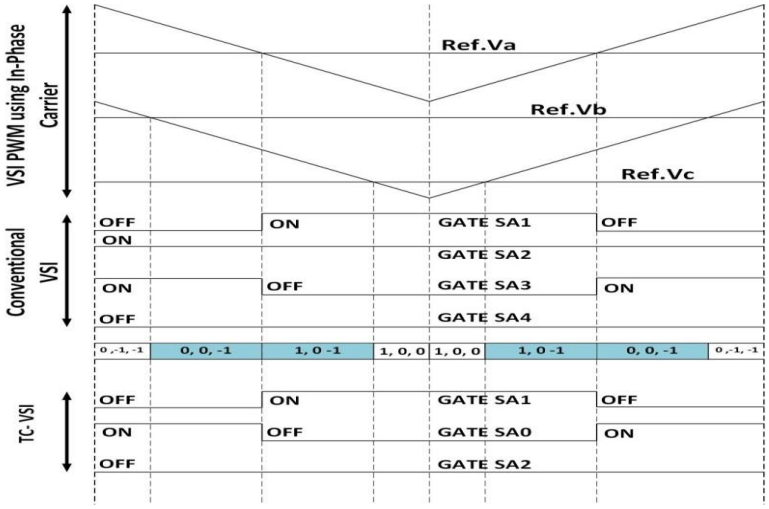

Figure 6. PWM technique description.

4. Proposed Configurations of Transistor Clamped Three-Level ZSI

The concept of ZSI is implemented in the above-discussed transistor clamped VSI. Different types of three-level ZSI configuration already presented in the literature [2–4,10–12] can extend to the transistor clamped configuration.

The attractive feature of the TC-ZSI is that it requires only two switches to be turned ON for shoot-through state insertion, whether it is upper, lower, or full dc-link shoot-through.

Figures 7 and 8 show the schematics of the three-level TC-ZSI using two impedance networks and one impedance network, respectively. Here, one impedance network indicates two inductors and two capacitors.

From Figure 8, it is clear that {'SX1', 'SX0'} is turned ON for the upper shoot-through, as shown in Figure 9a. {'SX2', 'SX0'} is turned ON for the lower shoot-through shown in Figure 9b, and {'SX1', 'SX2'} is turned ON for the full dc-link shoot-through presented in Figure 9c. However, the diode clamped NPC type ZSI requires three semiconductor switches and one diode for upper–lower shoot-through [2] and four switches for full dc-link shoot-through [3].

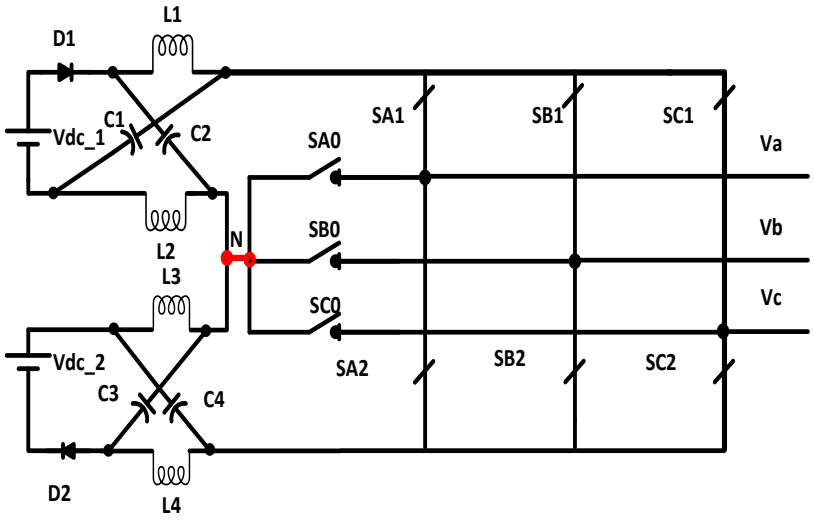

Figure 7. Three-level TC-ZSI using two impedance networks.

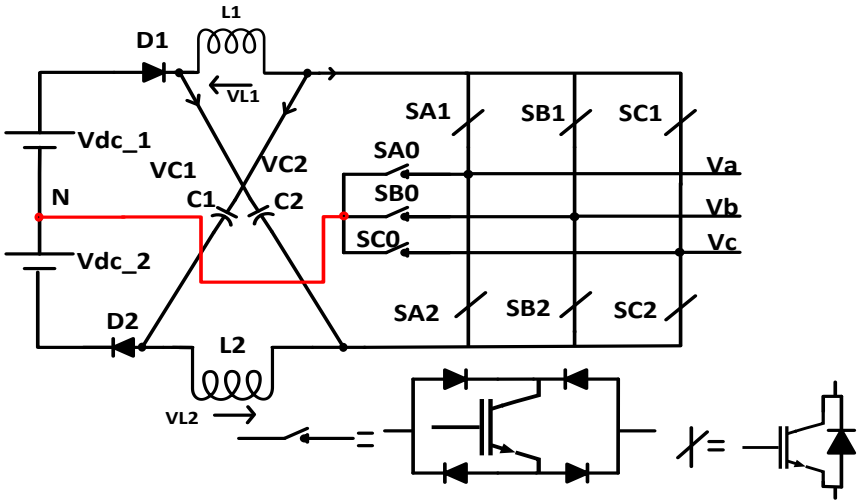

Figure 8. Three-level ZSI using a single impedance network.

This paper considers the ULST scheme for the three-level transistor clamped ZSI proposed in Figure 7. The ULST scheme offers better output waveform quality because of the nearest three vector (NTV) switching. NTV switching is not possible using the FST scheme.

The expression for the capacitor voltage, input dc-link peak voltage $\hat{v}_i$ and output peak phase voltage $\hat{v_x}$ of inverter for both schemes can be written as [12]:

Assuming $L_1 = L_2 = L$, $C_1 = C_2 = C$ and Vdc_1 = Vdc_2 = V_{dc}

FST scheme:

$$V_c = \frac{2V_{dc}(1 - T_o/T)}{(1 - 2T_o/T)}$$

$$\hat{v}_i = \frac{2V_{dc}}{(1 - 2T_o/T)} = 2BV_{dc}$$

$$\hat{v_x} = \frac{M\hat{v_i}}{2} = MBV_{dc} \quad (4)$$

ULST scheme:

$$V_c = \frac{2V_{dc}(1 - T'_o/2T)}{(1 - T'_o/T)}$$

$$\hat{v}_i = \frac{2V_{dc}}{(1 - T'_o/T)} = 2B'V_{dc}$$

$$\hat{v_x} = \frac{M\hat{v_i}}{2} = MB'V_{dc} \quad (5)$$

where "T'_o/T" is the sum of upper and lower shoot-through.

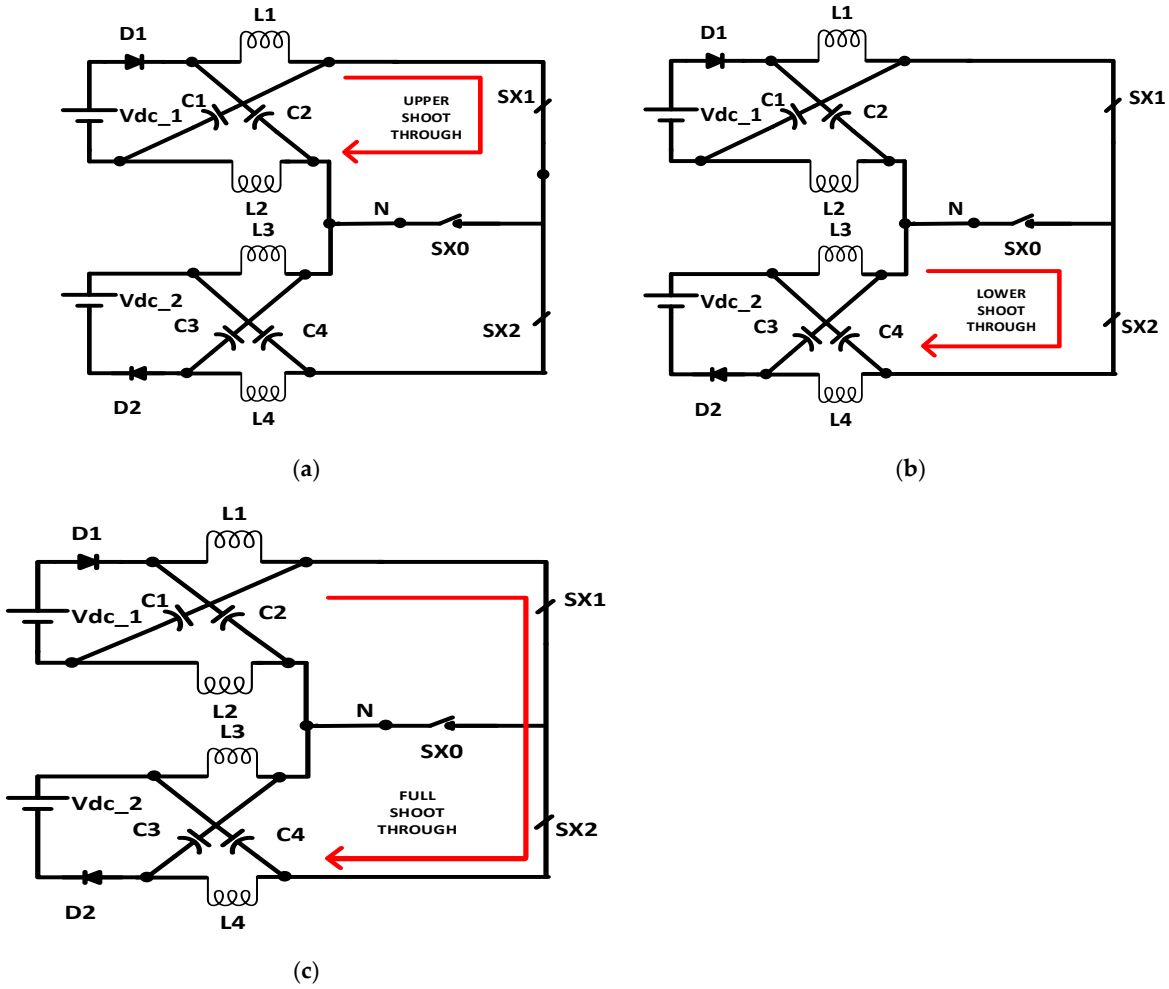

Figure 9. Description of shoot-through states: (**a**) upper shoot-through, (**b**) lower shoot-through, (**c**) full dc-link shoot-through.

4.1. PWM Techniques

The most commonly used sine triangle-based PWM techniques for multilevel inverters are:

- In phase disposition carrier (PD) PWM.
- Alternate phase opposition disposition (APOD) PWM.

The above-mentioned techniques have been used in the literature for the insertion of shoot-through in the three-level ZSI. As per the shoot-through insertion process, these techniques are further classified into continuous edge insertion PWM and modified reference PWM, which differs only in the number of switching transitions. With the addition of an appropriate offset signal in the sinusoidal reference signal, the advantages offered by the central space vector PWM can be realized. The offset signal for three-level ZSI based SVPWM and other discontinuous PWM schemes is reported in [14].

The primary considerations required for insertion of shoot-through in the PWM control technique of three-level NPC-type ZSI or TC-ZSI are summarized below:

- Minimum device commutation per half switching cycle.
- Equal shoot-through time for both impedance network, if two impedance networks are used.

- Shoot-through should always be inserted in the state transition, i.e., null to active, active to active, and active to null with a single switch transition.

Continuous edge insertion using POD/APOD carrier with added offset to increase the modulation index range (<= 1.15) has been used in this paper, as shown in Figure 10. Continuous edge insertion offers a balanced and symmetrical voltage boost per switching cycle, thereby reducing the current ripple.

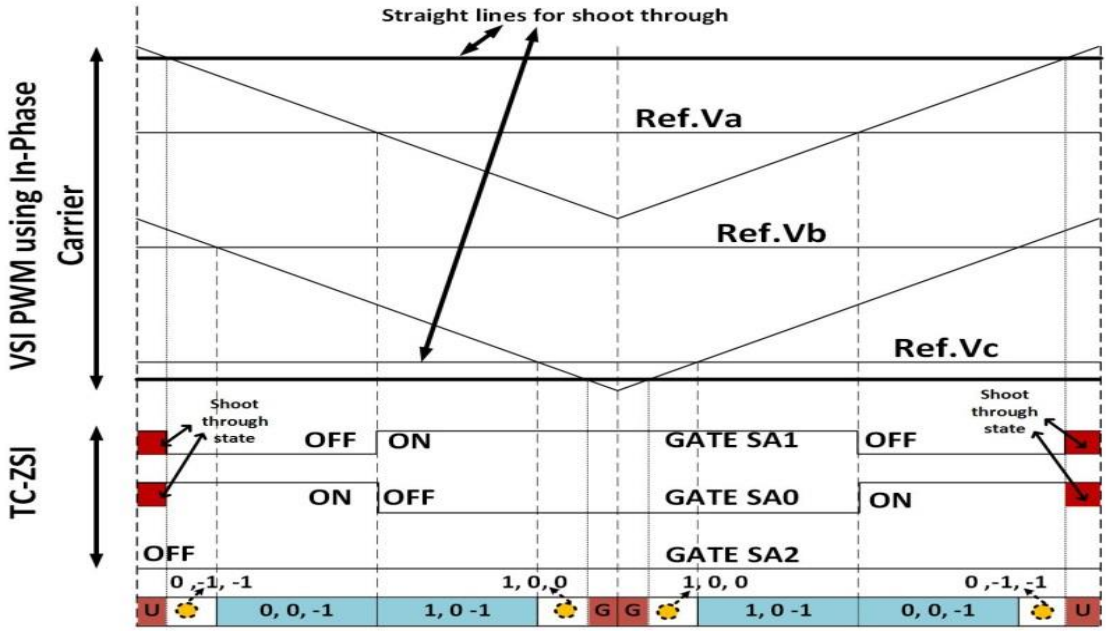

Figure 10. Description of shoot-through for TC-ZSI.

4.2. Conduction and Switching Losses

The conduction and switching losses are the two main contributors to total power losses in the inverter. For a pulsed output voltage and current, the average conduction losses per sub-cycle in IGBT and diode can be calculated as:

$$\begin{aligned} P_{cond.IGBT} &= V_{ce}\left(T_j, I_c\right) \times I_c \times D \\ P_{cond.Diode} &= V_f\left(T_j, I_f\right) \times I_f \times D \end{aligned} \tag{6}$$

The switching losses are further classified into turn-on and turn-off energy losses. The total switching losses in the case of IGBT is defined as:

$$P_{sw.IGBT} = \left(E_{on} + E_{off}\right).F_{sw} \tag{7}$$

Only turn-off losses (reverse recovery losses) have been considered in the case of diodes. These are written as:

$$P_{rec.diode} = E_{rec.} \times F_{sw} \tag{8}$$

The parameters mentioned in the above equations have been taken from the datasheets to find the efficiency and switching losses of the converter.

4.3. Impedance Network Design

The impedance network inductor and capacitor are designed based on the high-frequency ripple components of the inductor current and capacitor voltage, respectively.

The high-frequency component of the inductor ripple current is written as:

$$\Delta i_L = \frac{V_C}{L}\left(\frac{d_{sh}.\mathrm{T}}{2}\right) \tag{9}$$

where V_C is the average voltage across the capacitors of impedance network. It is written as:

$$V_C = V_{dc}\left(\frac{1-d_{sh}}{1-2.d_{sh}}\right) \tag{10}$$

The permissible value of inductor current ripple is defined as:

$$\Delta i_L = r_L.I_L \tag{11}$$

where r_L is the permissible percentage of the average inductor current ripple. I_L is the average inductor current and is expressed as:

$$I_L = \frac{P}{V_{dc}} \tag{12}$$

where 'P' denotes the total output power of the inverter. Substituting (1), (10), and (11) into (9), the expression for 'L' is written as:

$$L = \frac{(1-d_{sh}).V_{dc}.(1-M).\mathrm{T}}{4.(1-2.d_{sh}).r_L.I_L} \tag{13}$$

Similarly, the high-frequency ripple component of the capacitor voltage is written as:

$$\Delta V_C = \frac{I_L}{\mathrm{C}}\left(\frac{d_{sh}.\mathrm{T}}{2}\right) \tag{14}$$

The permissible value of capacitor voltage ripple is defined as:

$$\Delta V_C = r_C.V_C \tag{15}$$

where r_C is the permissible ripple percentage in the average capacitor voltage.

Using (1), (9), (14), and (15), the expression for 'C' can be written as:

$$C = \frac{I_L(1-2.d_{sh}).(1-M).\mathrm{T}}{4.r_C.V_C.(1-d_{sh}).V_{dc}} \tag{16}$$

5. Simulation Results

The proposed topologies are simulated in a MATLAB/SIMULINK environment. A prototype is developed in the laboratory, and the results are presented. The input voltage for the simulation is set to 200 V (100 of each source), RL load (R = 10 ohm and L = 10 mH), and the switching frequency is set to 5.5 kHz. The impedance network inductor and capacitor values are calculated using Equations (13) and (14) as 2 mH and 330 uF. The output waveforms of transistor clamped three-level VSI are shown in Figure 11. It can be seen from Figure 11 that the PD carrier PWM follows the nearest three vectors for synthetization of the output voltage. Figure 12 shows the waveform of the proposed three-level ZSI, based on transistor clamped topology. The configuration shown in Figure 7 is used with the in-phase disposition carrier PWM technique (PD) with modulation index M = 1*1.15 and To/T = 0 (without shoot-through). Then, the upper and lower shoot-through states are inserted, and waveforms are shown in Figure 13 with M = 0.7*1.15 and To/T = 0.3. With upper and lower shoot-through added, the expressions for the gain of the inverter are given in Equation (5) [12]. Where *T'o/T*; represents the sum of upper and lower shoot-through whose sum is equal to the 2*To/T*. By putting the values of M

(=1.15*0.7) and To′/T (=0.3) in the above equation, the output ac phase leg voltage of the inverter comes out to be 250 V, and peak line voltage is 500 V, which is clearly shown in Figure 13. Volt-sec error and minimum device commutation are kept in mind while adding shoot-through states. The same shoot-through time is used for both upper and lower shoot-through, in order to avoid unbalance in output voltage.

Figure 14 shows the TC-ZSI configuration with a single impedance network, as shown in Figure 8. Similar results can be found with the same value of M and B as the above case. APOD PWM technique is used for this configuration to add full dc-link shoot-through, as APOD uses {0 0 0} state, even at a high modulation index. This technique does not follow the nearest three vectors to synthesize the output voltage waveform, which can be seen in the first waveform of Figure 14. The output power quality is poor, and contains higher harmonic distortion, as compared to the phase carrier PWM, if the APOD PWM technique is used; however, it saves one impedance network.

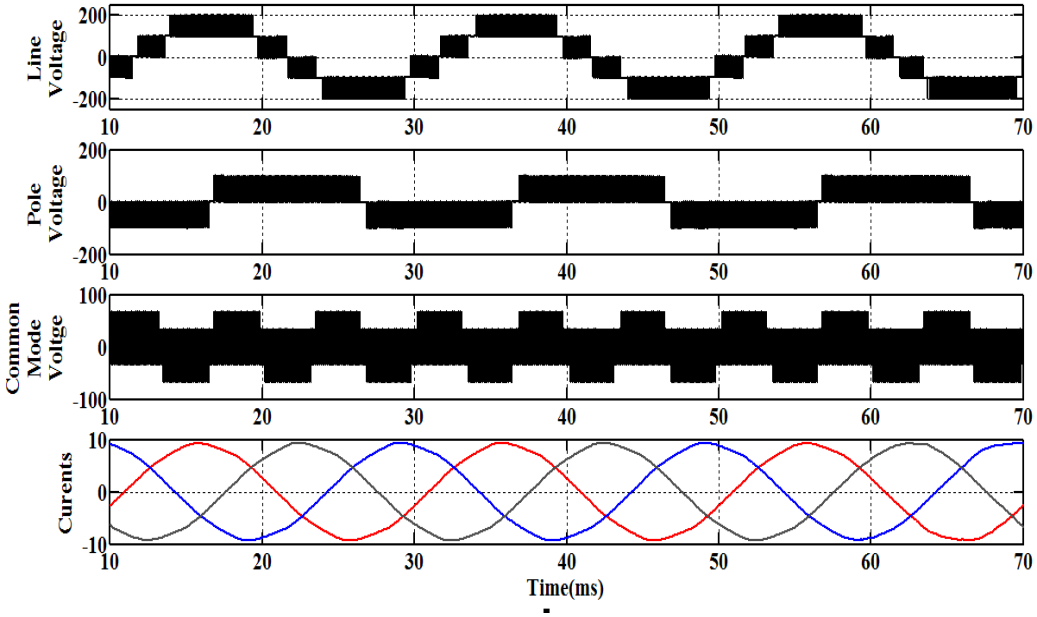

Figure 11. Simulated output waveforms of the transistor clamped VSI, as shown in Figure 1, at a carrier frequency of 5.5 kHz, with a modulation index of 0.9.

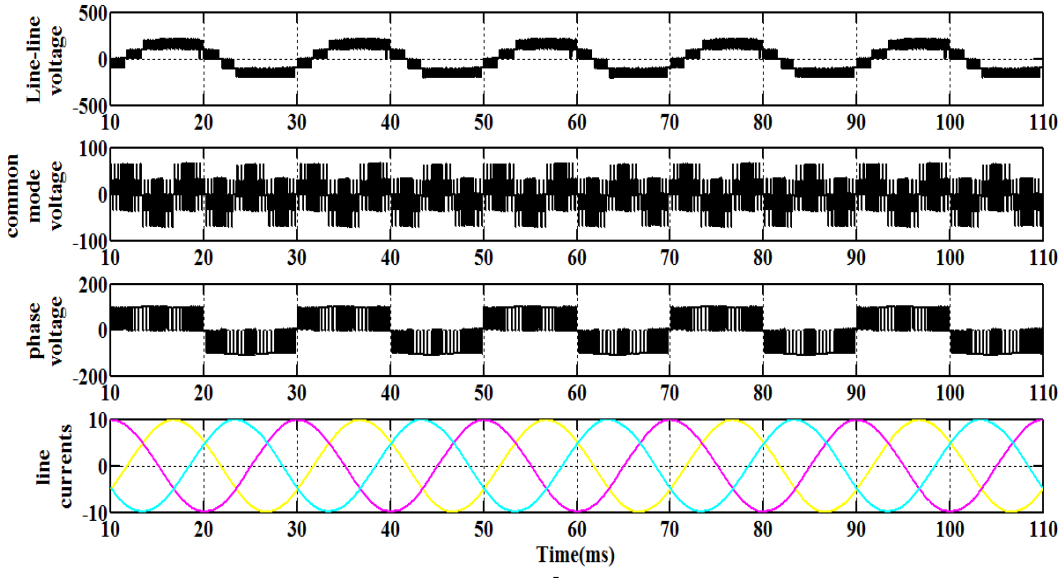

Figure 12. Simulated output waveforms of the transistor clamped ZSI, with M = 1*1.15, To/T = 0, fc = 5.5 kHz.

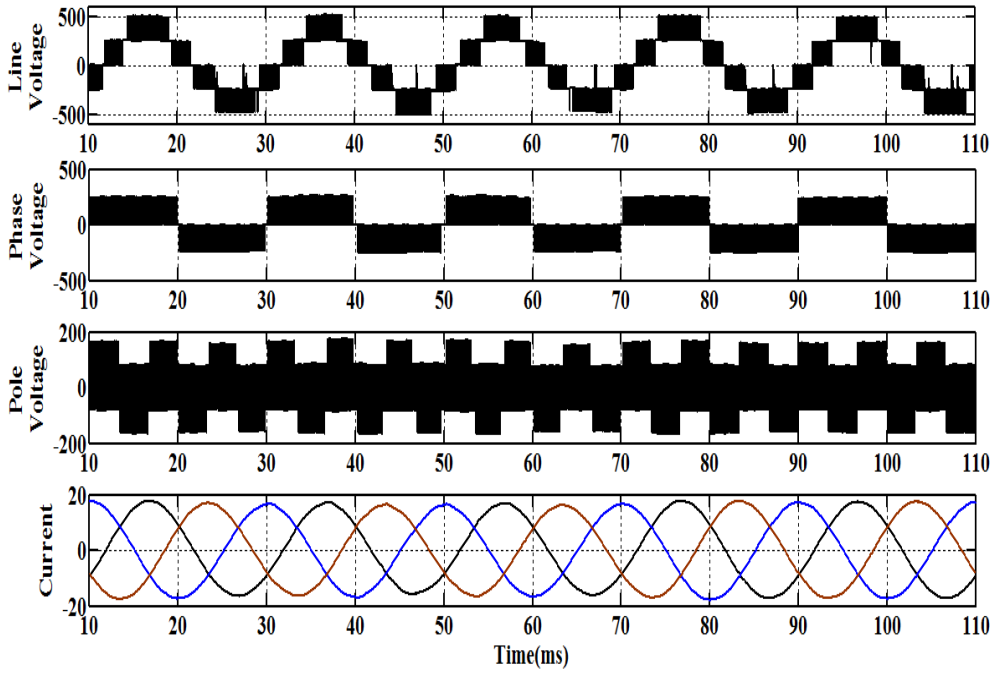

Figure 13. Output of the ZSI with two impedance networks, using phase disposition (PD) PWM with M = 1.15*0.7, To/T = 0.3, fc = 5.5 kHz).

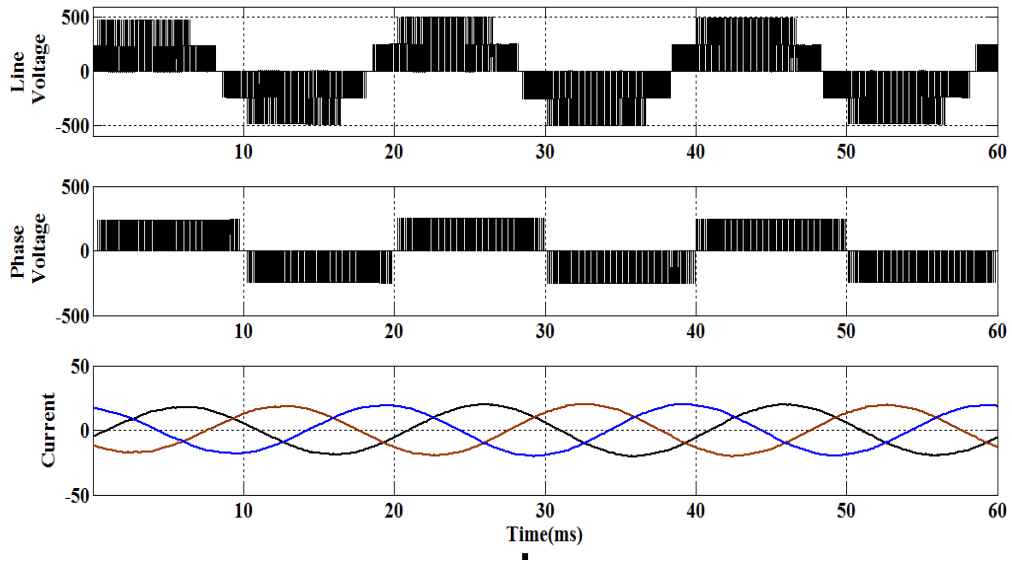

Figure 14. Output waveforms of the TC-ZSI with a single impedance network using the APOD PWM technique (configuration Figure 8).

Figure 15 shows a photograph of the prototype developed in the lab. Figure 16 shows the experimental waveforms of line voltage and pole voltage. Texas Instruments-based DSP TMS320F28335 was used for the generation of switching pulses. Figure 17 shows the waveform of the generated switching pulses. The experimental waveforms have a good agreement with the simulated waveforms. The explanation of the experimental results is same as that of the simulation results.

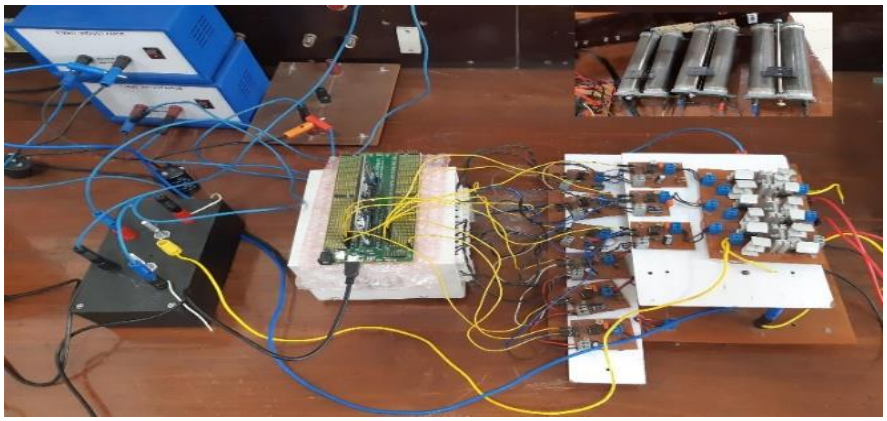

Figure 15. Experimental setup.

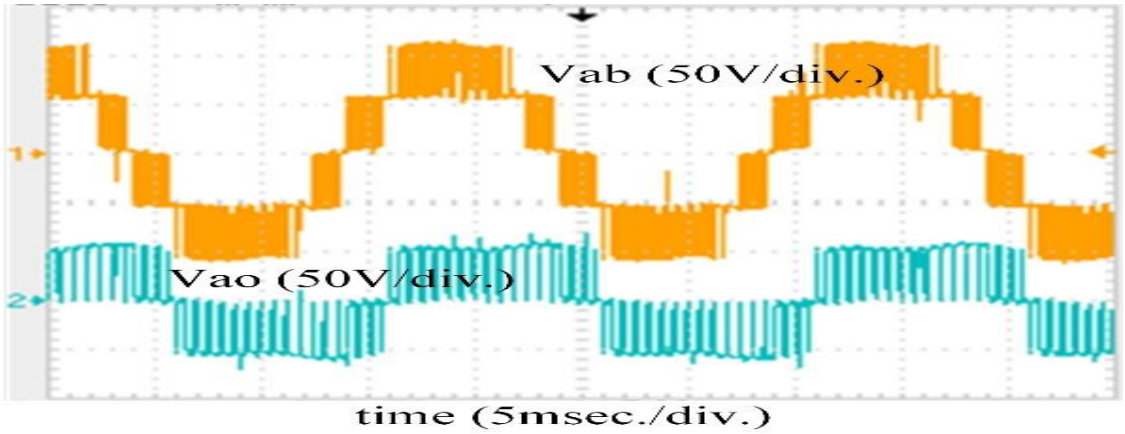

Figure 16. Experimental waveforms at M = 1 and input voltage **Vdc_1 = Vdc_2 = 50** volt. line voltage (V_{ab}) and pole voltage ($V_{ao} = V_{aN}$).

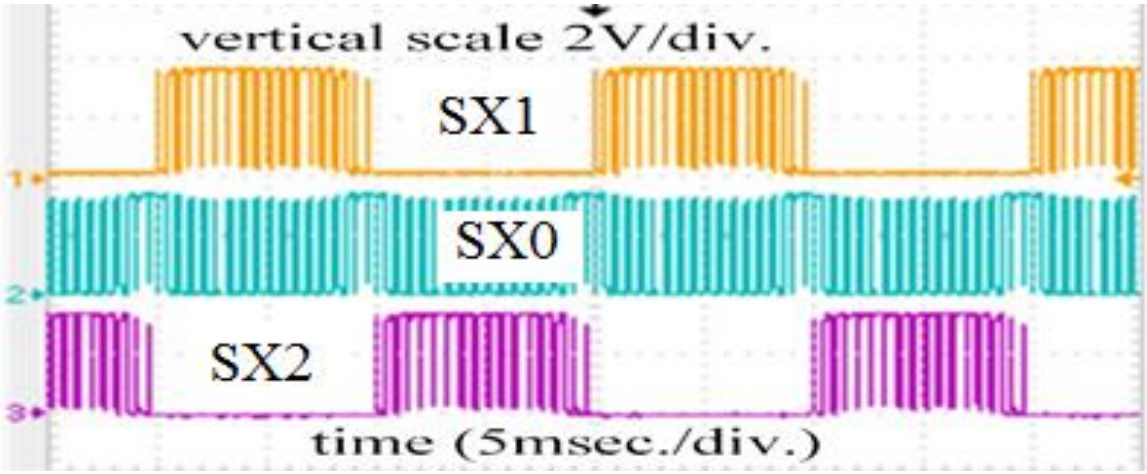

Figure 17. Switching pulses generated from TMS320F28335.

6. Conclusions

This paper presented a new configuration of three-level ZSI derived from a neutral point clamped and conventional ZSI, which uses less component counts and associated gate circuitry as compared to the existing topologies. The proposed converter offers a low-cost alternative to applications that need to ride through frequent input voltage sags. A comparison between diode clamped, transistor clamped, and t-type is presented. It has been revealed that upper–lower shoot-through and full dc-link shoot-through can be easily incorporated by turning ON two power semiconductor switches.

The proposed inverter topology can be modulated by any of the existing PWM techniques, and all current three-level ZSI configurations can be merged into this configuration by changing only the inverter switches. It is verified that the ULST scheme PD method offers better output voltage waveform, as it follows the nearest three vector approach, which is not possible in the FST scheme with the APOD carrier waveform.

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References

1. Peng, F.Z. Z-Source inverter. *IEEE Trans. Ind. Appl.* **2003**, *39*, 504–510. [CrossRef]
2. Loh, P.C.; Blaabjerg, F.; Feng, S.Y.; Soon, K.N. Pulse-Width modulated Z-source neutral-point-clamped inverter. *Proc. IEEE APEC* **2006**, 431–437. [CrossRef]
3. Loh, P.C.; Lim, S.W.; Gao, F.; Blaabjerg, F. Three-Level Z-source inverters using a single LC impedance network. *IEEE Trans. Power Electron.* **2007**, *22*, 706–711. [CrossRef]
4. Loh, P.C.; Gao, F.; Blaabjerg, F.; Feng, S.Y.C.; Soon, K.N.J. Pulsewidth-Modulated Z-source neutral-point-clamped inverter. *IEEE Trans. Ind. Appl.* **2007**, *43*, 1295–1308. [CrossRef]
5. Gao, F.; Loh, P.C.; Blaabjerg, F.; Vilathgamuwa, D.M. Dual Z-source inverter with three-level reduced common-mode switching. *IEEE Trans. Ind. Appl.* **2007**, *43*, 1597–1608. [CrossRef]
6. Loh, P.C.; Gao, F.; Blaabjerg, F. Topological and modulation design of three-level Z-source inverters. *IEEE Trans. Power Electron.* **2008**, *23*, 2268–2277. [CrossRef]
7. Loh, P.C.; Gao, F.; Blaabjerg, F.; Lim, S.W. Operational analysis and modulation control of three-level Z-source inverters with enhanced output waveform quality. *IEEE Trans. Power Electron.* **2009**, *24*, 1767–1775. [CrossRef]
8. Peng, F.Z.; Wang, J.; Joseph, A.; Shen, M.; Chen, L.; Pan, Z.; Ortiz-Rivera, E.; Huang, Y. Z-Source inverter for motor drives. *IEEE Trans. Power Electron.* **2005**, *20*, 857–863. [CrossRef]
9. Loh, P.C.; Gao, F.; Tan, P.C.; Blaabjerg, F. Three-Level AC-DC-AC Z-source converter using reduced passive component count. *IEEE Trans. Power Electron.* **2009**, *24*, 1671–1681. [CrossRef]
10. Boafo Effah, F.; Wheeler, P.; Clare, J.; Watson, A. Space-vector-modulated three-level inverters with a single Z-source network. *IEEE Trans. Power Electron.* **2013**, *28*, 2806–2815. [CrossRef]
11. Mo, W.; Loh, P.C.; Blaabjerg, F.; Wang, P. Trans-Z-Source and Γ-Z-source neutral-point-clamped inverters. *IET Power Electron.* **2014**, *8*, 371–377. [CrossRef]
12. Loh, P.C.; Gao, F.; Blaabjerg, F. Embedded EZ-source inverters. *IEEE Trans. Ind. Appl.* **2010**, *46*, 256–267.
13. Husev, O.; Roncero-Clemente, C.; Romero-Cadaval, E.; Dmitri Vinnikov, S. Single phase three-level neutral-point-clamped quasi-Z-source inverter. *IET Power Electron.* **2014**, *8*, 1–10. [CrossRef]
14. McGrath, B.P.; Holmes, D.G.; Lipo, T. Optimized space vector switching sequences for multilevel inverters. *IEEE Trans. Power Electron.* **2003**, *18*, 1293–1301. [CrossRef]
15. Nabae, A.; Takahashi, I.; Akagi, H. A new neutral-point-clamped PWM inverter. *IEEE Trans. Ind. Appl.* **1981**, *17*, 518–523. [CrossRef]
16. Schweizer, M.; Kolar, J.W. Design and implementation of a highly efficient three-level T-type converter for low-voltage applications. *IEEE Trans. Power Electron.* **2013**, *28*, 899–907. [CrossRef]
17. Noroozi, N.; Zolghadri, M.R. Three-Phase quasi-Z-source inverter with constant common-mode voltage for photovoltaic application. *IEEE Trans. Ind. Electron.* **2018**, *65*, 4790–4798. [CrossRef]
18. Do, D.; Nguyen, M. Three-Level quasi-switched boost T-type inverter: Analysis, PWM control, and verification. *IEEE Trans. Ind. Electron.* **2018**, *65*, 8320–8329. [CrossRef]
19. Barzegarkhoo, R.; Moradzadeh, M.; Zamiri, E. A New boost switched-capacitor multilevel converter with reduced circuit devices. *IEEE Trans. Power Electron.* **2018**, *33*, 6738–6754. [CrossRef]
20. Nguyen, M.; Tran, T. Quasi cascaded H-bridge five-level boost inverter. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8525–8533. [CrossRef]
21. Roncero-Clemente, C.; Romero-Cadaval, E.; Ruiz-Cortés, M.; Husev, O. Carrier level-shifted based control method for the PWM 3L-T-type qZS inverter with capacitor imbalance compensation. *IEEE Trans. Ind. Electron.* **2018**, *65*, 8297–8306. [CrossRef]

22. Xing, X.; Zhang, C.; Chen, A.; He, J.; Wang, W.; Du, C. Space-vector-modulated method for boosting and neutral voltage balancing in Z-source three-level T-type inverter. *IEEE Trans. Ind. Appl.* **2016**, *52*, 1621–1631. [CrossRef]
23. Qin, C.; Zhang, C.; Chen, A.; Xing, X.; Zhang, G. A space vector modulation scheme of the quasi-Z-source three-level T-type inverter for common-mode voltage reduction. *IEEE Trans. Ind. Electron.* **2018**, *65*, 8340–8350. [CrossRef]