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Nonlinear Characteristics Compensation of Inverter for Low-Voltage Delta-Connected Induction Motor

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Abstract: This paper proposes a scheme that can compensate for the nonlinear characteristics of voltage source inverters (VSIs) for low-voltage delta-connected induction motors (IMs). Due to the nonlinearity introduced by the dead-time, the on/off delay, and the voltage drop across the power device, the output voltage of VSIs is seriously distorted, causing distortion in the phase current of the IM, which will lead to output torque ripple. However, the existing compensation methods for three-phase VSIs are derived from star-connected loads, or ignore the conducting properties of power devices. Moreover, the current polarity detection near the current zero is quite complex. In this paper, by taking such nonlinear characteristics into consideration, especially the conducting property of metal-oxide-semiconductor field effect transistors (MOSFETs), an output voltage model of VSIs for low-voltage delta-connected induction motors is presented. After that, in view of the difficulty in detecting the line current polarity near the current zero which might lead to the wrong compensation, an advancing current crossing zero (ACCZ) compensation is proposed. Subsequently, a compensation scheme which combines the compensation based on the VSI output voltage model and ACCZ compensation is proposed. Finally, the proposed compensation scheme is implemented based on a digital signal processor (DSP) drive system. The experimental results show that the proposed scheme has better performance than the common method in terms of suppressing the effect of the nonlinear characteristics of VSI, which demonstrates that the proposed compensation scheme is feasible and effective for the compensation of the nonlinear characteristics of VSI for low-voltage delta-connected IMs.

Keywords: dead-time effect; electric vehicle; induction motor; voltage source inverter; compensation scheme

1. Introduction

In recent years, the use of low-voltage (48V) induction motor (IM) drive systems has become a trend for both pure electrical vehicles (EVs) and hybrid EVs due to their safety and lack of need of a high-voltage protection device [1]. In such a situation, the high-power battery pack with low-voltage outputs a large current, i.e., several hundred amperes. Thus, a delta-connected IM is better than a star-connected one in low-voltage IM drive systems [2]. However, introducing a delta-connected motor to drive system brings new challenges regarding the compensation of nonlinear characteristics which include dead-time, the on/off delay, and the voltage drop across the power devices in the voltage source inverter (VSI). Such nonlinear characteristics are detrimental to the performance of the inverter, and sequentially lead to large current harmonics as well as torque ripple [3,4].

To mitigate the negative effect of these nonlinear characteristics, two major types of compensation methods have been proposed [5–15]. The first type is to model the nonlinear characteristics as an average voltage loss where the voltage–second is averaged in one pulse-width modulation (PWM) cycle, and then the average voltage loss is added directly to the reference voltage [5–8,13–15]. The second type models the nonlinear characteristics as a pulse shift error which is compensated for in each PWM cycle [9–12]. A least mean square (LMS)-based algorithm is introduced to decrease the current harmonics caused by dead-time in permanent magnet synchronous motor *V*/*f* control systems [13]. The voltage error is estimated by adopting an observer which is based on harmonic analyses and the Kalman filter in the literature [14]. In the literature [15], an adaptive dead-time compensation method is proposed with PWM predictive control. The authors of [16] employed a revised repetitive controller (RRC) to reduce the phase current distortion caused by dead-time. The nonlinear characteristics are compensated for by monitoring the harmonic distortion in the *d* axis current [17]. A dead-time distortion shaping (DTDS) technique is proposed to displace the energy of the distortion away from the frequency band of interest in [18]. In [19], a graphical solution for compensating voltage error is proposed. Using an adaptive full-order observer, the VSI nonlinear error is compensated for by using feedback gains and self-tuning estimated current errors [20]. However, the existing compensation methods of nonlinear characteristics are based on the star connected load. Therefore, compensation based on the output voltage model of the VSI for delta-connected IMs should be rederived. Meanwhile, in [8,9], the voltage drop across the power device is ignored, and only dead-time and the on/off delay are compensated for. The authors of [4,7,10] built the output voltage model of VSI with a constant voltage drop across the power device. In low-voltage inverters, the metal oxide semiconductor field effect transistor (MOSFET) is the first choice for the power device in low-voltage inverters because it has more efficient performance than insulated gate bipolar translators (IGBTs) [21,22]. Due to the conductance modulation effect, the voltage drop observed in IGBTs could be regarded as a constant, which makes it possible that the compensation could be calculated offline [22]. However, there is no conductance modulation effect for MOSFETs. Therefore, MOSFETs have the property of resistance when they conduct. In fact, the voltage drop across MOSFETs should be regarded as a current-related variable, which has to be calculated online, rather than a constant [21]. More importantly, compared to high-voltage systems, the voltage drop across power devices in low-voltage induction motor drive systems is considerably higher because of the large current.

In addition, the line current polarity near the zero is difficult to detect due to the inevitable current ripple. In [23], accurate current polarity detection is implemented by a current polarity detection circuit and a field-programmable gate array (FPGA) in the VSI. Although this guarantees the accuracy of the detection, the cost increases at the same time. A method which filters the current and takes the results as the current polarity is proposed in [6]; however, it causes a phase delay and requires complex calculations. To simplify detection, the reference current polarity is regarded as the most practical current polarity method in the realization of compensation [8]. There is no doubt that this works in steady-state systems. Nevertheless, for EV drive systems, the error cannot be ignored. Thus, to compensate for the nonlinear characteristics of the VSI for low-voltage, delta-connected IMs, the conducting properties of the power device should be taken into consideration. Furthermore, the compensation value should be derived under delta-connected load conditions. Moreover, a current detection method near the zero point should be simplified.

This paper mainly focuses on the compensation for the nonlinear characteristics for low-voltage induction motor drive systems. In Section 2, the output voltage model of a VSI for a low-voltage, delta-connected IM is given, and the voltage drop across the MOSFET is modeled according to its conducting properties. In Section 3, a compensation scheme based on the output voltage model of the VSI for the delta-connected IM is proposed. Then, to overcome the difficulty of current polarity detection near zero, advancing current crossing zero (ACCZ) compensation is proposed. Finally, a compensation scheme which combines the two aforementioned compensation modes is proposed. In Section 4, by comparing the results of the experiment with no compensation and another common compensation method, the validity of the proposed compensation scheme is verified.

2. Nonlinear Characteristics of the Inverter for Low-voltage Electric Vehicles

There are two major types of inverter nonlinear characteristics, namely, the PWM cycle time error and the voltage drop across the power device. The PWM cycle time error contains the dead-time and the on/off delay for power device. On most occasions, the voltage drop across the power device can be deemed as a constant; however, in the VSI for low-voltage IMs, it should be treated as a variable which is associated with the conducting current [21]. All these factors must be tackled to obtain satisfactory performance from a VSI for a low-voltage IM.

2.1. Dead-time and Turn-on/off Delay

The typical MOSFET-based three-phase VSI topology with a delta-connected IM load is shown in Figure 1. T_1–T_6 represent the MOSFETs and D_1–D_6 represent the antiparallel diodes. Point O is the power neutral and i_A is the current in phase A of VSI or the line current of the IM. The time required for the MOSFET to turn on and off are denoted by T_{on} and T_{off}, respectively. It is essential to set a dead-time (T_d) between MOSFET T_1 and T_4 (T_3 and T_6, T_5 and T_2) in order to prevent short circuits in any of the legs of the VSI. The parasitic parameters of power devices and possible buffer circuits are ignored in this paper.

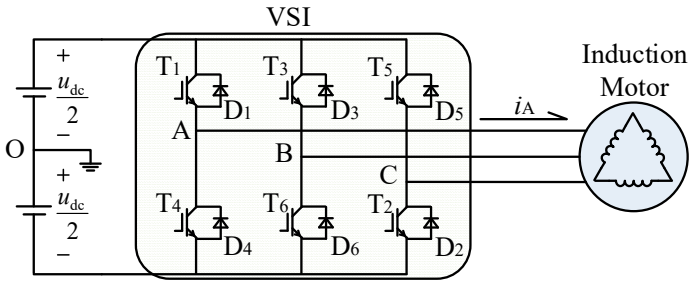

Figure 1. MOSFET-based, three-phase VSI with a delta-connected induction motor load.

The three phases in a motor drive system can be assumed to generally be identical, so only phase A in the VSI is analyzed below. The current direction is defined as positive, as shown in Figure 1. In addition, the gate drive signals for MOSFETs and the corresponding output voltage waveforms of the VSI legs (u_{AO}) under different current polarities are shown in Figure 2 [10]. In one PWM cycle, the ideal conducting time for phase A in the VSI is T_{Aideal}, and the average reference voltage is

$$\overline{u_{AOset}} = u_{dc}\frac{T_{Aideal}}{T_s} \tag{1}$$

where u_{dc} is the dc bus voltage and T_s is the switching period.

With a dead-time on the pulse rising edge, the practical gate drive signals for T_1 and T_4 are S_{T1} and S_{T4} respectively. Due to the MOSFET's turn on and off time delay, the practical conducting time for T_1 and T_4 are T_{T1} and T_{T4}, respectively. As a result, the output voltage of the VSI legs can be derived under different current polarities. From Figure 2, the average voltage error in one PWM cycle can be expressed as (2), which varies with the current polarity indicated by sign function

$$\overline{\Delta u_{AO}}' = u_{err}\cdot \mathrm{sign}(i_A) \tag{2}$$

where sign (i_A) is the sign function, which can be defined as

$$\mathrm{sign}(i_A) = \begin{cases} 1 & i_A > 0 \\ -1 & i_A < 0 \end{cases} \tag{3}$$

where i_A is the current in phase A of VSI, or the line current of the IM. u_{err} is defined as

$$u_{err} = \frac{u_{dc}(T_d + T_{on} - T_{off})}{T_s} \tag{4}$$

So, the practical conducting time in one PWM cycle for phase A can be derived as

$$T_{\mathrm{A}} = T_{\mathrm{Aideal}} + \mathrm{sign}(i_{\mathrm{A}})(T_{\mathrm{d}} + T_{\mathrm{on}} - T_{\mathrm{off}}) \tag{5}$$

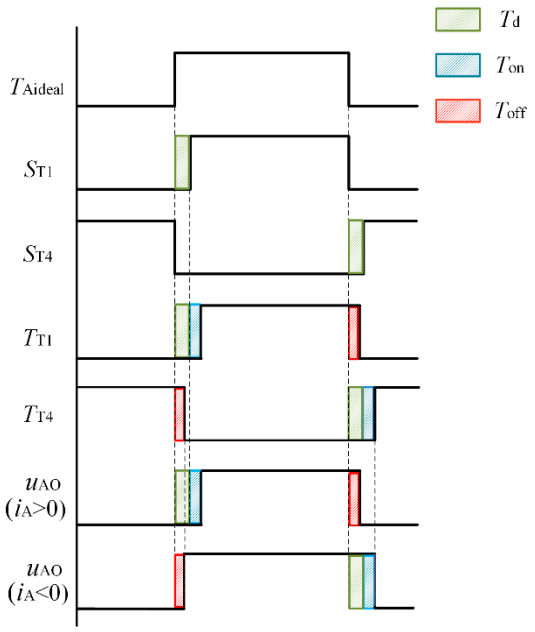

Figure 2. Drive signals and output voltage for phase A with dead-time and on/off delay.

2.2. Voltage Drop Across the MOSFET

For general motor drive systems, the impact of voltage drop across power devices is negligible. However, such an impact cannot be ignored if we wish to obtain a precise supply voltage and a stable torque output. Specially in low-voltage motor drive systems, large currents will make the voltage drop even larger. Hence, we cannot consider the voltage drop to be constant. However, it should be a variable which is related to the conducting current.

The impact of the voltage drop across power devices in one PWM cycle is shown in Figure 3. T_{T1} and T_{T4} are the practical conducting time for MOSFET $\mathrm{T_1}$ and $\mathrm{T_4}$. Due to the voltage drop across the power device, the practical output voltage of the VSI legs is u_{AO} under different current polarities [12]. As a consequence, the output voltage of the VSI legs can be expressed as (6), according to Figure 3

$$u_{\mathrm{AO}} = (u_{\mathrm{dc}} - u_{\mathrm{t}} + u_{\mathrm{d}})(K_{\mathrm{A}} - \frac{1}{2}) - \frac{1}{2}\mathrm{sign}(i_{\mathrm{A}})(u_{\mathrm{t}} + u_{\mathrm{d}}) \tag{6}$$

where u_{t} is the voltage drop across the MOSFET, and u_{d} is the voltage drop across the antiparallel diode. K_{A}=1 when the phase A drive pulse is at a high level, and K_{A}=0 when the phase A drive pulse is at a low level.

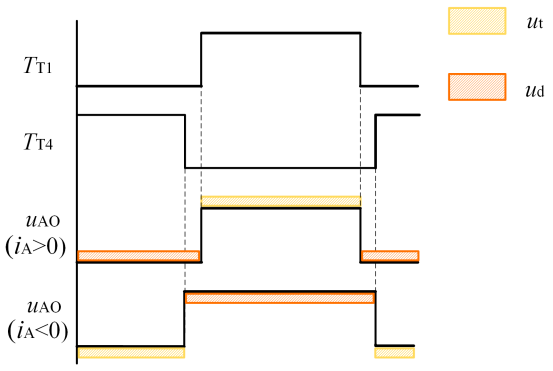

Figure 3. Drive signals and output voltage for phase A with voltage drop across power devices.

Thus, the average output voltage in one PWM cycle can be derived as

$$\overline{u_{\mathrm{AO}}} = (u_{\mathrm{dc}} - u_{\mathrm{t}} + u_{\mathrm{d}})(\frac{T_{\mathrm{A}}}{T_{\mathrm{s}}} - \frac{1}{2}) - \frac{1}{2}\mathrm{sign}(i_{\mathrm{A}})(u_{\mathrm{t}} + u_{\mathrm{d}}) \tag{7}$$

According to the above analysis, the voltage drop across the MOSFET is related to the conducting current. Moreover, the MOSFET presents resistance properties when it is conducting; thus, according to [17], the relationship between the voltage drop across the MOSFET and the conducting current can be derived as (8):

$$u_{\mathrm{t}} = u_{\mathrm{t0}} + R_{\mathrm{t}}\left|i_{\mathrm{A}}\right| \tag{8}$$

where u_{t0} is the cut-off voltage and R_{t} is the conducting resistance of MOSFET.

As a result, in the VSI for low-voltage motor drive systems, the average output voltage for phase A with consideration of the voltage drop across the MOSFET can be expressed according to (5), (7), and (8)

$$\overline{u_{\mathrm{AO}}} = (u_{\mathrm{dc}} - u_{\mathrm{t0}} + R_{\mathrm{t}}\left|i_{\mathrm{A}}\right| + u_{\mathrm{d}})[\frac{T_{\mathrm{Aideal}} + \mathrm{sign}(i_{\mathrm{A}})(T_{\mathrm{d}} + T_{\mathrm{on}} - T_{\mathrm{off}})}{T_{\mathrm{s}}} - \frac{1}{2}] - \frac{1}{2}\mathrm{sign}(i_{\mathrm{A}})(u_{\mathrm{t0}} + R_{\mathrm{t}}\left|i_{\mathrm{A}}\right| + u_{\mathrm{d}}) \tag{9}$$

Similarly, we can get $\overline{u_{\mathrm{BO}}}$ and $\overline{u_{\mathrm{CO}}}$; then, the output voltage model of the VSI for low-voltage motor drive systems is complete.

3. The Proposed Compensation Scheme

There are two modes in the proposed compensation scheme, namely, compensation based on the output voltage model of the VSI and ACCZ compensation. The mode of compensation depends on the state of the current.

3.1. Compensation based on the Output Voltage Model of VSI

According to (1), (5), and (9), the average voltage error in one PWM cycle can be obtained from the output voltage model of the VSI and the reference voltage in phase A

$$\begin{aligned}\overline{\Delta u_{\mathrm{AO}}} &= \overline{u_{\mathrm{AOset}}} - \overline{u_{\mathrm{AO}}} \\ &= u_{\mathrm{dc}}\frac{T_{\mathrm{Aideal}}}{T_{\mathrm{s}}} - (u_{\mathrm{dc}} - u_{\mathrm{t0}} + R_{\mathrm{t}}\left|i_{\mathrm{A}}\right| + u_{\mathrm{d}})(\frac{T_{\mathrm{Aideal}} + \mathrm{sign}(i_{\mathrm{A}})(T_{\mathrm{d}} + T_{\mathrm{on}} - T_{\mathrm{off}})}{T_{\mathrm{s}}} - \frac{1}{2}) \\ &\quad - \frac{1}{2}\mathrm{sign}(i_{\mathrm{A}})(u_{\mathrm{t0}} + R_{\mathrm{t}}\left|i_{\mathrm{A}}\right| + u_{\mathrm{d}})\end{aligned} \tag{10}$$

Similarly, we can get $\overline{\Delta u_{\mathrm{BO}}}$ and $\overline{\Delta u_{\mathrm{CO}}}$. As shown in Figure 1, 48V IM is delta connected. The relationship between the phase voltage of the stator and the output voltage of the VSI legs can be expressed as

$$\begin{cases} u_{\mathrm{Ap}} = u_{\mathrm{AO}} - u_{\mathrm{BO}} \\ u_{\mathrm{Bp}} = u_{\mathrm{BO}} - u_{\mathrm{CO}} \\ u_{\mathrm{Cp}} = u_{\mathrm{CO}} - u_{\mathrm{AO}} \end{cases} \tag{11}$$

where u_{Ap}, u_{Bp}, and u_{Cp} are the stator phase voltage.

For Clark transformation [13],

$$\begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} u_{\mathrm{Ap}} \\ u_{\mathrm{Bp}} \\ u_{\mathrm{Cp}} \end{bmatrix} \tag{12}$$

where u_{α} and u_{β} are the stator phase voltage in α–β reference frame.

Hence, in α–β reference frame, (12) can be rewritten as follows according to (11):

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} u_{AO} \\ u_{BO} \\ u_{CO} \end{bmatrix} \tag{13}$$

Similarly, the relationship between the average error voltage in the two-phase stationary coordinate system and the average output voltage of the VSI legs in one PWM cycle can be expressed as:

$$\begin{bmatrix} \overline{\Delta u_\alpha} \\ \overline{\Delta u_\beta} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \overline{\Delta u_{AO}} \\ \overline{\Delta u_{BO}} \\ \overline{\Delta u_{CO}} \end{bmatrix} \tag{14}$$

where $\overline{\Delta u_\alpha}$ and $\overline{\Delta u_\beta}$ are the stator phase voltage error in α–β reference frame, and $\overline{\Delta u_{AO}}$, $\overline{\Delta u_{BO}}$, and $\overline{\Delta u_{CO}}$ are the output voltage error of the VSI legs. Based on (10) and (14), the reference voltage of space vector modulation (SVM) is compensated for:

$$\begin{cases} u_\alpha = u_\alpha^* + \overline{\Delta u_\alpha} \\ u_\beta = u_\beta^* + \overline{\Delta u_\beta} \end{cases} \tag{15}$$

where u_α and u_β are the set value of the reference voltage of SVM, and u_α^* and u_β^* are the actual value of the reference voltage of SVM. From (15), the error voltage in the two-phase stationary coordinate system is directly added to the reference voltage of the SVM, and the output voltage of the VSI can be compensated for accurately. Meanwhile, it is noteworthy that the SVM modulation strategy for a delta-connected load should be rederived.

3.2. Advancing Current Crossing Zero (ACCZ) Compensation

According to the above analysis, the error voltage caused by nonlinear characteristics is related to the magnitude and polarity of the current in each phase of the VSI. When the current crosses zero, the polarity of the current may be judged incorrectly due to the zero current clamping effect and the current burr during detection. As a result, a wrong compensation will be caused. To get the accurate polarity of the current, the methods mentioned in Section 1, which include filtering the current or adopting the reference current as the practical current polarity, cannot be applied for EV drive systems. A method requiring fewer calculations should be proposed for low-voltage EVs.

It can be seen from (10) that when the current is nonzero, the current and the compensation voltage always show opposite polarities to each other. Therefore, at this point, applying a compensation voltage which has the same polarity to the current will accelerate the current crossing zero, as shown in Figure 4. Therefore, when the current polarity is difficult to detect and the current has not crossed zero, if we still adopt the compensation value based on the output voltage model of the VSI (such a compensation value is hereafter referred to as ε), incorrect compensation may result. Instead, we can assume the current has already crossed zero, and then set the compensation value magnitude to ε with the polarity opposite to ε, and maintain this compensation value. Such a compensation value will accelerate the process of the current crossing zero. After the current crosses zero and reaches a certain value, we can return to the compensation based on the output voltage model of the VSI. Because the zero crossing is accelerated, the zero current clamping effect will only occur for a very short time, which has little influence on the whole waveform. In other words, the overall development direction of the current is completely correct. Therefore, the problem of determining the direction of the current can be solved by simply advancing the current crossing zero compensation.

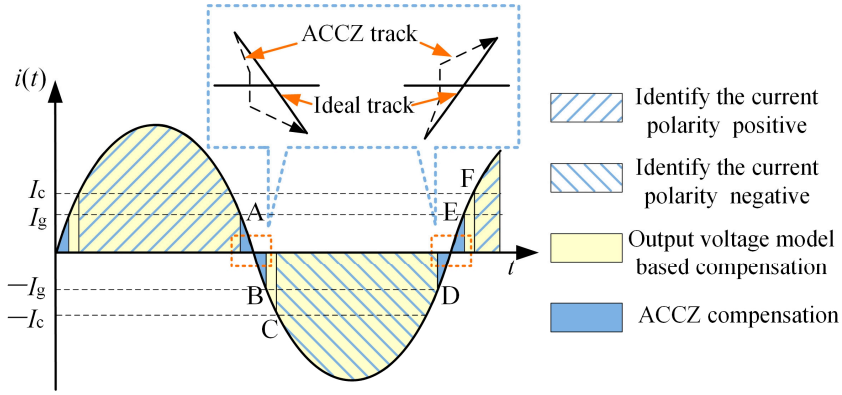

Figure 4. Advancing current crossing zero (ACCZ) Compensation.

The specific determination method of current direction is shown in Figure 4. Firstly, we can set two current limits, I_g and I_c, according to the actual working condition of the IM and the current detection noise tolerance. In the segment AC of Figure 4, before the current is less than I_g (point A in Figure 4), the current polarity can be determined to be positive. Once the current is lower than I_g, it is assumed that the current will continue to develop in a negative direction, and therefore, that the polarity cannot be detected accurately. The compensation value is set as the opposite number of the compensation value (ε) when the current is equal to I_g until the current is less than $-I_g$ (point B in Figure 4). At the same time, in order to avoid burr interference in the current detection near point B, the negative polarity of the current is not determined until the current is less than $-I_c$ (point C in Figure 4). After the current is less than $-I_c$, we can compensate according to the output voltage model of the VSI.

Conversely, in segment DF of Figure 4, before the current is more than $-I_g$ (point D in Figure 4), we can determine that the current polarity is negative. Once the current is more than $-I_g$, we can assume that current will continue to develop in a positive direction, and that the polarity cannot be accurately detected again. The compensation value is set as the opposite number of the compensation value when the current is equal to $-I_g$, until the current is more than I_g (point E in Figure 4). Similarly, in order to avoid burr interference in the current detection near point E, the negative polarity of the current is not determined until the current is more than I_c (point F in Figure 4). After the current is less more than I_c, we can compensate according to the output voltage model of the VSI, and enter the next current cycle.

3.3.A combination of Two Compensation Modes

To realize the two compensation modes described above, a determination strategy was carried out, as shown in Figure 5.

In Figure 5, we begin with the current sampling, and get the current value *i*. Next, by comparing with the current samples several PWM cycles ago, we can determine whether the current is increasing or decreasing. We built function *T* to indicate whether the current was increasing or decreasing. When T=1, the current was increasing. When T=0, the current was decreasing. Then, the compensation mode is determined by the judgment condition described in Section 3.2, and the current value *i*. During the determination and calculation, we created the current polarity function *P* for convenience. When P=0, the current polarity is negative. When P=1, the current polarity is positive. When P=2, the current polarity is assumed to be undetectable. The control strategy diagram for the proposed compensation scheme is shown in Figure 6.

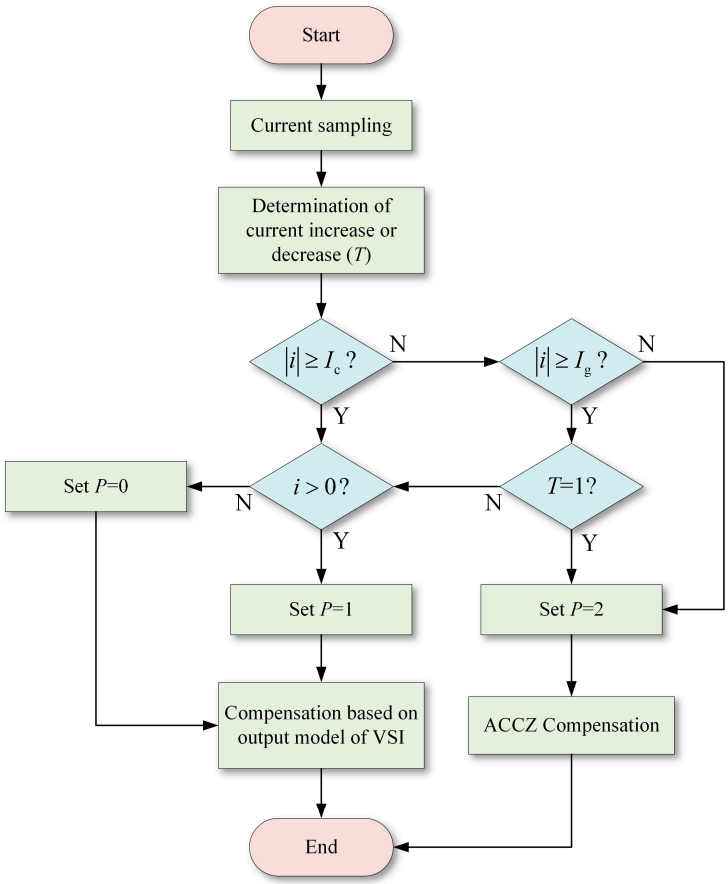

Figure 5. Determination strategy of two compensation modes.

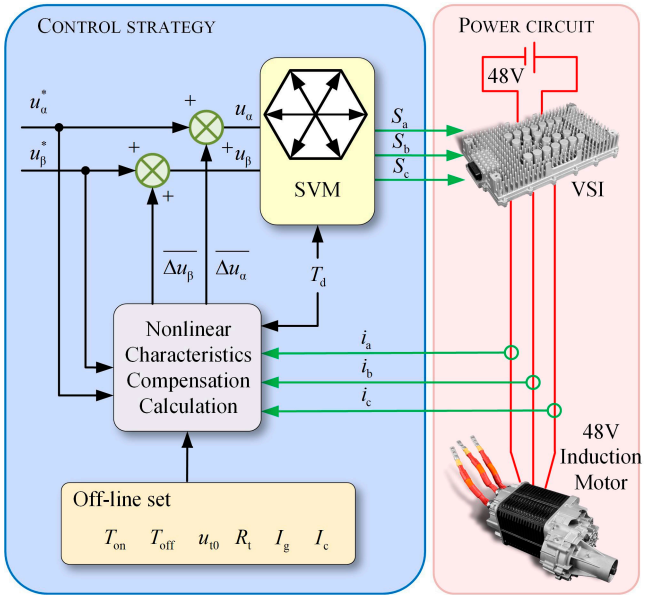

Figure 6. Diagram for the proposed compensation.

4. Experimental Verification

In order to verify the proposed compensation scheme, experiments were implemented on a digital signal processor (DSP) drive system. The experiments were done with 2μs dead-time and a 15kHz switching frequency. The parameters of the 48V IM are shown in Table 1. For the MOSFET (STH15810-2), the conducting resistance is 0.0039Ω with u_{t0}=0.43V, and the on/off delays are 33ns and

72ns, respectively, while I_g and I_c are set as 4A and 8A, respectively. DSP tms320-f28035 is adopted as the controller of the system to build the VSI induction motor driving experimental platform. Due to the 15kHz switching frequency, the current sampling delay and the effect of discretization to realize digital control are neglected.

Table 1. Parameters of 48V IM.

Parameters	Value
Rated voltage / frequency / power	48 V/ 50 Hz/ 15 kW
Rated torque / speed	20(N·m)/ 1500(r/min)
Stator resistance /Rotor resistance	0.00718065 Ω / 0.00839509 Ω
Stator leakage inductance	3.6284×10^{-5} H
Rotor leakage inductance	2.75251×10^{-5} H
Excitation inductance	0.00112 H
Rotational inertia	0.0164(kg·m^2)
Pole-pairs	2

The experimental platform of the 48V IM drive system is shown in Figure 7. To get better observations of the experiment and the data results, the drive system adopted a variable-voltage variable-frequency (VVVF) control strategy rather than field orient control (FOC). Three different voltage/frequencies were set without load: 5V/5Hz, 30V/5Hz, and 30V/30Hz. Furthermore, three different kinds of compensations were adopted: no compensation, a common compensation scheme (taking T_d, T_{on}, and T_{off} into consideration, treating u_t as a constant, with no more other compensation near current zero), and the proposed compensation scheme. We observed a phase A current waveform, as shown in Figures 8, 9, and 10, using the POWERGUI/FFT tool module in SIMULINK, and analyzed the current waveform, thereby obtaining the corresponding current total harmonic distortion (THD), as shown in Table 2.

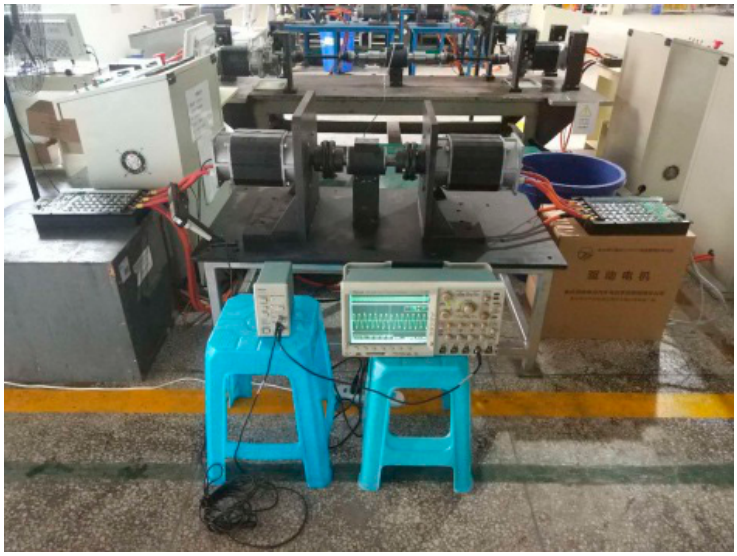

Figure 7. Experiment platform of the 48V IM drive system.

From the corresponding current waveform and THD analyses shown in Figure 8, we can see that both the common compensation method and the proposed compensation scheme can compensate for the nonlinear characteristics well under 5V/5Hz, and that the corresponding current THD for i_A are 19.33%, 15.33%, and 13.74% respectively. Due to the low current for this condition, the common compensation method treating u_t as a constant would not cause significant errors in compensation.

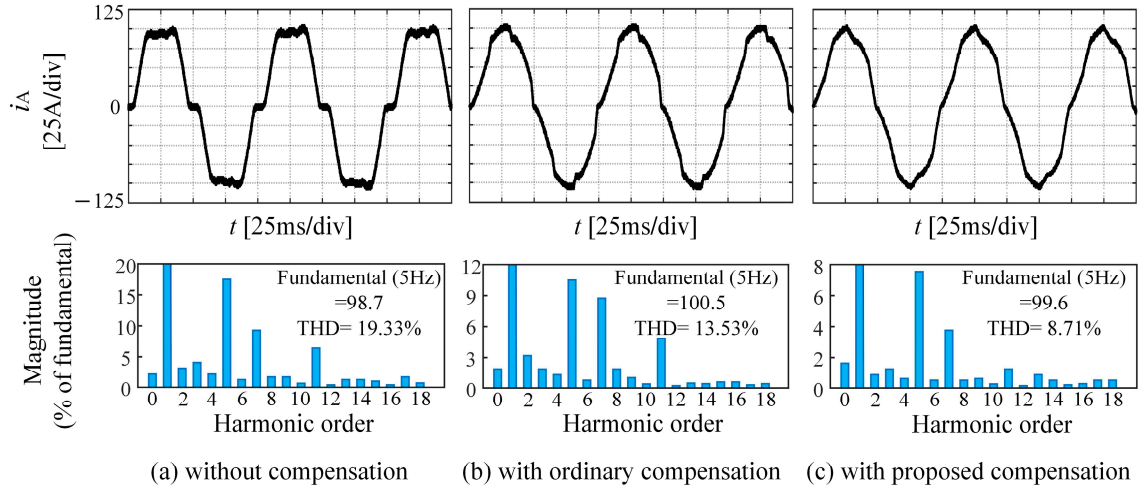

Figure 8. Experimental current waveform for phase A at a set 5V/5Hz voltage.

At a given voltage of 30V/5Hz conditions, the current increases, and the voltage drop across power devices changes. Therefore, the proposed synthetic compensation scheme has a better compensation effect than the common compensation method. As shown in Figure 9 and Table 2, the proposed compensation scheme can limit the current THD to 7.62%, while the current THD under the common compensation method reached 10.84%.

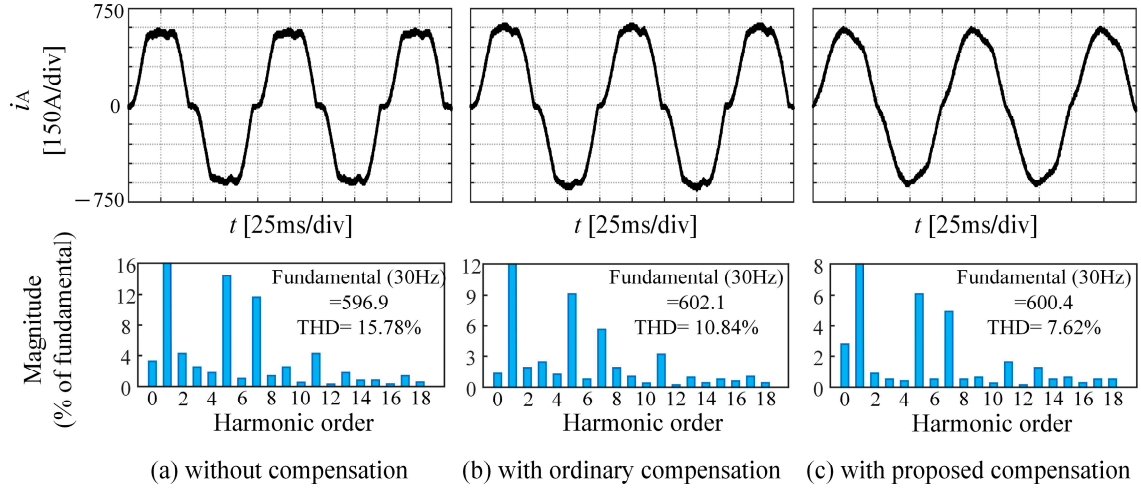

Figure 9. Experimental current waveform for phase A at 30V/5Hz.

Under the condition that of voltage = 30V/30Hz, the current also increases, and the forward voltage drop for devices changes. Therefore, it can no longer be regarded as a constant value in compensation calculations; to do so would cause the problem of inaccurate compensation. As shown in Figure 10 and Table 2, the common compensation method cannot effectively compensate for the nonlinear characteristics of the inverter because the current THD only decreases by 2.25%, compared with the uncompensated current THD (6.62%). By contrast, the proposed compensation scheme can significantly improve the current waveform quality. The current THD is 2.82%, which decreases by 3.80% compared with the uncompensated current THD, and 1.55% compared with the common compensation method. This means the proposed compensation scheme can achieve the ideal compensation effect.

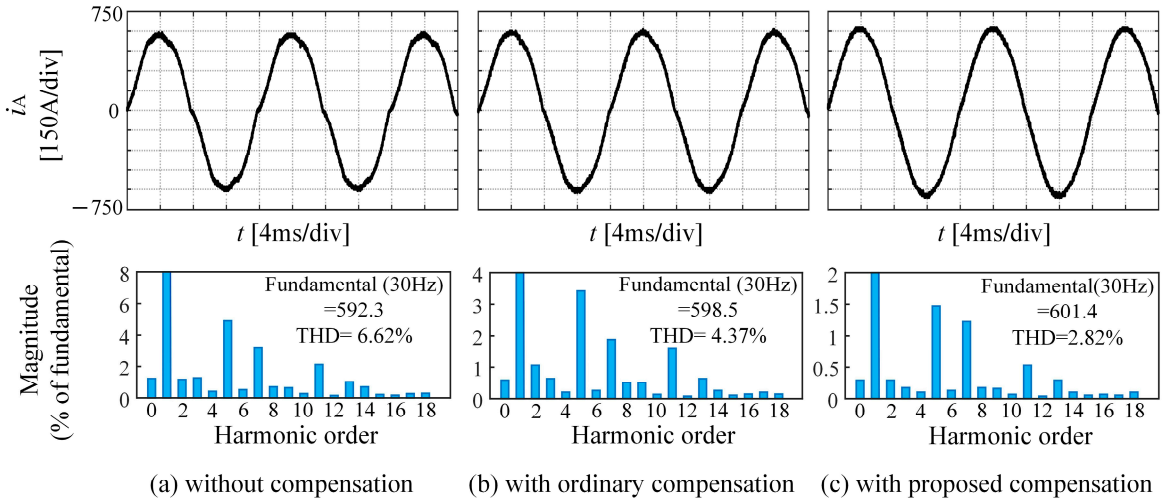

Figure 10. Experimental current waveform for phase A at 30V/30Hz.

At the same time, it can be seen from Figures 8c, 9c, and 10c that the currents have the tendency to cross through the zero in advance near the zero due to the ACCZ compensation, which effectively inhibits the effect of zero current clamping, and avoids the complex detection required for current polarities near zero.

Table 2. THD of the current waveforms.

Voltage set and compensation kind	THD
5V/5Hz and no compensation	19.33%
5V/5Hz and common compensation	13.53%
5V/5Hz and proposed compensation	12.71%
30V/5Hz and no compensation	15.78%
30V/5Hz and common compensation	10.84%
30V/5Hz and proposed compensation	7.62%
30V/30Hz and no compensation	6.62%
30V/30Hz and common compensation	4.37%
30V/30Hz and proposed compensation	2.82%

5. Conclusion

This paper analyzes the influence of nonlinear characteristics on the VSI for low-voltage EVs. Firstly, the output voltage model, which takes the conducting property of the MOSFET into consideration, was created. Next, an ACCZ compensation was also introduced for compensation when the current is near zero. Moreover, a compensation scheme based on a combination of the output voltage model and ACCZ is proposed. Finally, the proposed compensation scheme is verified on a 48V IM drive system experiment platform. From the experiment results, we observed that the phase current waveforms under the proposed compensation scheme had lower THD than those under the common compensation method with different voltage sets. The currents also had the tendency to cross through the zero in advance near the zero. The main conclusions of this paper may be summarized as follows:

- Compensation according to the VSI output voltage model with consideration of the conducting properties of MOSFET has a better effect than the common compensation method.
- ACCZ compensation not only avoids the complicated calculations required for current polarity, but also effectively inhibits the current waveform distortion near current zero.

- The proposed compensation scheme based on the combination of the output voltage model and ACCZ is suitable for nonlinear characteristics compensation for VSIs for low-voltage, delta-connected IMs.

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