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Hybrid DC Converter with Current Sharing and Low Freewheeling Current Loss

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Abstract: A new hybrid high-frequency link pulse-width modulation (PWM) converter using voltage balance capacitor and current balance magnetic coupling is proposed to realize low freewheeling current loss and wide load range of soft switching operation. Series-connected H-bridge converter is adopted for high voltage applications. In addition, a voltage balance capacitor and a current balance magnetic coupling core are employed for achieving voltage and current balance. To extend zero-voltage switching (ZVS) range of switches at lagging-leg of phase-shift PWM converter, soft switching LLC converter is linked to the lagging-leg of phase-shift PWM converter. Therefore, the wide ZVS load operation is realized in the presented hybrid converter. The other high freewheeling current disadvantage in conventional phase-shift PWM converter is improved by a snubber circuit used on low-voltage side. Thus, the primary current during the freewheeling state is decreased and close to zero. In addition, the conduction losses on primary-side components of studied converter are reduced. The secondary-sides of phase-shift PWM converter and LLC resonant converter are series-connected to achieve power transfer between input and output sides. Experimental results using a laboratory prototype are provided to demonstrate the effectiveness of the studied circuit and control algorithm.

Keywords: dc/dc converters; soft switching; hybrid converter; PWM

1. Introduction

Medium voltage high-frequency link power converters have been presented and developed for boat electric power applications [1], industry power units [2], dc microgrids [3–5] and dc traction vehicles [6,7] to reduce the environmental impacts and global warming issue. To deal the medium voltage input such as 750 V, power switches, 1200 V insulated gate bipolar transistor (IGBT) or silicon carbide (SiC), can be adopted in conventional pulse-width modulation (PWM) converters to achieve power transfer or energy conversion. The drawback of IGBT power devices is low switching frequency operation and high turn-off switching loss. The disadvantage of the SiC power devices is their high cost. MOSFET power devices have the advantages of low cost and high performance capabilities to realize and develop modern power converters. Three-level PWM converters [8–10] can be used for high voltage input applications by using low voltage stress power switches. Full bridge converters are widely adopted to accomplish high power output. Pulse-width modulation with phase shift technique can improve power devices to be turned on under soft switching condition. However, the main weaknesses of phase-shift PWM converters are high freewheeling current and switching loss under low load condition. In [11], the snubber circuit is used on the output-side in order to lessen voltage overshoots on the rectifier diodes and also decrease the freewheeling current at the commutation state. To improve the switching loss of power switches at lagging-leg of phase-shift PWM converter under low load condition, an auxiliary circuit connected to the lagging-leg has been used in [12]. To achieve high efficiency PWM converter, phase-shift PWM converters with a resonant circuit

connected to lagging-leg have been studied and developed in [13,14] to extend the soft switching range. For increasing power rating and circuit efficiency, the modular converter with series or parallel connection of several low power rating circuits has been studied and presented in [15]. The main challenge of modular converter is current balancing issue on each modular. Several current control approaches have been discussed in [16,17] to accomplish the current balance for each modular.

A hybrid PWM converter is studied and presented to achieve the advantages of low freewheeling current loss, the balanced current and voltage on two circuit modules and low switching loss on power switches. Two series-connected circuit modules are adopted to reduce the voltage stress on active devices and current stress on rectifier diodes. A flying capacitor is adopted on the primary-side to achieve voltage balance of input split capacitors. *LLC* converters sharing the lagging-leg switches of phase-shift PWM converters are used in the presented circuit to realize wide load range of soft switching operation. Two magnetic current balancing components are adopted on phase-shift PWM converters and *LLC* converters to achieve current sharing between two circuit modules. To reduce the high circulating current problem of conventional phase-shift PWM converters, a passive snubber is connected to the secondary-side rectified terminal. The structure and operation principle of the converter are discussed in Sections 2 and 3. In Sections 4 and 5, the circuit analysis and experiments with 1.68 kW prototype are provided. Finally, a conclusion of the studied converter is given in Section 6.

2. Circuit Diagram

In medium input voltage applications, the phase-shift PWM circuit topologies are widely used for medium and high-power converters. However, the conventional phase-shift PWM converter has the drawbacks of hard switching problem of power switches at the lagging-leg and high freewheeling current problem at the commutation state. For high voltage applications, three-level PWM dc converters or cascade converters shown in Figure 1 have been proposed to reduce voltage stress of active switches using high frequency power MOSFETs. The advantages of the cascade converters are less current rating of active switches compared to three-level converters and possible modular operation to extend input voltage range. However, the current sharing and input voltages balance are main problems of cascade full bridge converter. The circuit schematic in Figure 2a can overcome the problems of input voltage and current balance issues using a balance capacitor (highlighted in blue) between two circuit modules and a magnetic coupling element on primary-side (highlighted in red)). For extending the soft switching operation range at lagging-leg switches, *LLC* converter (remark in purple) and phase-shift PWM converter share the same lagging-leg switches shown in Figure 2b. Since a *LLC* converter has inductive input impedance characteristics, the wide soft switching operation of lagging-leg switches can be realized in the presented circuit and the weaknesses of conventional phase-shift PWM converters are overcome. Two phase-shift PWM and two *LLC* circuits are used on the input-side and two full-wave diode-rectifiers are adopted on the output-side. PWM scheme is adopted to control two full bridge converters. The magnetic coupling component MC1 is adopted to achieve current balance of i_{p1} and i_{p2} . If the currents i_{p1} and i_{p2} are balanced, the induced voltages on primary and secondary sides of MC1 are zero. If $|i_{p1}| > |i_{p2}|$, the induced voltages $V_{MC1,1}$ and $V_{MC1,2}$ decrease and increase respectively so that $|i_{p1}|$ and $|i_{p2}|$ will be decreased and increased respectively. After $i_{p1} = i_{p2}$, the induced voltages $V_{MC1,1} = V_{MC1,2} = 0$. A voltage balance capacitor C_b is connected between two full bridge circuits. Since S_1, S_2, S_5 and S_6 have the same duty cycle ($d = 0.5$), one can obtain $V_{Cb} = V_{C1} = V_{C2} = V_{in}/2$. Two full bridge circuits are series connection on primary-sides and parallel connection on secondary-sides with a single transformer T_1 to reduce the current rating on primary-side of phase-shift PWM circuits. Passive snubber circuit, C_p, D_{p1} and D_{p2} , is used to decrease i_{p1} and i_{p2} to zero at the commutation interval. Then, the high freewheeling current issue in conventional phase-shift PWM converter is eliminated. Since the switching frequency of *LLC* converters is close to series resonant frequency, the lagging-leg switches S_3, S_4, S_7 and S_8 are turned on at ZVS operation. At the active states (v_{AB} and $v_{DE} = +V_{in}/2$ or $-V_{in}/2$) of full bridge circuits, both PWM converters and *LLC* converters can achieve

power transfer between V_{in} and V_o . On the other hand, only LLC resonant circuits achieve power transfer at the commutation state (v_{AB} and $v_{DE} = 0$ V).

Figure 1. Circuit configuration of three-level converters (a) diode clamped three-level converter (b) cascade bridge three-level converter with primary-series and secondary-parallel.

Figure 2. Cont.

Figure 2. Proposed converter (a) circuit configuration with current balance (b) circuit diagram with low freewheeling current, current and voltage balance and wide ZVS operation.

3. Principles of Operation

In the proposed circuit topology, each active device has $T_{sw}/2$ turn-on time. The switching signals S_1 – S_4 and S_5 – S_8 are identical. The power components in the first and second circuits are identical to simplify the circuit analysis. In the proposed converter, $n_{T1,p1} = n_{T1,p2}$ (primary turns of T_1), $n_{T2,p1} = n_{T2,p2}$ (primary turns of T_2), $C_{S1} = \dots = C_{S8} = C_{oss}$, $L_1 = L_2 = L_{lk1}$, $L_{r1} = L_{r2} = L_r$, and $C_{r1} = C_{r2} = C_r$. Figure 3 gives the PWM waveforms of the studied circuit and the related step circuits during one-half of switching period are provided in Figure 4.

Figure 3. PWM waveforms of the proposed circuit.

(a)

(b)

(c)

(d)

Figure 4. Cont.

Figure 4. The related step circuits during one-half of switching period (a) step 1 circuit (b) step 2 circuit (c) step 3 circuit (d) step 4 circuit (e) step 5 circuit (f) step 6 circuit (g) step 7 circuit.

Step 1 $[t_0, t_1]$: Before time t_0 , S_1 , S_4 , S_5 and S_8 conduct. At time t_0 , active devices S_5 and S_1 are turned off. i_{p1} and i_{p2} will charge C_{S1} and C_{S5} and discharge C_{S2} and C_{S6} . If the energy on L_o , L_1 and L_2 is larger than C_{S1} , C_{S2} , C_{S5} and C_{S6} , then C_{S6} and C_{S2} are discharged and the zero-voltage switching of S_6 and S_2 can be realized at t_1 . Therefore, the time duration in this step is calculated:

$$\Delta t_{01} = \frac{C_{oss} V_{in}}{i_{p1}(t_0)} \approx \frac{C_{oss} V_{in}}{i_{Lo, \max} / n_1} \quad (1)$$

where $n_1 = n_{T1,p1}/n_{T1,s}$ turns ratio of transformer T_1 . Since $i_{Lr1} < i_{Lm1,T2}$ and $i_{Lr2} < i_{Lm2,T2}$, the secondary-side rectifier diodes D_4 conducts.

Step 2 $[t_1, t_2]$: The voltages $v_{CS2} = v_{CS6} = 0$ at t_1 . The body diodes of switches S_6 and S_2 conduct due to $i_{p1}(t_1) > 0$ and $i_{p2}(t_1) > 0$. Therefore, the ZVS turn-on operation of S_6 and S_2 are realized.

In step 2, $V_{Cb} = V_{C2}$, $v_{AB} = v_{DE} = v_{BC} = v_{EF} = 0$, i_{p1} and i_{p2} decrease and D_{p1} conducts. Therefore, the primary voltages of T_1 is equal to $n_1 v_{Cp}$ and the voltage on L_o is equal to $v_{Cp} - V_{o1}$. Since $v_{Lo} < 0$, i_{Lo} decreases in step 2. The time interval in step 2 is calculated in Equation (2):

$$\Delta t_{12} \approx \frac{L_{lk1} i_{Lo, \max}}{2n_1^2 v_{Cp}} \quad (2)$$

Since the primary voltages of T_1 are positive, the primary currents i_{p1} and i_{p2} will decrease to zero during the circulating state. LLC resonant circuits are operated at resonant frequency ($f_{sw} \approx f_r$). The rectifier diodes D_4 is conducting to deliver power to output V_{o2} .

Step 3 [t_2, t_3]: The secondary-side diode current i_{D1} decreases to zero at time t_2 . The currents $i_{p1} = i_{Lm1}$ and $i_{p2} = i_{Lm2}$ so that the wheeling currents are reduced in this step. The inductor current i_{Lo} flows through passive components D_{p1} and C_{p1} and i_{Lo} decreases due to $v_{Cp} < V_{o1}$. LLC resonant converter achieves energy transfer through T_2 and D_4 .

Step 4 [t_3, t_4]: Active devices S_8 and S_4 are turned off at t_3 . $i_{Lr1} < 0$ and $i_{Lr2} < 0$ so that C_{S7} and C_{S3} are discharged. At time t_4 , C_{oss3} is discharged to zero. Due to LLC resonant converters operated at the series resonant frequency, the ZVS turn-on operation of S_7 and S_3 are realized.

Step 5 [$t_4 \sim t_5$]: v_{Cs3} and v_{Cs7} decrease to zero voltage at t_4 . Since $i_{S7}(t_4)$ and $i_{S3}(t_4)$ are negative, the antiparallel diodes of S_7 and S_3 are forward biased. Therefore, the ZVS operation of S_7 and S_3 is achieved after time t_4 . At step 5, the ac side voltages $v_{Cb} = V_{C2}$, $v_{AB} = v_{DE} \approx -V_{in}/2$, $v_{BC} = v_{EF} \approx V_{in}/4$ and D_2 and D_3 conduct. Due to $|n_1 i_{p1} + n_1 i_{p2}| < i_{Lo}$, D_{p1} still conducts, $v_{L1} = v_{L2} = n_1 v_{Cp} - V_{in}/2 < 0$, and $v_{Lo} = v_{Cc} - V_o < 0$. Thus, i_{Lo} decreases and i_{p1} and i_{p2} decrease. LLC resonant converters are resonant with input voltage $V_{in}/2$ so that i_{Lr1} and i_{Lr2} increase. At t_5 , $|n_1 i_{p1} + n_1 i_{p2}| = i_{Lo}$ so that D_{p1} becomes reverse biased and D_{p2} becomes forward biased. The time interval between t_4 and t_5 can be calculated as:

$$\Delta t_{45} = t_5 - t_4 \approx \frac{L_{lk1} I_{Lo}}{2n_1 (V_{in}/2 - n_1 v_{Cp})} \quad (3)$$

No power is transferred in step 5 and the duty cycle loss in step 5 is calculated in (4):

$$d_{5, \text{loss}} = \Delta t_{45} / T_{sw} \approx \frac{L_{lk1} I_{Lo} f_{sw}}{2n_1 (V_{in}/2 - n_1 v_{Cp})} \quad (4)$$

Step 6 [t_5, t_6]: This step starts at time t_5 when D_{p1} (D_{p2}) are reverse (forward) biased. Since D_{p2} conducts, it can obtain $v_{Lo} = v_{Cp2}$ and i_{Lo} increases. L_1 and $C_p/(n_1)^2$ are resonant in step 6. In order to ensure D_{p2} becomes reverse biased before step 7, the half resonant period by L_1 and $C_p/(n_1)^2$ must be less than $d_{\text{eff}, \min} T_{sw}$ (the minimum turn-on time). In step 6, $v_{T1, p1} = v_{T1, p2} = -(v_{Cp} + V_{o1})$ and $i_{p1} = i_{p2} = -(i_{Lo} + i_{Cp})/(2n_1)$.

Step 7 [t_6, t_7]: At time t_6 , $i_{Dp2} = 0$. In this step, passive components D_{p1} and D_{p2} are reverse biased, $v_{Lo} = V_{in}/(2n_1) - V_{o1}$ and i_{Lo} increases. S_6 and S_2 turn off at t_7 and the first half switching cycle is ended.

4. Circuit Analysis

In the proposed converter, phase-shift PWM converter realize power transfer to V_{o1} in steps 5–7 in the one-half of switching period and LLC resonant converter achieve power transfer to V_{o2} in every switching cycle. Since the switching frequency of LLC converter is fixed and close to series resonant frequency, the output voltage V_{o2} is unregulated. The ZVS turn-on of S_3 , S_4 , S_7 and S_8 can be achieved due to LLC converter operation with the following condition:

$$i_{Lm1, T2, \max} = i_{Lm2, T2, \max} \geq \frac{V_{in}}{2} \sqrt{\frac{C_{oss}}{L_r}} \quad (5)$$

where $i_{Lm1,T2,max}$ and $i_{Lm2,T2,max}$ are the maximum magnetizing currents on $L_{m1,T2}$ and $L_{m2,T2}$, respectively. According to the switching frequency, transformer turns ratio, load voltage and the magnetizing inductances, $i_{Lm1,max}$ and $i_{Lm2,max}$ are obtained in Equation (6):

$$i_{Lm1,T2,max} = i_{Lm2,T2,max} = \frac{\Delta i_{Lm1}}{2} \approx \frac{n_2 V_{o2} T_{sw}}{4L_m} \quad (6)$$

The dead time between S_3 and S_4 is calculated in Equation (7):

$$t_d > \frac{C_{oss} V_{in}}{i_{Lm1,T2,max}} = \frac{4L_m C_{oss} V_{in}}{n_2 V_{o2} T_{sw}} \quad (7)$$

From the given dead time t_d , the maximum magnetizing inductances $L_{m1,T2} = L_{m2,T2} = L_{m,T2}$ are expressed in Equation (8):

$$L_{m,T2} \leq \frac{n_2 V_{o2} T_{sw} t_d}{4C_{oss} V_{in}} \quad (8)$$

Since the LLC converter has unity voltage gain at resonant frequency, the output voltage V_{o2} is calculated in Equation (9):

$$V_{o2} = \frac{V_{in}}{4n_2} \quad (9)$$

The zero-voltage switching condition of S_1 , S_2 , S_5 and S_6 is expressed in Equation (10):

$$L_{lk1} i_{p1}^2(t_0) + \frac{n_1^2 L_o i_o^2(t_0)}{4} \geq \frac{C_{oss} V_{in}^2}{2} \quad (10)$$

According to flux balance on leakage inductance on the secondary-side, the average voltage on C_p is obtained as $V_{Cp} \approx V_{in}/(2n_1) - V_{o1}$. The output voltage V_{o1} on steady state is calculated in Equation (11) by applying flux balance on L_o :

$$V_{o1} \approx \frac{V_{in}}{4n_1(1-d_{eff})} \quad (11)$$

where the effective duty cycle $d_{eff} = d - d_{5,loss}$ and d is duty ratio of phase-shift PWM converter. Thus, the load voltage V_o is expressed in Equation (12) and the dc voltage gain is calculated in Equation (13):

$$V_o = V_{o1} + V_{o2} = \frac{V_{in}}{4(1-d_{eff})n_1} + \frac{V_{in}}{4n_2} \quad (12)$$

$$G_{dc} = \frac{V_o}{V_{in}} = \frac{1}{4n_1(1-d_{eff})} + \frac{1}{4n_2} = \frac{n_2 + n_1(1-d_{eff})}{4n_1n_2(1-d_{eff})} \quad (13)$$

The ripple current Δi_{L_o} is expressed in Equation (14):

$$\Delta i_{L_o} \approx \frac{(V_{o1} - V_{Cp})(0.5 - d_{eff})T_{sw}}{L_o} = \frac{d_{eff}(1-2d_{eff})V_{in}T_{sw}}{4n_1(1-d_{eff})L_o} \quad (14)$$

The minimum output inductance L_o is derived in Equation (15) under the given ripple current Δi_{L_o} :

$$L_{o,min} \geq \frac{d_{eff}(1-2d_{eff})V_{in}T_{sw}}{4n_1(1-d_{eff})\Delta i_{L_o}} \quad (15)$$

The ripple currents on the magnetizing inductors of T_1 are calculated in Equation (16):

$$\Delta i_{Lm1,T1} = \Delta i_{Lm2,T1} \approx \frac{V_{in}d_{eff}T_{sw}}{2L_{m,T1}} \quad (16)$$

The theoretical voltage stress of $S_1 \sim S_8$ is $V_{in}/2$. The voltage stress of D_1 and D_2 are equal to V_{in}/n_1 . The voltage stresses of D_3 and D_4 are equal to $V_{in}/(2n_2)$. The approximate voltage ratings of diodes D_{p1} and D_{p2} are $V_{in}/[4n_1(1 - d_{eff})]$. The approximate average currents of D_1 and D_2 are equal to dI_o and the average currents of D_3 and D_4 are $(0.5 - d)I_o$. The inductor ratio $L_{m1,T2}/L_{r1}$ of LLC converter is selected as 8. From the obtained $L_{m1,T2}$, the L_{r1} and L_{r2} are equal to $L_{m1,T2}/8$ and C_{r1} and C_{r2} are equal to $1/[4\pi^2 f_{sw}^2 L_{r1}]$.

5. Design Considerations and Test Results

The design procedures and the test results are provided in this section with the following electric specifications: $V_{in} = 750\text{--}800$ V, $V_o = 48$ V, $I_o = 35$ A and f_r (resonant frequency of LLC converter) = f_{sw} (switching frequency) = 60 kHz. The assumed load voltages $V_{o1} = 28$ V and $V_{o2} = 20$ V. Since $f_{sw} = f_r$, the voltage gain of LLC resonant circuit is equal to unity. Therefore, n_2 of transformer T_2 can be calculated and expressed in Equation (17):

$$n_2 = \frac{V_{in,max}}{4V_{o2}} = 10 \quad (17)$$

G20N50C power MOSFETs with 500 V/20 A voltage/current stress and $C_{oss} = 300$ pF are used for power devices $S_1 \sim S_8$. The maximum magnetizing inductance of T_2 can be calculated as:

$$L_{m,T2} \leq \frac{n_2 V_{o2} T_{sw} t_d}{4C_{oss} V_{in,min}} \approx 1.8 \text{ mH} \quad (18)$$

where $t_d = 0.5$ μ s. The magnetic core EER42 is used to implement transformer T_2 with the magnetizing inductances $L_{m1,T2} = L_{m2,T2} = 0.664$ mH, the primary turns $n_{T2,p1} = n_{T2,p2} = 30$ and the secondary turns $n_{T2,s} = 3$. Therefore, the series resonant inductances $L_{r1} = L_{r2} = L_{m1,T2}/8 = 83$ μ H and the series resonant capacitances C_{r1} and C_{r2} are expressed as $C_{r1} = C_{r2} \approx 1/[4\pi^2 f_{sw}^2 L_{r1}] \approx 85$ nF. From the assumed $d_{eff,max} = 0.3$, the turns ratio n_1 of transformer T_1 is calculated as:

$$n_1 < \frac{V_{in,min}}{4V_{o1}(1 - d_{eff,max})} \approx 9.5 \quad (19)$$

The magnetic core EER42 is used to design transformer T_1 with the following parameters: $L_{m1,T1} = L_{m2,T1} = 4$ mH, $n_{T1,p1} = n_{T1,p2} = 57$ and $n_{T1,s} = 6$. The duty cycle loss $d_{5,loss}$ is assumed 0.01. Therefore, the necessary inductances L_1 and L_2 of full bridge converter are calculated in Equation (20):

$$L_1 = L_2 = L_{lk1} = \frac{2d_{5,loss}n_1(V_{in,min}/2 - n_1v_{Cp})}{I_{Lo,rated}f_{sw}} \approx 24 \text{ } \mu\text{H} \quad (20)$$

If the ripple current ratio $\Delta i_{Lo}/I_{o,rated}$ is assumed 0.2, then the minimum output inductance L_o is obtained in Equation (21):

$$L_{o,min} \geq \frac{d_{eff,max}(1 - 2d_{eff,max})V_{in,min}T_{sw}}{4n_1(1 - d_{eff,max})\Delta i_{Lo}} \approx 8 \text{ } \mu\text{H} \quad (21)$$

The inductance $L_o = 10$ μ H is used in the prototype circuit. MPR40100PT with $V_{RRM} = 100$ V/ $I_F = 40$ A are adopted for the secondary-side diodes $D_1\text{--}D_4$, D_{p1} and D_{p2} . The other capacitors $C_1 = C_2 = 180$ μ F/450 V, $C_b = 2$ μ F and $C_{o1} = C_{o2} = 2000$ μ F. The magnetic cores EER 42 are used for current balance magnetic cores MC1 and MC2 with $n_p = n_s = 24$.

Figure 5 gives the test results of switching waveforms of S_1 , S_4 , S_5 and S_8 at 750 V and 800 V input cases under full load. The switching signals S_1 (S_4) and S_5 (S_8) are identical and the PWM signals of S_4 (S_8) are lagging to the PWM signals of S_1 (S_5). Figure 6 shows the experimental voltages v_{AB} and v_{DE} and currents i_{p1} and i_{p2} of the phase-shift PWM converters under 20% and 100% loads.

The primary-side currents i_{Lp1} and i_{Lp2} are well balanced. The duty cycle on v_{AB} and v_{DE} at 100% load is larger than the duty cycle at 20% load due to $d_{5,loss}$ in step 5 is related to I_o . One can observe that the freewheeling currents of i_{p1} and i_{p2} are improved and close to zero. Figure 7 provides the experimental waveforms of the LLC resonant circuits at 20% and 100% loads. The inductors currents i_{Lr1} and i_{Lr2} are well balanced. Since $f_{sw} = f_r$, S_3 , S_4 , S_7 and S_8 are turned on at ZVS operation over whole load range. Figure 8 provides the test waveforms of capacitor voltages at primary-side under the full load with 800 V input. The capacitor voltages V_{C1} , V_{C2} and V_{Cb} are all balanced. Figure 9a,b show the measured secondary-side currents of phase-shift PWM converter at 100% load. Passive snubber diode D_{p1} is forward biased when the ac side voltages v_{AB} and v_{DE} are zero voltage (the circulating state) and diode D_{p2} is forward biased when diode current i_{D1} or i_{D2} is greater than inductor current i_{Lo} . Figure 9c provides the test waveforms of the output currents of LLC resonant converter at 100% load. The measured input current I_{in} , load current I_o and load voltage V_o at 800 V input and 100% load are provided in Figure 9d. Figure 10a,b illustrate the experimental voltage and current of S_1 at 20% and 100% loads. One can observe that S_1 is turned on under zero voltage for both 20% and 100% loads. Likewise, the measured waveforms of S_4 at lagging-leg at 20% and 100% loads are provided in Figure 10c,d. S_4 is also turned on under zero voltage for both 20% and 100% loads. The other switches at leading-leg and lagging-leg have the same turn-on characteristics as S_1 and S_4 , respectively. The measured results shown in Figures 5–10 of the proposed hybrid converter and theoretical waveform analysis are agreed each other. Figure 11a provides the picture of a laboratory prototype. Figure 11b gives the measured efficiencies of the proposed converter and the full bridge LLC converter in reference (Lin, 2018) at 750 V input and different load conditions. The nominal rated power of the studied circuit is 1680 W and the measured circuit efficiency at 750 V input is 93.1%.

Figure 5. PWM waveforms of $S_{1,gs}$, $S_{4,gs}$, $S_{5,gs}$ and $S_{8,gs}$ at rated power under (a) $V_{in} = 750$ V (b) $V_{in} = 800$ V.

(a)

(b)

Figure 6. Measured primary-side waveforms of phase-shift PWM converter under (a) 20% load (b) 100% load.

(a)

(b)

Figure 7. Measured primary-side waveforms of LLC resonant converters under (a) 20% load (b) 100% load.

Figure 8. Measured input-side capacitor voltages at 100% load and 800 V input.

(a)

(b)

(c)

Figure 9. Cont.

Figure 9. Test results of the output-side currents at 100% load (a) i_{D1} , i_{D2} , i_{L0} and i_{Cp} (b) i_{L0} , i_{FB} , i_{Dp1} and i_{Dp2} (c) i_{D3} , i_{D4} and i_{LLC} (d) input current I_{in} , load current I_o and load voltage V_o .

Figure 10. Cont.

Figure 10. Test waveforms of the active devices (a) S_1 (leading-leg switch) under 20% load and 800 V input (b) S_1 (leading-leg switch) under rated power and 800 V input (c) S_4 (lagging-leg switch) under 20% load and 800 V input (d) S_4 (lagging-leg switch) under rated power and 800 V input.

(a)

(b)

Figure 11. The picture and efficiency of the presented circuit (a) prototype circuit (b) circuit efficiency at 750 V input.

6. Conclusions

This paper presents a PWM circuit topology to achieve a low voltage rating on active devices, wide soft switching load range and low freewheeling current compared to the conventional phase-shift PWM converter. Two series-connected phase-shift PWM circuits are used at input-side so that the voltage rating of active devices is reduced. One balance capacitor is used to accomplish voltage balance issue for two input split capacitors. LLC circuit shares the lagging-leg switches of phase-shift PWM circuit so that the ZVS operation capability of lagging-leg switches is improved. Magnetic coupling elements are used to achieve current-sharing issue between two phase-shift PWM circuits. Snubber

circuit is employed on the output-side of phase-shift PWM circuit to improve the freewheeling problem at the circulating state. The feasibility and performance of the presented circuit are verified by a laboratory prototype with 1.68 kW rated power.

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