

Article

A Family of High Voltage Gain Three-Level Step-Up Converters for Photovoltaic Module Integration Applications

Ahmad Alzahrani ^{1,*} , Pourya Shamsi ² and Mehdi Ferdowsi ²¹ Electrical Engineering Department, Najran University, Najran 66446, Saudi Arabia² Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO 65401, USA; Shamsi@mst.edu (P.S.); ferdowsi@mst.edu (M.F.)

* Correspondence: asalzahrani@nu.edu.sa

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Abstract: This paper proposes a family of step-up three-level DC-DC converter topologies suitable for photovoltaic panel integration applications. The proposed family is suitable to convert the 10–30 V from photovoltaic panels to a 150 V direct current distribution bus. The proposed family enhances the three-level topology in terms of the voltage gain, power density, and filtering requirements at the input level. The filtration is reduced by interleaving. The three-level boost converter's voltage gain is enhanced by utilizing several options such as switched capacitor cells, switched inductor cells, and flyback transformers or coupled inductors. The enhancement techniques are illustrated by providing the circuit diagram and a comparison of the voltage gain and the number of required components. An example converter of a hybrid three-level boost converter with a flyback transformer is presented to convert 20 V from a photovoltaic panel to a 400 V. The theory of operation and steady-state analysis are provided for the example converter operating in the continuous conduction mode. The converter is simulated to extract the power from three PVL-136 photovoltaic (PV) panels by applying a maximum power point tracking algorithm. The theory of operation and simulation are confirmed with an 80 W experimental prototype, which has an efficiency of around 95% at 40 W load power.

Keywords: three-level; PV; step-up; flyback; MPPT; P&O; high voltage gain

1. Introduction

Power electronics converters are essential devices in all electronic systems and become increasingly important in renewable energy power processing and integration into the electric grid. The increase in renewable energy installations motivates the search for efficient, reliable, and inexpensive power converters and stimulates new technologies that facilitate renewable energy integration. Photovoltaic (PV) technology is the fastest growing technology due to the cost reduction of manufacturing and government subsidies. The PV global capacity grew from 23 GW in 2009 to more than 600 GW in 2019 [1]. Several technical challenges associated with the integration of photovoltaic systems need to be addressed. The PV system's output power is dependent of solar irradiance and weather, which are both intermittent. The stochastic solar irradiance makes the PV output power stochastic and causes a stochastic maximum power point. Extracting the most out of a PV panel requires a maximum power point tracker (MPPT) [2–4]. The shading of a part of or a whole PV panel reduces the PV panel's output power and might damage the internal cells due to the appearance of hot spots [5–7]. The PV panel's output voltage is not sufficient for integration in

a DC distribution system, which has around 200 V to around 600 V. Connecting multiple PV panels in series raises the output voltage and power of the system [8]. Nevertheless, potential mismatches between panels lead to a decline in efficiency and output power. The parallel connection of solar modules increases the current, but the voltage is still as the one of a single panel, which necessitates a high voltage gain boost converter [9–11].

The ideal traditional boost converter can achieve high voltage gain at high duty cycles. In practice, achieving a high voltage gain from the traditional boost converter is unachievable due to the conduction losses and the nonidealities [12,13]. Moreover, using the traditional boost converter to operate in continuous conduction mode (CCM) at a high duty cycle requires a sizeable magnetic element and high voltage rating switching components [13–15]. The voltage gain could be enhanced by adding several traditional boost converters consecutively. An individual stage works at a low duty cycle, and the total voltage gain equals the product of the voltage gain of each stage. However, connecting two or more traditional boost converters implies processing the power twice or more, degrading the converter's performance and making the control design complicated [16,17].

Similarly, connecting several traditional boost converters in series helps share the power and makes the components' current rating lower. However, the voltage gain is not improved, and some of the switches become floating, which requires a particular gate driving circuitry. Utilizing the flyback transformer with the traditional boost converter improves the voltage gain, as the turns ratio contributes to the output voltage [18]. The flyback transformer is designed at the switching frequency, which minimizes the power density and increases the converter's volume and weight. The three levels were proposed to mitigate the voltage stress and increase the effective frequency. The required magnetic component in the three-level boost converter is smaller than the one of the traditional boost converter because it sees the effective frequency, which is double the switching frequency. Yet, the voltage gain still equals the gain of the traditional boost converter. The traditional isolated converters, such as the forward or the flyback, can be designed to have a large voltage gain by setting the turns ratio value. The input current of such converters is pulsating, which might require a considerable input filter [19,20].

A flying capacitor multilevel converter was proposed to provide high voltage gain and reduce voltage stress across semiconductor elements. Therefore, the magnetic part sees a large effective frequency and can be designed for high power density requirements [21–23]. The number of levels determines the effective frequency and the phase shift of the switching pattern. The switching devices in this converter are floating, and they require signal isolation, special gate drives, and an isolated feedback loop. Moreover, there is a minimum duty cycle for the converter to function correctly, restricting the converter to limited applications.

The voltage gain can be enhanced by employing coupled inductors as built-in or integrated, such as in [24–26]. The voltage gain depends on the turns ratio, and therefore, increasing the turns ratio increases the voltage gain. Nevertheless, voltage spikes appear across the controlled switches due to the leakage inductance, which necessitates an additional energy circulation circuit. Adding a magnetic element to the circuit increases the weight and minimizes the power density. The combination of switched-capacitor topologies with an interleaved boost converter increases the power density and achieves high voltage gain [27,28]. However, many switches are used, which requires a large number of gate drive and signal isolation circuits and necessitates complicated control schemes.

This paper introduces a group of step-up DC-DC converters based on multilevel converters with voltage boost techniques. The advantages of using this family include:

- high voltage gain at lower duty cycles and allowing integration with a high voltage DC link.
- higher effective frequency across the input inductor or the primary side of the integrated coupled inductors, which allows the design of a small magnetic component.
- higher frequency of the current ripples at the input level, making it easy to filter.

- suitability for maximum power point tracking because of the continuity of the input current and wide range of duty operation.
- the voltage stress across semiconductor elements is reduced, and the required storage element size is small.

Several choices to construct a multilevel converter with a high gain conversion ratio are discussed and compared. An example converter of the proposed family, a three-level converter with a flyback transformer, is investigated and tested to show the advantages of combining high voltage cells with the multilevel converters. The example converter is tested with a maximum power point tracking algorithm to extract the power from the PV panels.

The remainder of this paper is organized as follows: An overview of the multilevel boost converter, interleaving techniques, and voltage gain improvement techniques is presented in Section 2. Section 3 presents an example converter, which is a three-level boost converter with a flyback transformer. This section provides details about the theory of operation and the static voltage gain analysis. The design information and component selection for the example converter is given in Section 4. The simulation and experimental results are presented in Sections 5 and 6, respectively. Conclusions and future works are in Section 6.

2. Overview of the Presented Multilevel Boost Converters

2.1. The Effect of the Phases and Level Number on the Effective Frequency

Interleaved boost converters have an inductor in each phase, and the summation of inductor currents equals the input current. The current ripples of the input current have a higher frequency, usually equal to the product of the switching frequency and the number of phases. The inductor current ripples have the same frequency as the switching frequency, which is still equal to the traditional boost converter's voltage gain. Therefore, the magnetic element is designed with respect to the switching frequency. Thus, in order to minimize the size of the magnetic component, the converter must be designed to operate at a higher switching frequency, increasing the switching loss. There are techniques to increase the magnetic components' frequency with no need to increase switching frequency. A multilevel boost converter offers an effective frequency applied on the magnetic component multiple times higher than the switching frequency. The number of levels determines the multiplication factor, and increasing the number of levels in multilevel converters increases the frequency of the inductor currents' AC components. The frequency seen by the inductor in the three-level boost converter is twice the switching frequency. Figure 1a shows the switching pattern of the three-level boost converter, and Figure 1b shows a two-phase boost converter. Multiphase offers a reduction of the average inductor current, and multilevel offers an increase in the effective frequency. The two previous methods can be combined, as shown in Figure 1c. The combination reduces the magnetic storage requirement and allows the design of minimal magnetic components. This paper explores only the combination of the multilevel converters and voltage boosting cells.

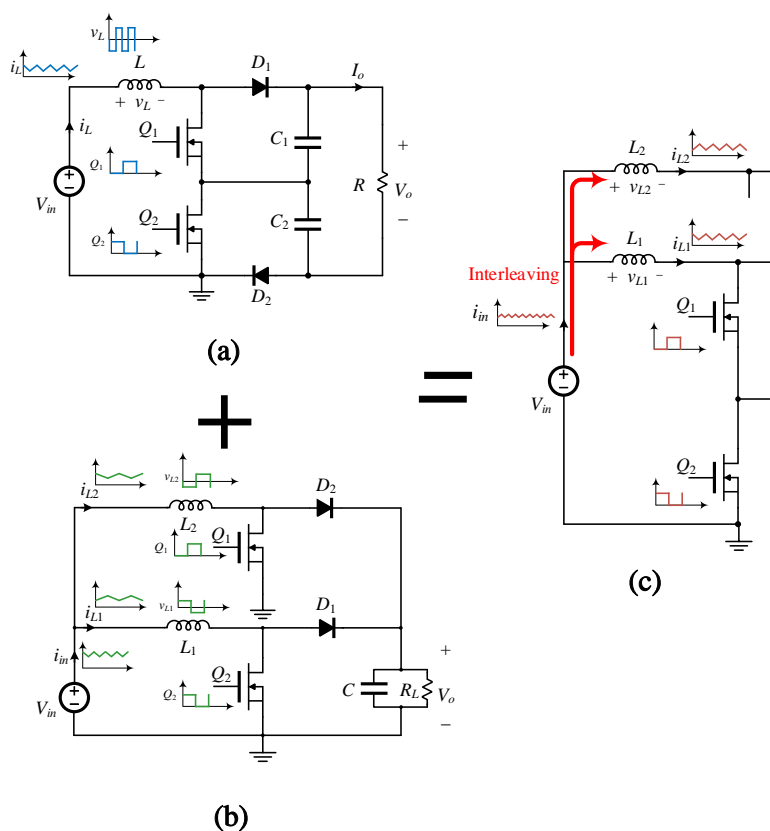


Figure 1. Illustration of an interleaved multilevel converter: (a) a three-level converter; (b) a two-phase interleaved boost converter; (c) an interleaved three-level boost converter. The AC components of the input have a higher frequency than the switching frequency.

2.2. High Voltage Gain Techniques

The multilevel boost converter family can be extended starting from a three-level boost converter, four-level boost converter, and n -level boost converter, as shown in Figure 2a–c, respectively. The effective frequency is $(n - 1)$ times the switching frequency. The voltage gain of the multilevel boost converter, regardless of the number of levels, is still equal to the traditional boost converter's voltage gain. This section provides several techniques to improve the voltage gain. Figures 3 and 4 show the converters capable of offering high voltage gain and that inherit the advantages that multilevel converters bring. The circuit in Figure 3a provides a high voltage gain employing the coupled inductor without isolation. The turns ratio of the coupled inductors impacts the voltage gain. The converter was previously introduced in [29]. It was tested to convert a 14 V input to a 42 V output, with an efficiency of up to 96%. The coupled inductor can be connected to a four-level boost converter, as illustrated in Figure 3d, and the frequency seen by the coupled inductors is thrice the switching frequency.

Switching inductor cells enhances the converter's voltage gain, as reported in the literature [30–32]. The inductor in the three-level or four-level boost converters can be replaced by a switched-inductor cell, as illustrated in Figure 3b,c,e,f. During ON states, in which all controlled switched are ON, the inductors will be connected in parallel and draw energy from the input source. During the OFF states, the inductors are connected in series and release their stored energy to the output. The main disadvantage of using switched-inductor cells is that placing a diode in a high current loop decreases the

converter's overall efficiency due to the forward conduction power loss, which might also require bulky heat dissipation components.

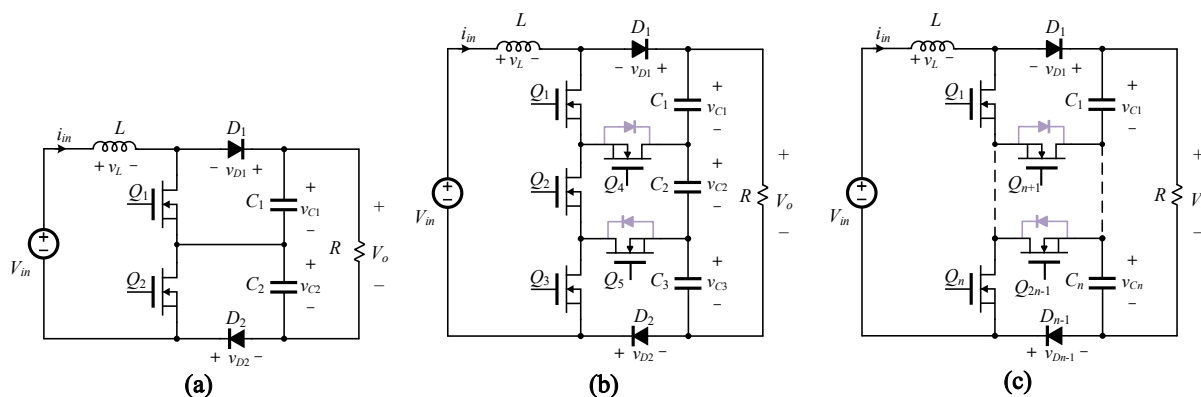


Figure 2. Illustration of multilevel step-up DC-DC converter topologies: (a) three-level boost converter; (b) four-level boost converter; (c) n -level boost converters.

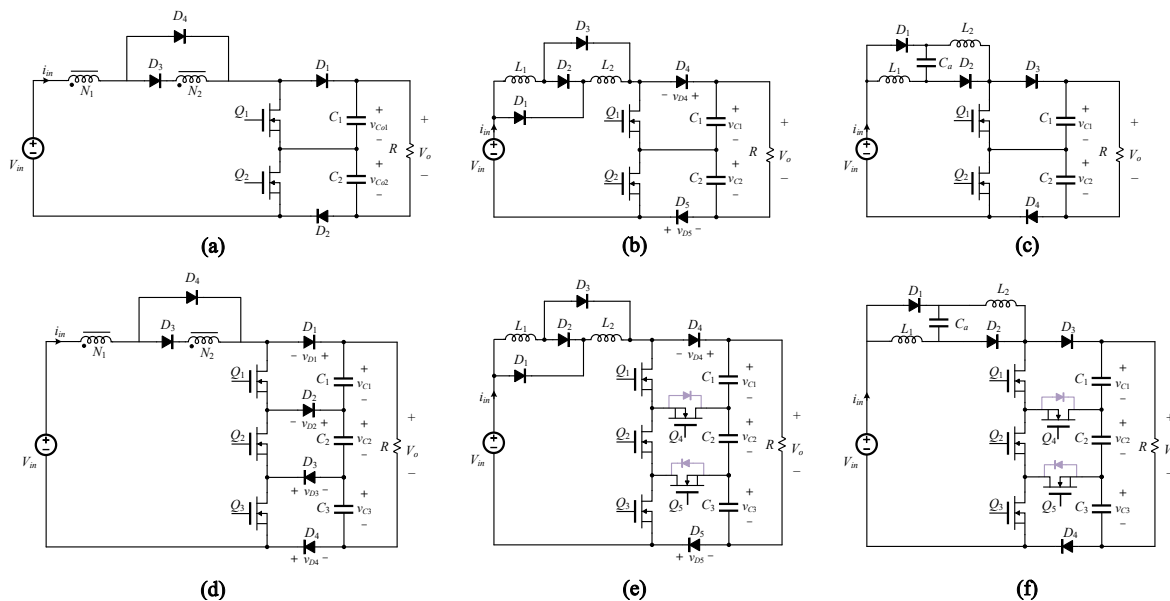


Figure 3. Hybridization of the high voltage cells with multilevel boost converters: (a) three-level boost with coupled inductors; (b) three-level boost converter with switched-inductor Cell A; (c) three-level boost converter with switched-inductor Cell B; (d) four-level boost converter with coupled inductors; (e) four-level boost converter with switched-inductor Cell A; (f) four-level boost converter with switched-inductor Cell B.

The flyback transformer is used in this paper with the three-level boost converter, as shown in Figure 4a, and can also be connected to the four-level boost converter, as illustrated in Figure 4b. The advantage of using flyback transformers over previously mentioned techniques is that there are no lossy elements in the high current loop. Throughout the paper, the three-level converter with flyback is analyzed, simulated, and experimentally tested. Table 1 summarizes and compares the gain and the number of components of the high voltage gain three-level converters shown in Figure 4a–c.

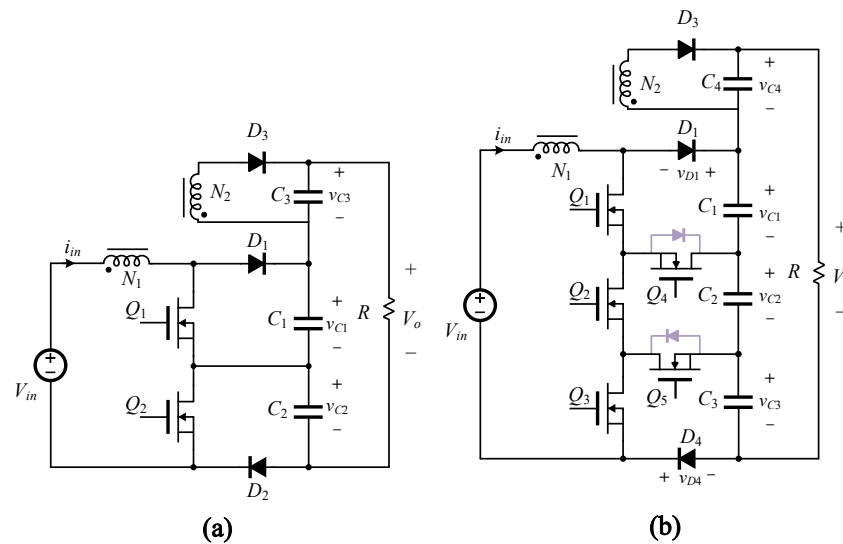


Figure 4. Illustration of using the flyback transformer with the multilevel converter: (a) the three-level boost converter with the flyback transformer; (b) the four-level boost converter with the flyback transformer.

Table 1. Summary of the high voltage gain converters shown in Figures 3a–c and 4.

Converter	Figure 2a	Figure 3a	Figure 3b	Figure 3c	The Proposed Converter, Figure 4a
Voltage gain	$\frac{1}{1-d}$	$\frac{N_2}{N_1} \frac{1}{1-d}$	$\frac{2d}{1-d}$	$\frac{2}{1-d}$	$\frac{N_2}{N_1} \frac{(2d-1)+2}{2(1-d)}$
Caps	2	2	2	3	3
Diodes	2	4	5	4	3
Coils	1	—	2	2	—
Coupled Ind.	—	1	—	—	1
Flyback xml	—	—	—	—	—

3. An Example Converter of a Three-Level Boost Converter with a Flyback Transformer

Principle of Operation

The three-level boost converter with flyback transformer shown in Figure 4a is presented in this section. The flyback transformer is used to provide an extra voltage through the capacitor C_3 . The capacitors C_1 , C_2 , and C_3 are connected in series. Therefore, the output voltage equals the summation of all capacitors' voltage. The converter is controlled with two MOSFETs connected as a half-bridge, and their gate signals are out of phase. The switching patterns make the converter operate in three modes, as presented in Figure 5. The analysis of these modes is performed next, with several considerations: (1) the elements are lossless; (2) the capacitors have large capacitance so that voltage ripples are negligible; (3) the MOSFETs have the same duty cycles $d = d_1 = d_2$; and (4) the operation is in the steady-state region.

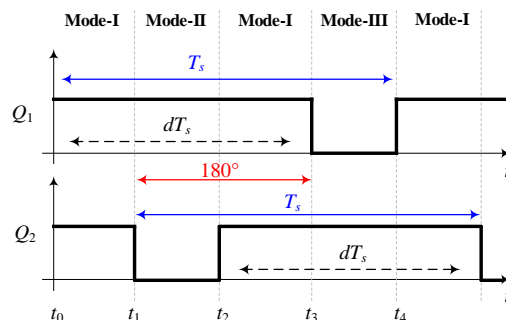


Figure 5. The controlling signal of the MOSFETs. Both duty cycles are assumed to be the same, and they are phase shifted.

Based on the assumptions and the switching pattern previously mentioned, the circuit enters three modes of operation. The equivalent circuits of the converter during these modes are presented in Figure 6. The converter operates in Mode 1 when both MOSFETs are ON. During this mode, all diodes are in reverse-bias and not conducting, and the input source charges the magnetizing inductor. The equivalent circuit of the converter in Mode 1 is presented in Figure 6a. The state equations are as follows:

$$V_{Lm} = V_{in} \quad (1)$$

$$V_o = V_{C1} + V_{C2} + V_{C3} \quad (2)$$

$$I_{C1} = I_{C2} = I_{C3} = -\frac{V_o}{R}. \quad (3)$$

The converter enters Mode 2 when the high side switch Q_1 is conducting, and the low side switch Q_2 is OFF. During Mode 2, the energy stored in the magnetizing inductor is released to capacitors C_1 and C_3 . The diode D_1 is not conducting, while other diodes are conducting. Figure 6b illustrates the equivalent circuit of the converter operating in Mode 2. The state equations are calculated as:

$$V_{Lm} = V_{in} - V_{C2} = \frac{V_{in} + V_{C1} - V_o}{\left(1 + \frac{N_2}{N_1}\right)} \quad (4)$$

$$I_{C1} = -\frac{V_o}{R} \quad (5)$$

$$I_{C2} = I_{Q1} - \frac{V_o}{R} \quad (6)$$

$$I_{Q1} = I_{in} - \left(\frac{N_2}{N_1}\right) I_S \quad (7)$$

$$I_{C3} = I_S - \frac{V_o}{R}. \quad (8)$$

The converter operates in Mode 3 when Q_2 is ON and Q_1 is OFF. During Mode 3, the diode D_2 is not conducting, and other diodes are in the forward conduction mode and are ON. The energy stored in the magnetizing inductor is released to the capacitors C_1 and C_3 . The equivalent circuit of the converter in Mode 3 is demonstrated in Figure 6c. The capacitor and inductor equations in this mode are given by:

$$V_{Lm} = V_{in} - V_{C1} = \frac{V_{in} + V_{C2} - V_o}{\left(1 + \frac{N_2}{N_1}\right)} \quad (9)$$

$$I_{C1} = I_{Q2} - \frac{V_o}{R} \quad (10)$$

$$I_{Q2} = I_{in} - \left(\frac{N_2}{N_1}\right) I_s \quad (11)$$

$$I_{C2} = -\frac{V_o}{R} \quad (12)$$

$$I_{C3} = I_s - \frac{V_o}{R} \quad (13)$$

The steady-state equations are derived by applying volt-second balance. The average values of the voltage on the capacitors are given by:

$$V_{C1} = V_{C2} = \frac{0.5 V_{in}}{1 - d} \quad (14)$$

$$V_{C3} = \frac{\frac{N_2}{N_1}(2d - 1)}{2(1 - d)} \times V_{in} \quad (15)$$

The static voltage gain of the three-level converter with flyback transformer is calculated by:

$$M = \frac{V_o}{V_{in}} = \frac{\frac{N_2}{N_1}(2d - 1) + 2}{2(1 - d)} \quad (16)$$

The proposed converter has a voltage gain dependent on the turns ratio and the duty cycle. The turns ratio and the duty cycle impact on the voltage gain is shown in Figure 7a. The comparison of the voltage gain of the proposed converter to the other converters is given in Figure 3.

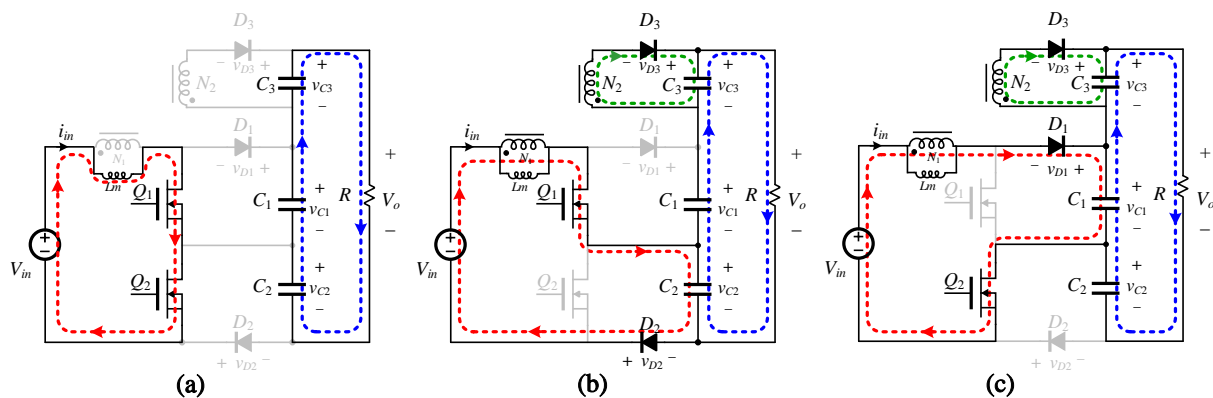


Figure 6. The equivalent circuit of the converter operating in: (a) Mode 1: both MOSFETs are conducting; (b) Mode 2: only Q_1 is conducting; and (c) Mode 3: only Q_2 is conducting.

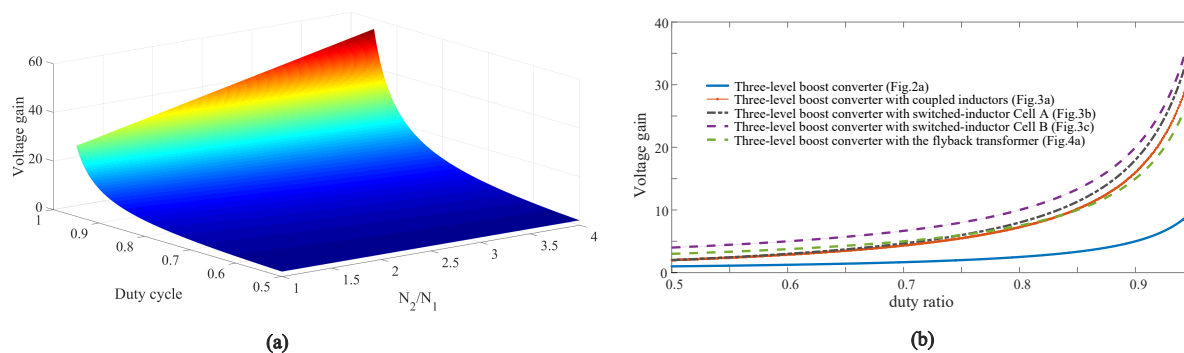


Figure 7. The voltage gain of the three-level boost converter with flyback transformer: (a) effect of the turns ratio and duty cycle; (b) the voltage gain of the introduced converter compared to other converters.

4. Analysis of the Component Ratings and Power Loss

Component selection is a crucial step in the design process. The switching components are designed based on their voltage and current rating, and capacitors are selected based on the energy storage requirements and the desired voltage ripples.

4.1. MOSFETs

The proposed converter inherits some of the three-level boost converter characteristics, such as the reduced voltage stress on the MOSFETs. The maximum voltage on the MOSFETs is given by:

$$V_{Q1} = V_{Q2} = \frac{0.5V_{in}}{1-d} \quad (17)$$

The average value of currents passing via MOSFETs is calculated using:

$$I_{Q1(avg)} = I_{Q2(avg)} = I_{in} \times \frac{\frac{N_2}{N_1}(2d-1) + 2d}{\frac{N_2}{N_1}(2d-1) + 2} \quad (18)$$

where I_{in} is the input current and can be calculated using:

$$I_{in} = I_o \times \frac{\frac{N_2}{N_1}(2d-1) + 2}{2(1-d)} \quad (19)$$

The MOSFETs' current rating must be selected to be higher than the peak value of the current. The peak value of the current passing through the MOSFETs are calculated as follows:

$$I_{Q1(pk)} = I_{Q2(pk)} = I_{in} + \frac{V_{in}(2d-1)}{2f_s L_m} \quad (20)$$

The peak value of the input current equals the peak value of the MOSFETs' current. The power loss of the MOSFETs depends on the effective value of the MOSFETs' current. The effective value of the MOSFETs' current is given by:

$$I_{Q1(rms)} = I_{Q2(rms)} = \sqrt{\left(I_o \frac{\frac{N_2}{N_1}(2d-1)+2d}{\frac{N_2}{N_1}(2d-1)+2}\right)^2 + I_o \frac{\frac{N_2}{N_1}(2d-1)+2}{2(1-d)} \frac{V_{in}(2d-1)}{f_s L_m} + \left(\frac{V_{in}(2d-1)}{\sqrt{3}f_s L_m}\right)^2} \quad (21)$$

4.2. Diode Selection

Diodes' reverse voltage must be higher than the voltage stress across the diode. The voltage stress across diodes D_1 and D_2 :

$$V_{D1} = V_{D2} = \frac{0.5V_{in}}{1-d} \quad (22)$$

The voltage stress on D_3 is calculated by:

$$V_{D3} = \frac{0.5 \frac{N_2}{N_1} V_{in}}{1-d} \quad (23)$$

The average value of the current passing through the diodes equals the load current, and the effective value of the current passes via D_1 and D_2 is calculated using:

$$I_{D1(rms)} = I_{D2(rms)} = \frac{I_o}{\sqrt{1-d}} \quad (24)$$

The effective value of the current passes though D_3 is given by:

$$I_{D3(rms)} = \frac{I_o}{\sqrt{2(1-d)}} \quad (25)$$

4.3. Capacitors

The capacitors are selected based on the voltage and tolerated voltage ripples. The voltage across capacitors was already given in the previous section, and the tolerated voltage ripples are determined based on the regulation requirements, which is typically less than 2%. The capacitance is calculated by:

$$C = I_o \frac{d}{\Delta v \times f_s} \quad (26)$$

The capacitance required by C_3 is half the capacitance required by C_2 or C_1 because of the effective frequency. That is, capacitor C_3 sees twice the switching frequency. The voltage ripples of the output load might appear less than the approximated because of the ripple cancellation between C_1 and C_2 . The ripple cancellation is caused by the phase shift between the gate signals of the MOSFETs. The effective value of the capacitors is approximated by:

$$I_{C1(rms)} = I_{C2(rms)} = I_o \sqrt{\frac{d}{1-d}} \quad (27)$$

$$I_{C3(rms)} = I_o \sqrt{\frac{2d-1}{2(1-d)}} \quad (28)$$

4.4. Flyback Transformer

The flyback transformer is used to improve the voltage gain and store energy during Mode 1. The voltage gain transfer function relates to the turns ratio term, and therefore, one can obtain the proportion of the secondary winding to the primary winding, which is given by:

$$\frac{N_2}{N_1} = 2 \times \frac{\frac{V_o}{V_{in}}(1-d) - 1}{2d-1} \quad (29)$$

The duty cycle must be higher than 0.50 to allow the magnetizing inductance to store energy. The tolerated current ripples Δ_i are determined before calculation, which typically has a value of less than 30%. The magnetizing inductance is calculated by:

$$L_m = \frac{V_{in}(2d - 1)}{2\Delta_i f_s} \quad (30)$$

4.5. Components Loss Calculation

The total loss of the proposed converter can be determined by calculating the loss of each component individually. The loss in the flyback transformer is given by:

$$P_L = \underbrace{I_{in(rms)}^2 \times R_{DC}}_{copper\ loss} + \underbrace{K_{Fe} \left(\frac{dV_{in}}{2f_s N_1 A_c} \right)^\beta (core\ volume)}_{core\ loss} \quad (31)$$

where K_{Fe} is the core loss coefficient and β is the core loss exponent, which typically has a value of around 2.5 for ferrite materials. The values of K_{Fe} and β are obtained from the datasheets. R_{DC} is the DC resistance of the winding, and A_c is the core cross-sectional area. The power loss caused by the controlled switches is given by:

$$P_{Q,total} = 2 \underbrace{(I_{Q(rms)}^2 R_{on})}_{conduction\ loss} + \underbrace{I_{Q(avg)} V_Q (t_r + t_f) f_s}_{overlap\ loss} + \underbrace{C_{(oss)} V_Q^2 f_s}_{parasitic\ output\ capacitance\ loss} \quad (32)$$

where $R_{ds(on)}$ is the resistance between the drain and the source during the conduction operation. t_r and t_f are the rise and fall times, respectively. $C_{(oss)}$ represents parasitic output capacitance. The power dissipated in diodes is calculated by:

$$P_D = \underbrace{V_F \times I_o}_{conduction} + \underbrace{Q_R \times V_r \times f_s}_{reverse\ recovery\ loss} \quad (33)$$

where V_F is the diode's junction potential, V_r is the reverse voltage, and Q_R is the reverse recovery charge. The power loss caused by capacitors is generally insignificant, and the source of the power loss is the equivalent series resistance ESR . The power loss in the capacitors is calculated by:

$$P_C = I_{C(rms)}^2 ESR \quad (34)$$

5. Simulation Results

The analysis of the converter in the previous section is confirmed with a simulation model. The input voltage of the simulated converter is 20 V, and the output voltage and power are 200 V and 80 W, respectively. A 500 Ω resistor represents the output, and all the capacitors have a capacitance of 30 μ . The converter operates at 100 kHz and a duty cycle of 0.82. The turns ratio of the coupled inductors has a value of $\frac{N_2}{N_1} = 2.7$ and magnetizing inductance 500 μ H. Some small parasitic elements were added to the model to remove the singular loops.

The simulation results are shown in Figure 8. The maximum voltage on the MOSFETs and the diodes D_1 and D_2 is about 56 V. The diode on the secondary side of the flyback transformer has to block 150 V. The current passing through MOSFETs has an average value of 3.870 A and an effective value of 4.430 A. The current passing through D_3 has an average value of 0.410 A and an effective value of 0.981 A.

The average value of the current passing through diodes D_1 and D_2 is 0.410 A and has an effective value of 0.981 A.

The voltage waveforms of the output, input, and capacitors are shown in Figure 8d. The simulation matches the analysis, as the average voltage across the capacitors matches the steady-state equations. The effective values of the currents passing through C_1/C_2 and C_3 are 0.89 A and 0.5543 A, respectively. The simulated loss breakdown in the components is shown in Figure 8e. The forward conduction loss is accountable for about 46% of the total loss and the MOSFETs switching, and conduction loss represents about 29.0% of the loss. The coupled inductors and capacitors have 23.9% and 1.1% of the total loss, respectively.

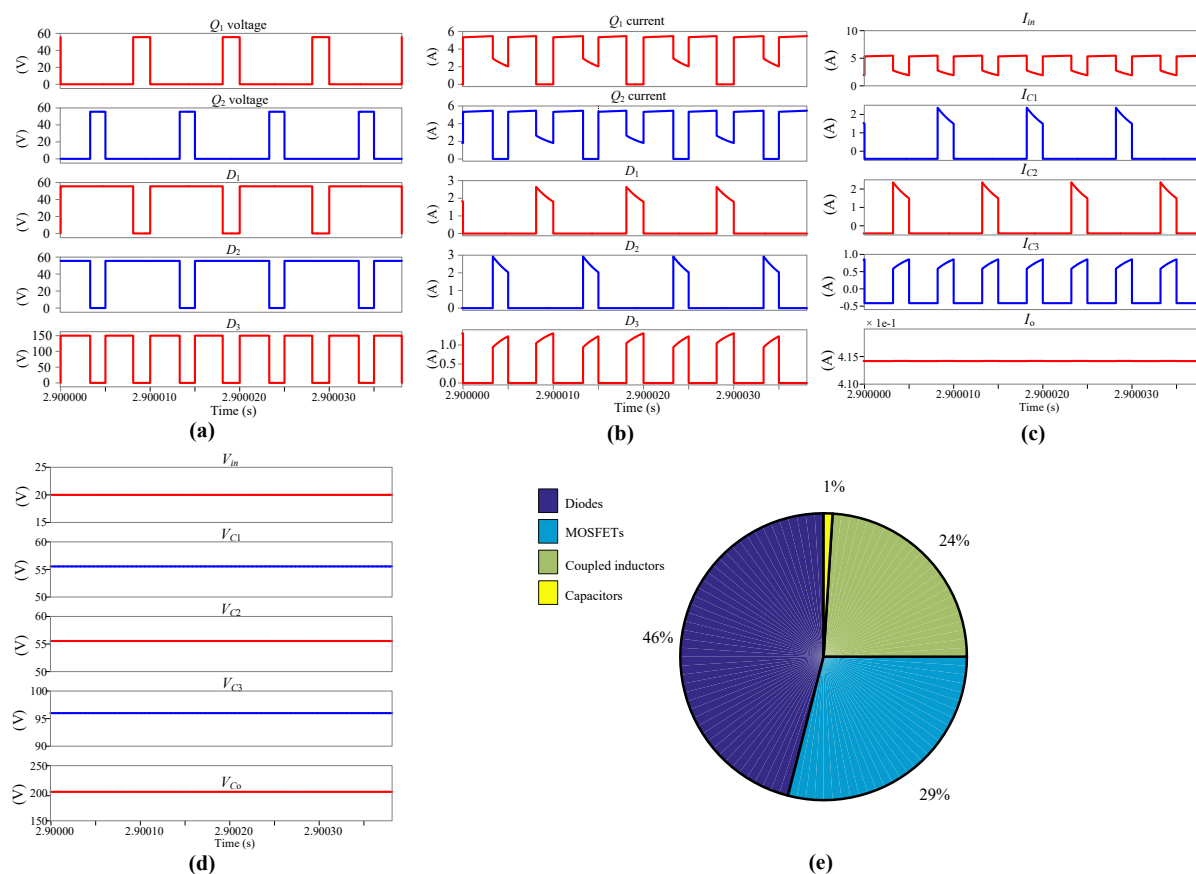


Figure 8. Simulation results of the example converter (a) Voltage stress across the semiconductor elements (b) Currents Passing through the diodes and MOSFETs (c) Input and output currents (d) the voltage of the input source, capacitors and the output (e) Components loss breakdown.

Simulation of the Proposed Converter with the Maximum Power Point Tracker

The converter in this case was used to interface with a PV panel and extract the maximum power. The Uni-solar PVL-136 PV module was used in the simulation. The PV module was tested in the standard test conditions (STC) and had an open circuit voltage of about 46.2 V and a short circuit current equal to 5.10 A. The maximum power at the STC was 135.3 W and occurred at $V_{mp} = 33.0$ V and $I_{mp} = 4.10$ A. The parameters were extracted to simulate the module performance. The ideality factor, shunt, and series resistance were 1.48, 1.85 Ω , and 60 Ω , respectively. Figure 9a shows the current voltage and power voltage curves. The effect of the temperature and solar irradiance variation on the PV module's performance is

shown in Figure 9b,c. The increase in temperature reduces the output power from the PV and reduces the open-circuit voltage value. Similarly, the solar irradiance variation affects the PV's current, and therefore, it affects the power.

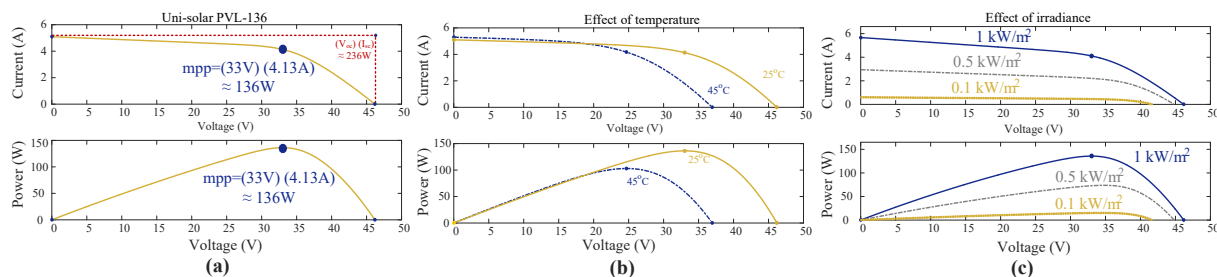


Figure 9. Characteristics of the PVL-136 panel: (a) the current voltage and power voltage curves in the standard test conditions. The MPP in the standard test condition is about 136 W. (b) The effect of temperature on the the performance of the PV panel. (c) The effect of the solar irradiance level on the performance of the PV panel.

The variation of solar irradiance and temperature affects the location of the maximum power point. The converter must track the maximum power point to extract the most power from the PV module. Several tracking algorithms have been reported in the literature. The perturb and observe (P&O) approach was used to extract the maximum power from the PV and provide the duty cycles to the MOSFETs. The operation of P&O is simple. First, the voltage and the PV module's current are sensed, and the power then is calculated. Second, the new value of the power is compared to the previous value of the power. Then, the new duty cycle is either increased or decreased by a step. The selection of the step is crucial to reach the real maximum power and ensure stable operation. Figure 10 illustrates the impact of the step size on the operation of the tracker. The implementation of P&O with a small step size makes the tracker slow. In this case, the tracker takes many steps until reaching close to the maximum power point, as shown in Figure 10a. On the other hand, P&O with a large step size cannot reach the maximum power point and might cause the zigzagging operation of the tracker, as shown in Figure 10b. The P&O approach in the paper was implemented with a dynamic step size, where the value of the step becomes smaller when the tracker reaches close to the top of the P-V curve, as shown in Figure 10c. The performance of the controller and the solar irradiance used in the simulation are shown in Figure 11a and Figure 11b, respectively. The tracker is able to track the maximum power point under the variation of the irradiance, and the converter is suitable as a grid interface to a PV module.

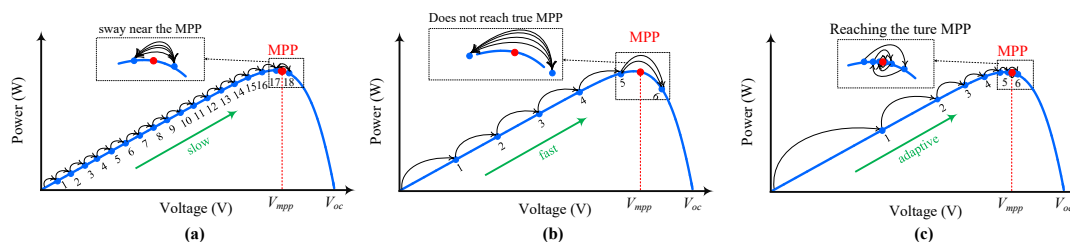


Figure 10. Illustration of the step size impact on the conversion: (a) small step; (b) big step; (c) adaptive step.

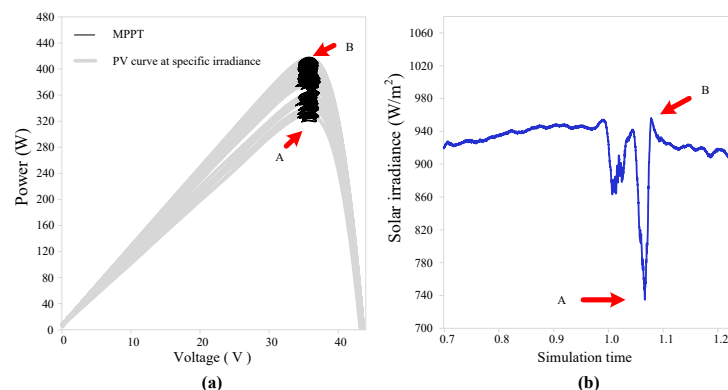


Figure 11. The simulation outcomes of the converter with the tracking controller: (a) the behavior of the maximum power tracking control; (b) the applied solar irradiance on the PV module.

6. Implementation of the Hardware Prototype and Experimental Results

An 80 W experimental prototype was constructed and evaluated to confirm the operation theory and validate the simulation. The proposed converter's flyback transformer was implemented using *ETD49* with a turns ratio of 2.7, and magnetizing inductance was measured as 0.2 mH. The selected MOSFET for Q_1 and Q_2 was *IPA105N15N3*, which has a voltage and current rating of 150 V and 37 A, respectively. The MOSFET's conduction resistance is 10.53Ω , and it has very low total gate charge. The *KRM55TR72A106MH01K* ceramic capacitors were used as the C_1 – C_3 capacitors. The ceramic capacitors were selected because of the low equivalent circuit resistance. The diodes were implemented using *MBR4025G* diodes, which have a voltage and current rating of 250 V and 40 A, respectively. The forward voltage equals 0.86 V, and the reverse recovery time is 35 ns. All components were placed on a two-layer printed circuit board, as shown in Figure 12a. The size of the prototype is $5 \text{ cm} \times 5 \text{ cm}$. The converter was used to convert a 20 V from a DC power supply to a 200 V resistive load. The experimental results are shown in Figure 12b–h. Figure 12b shows the voltage across capacitors. The average voltage across capacitors is shown, and Figure 12c shows the output voltage, which has an average value of 199.8 V, with the voltage ripple less than a volt. The waveforms in Figure 12d,e show the voltage stress across the switching elements, which matches the simulation. Similarly, the input current and currents passing through the switching devices are shown in Figure 12f,g. The AC components of the input current have a frequency of 100 kHz. The prototype's efficiency is shown in Figure 12i, which is compared to the simulated efficiency. The converter has a maximum efficiency of 95% at around 40 W of load power and has an efficiency of around 94.6% at full load. The parasitics cause a difference in the simulation and experimental efficiency, which is an error of less than 1%.

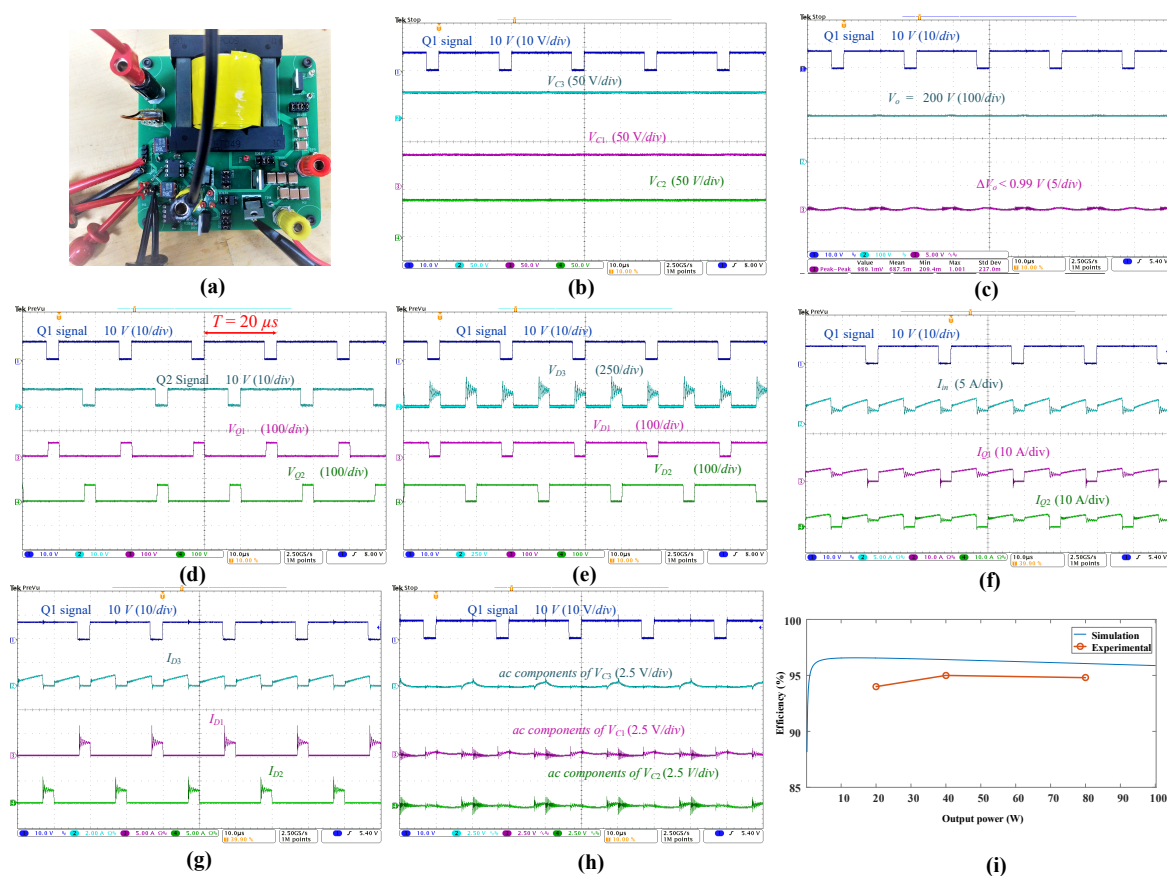


Figure 12. Experimental setup and results: (a) the experimental prototype; (b,c) capacitor voltages; (d,e) voltage stress across switching elements; (f,g) the current passing through switching elements; (h) the AC components of capacitors' voltage; (i) the efficiency of the experimental prototype.

7. Conclusions

This paper presents a family of high voltage gain three-level boost converters suitable for photovoltaic energy integration. The family enhances the three-level boost converter by adding high voltage boosting techniques, including using switched-inductor cells and coupled inductors. An example of a three-level boost converter with a flyback transformer is analyzed, simulated, and experimentally implemented to convert 20 V to 200 V, with a peak efficiency of about 95%. The converter also extracts the maximum power from photovoltaic panels using the perturb and observe tracking algorithm. The three-level boost converter with a flyback transformer has several advantages over high voltage gain converters, such as low voltage stresses across components and an effective frequency across the magnetic element that is twice the switching frequency. The example converter's voltage gain is a function of the turns ratio, which can be increased by increasing the turns ratio. This work was limited to a three-level boost converter to confirm the operation. However, future work includes applying the high voltage techniques on a four-level and a five-level boost converter and testing the operation and performance.

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Abbreviations

The following abbreviations are used in this manuscript:

PV	Photovoltaics
MPPT	Maximum power point tracking
CCM	Continuous conduction mode
MOSFET	Metal oxide silicon field effect transistor

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