DC-DC High-Voltage-Gain Converters with Low Count of Switches and Common Ground

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Abstract: This paper presents a new concept and research results of DC-DC high-voltage-gain, high-frequency step-up resonant converters. The proposed topologies are optimized towards minimizing the number of switches and improvements in efficiency. Another relevant advantage of such type of converters is that they have a common input and output negative point. The proposed converters are based on the resonant switched-capacitor voltage multiplier circuit, and that is why they are compared with a classic converter from this family. The included results show the operating principle, possible switching methods with the consideration of their impact on the voltage gain level, as well as the voltage and current ripples. The operating concepts and analytical calculations are confirmed by simulation and experimental results.

Keywords: DC-DC converter; resonant converter; high-voltage-gain converter; switched-capacitor converter; inductiveless converter

1. Introduction

Switched capacitor (SC) circuits can be effectively used in power electronic converters [1]. The significant advantages of SC-based DC-DC power converters are high-voltage-gain, low volume, and quasi inductiveless design. To achieve oscillating currents, low-volume inductors can be used in those converters. They can be designed as air-chokes, or even be based on parasitic inductances of the circuits, resulting in a decrease in the weight of the converter. The design without ferrite chokes allows for the use of the converter in high ambient temperature and/or with a low-volume heat sink.

SC DC-DC converters represent one of the classes of non-isolated step-up converters [2–4]. Nowadays, there are a significant number of applications where isolated DC-DC step-up converters are required [3], due to technical reasons and safety requirements. However, various kinds of non-isolated converters are extensively developed as well. One of the prospective applications for non-isolated DC-DC step-up converters proposed in the literature [5–10] are photovoltaic (PV) systems. High step-up DC-DC converters are often required in grid-connected PV systems to transfer the energy from a low-voltage PV source to the grid [5,6]. In transformerless PV systems [7,8], as well as in microinverters [9], dual-stage DC-AC converters are one of the investigated solutions.

The SC step-up DC-DC converter could be a competitive solution to the switch-mode boost converter. An example of such an idea is presented in Reference [10]. The non-isolated step-up converter can be used not only for a single stage supply, but as a part of a system composed of series-connected converters as well. In such systems, isolation can be implemented in another stage of conversion, e.g., by using a series resonant converter [6,11].

High-voltage-gain in SC-based DC-DC converters can be achieved by applying a suitable topology concept. In References [12–14], an SC voltage multiplier (SCVM) has been presented. It is

a series-parallel converter in that a high-voltage-gain can be obtained, as it is proportional to the number of switching cells. The advantage of an SCVM is its modular topology; however, the number of required transistors is relatively high. Series-parallel SC converters have also been presented in recent publications [15,16]. In Reference [15], a converter with regulated voltage gain has been discussed. This device utilizes three switches, which means that the voltage gain can reach three. Reference [16] has presented a very effective method that allows the switch count in high-gain series-parallel converters to be decreased. However, the converter presented in Reference [16] does not have a common input and output negative point, and the output voltage is asymmetrically divided. In Reference [17], a converter that combines Dickson-based and ladder SC converter concepts has been presented. In the proposed topology, high-voltage-gain is achieved with limited voltage and current stresses on the switches. The Dickson-based SC concept has also been used in the converter presented in Reference [18] that is composed of an SC part and an interleaved boost converter. The converter achieves a very high-voltage-gain with the output voltage regulation and soft switching operation, using four switches and seven diodes. In Reference [19], high-voltage-gain is achieved in a converter with switched-capacitor and switched-inductor networks. A concept of a family of converters composed of a boost stage and switched-capacitor-inductor cells has been presented in Reference [20]. This increases the voltage gain of the converter significantly with favorable voltage stress levels, efficiency, and component count. References [21–24] have demonstrated high-voltage-gain multilevel converters based on typical multilevel converter concepts. When we take into consideration the number of the utilized components and the reached voltage gain, the multilevel SC converters can be more beneficial in comparison to the SCVMs. The converter described in Reference [21] is based on a modified classic multilevel SC topology; however, it is composed of a significant number of switches. In Reference [22], an improvement in the operation of the multilevel resonant SC converter (MRSCC) has been proposed. The MRSCC makes it possible to operate with high-voltage-gain and limited voltage stress on the switches with the ability of bi-directional energy transfer. In Reference [23], a multilevel structure has been achieved in the converter with two switches and circuits composed of diodes and capacitors. The converter can operate with zero voltage switching (ZVS) and voltage regulation. In Reference [24], a DC-DC bidirectional SC converter has been presented that improves the total device power ratings in comparison to the multilevel modular capacitor clamped converter (MMCCC) and well-established flying-capacitor converters.

One of the major issues of the SC converters is a large number of switches used in the topology. This problem can be solved by the concepts of cascaded or series systems composed of SC units [25,26] or by new concepts of topologies [16,27,28]. In the concept for the switch count reduction presented in Reference [26], a high-power converter has been analyzed in a multi-section topology. The converter is composed of the typical SCVM sections separated by LC filters. According to this concept, a significant reduction in the number of switches has been achieved. However, an increased number of passive components are utilized as LC filters between the sections in the multi-section converters [26]. The problem of the switch count reduction in an SCVM converter has been analyzed in Reference [29], where the charging of the switched capacitors is controlled by a single switch. For high-voltage-gain, the system is significantly simplified. The design of such a cost-effective converter should assume a much higher current stress of the switch that controls the charging of the switched capacitors.

The converters proposed in this paper are optimized towards a low count of transistors (and they are called Low Count of Transistors Switched Capacitor Voltage Multipliers—LCSCVMs). The basic concept of the topology and operation assumes that every second cell has no transistors whatsoever, but the utilization of all the switched capacitors remains possible, and the effect of voltage gain is comparable to that of the multipliers (SCVMs) presented in Reference [13,14]. Furthermore, the optimized concept is introduced into the cost-effective topology presented in Reference [29], which gives a new relevant converter. Taking into consideration the count of switches, SC converters, such as the SCVM [20], may not be in competition with the LLC converters or other established topologies. However, the concepts proposed in this paper demonstrate a development of the SC topologies towards a

significant decrease in the number of switches. One of the converters presented in this paper requires only three switches, which is below the number of transistors used in a full-bridge LLC converter. Other advantages of the SC converters, such as: high gain, high power density and low weight (no transformer or bulky choke), fast dynamic response [3], ability for operation in high temperature (no ferrites), and simple control, can make them an alternative solution for existing topologies intended for high-voltage-gain non-isolated DC-DC conversion. SC-based topologies can be suitable for the miniaturization of converters that can be applied in emerging power electronics applications, such as wearable technology.

For the operational parameters of an SC converter, the switching strategy applied for a given topology can be essential, which has been demonstrated in Reference [14]. For the optimization purposes analyzed in this paper, various switching strategies are proposed for the new topologies. This makes it possible to determine the advantages of the presented topologies, also taking into consideration a variety of qualities, other than the count of switches.

The proposed converters are nearly pure switched-capacitor circuits, where a vast majority of energy is transferred via capacitors rather than inductors. The resonant inductors are used to achieve oscillatory currents. The inductors can be designed as air chokes, which reduces the weight of the converters and allows them to work in higher temperatures. However, another trend in the development of very high-voltage-gain converters can be observed in the literature. The concept presented in Reference [30] is based on coupled inductor (CI) converters that achieve good parameters such as voltage ratio, efficiency, low number of switches, or low voltage stress on switches. Notwithstanding, such converters use chokes and, therefore, differ from the presented SC-based concept regarding admissible ambient temperature of operation, weight, and volume. The design comparison can be analyzed in particular case studies.

In this paper, the qualities introduced by the new topologies will be compared with those of a classic SCVM and of other converters discussed in recently published papers.

The paper is organized as follows. Section 2 demonstrates two proposed topologies of the SC converters and presents the principles of their operation. For both converters, switching strategies are analyzed. The discussion is supported by the results of computer simulations of their operation in five cases of switching strategies. Moreover, with the use of the simulation results, a number of parameters of the converters operating under various switching strategies are compared as well. Section 3 contains efficiency models of the proposed converters that demonstrate their efficiency as a function of their parameters. Section 4 presents the laboratory setup and the experimental verification of its operation, including the efficiency of the converter. All the research results are concluded in Section 5.

2. Operating Principle of the Converters

The operating principle of the converters in Figure 1 is similar to that of other SC multipliers, and is based on the charging and discharging of the switched capacitors in consecutive stages (time intervals). However, various switching strategies can be proposed for the new converters, which creates differences in their parameters. In the SCVM, as well as in the case of the converters proposed in this paper, the switched capacitors are recharging in resonant circuits composed of a switched capacitor and a low-volume resonant inductor. This creates ZCS (zero current switching) operating conditions, and limits the current flow between the capacitors and the voltage source connected in parallel.
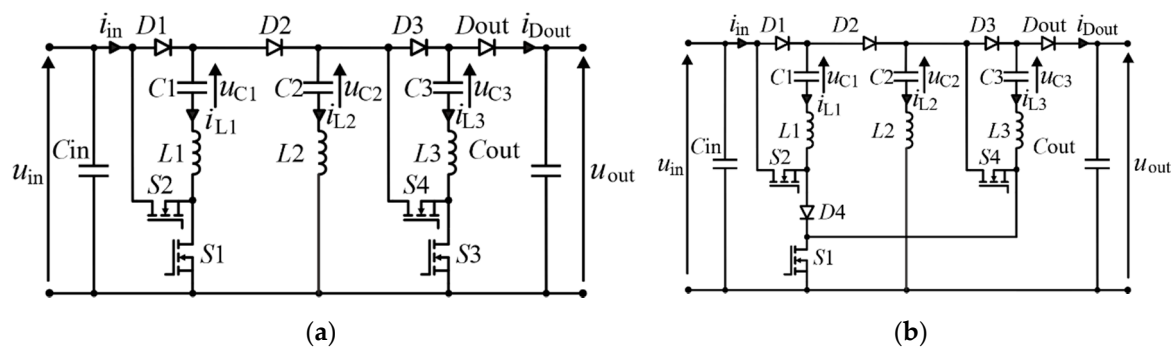
Figure 1. Proposed new resonant converters with low count of switches and common input/output negative point: (**a**) LCSCVMa, (**b**) LCSCVMb.

The main difference between the topology of the proposed converters and the classic SCVMs is that in the former case, an LC circuit that is not a part of a traditional cell is used, usually consisting of a diode and two transistors [13]. This circuit is charged using the energy of the input source and the electric charge of the switched capacitor that is the nearest to the input source. Then, the middle capacitor is discharged to the output capacitor or to the switched capacitor nearer to the output. Its function is to increase the output voltage and the amount of converted power, simultaneously maintaining the same value of the input voltage and the same cell number as in the case of a typical SCVM.

The LCSCVMa (Figure 1a) offers a larger number of strategies than the LCSCVMb (Figure 1b), due to the possibility of independent control of switches S_1 and S_3. The basic switching strategies can be composed of 2, 3, or 5 stages.

2.1. Switching Strategy Concepts for the LCSCVMa

Table 1 presents three switching strategies for the LCSCVMa, and Figures 2–5 depict the corresponding simulation waveforms.

Table 1. Switching strategy concepts of the LCSCVMa. States of switches S_1–S_4.

| The Concept for Switching Strategy of LCSCVMa		Description—Stages of Charge Transfer in the Converter
Strategy C1		1.Simultaneous charging of all the switched capacitors 2. Discharging of the capacitor that is the nearest to the source (C_1) to the internal branch (C_2) 3. Charging C_1, and discharging C_2 and the next SC capacitor (C_3) to the output 4. Discharging C_1 to the internal branch (as in 2) 5. Discharging C_2 and C_3 to the output
Strategy C2		1. Simultaneous charging of all the switched capacitors 2. Discharging C_1 to the internal branch (C_2) 3. Discharging C_2 and C_3 to the output
Strategy C3		1. Simultaneous charging of all the switched capacitors (C_1 and C_3) 2. Simultaneous discharging of all the switched capacitors and charging the internal branch capacitor (C_2)
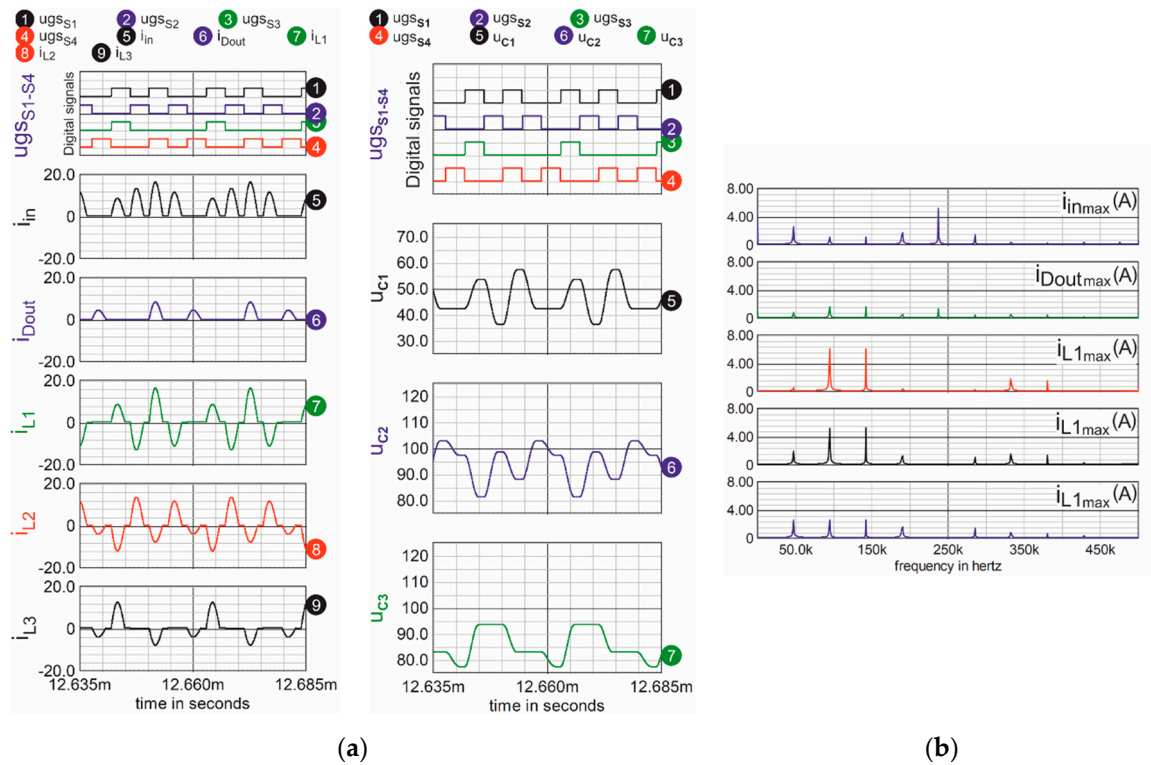
Figure 2. Steady-state operation of the LCSCVMa converter under switching strategy C1: (**a**) waveforms of the gate to source signals of transistors (presented with level shift), input current (in amperes), and voltages (in volts) on capacitors C_1, C_2, and C_3. (**b**) Spectrum of the input current, and currents of switched capacitors and output capacitor. The results were obtained with the use of ICAP/4 simulation software.
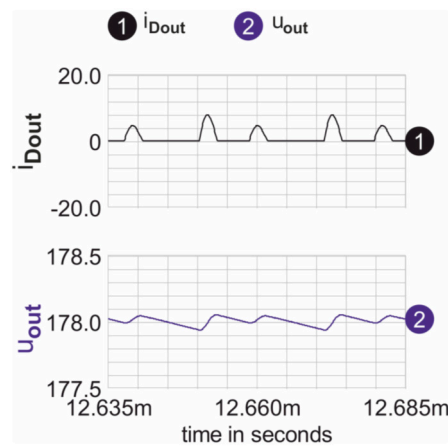

Figure 3. Steady-state output current and voltage waveforms of the LCSCVMb converter under switching strategy C1 (4 A/div and 100 mV/div). The results were obtained with the use of ICAP/4 simulation software.
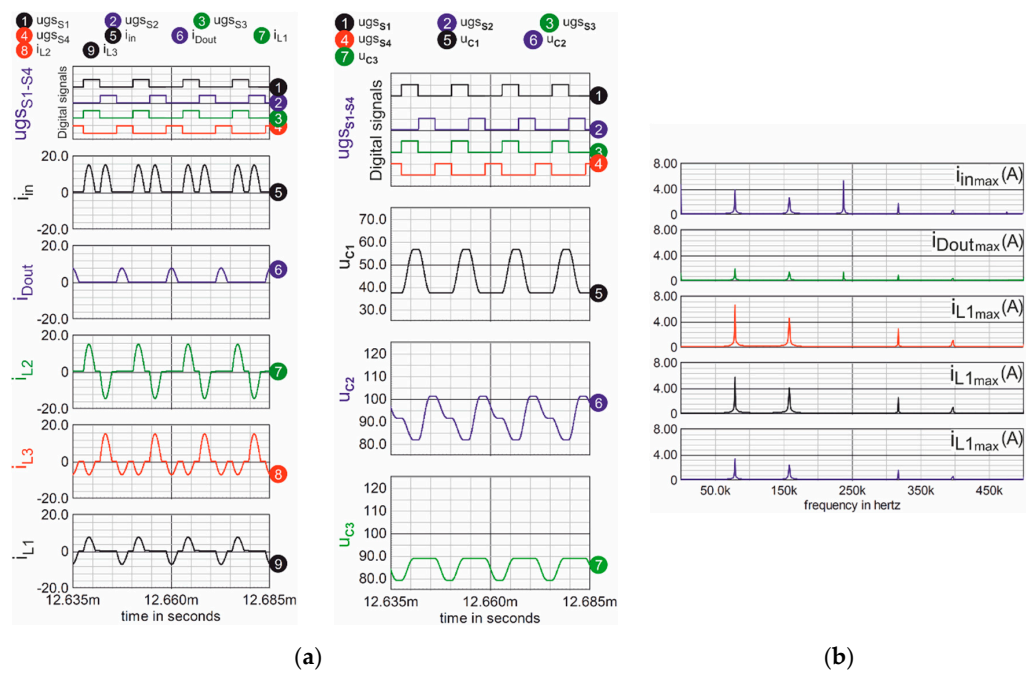
Figure 4. Steady-state operation of the LCSCVMa converter under switching strategy C2: (**a**) waveforms of the gate to source signals of transistors (presented with level shift), input current (in amperes), and voltages (in volts) on capacitors C_1, C_2, and C_3. (**b**) Spectrum of the input current, and currents of switched capacitors and output capacitor. The results were obtained with the use of ICAP/4 simulation software.

Figure 5. Steady-state operation of the LCSCVMa converter under switching strategy C3: (**a**) waveforms of the gate to source signals of transistors (presented with level shift), input current (in amperes), and voltages (in volts) on capacitors C_1, C_2, and C_3. (**b**) Spectrum of the input current, and currents of switched capacitors and output capacitor. The results were obtained with the use of ICAP/4 simulation software.
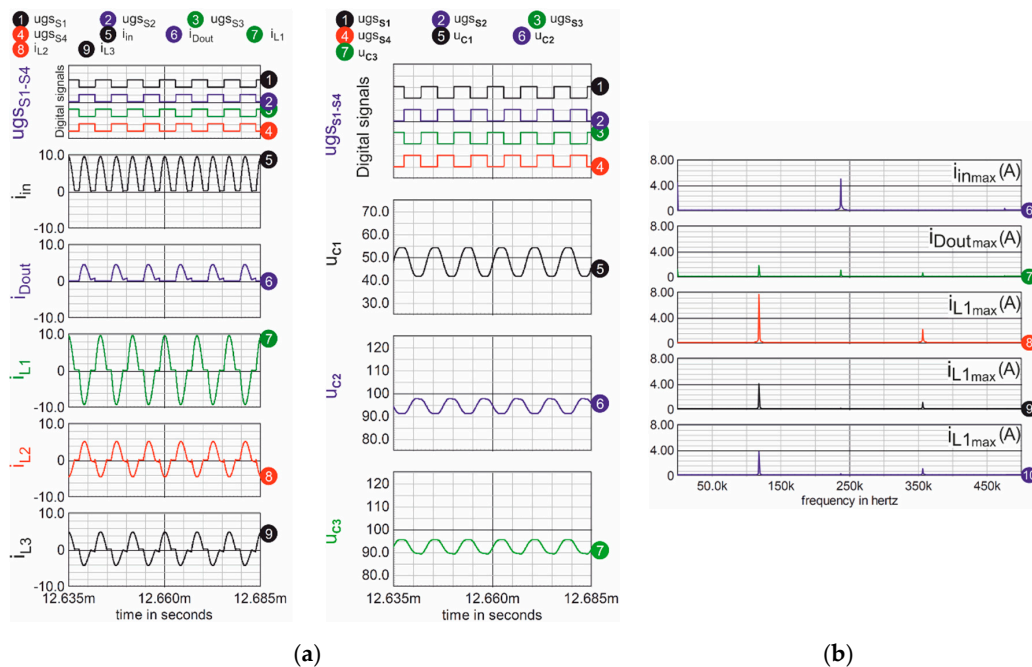
To characterize the switching strategies, Table 1 contains the idealized control logic waveforms of the transistors (signals S_1 to S_4), as well as the description of the particular operation stages. Dead times have been neglected in Table 1, but they have been taken into account in the simulations and experiments. Capacitor C_2 (Figure 1) is not referred to as a switched capacitor. The maximum switching frequency (strategy C3) is defined as:

$$f_{S_{max}} = \frac{1}{2T_{pulse}}$$

(1)

where T_{pulse} is the sum of the duration time $T_0/2$ of a single current pulse of any transistor and the dead time t_d (any period of time denoted as 1–5 in Table 1),

$$T_0 = \frac{1}{f_0} = 2\pi \sqrt{LC}$$

(2)

and $L = L_1 = L_2 = L_3$, $C = C_1 = C_2 = C_3$ (Figure 1).

All the simulation results were obtained for the following parameters: U_{in} = 50 V, L_n = 620 nH, C_n = 1.47 μF, f_0 = 166.7 kHz, T_{pulse} = 4.2 μs (f_{Smax} = 119 kHz), C_{out} = 100 μF, P_{out} = 200 W (n = 1, 2, 3). A resistance of 100 mΩ has been inserted into each branch as an equivalent to parasitic resistances. The time period T_{pulse}, as well as the duty cycle of the switching signals of the transistors, remain constant in each switching strategy. The selection of the switching frequency depends on the power of the converter, achievable resonant inductance, and switching losses [13]. This parameter, as well as the others, can be fixed in the following steps. In the ZCS mode, the SC converters' transistors do not operate in the ZVS mode, and during their turn-ons, the output charge is shorted (C_{oss} losses). The limit of C_{oss} losses determines the switching frequency of the transistors taking into consideration their type and voltage stresses. The oscillation frequency should be nearly equal to the switching frequency to minimize conduction losses [13]. This frequency depends on the product of L_nC_n, and allows to select C_n for a known value of L_n. The maximum power of the converter depends on capacitance C_n and the switching frequency [13], and it should be higher than or equal to the rated power for the selected parameters. The simulation results presented in this section have been obtained with the use of ICAP/4 simulation package based on the IsSpice4 simulator.

2.1.1. Simulation Results of the Switching Strategy C1

Figure 2 presents steady-state simulation waveforms of the LCSCVMa controlled according to strategy C1. From all the results, it can be seen that the switched capacitors are recharged by oscillatory currents and each stage of the switching is longer than the half-period of the oscillations.

The entire switching cycle is composed of five stages (Table 1). According to the principle of operation, turning on switches S_1 and S_3 involves the charging of the switched capacitors C_1 and C_3. Capacitor C_3 is being charged from capacitor C_2 of the internal branch whose voltage is going down in this stage. The diode D_2 remains turned off, as $u_{C2} > u_{C1}$ and $u_{C2} > u_{in}$ (Figure 2). In the next stage, switch S_2 is turned on, and capacitor C_2 is being charged from the source u_{in} and capacitor C_1 connected in series with it. The charging of the output capacitor, from capacitors C_2 and C_3 connected in series, occurs in the next stage when the switch S_4 is turned on. At the same time, capacitor C_1 is being charged from the source. In the next two stages, capacitor C_2 and capacitor C_{out} are being charged, consecutively.

The advantage of this switching strategy is reducing the number of the performed switching operations, which leads to switching losses limitation. In three of five stages of the switching period, only one switch is affected.

The input current has various values in each switching state, which is a drawback of this strategy. Therefore, a low-frequency component $f_S = f_{ac\text{-}in} = f_{Smax}/2.5$ appears in current i_{in}, as well as in all other currents and voltages in the circuit. Using this kind of switching requires using a large input

filter and a large output capacitor. From the standpoint of the components' volume and input current filtering, this strategy is not favorable.

The output voltage used for the voltage gain calculation in relation (3) has been measured as the average value of the waveform presented in Figure 3 together with the output current. Further results, given in Equations (4)–(7), were obtained in the same manner.

In this strategy, the measured average value of the output voltage of the converter equals $U_{out} = 178$ V. For the input voltage of the converter $U_{in} = 50$ V (maintained by the voltage source in simulations), the voltage gain of the converter under switching strategy C1 equals:

$$G_{UC1} = \frac{U_{out}}{U_{in}} = \frac{178.0}{50.0} = 3.56 \tag{3}$$

2.1.2. Simulation Results of the Switching Strategy C2

Figure 4 presents simulation waveforms in the LCSCVMa controlled according to strategy C2. In this strategy, each switching period consists of three stages. The first two switching stages correspond to those in strategy C1. In the third stage, only transistor S_3 is on. The last two stages of strategy C1 do not occur here, and capacitor C_2 is charged and discharged only once in a switching period. The number of the switching operations is lower in comparison to that in strategy C1. The spectrum of currents and voltages shows more favorable qualities in strategy C2 versus C1, as the 50 kHz components are not present (the lowest frequency is 75 kHz).

In this strategy, the measured average value of the output voltage of the converter equals $U_{out} = 177$ V. For $U_{in} = 50$ V, the voltage ratio is

$$G_{UC2} = \frac{U_{out}}{U_{in}} = \frac{177.0}{50.0} = 3.54 \tag{4}$$

2.1.3. Simulation Results of the Switching Strategy C3

Figure 5 presents simulation waveforms in the LCSCVMa controlled according to strategy C3. In this strategy, there are only two stages. In the first stage, the charging of the switched capacitors takes place (switches S_1 and S_3 are turned on). During the second stage, the output capacitor and C_2 are being charged (with switches S_2 and S_4 turned on).

In this strategy, each switch operates with a much higher frequency than in the case of strategies C1 and C2. This brings an improvement in the spectrum of the currents and voltages, as the lowest frequency is 120 kHz. It is favorable from the passive components volume optimization standpoint.
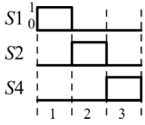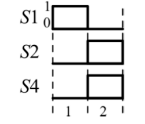
In strategy C3, the measured average value of the output voltage of the converter equals $U_{out} = 185$ V, and for $U_{in} = 50$ V, the voltage ratio is

$$G_{UC3} = \frac{U_{out}}{U_{in}} = \frac{185.0}{50.0} = 3.7 \tag{5}$$

2.2. Switching Strategy Concepts for the LCSCVMb

The LCSCVMb converter is simpler than the LCSCVMa, and contains three switches only. There is only one stage of charging the switched capacitors, realized by the switch S_1, and two possible stages of discharging them, controlled by switches S_2 and S_3. This creates two switching strategies for this converter, which are presented in Table 2. Figures 6 and 7 depict simulation waveforms of the LCSCVMb controlled according to these strategies.

Table 2. Switching strategy concepts of the LCSCVMb. States of switches S_1, S_2, and S_4.

The Concept for Switching Strategy of LCSCVMb		Description—Stages of Charge Transfer in the Converter
Strategy C4		Similarly to strategy C2 for the LCSCVMa, strategy C4 gives the following characteristic in the LCSCVMb: 1. Simultaneous charging of all the switched capacitors 2. Discharging C_1 to the internal branch (C_2) 3. Discharging C_2 and C_3 to the output
Strategy C5		Similarly to strategy C3 for the LCSCVMa, strategy C5 gives the following characteristic in the LCSCVMb: 1. Simultaneous charging of all the switched capacitors 2. Simultaneous discharging of all the switched capacitors and charging the internal branch (C_2)
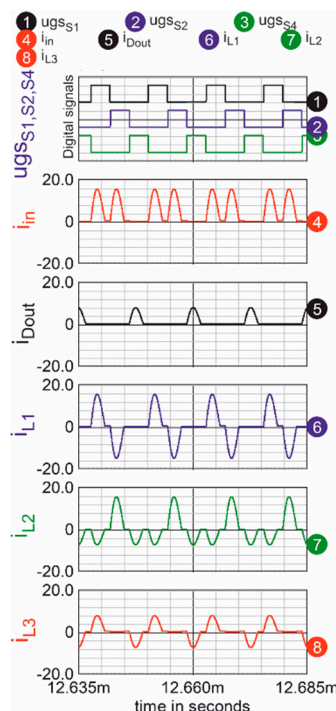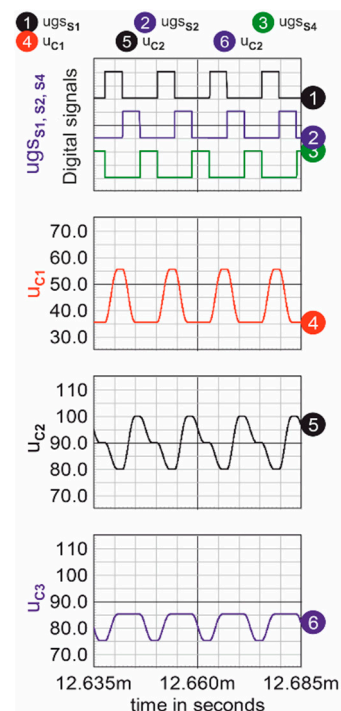
(**a**)　　　　　　　　　　　　　　　　　　　　(**b**)

Figure 6. Steady-state operation of the LCSCVMb converter under switching strategy C4: (**a**) Waveforms of the input current, inductor currents, and the current of the output diode (in amperes). (**b**) Voltages (in volts) on capacitors C_1, C_2, and C_3. The results were obtained with the use of ICAP/4 simulation software.
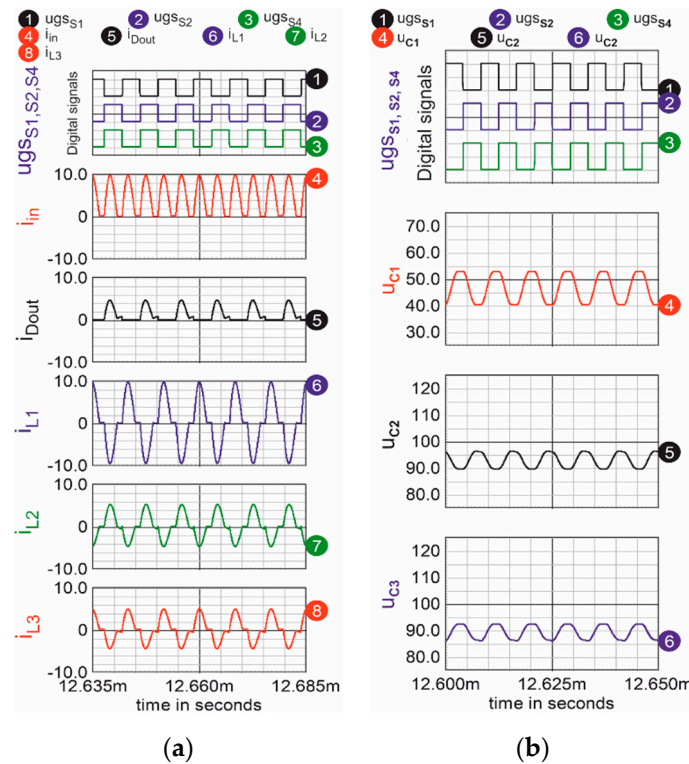
(**a**) (**b**)

Figure 7. Steady-state operation of the LCSCVMb converter under switching strategy C5: (**a**) Waveforms of the input current, inductors currents, and the current of the output diode (in amperes). (**b**) Voltages (in volts) on capacitors C_1, C_2, and C_3. The results were obtained with the use of ICAP/4 simulation software.

2.2.1. Simulation Results of the Switching Strategy C4

Figure 6 presents simulation waveforms of the LCSCVMb controlled according to strategy C4. The current and voltage waveforms in strategy C4 are nearly identical with those in strategy C2.

In this strategy, the measured average value of the output voltage of the converter equals $U_{\text{out}} = 172.1$ V, which yields (for $U_{\text{in}} = 50$ V):

$$G_{UC4} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{172.1}{50.0} = 3.44 \tag{6}$$

2.2.2. Simulation Results of the Switching Strategy C5

Figure 7 presents simulation waveforms for the LCSCVMb controlled according to strategy C5. The current and voltage waveforms of the strategy C5 are nearly identical with those in strategy C3.

In this strategy, the measured average value of the output voltage of the converter equals $U_{\text{out}} = 181.4$ V. For $U_{\text{in}} = 50$ V, the voltage ratio is:

$$G_{UC5} = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{181.4}{50.0} = 3.63 \tag{7}$$

2.3. Comparison among the Topologies and Switching Strategies

In Sections 2 and 2, a significant number of waveforms are presented for the particular strategies. The differences in the waveforms of the currents and voltages are clear, but to compare the concepts of the converters and the switching strategies, the following parameters will be taken into consideration and presented in charts:

- Number of components,
- Voltage gain,
- The lowest frequency in the input current (f_{ac_in}),
- The lowest frequency in the output current (f_{ac_out}),
- Voltage pulsation on capacitors (U_{C1p-p}, U_{C2p-p}, U_{C3p-p}),
- rms values of inductor currents (I_{L1_rms}, I_{L2_rms}, I_{L3_rms}),
- Maximum values of inductor currents (I_{L1_max}, I_{L2_max}, I_{L3_max}),
- Symmetry of inductor currents (Sym_i_L).

The data are presented in Table 3, where the parameters of the SCVM (on the basis of Reference [14] for an appropriate strategy) are included as well.

Table 3. Major parameters comparison among the parameters of LCSCVMa and LCSCVMb converters in the tests of 200 W operation.

Parameter	LCSCVMa Strategy			LCSCVMb Strategy		SCVM
	C1	C2	C3	C4	C5	
No. of switches	4	4	4	3	3	6
No. of diodes	4	4	4	5	5	4
U_{out}, V	178.0	177.0	185.0	172.1	181.4	191.2
T_S, µs	21.0	12.6	8.4	12.6	8.4	8.4
f_{ac_in}, kHz	47.6	79.4	238.1	79.4	238.1	238.1
f_{ac_out}, kHz	47.6	79.4	119.0	79.4	119.0	119.0
U_{C1p-p}, V	21.02	19.41	12.4	19.8	12.6	5.98
U_{C2p-p}, V	21.61	19.41	6.54	19.8	6.65	5.98
U_{C3p-p}, V	16.08	9.7	6.18	9.92	6.29	5.98
I_{L1_rms}, A	6.75	7.25	5.65	7.41	5.75	2.73
I_{L2_rms}, A	6.22	6.28	2.92	6.42	2.97	2.73
I_{L3_rms}, A	4.11	3.63	2.75	3.71	2.80	2.73
I_{L1_max}, A	16.1	14.8	9.46	15.1	9.60	4.57
I_{L2_max}, A	13.2	14.8	5.01	15.2	5.09	4.57
I_{L3_max}, A	12.3	7.43	4.74	7.56	4.80	4.57
Symmetry of current i_{L1}	no	yes	yes	yes	yes	yes
Symmetry of current i_{L2}	no	no	yes	no	yes	yes
Symmetry of current i_{L3}	no	yes	yes	yes	yes	yes

Figures 8–10 present a comparison between the values of parameters of the discussed converters, and the corresponding parameter of the SCVM.
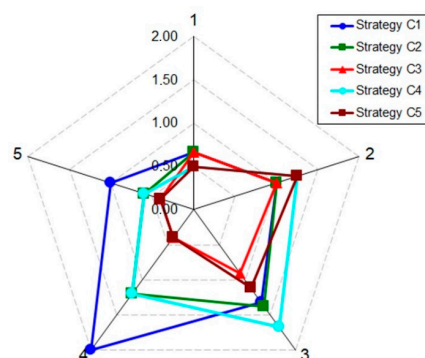

Figure 8. Comparison of converters' parameters under strategies C1–C5: Ratios of number of switches (axis 1) and number of diodes (axis 2) to those in SCVM (on the basis of data in Table 3). Quantity proportional to undesired output voltage decrease: 0.06·(200 − Uout) (axis 3). Ratios of the lowest frequencies in the input and output current: 0.4·f_{ac_in} SCVM/f_{ac_in} (axis 4), 0.4·f_{ac_out} SCVM/f_{ac_out} (axis 5).
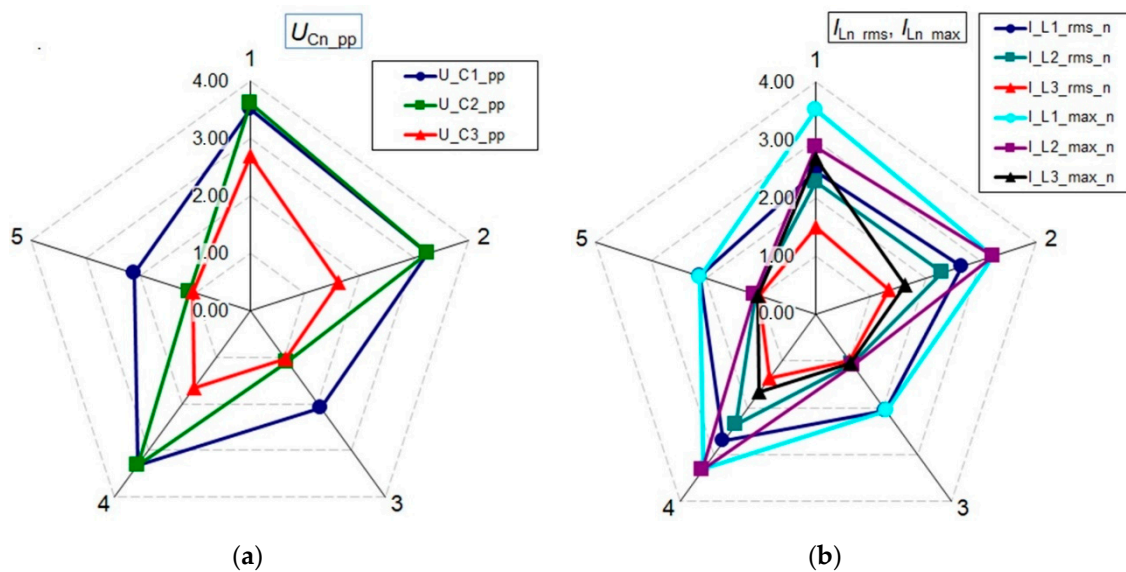
(a)

(b)

Figure 9. Ratios of the following parameters of strategies C1–C5 (axes 1–5): (**a**) Peak-to-peak voltages across capacitors C_1–C_3, (**b**) rms and maximum values of currents in inductances L_1–L_3. The results are based on the data in Table 3.
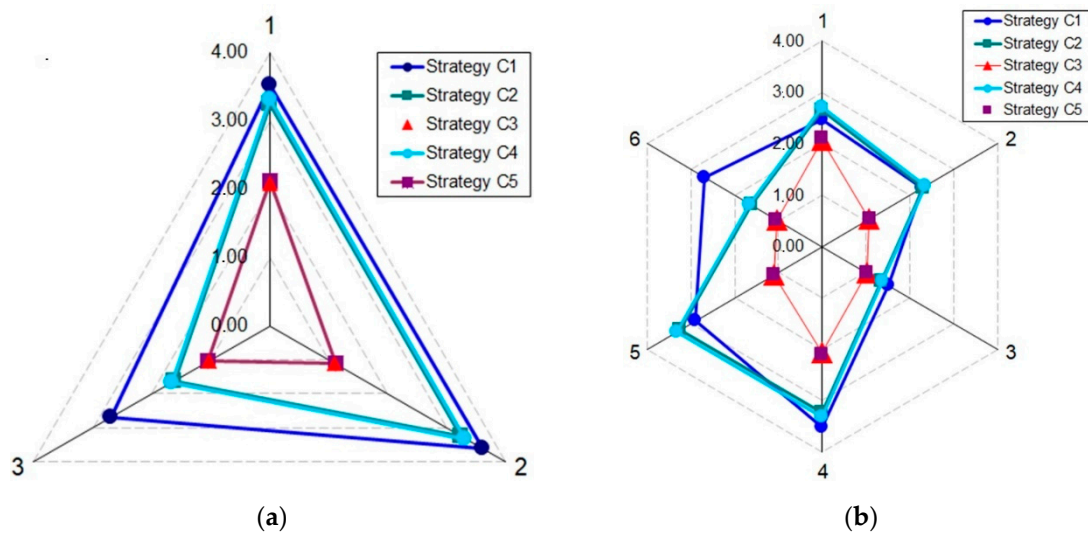

(a)

(b)

Figure 10. Ratios of the following parameters (strategies C1–C5) to the corresponding parameter of SCVM: (**a**) Peak-to-peak voltages across capacitors C_1–C_3, (**b**) rms (axes 1–3) and maximum values of currents in inductances L_1–L_3 (axes 4–6). The results are based on the data in Table 3.

In Figure 8, the coefficients 0.06 and 0.4 are used respectively, to better visualize the undesired output voltage decrease in regard to the theoretical value of 200 V, and the lowest frequencies in the input and output current of the discussed converters compared to those in the SCVM. In each case, a lower value on the graph is better.

From the chart presented in Figure 9a, it follows that the lowest peak-to-peak (p-p) voltages, in all the strategies, are equal the voltage across capacitor C_3. Moreover, the strategies C3 and C5 show the lowest p-p voltages for all the internal capacitors (C_1–C_3). Figure 9b demonstrates that the currents of inductor L_3 are the lowest, and the strategies with the lowest inductor currents are C3 and C5.

The same qualities are visible in charts presented in Figure 10, which clearly demonstrate that the parameters of strategy C4 are nearly the same as those of strategy C2. The same refers to strategies C5 and C3.

The LCSCVMa and LCSCVMb converters can be further extended to units of higher voltage gain, similarly as in the case of the converters presented in References [13,22,25,26,29]. Taking into consideration the number of switches and diodes, as well as the frequency of the input current, both the proposed converters are very attractive for high-voltage-gain (Table 4). It should be noticed that the converter extension is very effective in the case of the LCSCVMb concept. For voltage gain $G_U = 8$, it requires only four switches, which is an excellent result in comparison to other pure SC converters. Other parameters such as voltage stresses on the switches can be found in the literature.

Table 4. Comparison of the number of switches and diodes, and the lowest frequency of the input current in selected topologies versus the voltage gain. Ref. = Reference.

Parameter		Toplogy							
	Gain	LCSCVMa	LCSCVMb	Ref. [13]	Ref. [22]	Ref. [16]	Ref. [25]	Ref. [26]	Ref. [27]
No. of switches (and diodes)	4	4 (4)	3 (5)	6 (4)	8 (0)	-	8 (0)	4 (4)	4 (6)
	7	-	-	12 (7)	14 (0)	7 (5)	-	-	7 (12)
	8	6 (6)	4 (7)	14 (8)	16 (0)	-	12 (0)	6 (6)	8 (14)
f_{iin_min}/f_{Smax} for all gains(f_{Smax}—in (1))		1	1	0.5	1	1/4	1	1	0.5

3. Efficiency Model of the LCSCVM Converters

The analysis below concerns the LCSCVMa operating under the strategy C3 (Table 1) and LCSCVMb operating under the strategy C5 (Table 2). In both cases, there are two stages of operation. Figure 11 depicts the current paths in the LCSCVMa. In the LCSCVMb, the switch S_1 conducts the sum of currents i_{L1} and i_{L3} in the stage 1, whereas the current paths in the stage 2 are the same as in the LCSCVMa.
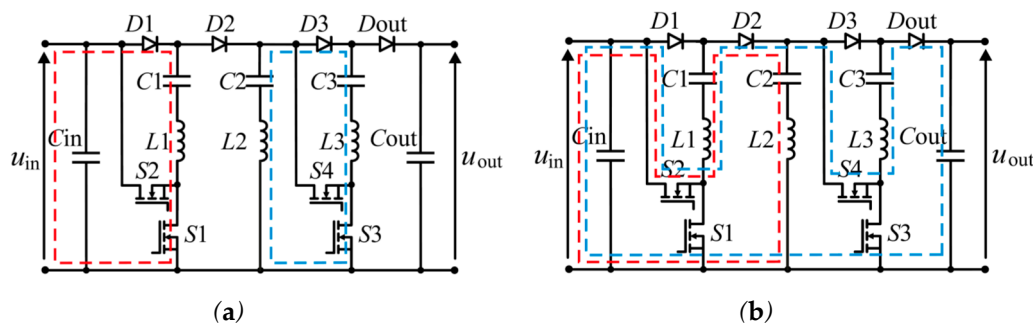

Figure 11. Current paths in the LCSCVMa: (**a**) in the stage 1 and (**b**) in the stage 2.

Assuming ideal power electronic switches, and a constant value of the input (U_{in}) and the output (U_{out}) voltage, as well as neglecting parasitic resistances and voltage drops across the power electronic devices, the currents in the stage 1 (Figure 11a) can be described as follows:

$$i_{L1}(t) = i_{C1}(t) = \frac{U_{in} - U_{C11}}{\rho} \sin\omega_0 t = I_{1m} \sin\omega_0 t \tag{8}$$

$$i_{L3}(t) = i_{C3}(t) = \frac{U_{in} - U_{C11}}{2\rho} \sin\omega_0 t = \frac{I_{1m}}{2} \sin\omega_0 t \tag{9}$$

$$i_{L2}(t) = i_{C2}(t) = -i_{L3}(t) \tag{10}$$

With the characteristic impedance and the angular resonant frequency given by

$$\rho = \sqrt{L/C}, \; \omega_0 = 1/\sqrt{LC} \tag{11}$$

where U_{C11} is the initial voltage across capacitor C_1, and I_{1m} and $I_{2m}/2$ are the current amplitudes. Equation (8) presents the current of a typical series LC circuit supplied from a voltage source, and Equation (9) was obtained also taking into account the initial values of the capacitor voltages.

The values of the passive components depend on the assumed nominal power (P_{nom}), switching frequency (f_S), and the volume of the resonant inductor. The values of time T_{pulse} (1), and finally T_0 (2) and ω_0 (11), are assumed taking into account the limit of the switching losses in the converter. The capacitance of the switched capacitors is determined by the charge required to be transferred in a single switching pulse. The maximum power of the SCVM-type converter is achieved when the switched capacitors are fully discharged in a switching cycle (and then charged to the voltage equal to $2U_{in}$). This determines the minimum capacitance, which in the SCVM composed of n switching cells is defined as follows:

$$C_{min} = 2nf_S U_{in}^2/P_{nom}. \tag{12}$$

In a quasi inductiveless SCVM-type converter, the value of resonant inductance (L) is very small (L can be designed as a PCB air choke). Therefore, to achieve the assumed switching frequency, the capacitance of the switched capacitors can be selected considerably bigger than C_{min} (as in the case of the experimental setup presented in this paper). In the stage 2 (Figure 11b), the currents of capacitors C_1–C_3 and inductances L_1–L_3 have the same values (Equations (8)–(10)) as in the stage 1, but with the opposite signs. The voltages across the capacitors C_1, C_2, and C_3 in the stage 1 are given by

$$u_{C1}(t) = (U_{in} - U_{C11})(1 - \cos \omega_0 t) + U_{C11} \tag{13}$$

$$u_{C2}(t) = -\frac{(U_{in} - U_{C11})}{2}(1 - \cos \omega_0 t) + U_{C21} \tag{14}$$

$$u_{C3}(t) = \frac{(U_{in} - U_{C11})}{2}(1 - \cos \omega_0 t) + U_{C31} \tag{15}$$

where U_{C21} and U_{C31} are the initial voltages across capacitors C_2 and C_3, respectively.

In the stage 2 (Figure 11b), the expressions for voltages have similar forms with appropriate signs and initial values.

Based on the formulas mentioned above, all the voltage initial values and the output voltage can be computed as a function of U_{C11}. For example, we obtain

$$U_{out} = 5U_{in} - U_{C11} \tag{16}$$

U_{C11} can be calculated taking into account (8) and the following relation

$$I_{in-av} = I_{L1av} = \frac{2}{\pi}I_{1m}f_{Sn} = \frac{P_{in}}{U_{in}} \tag{17}$$

$$U_{C11} = U_{in} - \frac{\pi \rho P_{in}}{2f_{Sn}U_{in}} \tag{18}$$

where

$$f_{Sn} = f_S/f_0 \tag{19}$$

From Equations (16) and (18), we have

$$U_{out} = 4U_{in} + \frac{\pi \rho P_{in}}{2f_{Sn}U_{in}} \tag{20}$$

In practical converters, there are voltage drops across the circuit elements like the diodes and the transistors, which result in a variation of the output voltage with power and frequency.

The efficiency of an SCVM-type converter is determined by the resistances of its components, voltage drops on the diodes and transistors, the input voltage, power, and by the relation between the

switching period T_S and period T_0 (2), which can be expressed by f_{Sn} (19). Therefore, it is necessary to calculate the average and rms values of the currents. It is assumed that transistors S_1 and S_3 are IGBTs, and S_2 and S_4 are MOSFETs.

$$I_{D1av} = I_{D2av} = \frac{I_{L1av}}{2} = \frac{1}{\pi}I_{1m}f_{Sn} = \frac{P_{in}}{2U_{in}}, \; I_{D3av} = I_{Dout-av} = \frac{I_{L2av}}{2} = \frac{I_{L3av}}{2} = \frac{I_{L1av}}{4} = \frac{P_{in}}{4U_{in}} \tag{21}$$

$$I_{S2} = \frac{1}{2}I_{1m}\sqrt{f_{Sn}} = \frac{\pi P_{in}}{4U_{in}\sqrt{f_{Sn}}}, \; I_{S4} = \frac{1}{4}I_{1m}\sqrt{f_{Sn}} = \frac{\pi P_{in}}{8U_{in}\sqrt{f_{Sn}}} \tag{22}$$

For the LSCVMa, we have:

$$I_{S1av} = I_{D1av} = \frac{P_{in}}{2U_{in}}, \; I_{S3av} = I_{D3av} = \frac{P_{in}}{4U_{in}} \tag{23}$$

Conduction losses, ΔPc, in both converters are

$$\Delta P_c = \sum_k r_k I_{Sk}^2 + \sum_l \Delta U_{Dl}I_{Dlav} + \sum_m \Delta U_{Sm}I_{Smav} + \sum_n r_T I_n^2 \tag{24}$$

where r_k denotes the total resistance of the branch with MOSFET transistor S_k ($k = 2, 4$), including the resistance of the transistor. ΔU_{Dl} is the voltage drop across diode D_l, ΔU_{Sm} is the voltage drop across IGBT transistor S_m, r_T is the resistance of each circuit with an IGBT transistor, and I_n is its rms current.

It is assumed that the voltage drops across the devices remain constant in the conducting state. We assume that all the resistances and voltage drops are the same, i.e.

$$r_2 = r_4 = r, \; \Delta U_{S1} = \Delta U_{S2} = \Delta U_S, \; \Delta U_{D1} = \Delta U_{D2} = \Delta U_{D3} = \Delta U_{D4} = \Delta U_{Dout} = \Delta U_D \tag{25}$$

The efficiency of the LSCVMa converter can be calculated as follows. The resistive losses in the circuits containing IGBTs are:

$$\Delta P_{c2} = r_T I_{L11}^2 + 2r_T I_{L31}^2 = \frac{3\pi^2 P_{in}^2 r_T}{32U_{in}^2 f_{Sn}} \tag{26}$$

Taking (21)–(26) into account, the conduction losses can be presented as

$$\Delta P_c = \frac{5\pi^2 P_{in}^2 r}{64U_{in}^2 f_{Sn}} + \frac{3\pi^2 P_{in}^2 r_T}{32U_{in}^2 f_{Sn}} + \frac{3P_{in}}{2U_{in}}\left(\Delta U_D + \frac{1}{2}\Delta U_S\right) \tag{27}$$

The turn-off switching loss is zero, due to the ZCS switching. However, there is a turn-on switching loss, associated with charging and discharging the transistors' output capacitances. The total switching power loss, ΔP_{sw}, is

$$\Delta P_{sw} = \Delta W_{sw}f_S = \Delta P_{sw0}f_{Sn} \tag{28}$$

where ΔW_{sw} is the energy lost at turn-on in the transistor's resistances in a single switching cycle, and $\Delta P_{sw0} = \Delta W_{sw} \cdot f_0$ is power loss at resonant frequency. A way of calculating these losses is presented in Reference [31].

The efficiency is (Equations (27) and (28))

$$\eta = 1 - \frac{\Delta P_c}{P_{in}} - \frac{\Delta P_{sw}}{P_{in}} = 1 - \frac{5\pi^2 P_{in}^2 r}{64U_{in}^2 f_{Sn}} - \frac{3\pi^2 P_{in}^2 r_T}{32U_{in}^2 f_{Sn}} - \frac{3P_{in}}{2U_{in}}\left(\Delta U_D + \frac{1}{2}\Delta U_S\right) - \frac{\Delta W_{sw}f_S}{P_{in}} \tag{29}$$

Introducing normalized quantities:

$$r_n = \frac{r}{U_{in}^2/P_{in}}, \; r_{Tn} = \frac{r_T}{U_{in}^2/P_{in}}, \; \Delta U_{Dn} = \frac{\Delta U_D}{U_{in}}, \; \Delta U_{Sn} = \frac{\Delta U_S}{U_{in}}, \; \Delta P_{sw0n} = \frac{\Delta P_{sw0}}{P_{in}} \tag{30}$$

We can simplify the efficiency formula to the form

$$\eta = 1 - \frac{5\pi^2 r_n}{64 f_{Sn}} - \frac{3\pi^2 r_{Tn}}{32 f_{Sn}} - \frac{3}{2}\left(\Delta U_{Dn} + \frac{1}{2}\Delta U_{Sn}\right) - \Delta P_{sw0n} f_{Sn} \tag{31}$$

The efficiency of the LSCVMb can be calculated with the use of the following components:

$$I_{S1av} = I_{D1av} + I_{D3av} = \frac{3P_{in}}{4U_{in}}, \; I_{D4av} = I_{D1av} = \frac{P_{in}}{2U_{in}} \tag{32}$$

where D_4 is the LSCVMb additional diode (Figure 1b).

Conduction losses, ΔPc, of LSCVMb are as follows:

$$\Delta P_c = \frac{5\pi^2 P_{in}^2 r}{64 U_{in}^2 f_{Sn}} + \frac{3\pi^2 P_{in}^2 r_T}{32 U_{in}^2 f_{Sn}} + \frac{P_{in}}{U_{in}}\left(2\Delta U_D + \frac{3}{4}\Delta U_S\right) \tag{33}$$

and the efficiency of the LSCVMb is

$$\eta = 1 - \frac{5\pi^2 r_n}{64 f_{Sn}} - \frac{3\pi^2 r_{Tn}}{32 f_{Sn}} - \left(2\Delta U_{Dn} + \frac{3}{4}\Delta U_{Sn}\right) - \Delta P_{sw0n} f_{Sn} \tag{34}$$

It can be seen from (30), (31), and (34) that the impact of the voltage drops across the diodes on the efficiency depends only on the ratio of these voltage drops to the supply voltage. The impact of the losses in the resistances is more complex. They increase with rising resistances and rising power, and decrease with rising input voltage and frequency f_S. Switching losses are proportional to switching frequency f_S.

The relationship between the efficiency and normalized frequency $f_{Sn} = f_S/f_0$ for three values of r_n (30): 0.016, 0.0304, and 0.040, ΔU_{Dn} (30) = 0.008 for the LCSCVMa and the LCSCVMb is shown in Figure 12. The value of $r_n = 0.0304$ corresponds to, e.g., $U_{in} = 50$ V, $P_{in} = 200$ W, $L = 500$ nH, $C = 1.5$ μF, $r = 380$ mΩ, and ΔU_{Dn} is equal to 0.008 for, e.g., $\Delta U_D = 0.40$ V and $U_{in} = 50$ V. The value of relative switching losses P_{sw0n} (30) = 0.0101 (Figure 12b) is valid, e.g., for ΔW_{sw} (28) = 11 μJ, $f_0 = 183.8$ kHz, and $P_{in} = 200$ W. The efficiency of the LCSCVMb is slightly lower. In both cases, it increases with increasing normalized frequency, f_{Sn}, and strongly depends on the circuit parasitic resistances. Therefore, it is important to minimize them, and use transistors with low values of $R_{DS(on)}$ and $V_{CE(on)}$.
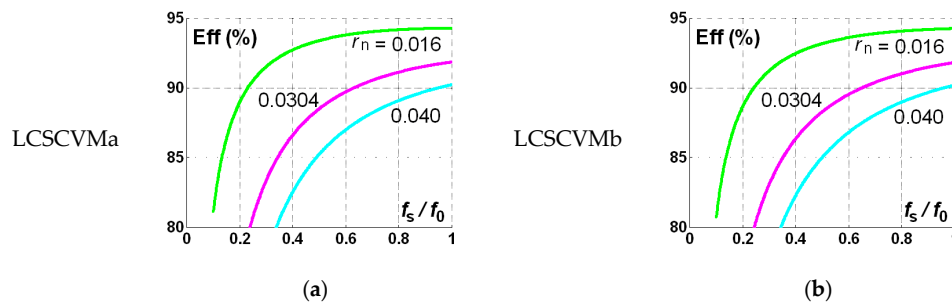

Figure 12. Theoretical charts of efficiency vs. $f_{Sn} = f_S/f_0$ for three values of r_n: 0.016, 0.0304, and 0.040, and $\Delta U_{Dn} = 0.008$: (**a**) LCSCVMa at switching losses $\Delta P_{sw0n} = 0.0138$, (**b**) LCSCVMb at switching losses $\Delta P_{sw0n} = 0.0101$.

The efficiency can be computed in a similar way for the other switching strategies. However, the calculations will be more complex in the case of the strategies with more than 2 stages.
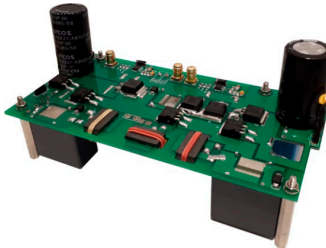
4. Experimental Verification

This chapter presents the experimental results of the LCSCVMb converter operation. All the tests were carried out under switching strategy C5. The experimental verification confirms the proper operation of the converter, according to its concept. The measured voltage gain was on the expected level, and all the relevant waveforms were consistent with the simulation results as well.

4.1. Experimental Setup

All the parameters of the converter used during the experimental research, as well as a photograph of the investigated converter, are collected in Table 5. The parameters of the experimental setup correspond to the simulation model, and the major difference can be found in the inductance of the planar PCB choke. The switching frequency in the experimental measurements has been adjusted to the oscillation period of the switched capacitor currents and differs from the value selected for the simulation tests. An IGBT switch was selected as S_1 in the LSCVMb, as this switch conducts the total charging current. This current can be significant, especially when the converter contains a larger number of the switching cells. In order to generate appropriate control signals, an FPGA evaluation board (INTEL DE0) was utilized. The basic clock frequency of this device was set at 200 MHz, and the time resolution of the generated signals was 5 ns. The test setup is an example design of the converter prepared for the purpose of research, to verify its concepts and feasibility. The tests were conducted with 50 V at the input; however, the voltage range as well as power and the design concept can be rescaled to the parameters of a target application. Moreover, it is important that the prospective applications of the non-isolated DC-DC converter should comply with safety standards.

Table 5. The most important parameters of the laboratory converter.

Parameter	Value	The Laboratory Setup
Input voltage	50 V	
Output load	200 W	
Switching frequency	133 kHz	
Resonant capacitors	1.5 µF (KEMET R76 series)	
Resonant inductances	Planar chokes: L = 500 nH, R_{ESR} = 18 mΩ @ 100 kHz	
Transistors	IKB15N65EH5 (V_{DS} = 650 V, V_{CE} = 1.65 V) as S_1 IPB50R140CP (V_{DS} = 550 V, R_{DSon} = 0.14 Ω) as S_2 and S_4	
Diodes	STTH30L06G (I_F = 30 A, V_F = 1.0 V, V_{RRM} = 600 V)	
PCB	2 layers, 35 µm	
Laboratory equipment	Digital scope: Tektronix MDO3104, current probes: Tektronix TCP0030 150 MHz (input current measurement), Rogowsky coil (switch current measurements) voltage probes: Tektronix THDP0200 200 MHz, Tektronix P5205 100 MHz, power analyzer: Yokogawa WT 1801	

4.2. Test Results

Figure 13a,b presents the waveforms of the switching signals with the input and output current. They confirm that the converter operates correctly according to strategy C5. From the waveforms presented in Figure 13c, it follows that the converter boosts the input voltage. The measured voltage ratio is 3.65. Figure 13d,e presents the input current waveform and the voltages across the resonant capacitors. From the waveforms presented in Figure 13d, the average voltage across the capacitors can be seen. To demonstrate more clearly the magnitude of the oscillation around the average voltage value of each resonant capacitor, the voltage traces in AC coupling mode were recorded as well (Figure 13e). Figure 13f presents voltage stresses across the switches. From these results, it follows that the voltage

stresses on switches are significantly below the output voltage of the converter, which is very favorable from the switching losses standpoint.
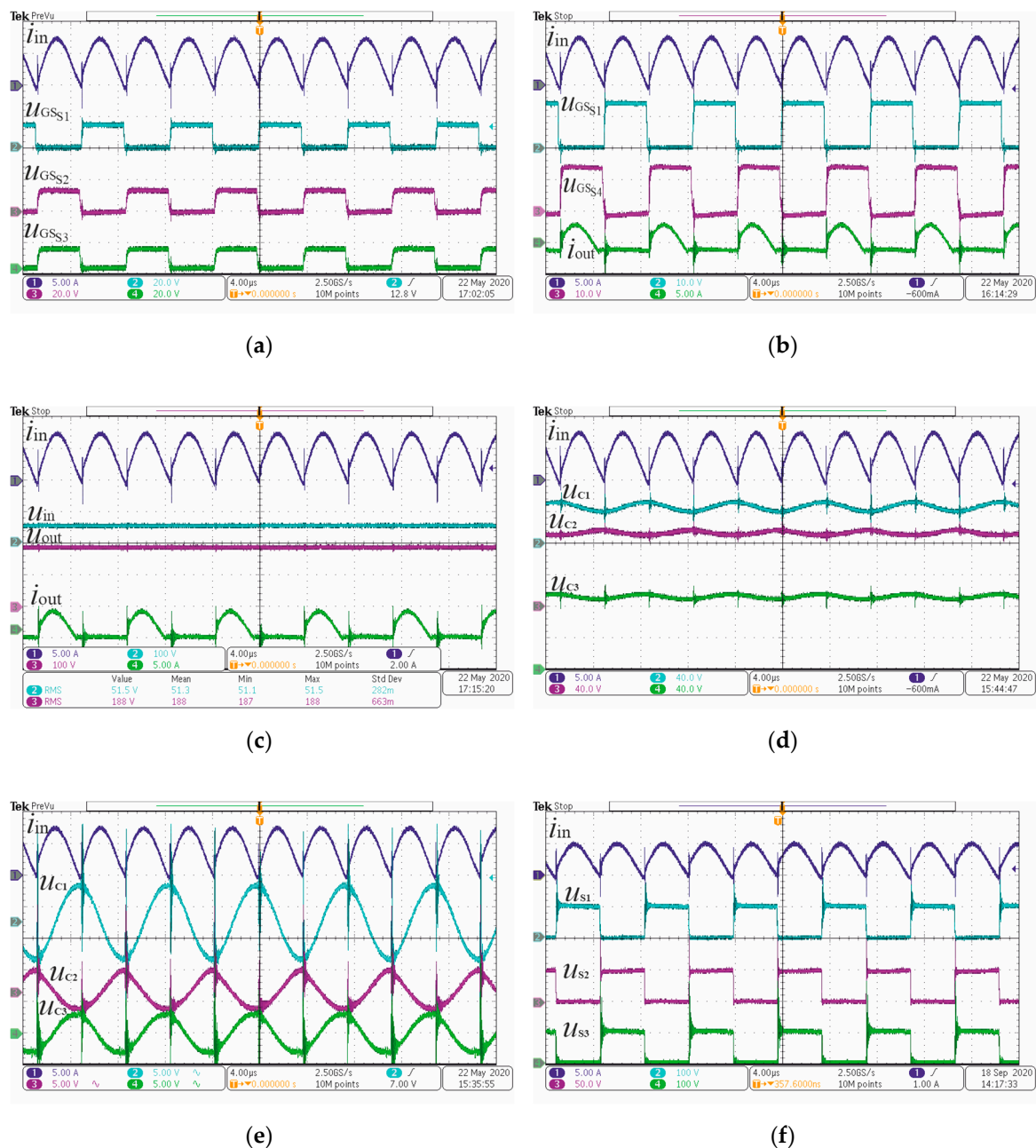

Figure 13. A set of recorded waveforms during experimental tests: (**a**) Switching signals of transistors and the input current, (**b**) input and output current of the converter on the background of switching signals, (**c**) input and output waveforms of the converter (current and voltage traces), (**d**) converter input current and voltages across resonant capacitors recorded in DC coupling mode, (**e**) converter input current and voltages across resonant capacitors recorded in AC coupling mode, and (**f**) voltage stresses across the switches on the background of converter input current. Switching strategy C5.

During the experimental research, the basic operation concept of the investigated converter has been checked. Furthermore, the working correctness of the examined device under different output loads was verified. The tests were carried out for three output load values: 62, 146, and 290 W, focusing especially on the transistor currents and voltages. Figure 14 present the results of the conducted tests

for different output load conditions. From the results, it follows that the converter operates properly in low and medium load conditions.
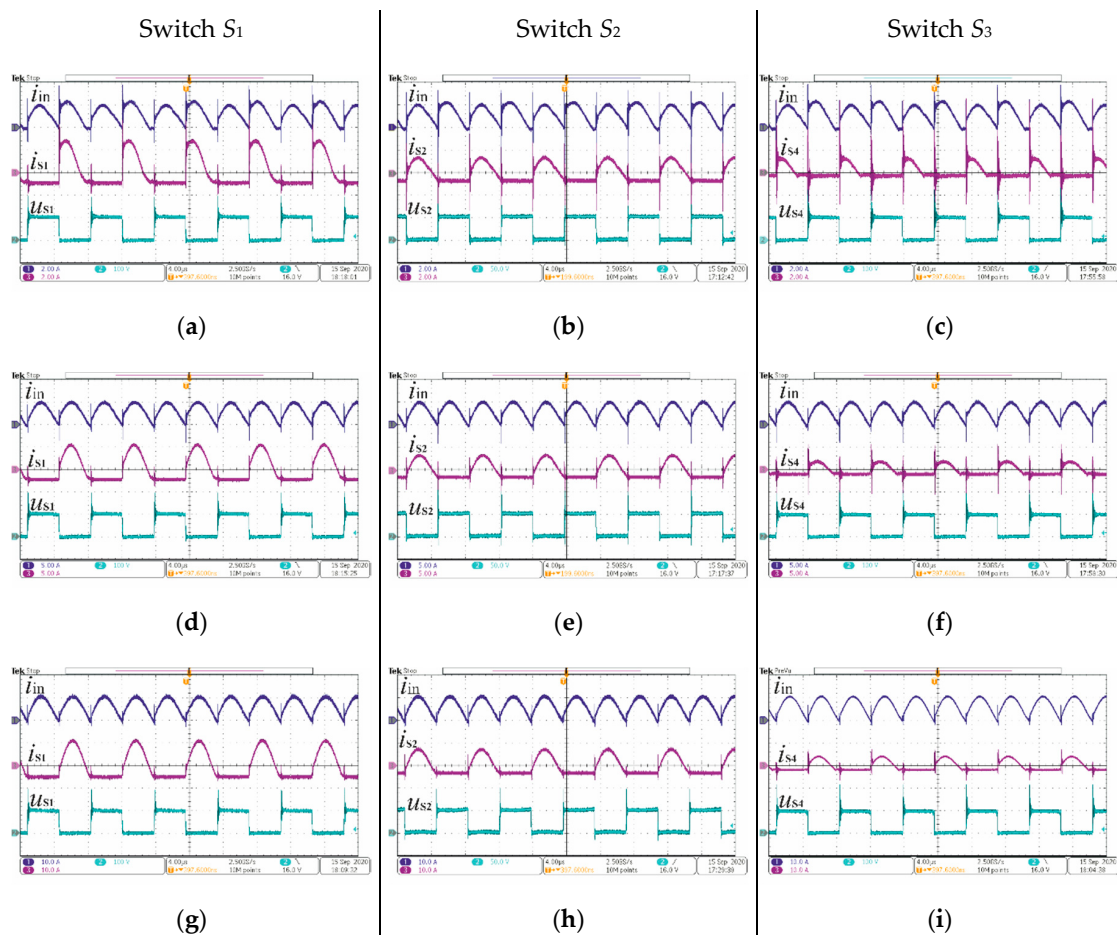
Switch S_1	Switch S_2	Switch S_3
(a)	(b)	(c)
(d)	(e)	(f)
(g)	(h)	(i)

Figure 14. Waveforms of the input current as well as the currents and voltages across switches, during experimental test proceeded with different values of converter output power: (**a**–**c**) P_{out} = 62 W, 2A/div, 100V/div, (**d**–**f**) P_{out} = 146 W, 5A/div, 100V/div, (**g**–**i**) P_{out} = 290 W, 10A/div, 100V/div. Switching strategy C5.

Figure 15 presents the results of the spectral analysis calculated for the input and output currents. The calculations have been carried out with the use of MATLAB software, based on the recorded experimental data. The data was collected by the digital oscilloscope (Tektronix MDO3104) with the sampling rate of 1 MS/s.
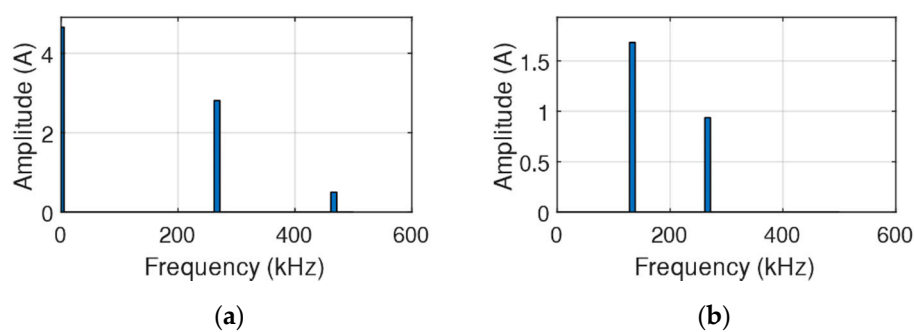
Figure 15. Results of spectral analysis for: (**a**) The input current and (**b**) the output current.

The experimental results of the output voltage of the LCSCVMb converter and its efficiency are presented in Figure 16. The efficiency is on an acceptable level. The voltage and efficiency drop versus power is typical for such SC-based converters, and results from their resistive losses. It should be noticed that the presented experimental setup is optimized towards the converter cost reduction. It was designed on a two-layer PCB of 35 μm. To increase the efficiency by reducing the parasitic resistance, a more expensive PCB and switches can be selected.
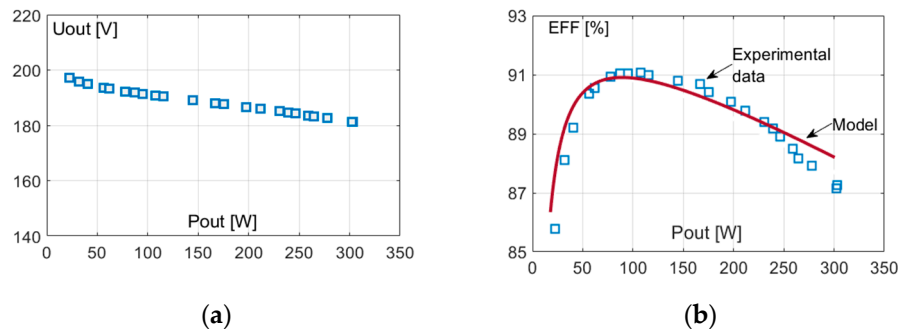

(a) (b)

Figure 16. Experimental and simulation results for LSSCVMb under strategy C5 at U_{in} = 50 V, f_S = 133 kHz: (**a**) Measured output voltage U_{out} vs. P_{out}, (**b**) measured efficiency vs. P_{out} with comparison to theoretical results obtained from (34) for r = 380 mΩ, V_F = 400 mV, $V_{CE(on)}$ = 1 V, W_{sw} = 11 μJ.

5. Conclusions

The presented concepts of the new topologies, as well as the comparison of parameters presented in Table 3, and charts in Figures 8–10, lead to the following conclusions:

- The major idea of the proposed new converters is based on the elimination of the number of switches in a voltage multiplier (SCVM), while maintaining its proper operation. By the modification of an SCVM, the new topology concepts LCSCVMa and LCSCVMb were proposed, with a reduced number of switching cells and redesigned functions of the diodes. Depending on the technology of practical implementation, either of these converters can be more attractive than the other.
- Various switching strategies are possible for the converters, which affect the parameters of operation related to switching losses and the sizing of the passive components of the converter, but also the required input and output filters.
- The converter operates properly with a wide range of output loads.
- From the compared results, it follows that the most effective topology, the LCSCVMb, can operate with nearly the lowest parameters of AC component in the voltages on capacitors, and the highest frequency in the input and output current. This allows for a reduction of the converter volume, especially by optimizing the input and output filters.
- The discussed converters demonstrated an improvement in the SCVM topology, which may result in a prospective cost reduction.

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