



Article An Analytical Approach for Design of a Cross-Connected Fibonacci Switched Capacitor Converter

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Abstract: Switched capacitor converters (SCCs) are used for low-power applications because they are designed without magnetic components. Among various types of SCCs, the Fibonacci SCC (FSCC) features a small size and high voltage gain. However, the FSCC performance can be more improved, which leads to suggest a cross-connected FSCC (CCFSCC). However, in the considered four-terminal equivalent circuit model for analyzing the CCFSCC, some circuit parameters, such as the operation frequency and capacitor capacitance of the SCC are neglected. In this paper, we propose an analytical approach to optimize the CCFSCC circuit parameters by deriving its voltage gain function. The validity of the addressed methodology is confirmed by comparing the outcomes with the results of simulations and experiments. It is shown that the average errors between the calculated and experimental voltage gains are 9%, and the average absolute errors between the calculated and simulated ones are under 0.1.

Keywords: switched capacitor converter; modeling; optimization

1. Introduction

Switched capacitor converters (SCCs) have been utilized for low-power applications such as wearable devices and energy harvesting systems [1–10]. This is because the SCCs do not have magnetic components and it reduces their sizes and weights [11]. Up to now, various kinds of SCCs have been suggested and developed, e.g., Dickson [12,13], series-parallel [14–16], multilevel modular [17–19], Fibonacci [20–22], etc. The Fibonacci SCC (FSCC) can provide high boosted output with the smallest size [23–25]. However, the output ripple voltage, power efficiency, and conversion ratio of the FSCC can be improved. For this reason, a cross-connected Fibonacci switched capacitor converter (CCFSCC) was suggested and analyzed in recent studies [26,27]. By merging two FSCCs and cross-connecting them, the CCFSCC generates its boost conversion ratio of 2^{2n-1} with a smaller output ripple voltage, where *n* is the stage of charging cells consisting of three switches and one capacitor.

The CCFSCC in [26,27] was analyzed based on a four-terminal equivalent circuit model [28], in which the analysis neglects circuit parameters such as its operation frequency and capacitances of capacitors. Some analysis methods consider these parameters, e.g., slow and fast switching limit model [29–31] and charge-balance transient method [32–34]. In [29–31], a target circuit is modeled with an assumption of its 50% duty ratio. In addition, this method neglects analysis parameters such as on-resistors of switches and variation in voltages of capacitors. In [32–34], an SCC is examined based on the fundamental circuit laws such as Kirchhoff's voltage law (KVL), Kirchhoff's current

law (KCL), and RC network solving methods. This analysis method can accurately model the SCCs compared with their simulations. However, the method in [32–34] calls for complex calculations as circuit components increase because all of capacitors' voltages must be derived.

In this paper, we suggest an analytical technique, maintaining its simplicity by using proper approximations, as well as its accuracy by solving differential equations of RC networks. The proposed analysis derives the voltage gain function of the CCFSCC, which can provide a standard for the circuit component selection when its hardware is designed. The validity of the proposed analysis method was confirmed by comparing it with the results of both simulations and experiments.

The rest of this paper is organized as follows. Section 2 explains the circuit configuration of the CCFSCC. Section 3 shows the proposed analysis method and provides a guidance to select values of circuit components for the CCFSCC as a target. In addition, the stability of the CCFSCC is checked in Section 3. In Section 4, we compare the derived voltage gain function with simulated and experimental results. Lastly, we conclude this paper and discuss our future study in Section 5.

2. Circuit Configuration

Figure 1 shows the cross-connected Fibonacci switched capacitor converter (CCFSCC) with its four times step-up mode, where V_{in} is the average input voltage, V_{out} is the average output voltage, *S*1 and *S*2 are semiconductor switches, $C_i(i = 1, 2, a, b)$ are flying capacitors, R_L is the load resistor, and C_L is the output capacitor [27]. The CCFSCC consists of two cross-connected FSCCs (Cells 1 and 2). It is operated by turning on and off switches (*S*1 and *S*2). They are controlled by the pulse width modulation (PWM) signals (Φ_1 and Φ_1) with its dead-time, as described in Figure 2, where S_1 and S_2 are for State-1 and State-2, *T* is the operation period during one cycle, and *D* is its duty ratio. In terms of the duty ratio *D*, the CCFSCC features a symmetric construction. Therefore, the duty ratio *D* is designated as 50%.



Figure 1. Four times step-up CCFSCC.



Figure 2. PWM signals for operation of CCFSCC.

Figure 3 describes instantaneous equivalent circuits in steady-state at State-1 and State-2, where R_{on} s are the on-resistors of the switches and I_i and I_o are the input and output currents, respectively. In steady-state, if there is no power loss, capacitors C_1 and C_a are charged up to the input voltage V_{in} . Then, each of them charges capacitors C_2 and C_b up to $2V_{in}$. Finally, these capacitors charge the output capacitor C_L up to $4V_{in}$. In the next section, the CCFSCC is theoretically analyzed.



Figure 3. Instantaneous equivalent circuits in steady state during one operating cycle.

3. Theoretical Analysis

3.1. Voltage Gain Function

In this subsection, an analysis is conducted with some the assumptions that the dead time is zero and the output capacitor has no influence on the output voltage, and this analysis focuses on the CCFSCC in steady state [26,27].

By using KCL and KVL in the instantaneous equivalent circuit at State-1 in Figure 3a, Equations (1)–(3) are derived, where *R* is the resistance of on-resistors, C_f is the capacitance of flying capacitors, and $V_{C_x}(x = 1, 2, a, b)$ are the voltages of the capacitors [26,27].

$$C_f \frac{dV_{C_a}}{dt} = -C_f \frac{dV_{C_b}}{dt} + C_f \frac{dV_{C_2}}{dt}.$$
 (1)

$$-V_{in} - RC_f \frac{dV_{C_a}}{dt} + RC_f \frac{dV_{C_1}}{dt} + V_{C_1} + RC_f \frac{dV_{C_1}}{dt} = 0.$$
(2)

$$-2RC_f \frac{dV_{C_b}}{dt} - V_{C_b} - 2RC_f \frac{dV_{C_2}}{dt} - V_{C_2} + V_o = 0.$$
(3)

Considering the symmetric structure of the CFSCC and using Equation (3), the output voltage is obtained as Equation (4). From Equation (4), the output voltage can be approximately rewritten as Equation (5), where $V_{C_{x,min}}$ and $V_{C_{x,max}}$ (x = 1, 2, b) are the minimum and maximum voltages of the capacitors. If this approximation is not conducted, all of the minimum and maximum voltages of the capacitors should be derived such as in the method in [32–34].

$$V_o = V_{C_2} + V_{C_b}.$$
 (4)

$$V_o \approx \frac{V_{C_{2,min}} + V_{C_{2,max}}}{2} + \frac{V_{C_{b,min}} + V_{C_{b,max}}}{2} \approx 2\left(V_{C_{1,min}} + V_{C_{1,max}}\right).$$
(5)

By using Equation (2), the relation of C_1 voltage and input source during State-1 can be expressed as given in Equation (6).

$$V_{C_1}(t) = \left(V_{C_{1,min}} - V_{in}\right) e^{-\frac{1}{3RC_f}t} + V_{in}.$$
(6)

From Equation (6), the maximum voltage of C_1 at $t = \frac{T}{2}$ is given by Equation (7).

$$V_{C_{1,max}} = \left(V_{C_{1,min}} - V_{in}\right) e^{-\frac{1}{3RC_f}\frac{T}{2}} + V_{in}.$$
(7)

From the symmetric structure of the CFSCC, the average output current can be rewritten as Equation (8).

$$I_o T = \frac{V_o}{R_L} T = C_f \left(V_{C_{1,max}} - V_{C_{1,min}} \right).$$
(8)

Solving a linear equation consisting of Equations (7) and (8), minimum voltage of C_1 is obtained, as presented in Equation (9).

$$V_{C_{1,min}} = \frac{T}{R_L C_f (K-1)} + V_{in},$$
(9)

where $K = e^{-\frac{1}{3RC_f}\frac{T}{2}}$.

By substituting the maximum and minimum voltages of C_1 and Equations (7) and (9) into Equation (5) and rearranging the result, the voltage gain function, g, of the CFSCC is obtained, as given in Equation (10).

$$g = \frac{V_o}{V_{in}} = \frac{4}{-\frac{4T}{R_L C_f (K-1)} - \frac{2T}{R_L C_f} + 1}.$$
(10)

3.2. Optimization

For efficient design and desirable operation of the CCFSCC, it is required to select proper values of circuit parts such as capacitances of its capacitors and operation frequency. In this subsection, an optimization approach for appropriate values of circuit parts is conducted based on the voltage gain function presented in Equation (10).

The optimization is implemented with the default set-up shown in Table 1. Fixing the default setting, the proper value is decided by tuning the target parameter.

Table 1. Circuit parameters for optimization.

Parameters	Value
Vin	5 V
C_{f}	4.7 μF
C_L	4.7 μF
T	$4 \mathrm{ms}$
Ron	11Ω
R_L	$1 \mathrm{k} \Omega$

3.2.1. Operation Frequency

When an operation frequency for a power converter is selected, circuit designers should consider the influence on the voltage gain as well as charging time constants of flying capacitors. In terms of the time constant, the flying capacitors can be charged up to over 95% of their fully-charged voltage as long as the operation period is over three times the charging time constant.

In the case of the CCFSCC, the boundary of the time constant can be set up to $9R_{on}C_f$, because all flying capacitors have the same charging time constants according to Equation (5).

The voltage gain regulations at different operation frequencies is shown in Figure 4, where the range of the frequency is from 10 Hz to 10 kHz. In this case with the default set-up, selecting the frequency over 1 kHz makes the voltage gain on a stable condition. The higher limit of the frequency should be selected by falling and rising times of the switches.



Figure 4. Voltage gain regulations at different frequencies.

3.2.2. Flying Capacitors Capacitance

The voltage gain function provides only the lower limit of the capacitance. Its higher limit should be considered regarding the operation frequency because of its impact on the charging time constant.

In the example case with the default set-up, the voltage gain regulations at different capacitances from 0.1 nF to 1 μ F is illustrated in Figure 5. This figure states that the voltage gains with the capacitances higher than 0.1 μ F are stable. To maintain 95% of the fully charged voltage, the capacitance is required to be lower than $\frac{T}{18R_{on}}$. With these conditions, the appropriate capacitance range can be expressed as follows

$$0.1 \ \mu F < C_f < 20.2 \ \mu F. \tag{11}$$



Figure 5. Voltage gain regulations at different flying capacitors capacitances.

3.2.3. Output Capacitor Capacitance

The output capacitor of a practical CCFSCC is charged during State-1 and State-2 and discharged during dead-times. This operation causes the output ripple voltage. The instantaneous circuit during the dead-times is shown in Figure 6. The output ripple voltage is the difference between the maximum and minimum output voltages. Therefore, deriving the output ripple voltage is implemented with an assumption that the maximum output voltage of the CCFSCC is approximately gV_{in} . From this assumption, the output ripple voltage, $V_{o,ripple}$, can be expressed as Equation (12).

$$V_{o,ripple} = V_{o,max} - V_{o,min} = gV_{in} - V_{o,min} = gV_{in} - gV_{in}e^{-\frac{1}{R_{L}C_{L}}},$$
(12)

where $V_{o,min}$ is derived from the instantaneous circuit in Figure 6.

Using the ripple voltage of Equation (12) and the default set-up, the output ripple voltage at different capacitances of the output capacitor (from 0.1 nF to 1 μ F) is shown in Figure 7. The waveform in Figure 7 can provide the lower limit of the output capacitor capacitance. The range of the output capacitor capacitance can be expressed as follows

$$C_f > 0.1 \mu F. \tag{13}$$



Figure 7. Output ripple voltages at different capacitances of the output capacitor.

3.3. Power Stage Transfer Function

Generally, stability of a power converter is judged by deriving and analyzing its power stage transfer function [35–37]. The power stage transfer function of the CCFSCC is obtained in this subsection by directly modeling it in z-domain. This modeling is conducted with consideration of the dead time.

During State-1, the flying capacitors (C_1 and C_b) and the output capacitor C_L are charged. The others are discharged. The voltages across C_1 and C_b are approximately V_{in} and $2V_{in}$, and the voltage across C_L is the same as the output voltage, V_o . Therefore, the charged and discharged charges (Q_{char} and Q_{dis}) at (n - 1)T can be derived as Equations (14) and (15), respectively.

$$Q_{char}\left((n-1)T\right) = 3C_f V_{in}\left((n-1)T\right) + C_L V_o\left((n-1)T\right).$$
(14)

$$Q_{dis}((n-1)T) = 2C_f V_{in}((n-1)T).$$
(15)

During the dead-time, the discharged charge ($Q_{dis,dead}$) is also obtained, as given in Equation (16).

$$Q_{dis,dead}\left(nT\right) = C_L V_o\left(nT\right). \tag{16}$$

In agreement with the charge conservation law, the net current on the flying capacitors should be the same as the output current during one operating period T. This can be expressed as Equation (17).

$$\frac{C_f V_{in} \left((n-1)T \right) + C_L V_o \left((n-1)T \right) - C_L V_o \left(nT \right)}{\frac{T}{2}} = \frac{Vo \left((n-1)T \right)}{R_L} + \frac{Vo \left(T \right)}{R_L}.$$
 (17)

By rearranging and z-transforming Equation (14), the power stage transfer function is given by Equation (18).

$$\frac{V_o}{V_{in}} = \frac{\frac{C_f}{C_L + \frac{T_{ioal}}{2R_L}}}{z - \frac{C_L - \frac{T_{ioal}}{2L}}{C_L + \frac{T_{ioal}}{2R_L}}}.$$
(18)

Equation (18) has only one pole at $\frac{C_L - \frac{T_{toal}}{2_L}}{C_L + \frac{T_{toal}}{2_{R_L}}}$, and this leads the CCFSCC to stably operate unless a low-frequency pole is added to its control loop [38–40].

4. Simulation, Experiment and Comparison

4.1. Simulation Result

To confirm the reliability of the proposed model, the CCFSCC was simulated through the SPICE simulation with the given parameters in Table 2. In this simulation, ideal capacitors and resistors without parasitic components were used. Figure 8 shows the simulated voltage gain regulations at different load register values.



Figure 8. Simulated voltage gains at different load values.

Parameters	Value
Vin	5 V
C_{f}	$4.7 \mu\text{F}$
C_L	4.7 μF
T	4 ms
Ron	11Ω
R.	$180\ \Omega, 200\ \Omega, 300\ \Omega, 510\ \Omega, 680\ \Omega, 750\ \Omega, 1\ k\Omega, 2\ k\Omega, 3\ k\Omega, 4.7\ k\Omega, 5.6\ k\Omega, 6.8\ k\Omega,$
кL	7.5 kΩ, 8.2 kΩ, 9.1 kΩ, 15 kΩ, 18 kΩ, 27 kΩ, 39 kΩ, 51 kΩ, 68 kΩ, 100 kΩ

 Table 2. Circuit parameters for simulation.

4.2. Experimental Result

To affirm the accuracy of the proposed model, an experimental test was implemented with the circuit components in Table 3 and the experimental set-up shown in Figure 9a. In Table 3, T_{on} is the on-time of the switches and T_{dead} is the dead-time. Figure 9b shows the prototype configuration of the CCFSCC. The CCFSCC is operated by the PWM signals, as shown in Figure 9c. Figure A1 describes the measured output voltages with the input voltage and the PWM signals at different load values (from 180 Ω to 15 k Ω). In Figure A1, yellow signals are output voltages, green signals are input voltages, and other signals are PWM signals.



(a) Experimental set-up.



(b) CCFSCC prototype.

Figure 9. Cont.



(c) PWM signals.

Figure 9. Experimental test.

Parts and Parameters	Value
V _{in}	5 V
C_{f}	4.7 μF
C_L	4.7 μF
T	4.9 ms
T _{on}	2 ms
T _{dead}	0.45 ms
Ron	11 Ω
Switch	AOW217
Microcontroller	LPC1768
R_L	180 Ω, 200 Ω, 300 Ω, 510 Ω, 680 Ω, 750 Ω, 1 kΩ, 2 kΩ, 3 kΩ, 4.7 kΩ, 5.6 kΩ, 6.8 kΩ, 7.5 kΩ, 8.2 kΩ, 9.1 kΩ, 15 kΩ, 18 kΩ, 27 kΩ, 39 kΩ, 51 kΩ, 68 kΩ, 100 kΩ

4.3. Comparison of Calculation, Simulation and Experimental Results

Figure 10 illustrates the calculated, simulated, and experimental voltage gain regulations at different load values. The average errors between the calculated and simulated voltage gains is 6.9% on average. The difference of average errors between the proposed approach and the experiments is 9%, the details of which are as follows: 30.39% (the calculations and the experiments) and 21.39% (the simulations and the experiments) on average. However, the curve of the calculated voltage gains follows closely the simulated and experimental ones as the load values increase. Additionally, the average absolute errors of the voltage gains are as follows: 0.42 (the calculations and the experiments), 0.33 (the simulations and the experiments), and 0.09 (the calculations and the simulations).



Figure 10. Comparison of the calculated, simulated, and experimental voltage gains at different load values.

4.4. Comparison with Existing Methods

Figure 11 describes the comparison of voltage gains by the proposed approach and existing methods in [29–34] at different load values. These are derived with the parameters in Table 2.

In the slow and fast switching limit model, an SCC is modeled. The duty ratio is fixed 50%, resistors of switches are neglected, and variations in charging and discharging voltages of capacitors are also neglected [29–31]. Unlike the conventional method, the proposed method can reflect the influence on the gain function by the duty ratio when maximum and minimum voltages of capacitors are derived. When the relation of the operation frequency, capacitors, and switches is modeled, the method in [29–31] neglects on-resistors of switches (slow switching limit) and considers the capacitors as voltage sources (fast switching limit). These characteristics decrease the accuracy of the voltage gain, as shown in Figure 11. However, in the proposed method, these parameters are examined through all analysis processes, as explained in Section 3.1. These differences from the existing method can increase the modeling accuracy of the proposed method. If the CCFSCC is analyzed by using the given method in [32–34], the voltages of all of the capacitors need to be derived. This can improve the reliability of the voltage gains at load values under 2 k Ω , as described in Figure 11, but requires complex calculations as the number of circuit components rises to generate higher output voltages. Differently from this method, the proposed method approximates the voltages of capacitors, as formulated in Equation (5). This can reduce the amount of calculations.



Figure 11. Comparison of calculated voltage gains from proposed and existing methods, as well as simulated ones, at different load values.

5. Conclusions

In this paper, we propose an analytical method to analyze the CCFSCC in steady state condition. From the proposed modeling, the voltage gain function of the CCFSCC is derived to provide a guidance for selecting the circuit parameters such as the operation frequency and the capacitances of the flying and output capacitors. To verify the proposed method, the outcomes were compared with the simulated and experimental results at different load values. The absolute error between the calculations and the simulations is under 0.1 on average. This comparison shows that the proposed analytical method can be considered as a guidance to design hardware for the CCFSCC.

In a future study, hardware for the CCFSCC will be designed by selecting proper circuit components based on the proposed guidance, which can prove the reliability of the proposed analytical method. Additionally, analyzing and designing different types of SCCs with the proposed method will be implemented, which can prove generality and versatility of the proposed method.

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Appendix A

Figure A1 illustrates the measured input and output voltages and PWM signals.



Figure A1. Measured output voltages at different load values from 180 Ω to 15 k Ω .

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