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NSGA-II-Based Codesign Optimization for Power Conversion and Controller Stages of Interleaved Boost Converters in Electric Vehicle Drivetrains

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Abstract: This article proposes a holistic codesign optimization framework (COF) to simultaneously optimize a power conversion stage and a controller stage using a dual-loop control scheme for multiphase SiC-based DC/DC converters. In this study, the power conversion stage adopts a non-isolated interleaved boost converter (IBC). Besides, the dual-loop control scheme uses type-III controllers for both inner- and outer- loops to regulate the output voltage of the IBC and tackle its non-minimum phase issue. Based on the converter architecture, a multi-objective optimization (MOO) problem including four objective functions (OFs) is properly formulated for the COF. To this end, total input current ripple, total weight of inductors and total power losses are selected as three OFs for the power conversion stage whilst one OF called integral of time-weighted absolute error is considered for the controller stage. The OFs are expressed in analytical forms. To solve the MOO problem, the COF utilizes a non-dominated sorted genetic algorithm (NSGA-II) in combination with an automatic decision-making algorithm to obtain the optimal design solution including the number of phases, switching frequency, inductor size, and the control parameters of type-III controllers. Furthermore, compared to the conventional 'k-factor' based controller, the optimal controller exhibits better dynamic responses in terms of undershoot/overshoot and settling time for the output voltage under load disturbances. Moreover, a liquid-cooled SiC-based converter is prototyped and its optimal controller is implemented digitally in dSPACE MicroLabBox. Finally, the experimental results with static and dynamic tests are presented to validate the outcomes of the proposed COF.

Keywords: simultaneous codesign optimization; non-dominated sorted genetic algorithm; multiport converter; interleaved boost converter; optimal type-III controller; SiC MOSFET modules; finite element analysis; electric vehicle drivetrains

1. Introduction

In electric vehicle (EV) drivetrains, multiport converters (MPCs) consisting of multiple DC/DC converters have been widely adopted to manage power between different energy sources (i.e., battery, fuel cell (FC) and supercapacitor (SC)) [1]. The DC/DC converters can boost the low voltage range of the energy sources to a high DC-link voltage that feeds to an electric motor (EM) via an electric drive DC/AC inverter [2]. Due to limited space, high reliability and high power-density converters are normally required in EV applications. To this end, wide bandgap technology such as silicon carbide (SiC) MOSFETs have recently been used to replace traditional silicon (Si) IGBTs, which leads to an overall reduction of 30% for the total converter volume [3]. Besides, by applying a multiphase

concept along with interleaving operation and current sharing control techniques for the DC/DC converter, its input current ripple, and the sizing of passive components can be remarkably reduced [4]. Beyond that, a holistic and strategic design methodology is needed to unleash the potential of emerging technologies for the power converters.

Traditionally, as shown in the left-side of Figure 1, a sequential workflow comprising three stages has been used to design a DC/DC converter. In the first stage, converter topology is selected and optimized considering the specification of commercial EVs. Each topology selection determines the design constraints for the following steps. Typically, non-isolated (bidirectional) interleaved boost converters (IBCs), have been widely selected as power electronics (PE) interfaces with multiple energy sources [5]. In the second stage, based on a fixed topology, suitable technology and hardware (HW) sizing optimization can be executed separately for components or sub-systems. Finally, in the third stage, the controller or software (SW) is designed considering the constraints created from previous stages. The iterations between stages are conducted until the design requirements are satisfied.

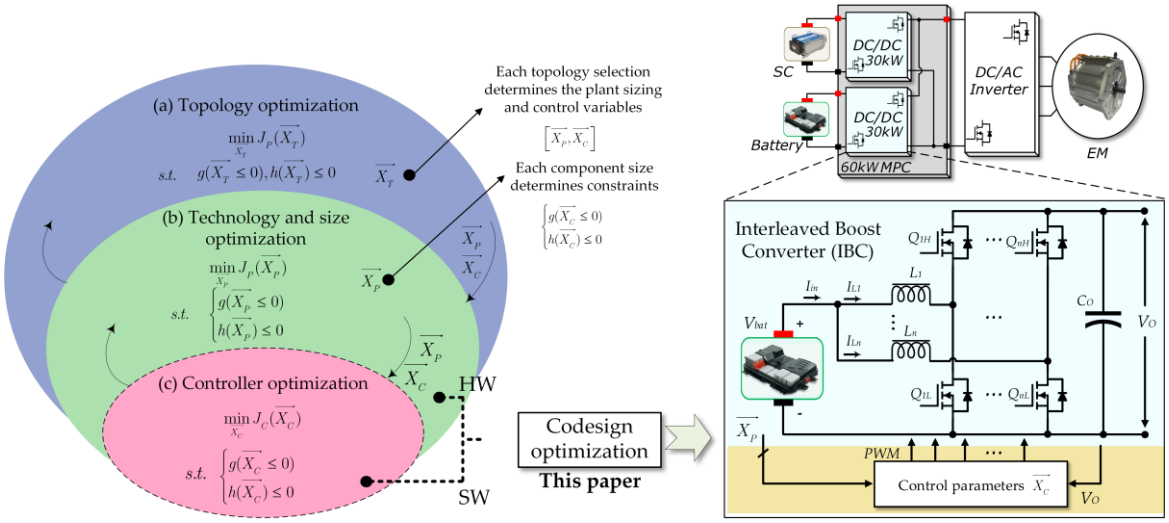


Figure 1. Sequential system-level design and coordination of HW sizing and SW controller optimization (codesign) for IBC.

Through the literature, numerous optimization techniques for HW sizing of the PE converters can be classified into four main types: *(i)* Pareto-front (PF) analysis [6–10] based on brute-force (BF) search (known as exhaustive search), *(ii)* gradient-based algorithms [11–13], *(iii)* derivative-free based algorithms [14–21], and *(iv)* other types such as geometry programming [22,23]. Generally, the main design variables involve switching frequency, geometry parameters, inductance- or capacitance- values, and thermal resistance. Those variables are widely selected for different optimization problems (e.g., minimization of sizing, cost, and losses) of various applications such as inductor [14], medium-frequency transformer [18], solid-state transformer [16], AC/DC converter [8], DC/AC converter [24], resonant tank of dual-active bridge [15], power correction factor [13,17], and heat sink [24].

Conventionally, Pareto-front analysis has been used to find an optimal solution from an optimization problem incorporated with multiple design objectives (e.g., volume and efficiency). However, in the Pareto-front method, the optimal solution can be found at the end of an exhaustive search. This searching method sweeps and evaluates all possible combinations of design parameters, resulting in a computationally-intensive process. In contrast, the gradient-based techniques exploit the derivative information of mathematical equations representing objective functions to solve the optimization problem. Nonlinear programming (NP) based on Lagrangian functions [11], augmented Lagrange penalty function (ALPF) [12] and sequential quadratic programming (SQP) [13] can be categorized as the gradient-based techniques. On the other hand, the derivative-free techniques

are based on evolutionary nature-inspired algorithms such as particle swarm optimization (PSO) [14,15], differential evolution (DE) combined PSO [16], genetic algorithm (GA) [17] and multi-objective genetic algorithm (MOGA) [18–21]. A review of those metaheuristic-based optimizations in the PE application was comprehensively reported in [25]. The features of four main techniques for the HW sizing optimization are summarized in Table 1 covering their merits and demerits, main applications, and prevalent objective functions.

Through the extensive literature review, research gaps are identified as follows. It is noticed that the HW and controller designs for the PE converters have been treated independently. So far limited publications have reported possibilities for the coordination architecture of HW-controller codesign. However, especially in the IBC, the potential to combine its HW and controller design in a holistic framework can be feasible for the following reasons. From the HW perspective, an inductance value, which is physically decided by core size and the number of winding turns, should be optimized to minimize the power losses. Besides, from the control aspect, it should be pointed out that in a boost converter, the inductance value has an impact on the position of a right-half-plane (RHP) zero which inherently causes the non-minimum phase issue. The inductance value should be also minimized to keep the RHP zero at high frequency to increase the bandwidth of the closed-loop system, resulting in better dynamic response performance. In this regard, the HW and controller should be codesigned for the IBC. Therefore, this paper focuses on the coordination of HW sizing and SW/controller optimization called a codesign optimization framework (COF) for the IBC in the EV applications, which has been rarely reported in the literature. To this end, the main contributions of this paper may be summarized as follows:

(1) A simultaneous COF based on metaheuristic-evolutionary searching and automatic decision-making algorithms is introduced for high-power multiphase DC/DC converters in EV applications;
(2) Four key objective functions involving both the power conversion stage and the controller stage are well-defined in analytical forms to facilitate the optimization process. The optimal results obtained from the COF using those analytical models are verified by finite element analysis (FEA) simulation and experimental results;
(3) Based on the optimal parameters, a liquid-cooled SiC-based converter and its real-time controller are prototyped and demonstrated. Experimental validations are conducted including *(i)* a mechanical design for inductor; *(ii)* integration of the entire converter system in comparison with other prototypes available in the literature; *(iii)* implementation of field-programmable gate array (FPGA)-based digital controllers; and *(iv)* static and dynamic load transient testing.
(4) The proposed COF provides a practical design tool to explore holistically the design space of the PE converter. As the proposed COF is considered as a modular approach, it can be simplified or extended considering other aspects such as reliability and total cost of ownership, which may open new research trends.

As mentioned previously, the MPC contains two separate battery and SC ports with 30 kW/port which employs the same IBC topology, as shown in the right-side of Figure 1. In light of concept verification, the proposed COF and the optimal solution will be mainly demonstrated for the IBC connecting to the battery port (port 1). It should be highlighted that in the entire hardware prototype as demonstrated later on, two ports are shared a common cold plate, yielding a total nominal power of 60 kW.

In this regard, the rest of this paper is organized as follows: Section 2 presents the technology selection for power conversion and controller stages of the IBC. Section 3 explains the formulation of multi-objective codesign optimization problem along with the principle of the proposed simultaneous COF, leading to the optimal solution. Section 4 shows the detailed design of the optimal inductor and its FEA simulation. Section 5 illustrates a full-scale hardware prototype alongside with experimental results. Section 6 presents conclusions and suggests future research trends.

Table 1. Summary of optimization algorithms for the power electronics converters.

Algorithms (1)		Applications (2)	Ref.	Objective Functions				Advantages	Disadvantages
				Efficiency/ Loss	Weight/ Sizing	Cost	Thermal/ Heatsink		
Brute-force search-based Pareto-front analysis	BF-PF	Single-phase PFC rectifier	[6]	✓	✓			- Iterative calculation and check all possible combinations of components.	- High computational cost; - The gap between the selected mathematically optimal and standard available off-the-shelf components; - Heuristics-based decision making for the selection of an optimal solution.
	BF-PF	Phase-shift full-bridge converter	[7]	✓	✓				
	BF-PF	Isolated 3-phase AC/DC converter	[8]	✓	✓				
	PF	MFT	[9]	✓	✓		✓		
	BF	3-phase DC/AC	[10]	✓	✓		✓		
Gradient-based	NP	Switched-capacitor converter	[11]	✓	✓			- Fast calculation; - Can be used in the preliminary design stage.	- The optimizer may be trapped by a local optimum. The optimal result and the speed of convergence are dependent on the selection of the initial design point; - It is difficult to detect the infeasibility of a problem; - Discrete variables need to be either fixed or converted to continuous variables.
	ALPF	Half-bridge buck converter	[12]	✓	✓				
	SQP	Boost PFC converter	[13]			✓			
Derivative-free-based	PSO	HB DC/AC	[14]	✓	✓			- Can be applied to all kind of optimization problems (nonlinear, nonconvex, discrete, continuous, mix-integer, and multiple objectives); - The capability to find globally optimal solutions; - Discontinuous objective function does not affect the global convergence.	- Require building database commercially off-the-shelf components for searching space; - The feasibility and accuracy of optimization solutions depend on the algorithm parameters (e.g., the number of individuals, and the number of generations).
		Resonant tank of DAB	[15]	✓					
	DE-PSO	HFT (SST)	[16]	✓					
	GA	Boost PFC converter	[17]			✓			
	MOGA	MFT in DAB and LLC converters	[18]	✓	✓				
		Buck converter	[19]	✓	✓				
		Resonant boost HB	[20]	✓		✓			
		Boost converter	[21]	✓		✓			
Other	GP	Boost and synchronous buck	[22]	✓				- Quickly produce globally optimum designs.	- The requirement of convexation for nonlinear problems by a logarithmic change of variables.
		Multi-level converter	[23]	✓	✓				

(1) *Abbreviations for algorithms*: BF: brute force, PF: Pareto front, NP: nonlinear programming, ALPF: augmented Lagrange penalty function, SQP: sequential quadratic programming, PSO: particle swarm optimization, DE-PSO: differential evolution combined PSO, GA: genetic algorithm, MOGA: multi-objective genetic algorithm, GP: geometry programming.
(2) *Abbreviations for applications:* PFC: power factor correction, MFT: medium-frequency transformer, HB: half-bridge, DAB: dual active bridge, HFT: high-frequency transformer, SST: solid-state transformer.

2. Technology Selections of Power Conversion and Controller Stages

This section narrows down the suitable technologies for semiconductor devices and inductors in the power conversion stage along with the control strategy in the controller stage.

2.1. Technology Selections of Power Conversion Stage

The design specifications of the IBC are as follows: nominal power P_{nom} = 30 kW, output voltage V_O = 400 V, nominal input voltage V_{in} = 200 V, input voltage range from 185 V to 250 V. It is noted that the IBC operates under hard-switching transitions, high power, and high switching frequency. Considering the operating conditions, suitable technologies need to be adopted for the IBC's critical components. Those components include semiconductor devices and inductors, which mainly contribute to the sizing and performance of the IBC.

Regarding semiconductor devices, wideband gap (WBG) technologies (i.e., silicon carbide (SiC) and gallium nitride (GaN)) have been recently used in for power converters [26]. Among different packages of semiconductor devices, SiC half-bridge (HB) modules are attractive for high-voltage and high-power applications thanks to their modular capability, low packaging loop inductance (about 15 nH to 19 nH), and low thermal impedance [27]. Table A1 in Appendix A shows a comparison between commercially available SiC modules. It is noted that the CAS300M12BM2 (CREE, Durham, NC, USA) and SKM350MB120SCH17 (Semikron, Nuremberg, Germany) share similar packaging. In this study, a commercial 1200 V, 300 A CAS300M12BM2 SiC HB module from Wolfspeed (formerly CREE) [28] is selected for the power circuit because it offers low switching energy, low thermal resistance, and a competitive price.

Regarding the inductor design, the magnetic materials of the inductor core and the winding type are two key factors, which significantly contribute to the weight, volume, power losses of an inductor. Table A2 in Appendix A lists different magnetic core materials used for a multiphase bidirectional converter in EV drivetrains [29] and railway traction [30]. The suitable core material should exhibit high saturation flux, low loss, low cost, and low thermal resistance. Compared to other magnetic counterparts, nanocrystalline materials exhibit many advantages such as favorable high-frequency characteristics up to several hundred kilohertz, high saturation flux density, high permeability and low core loss. However, the manufacturability of nanocrystalline poses high cost and complexity. It can be observed that in automotive powertrains, the amorphous core attracts more interest since it has a suitable temperature, low core losses, and high saturation flux density of 1.5 T [29]. More importantly, the cost of amorphous cores is far cheaper than that of nanocrystalline cores [30]. Regarding the winding selection, compared to the solid-round wire, the Litz-wire conductor has multiple insulated-braided-parallel strands. Hence, Litz-wire can mitigate the AC-winding losses caused by eddy current effects (i.e., skin and proximity effects [31]), improving the inductor efficiency. Another winding type is a copper foil which offers a good utilization of window area, providing increased copper space factor [32]. However, in this paper, multi-strand Litz-wires are more preferable to develop an inductor prototype. To recap, the 1200 V CREE CAS300H12BM2 power modules, iron-based amorphous metal materials (2605SA1 from Hitachi Metglas, a subsidiary of Hitachi Metals America, Ltd, Conway, SC, USA), and multi-strand Litz-wires have been selected for the development of the IBC's power conversion stage.

2.2. Controller Type and Control Strategy Selections of Controller Stage

In this paper, a dual-loop control architecture consisting of an inner current loop and an outer voltage loop has been selected to regulate the output voltage at a constant set point V_O^*. Besides, the plant models of duty cycle-to-inductor current $G_{id}(s)$ and duty cycle-to-output voltage $G_{vd}(s)$ in the continuous s-domain are required to design the controllers for each loop. To this end, the small-signal averaging technique [4] is employed to obtain the transfer functions of the plants. Table 2 shows the transfer functions of $G_{id}(s)$ and $G_{vd}(s)$ which are derived in continuous conduction mode (CCM) [4].

The open-loop gains $T_i(s)$ and $T_v(s)$ for the inner current loop and the outer voltage loop can be expressed as Equation (1) and Equation (2), respectively:

$$T_i(s) = C_i(s) \cdot G_{id}(s) \tag{1}$$

$$T_v(s) = \frac{C_v(s) \cdot C_i(s) \cdot G_{vd}(s)}{1 + T_i(s)} \tag{2}$$

where $C_i(s)$ and $C_v(s)$ are the transfer functions of inner current- and outer voltage-controllers, respectively. The plant transfer function $G_v(s)$ of the voltage control loop is given in Equation (3):

$$G_v(s) = \frac{C_i(s) \cdot G_{vd}(s)}{1 + C_i(s) \cdot G_{id}(s)} \tag{3}$$

Table 2. Transfer functions of duty cycle-to-inductor current $G_{id}(s)$ and duty cycle-to-output voltage $G_{vd}(s)$, where C is output capacitance, R_C is capacitor internal resistance, L is boost inductance, R_L is inductor internal resistance, N_{ph} is a number of phases, D is nominal duty ratio, and R_O is the load resistance.

	Duty Cycle-to-Inductor Current		**Duty Cycle-to-Output Voltage**	
Transfer function	$G_{id}(s) = \frac{\widetilde{i_L}(s)}{\widetilde{d}(s)} = G_{di}\frac{1+\frac{s}{\omega_{zi}}}{\Delta}$	(4)	$G_{vd}(s) = \frac{\widetilde{v_O}(s)}{\widetilde{d}(s)} = G_{dv}\frac{\left(1+\frac{s}{\omega_{zv\_ESR}}\right)\left(1-\frac{s}{\omega_{zv\_RHP}}\right)}{\Delta}$	(5)
Open-loop gain	$G_{di} = \frac{2V_O}{R_L+N_{ph}(1-D)^2R_O}$	(6)	$G_{dv} = \frac{V_O}{1-D}$	(7)
Zero	$\omega_{zi} = \frac{1}{C(R_C+\frac{R_O}{2})}$	(8)	$\omega_{zv\_ESR} = \frac{1}{C\cdot R_C}$ $\omega_{zv\_RHP} = \frac{-R_L+N_{ph}(1-D)^2R_O}{L}$	(9)
The denominator in Equation (4) and Equation (5)	$\Delta = \frac{s^2}{\omega_0^2} + \frac{s}{Q\cdot\omega_0} + 1$			(10)
Nature frequency ω_0	$\omega_0 = \sqrt{\frac{R_L+N_{ph}(1-D)^2R_O}{L\cdot C(R_O+R_C)}}$			(11)
Quality factor Q	$Q = \frac{1}{2\zeta}$			(12)
System damped ratio ζ	$\zeta = \frac{L+C\left[R_L(R_O+R_C)+N_{ph}(1-D)^2R_O\cdot R_C\right]}{2\sqrt{L\cdot C(R_O+R_C)\left[R_L+N_{ph}(1-D)^2R_O\right]}}$			(13)

It is noticed that the control-to-output voltage transfer function $G_{vd}(s)$ in Equation (5) is a second-order transfer function with one left-half-plane (LHP) zero, one right-half-plane (RHP) zero, and double LHP poles. The effect of RHP zero on the system dynamics can be seen obviously when the duty cycle increases. Initially, the output voltage is reduced, the control command needs to increase the duty cycle of the lower switch. However, the power in the inductor is delivered to the output during the turn-off duration of the bottom switch. Consequently, after 4~5 times of the time constant associated with the RHP zero, the output voltage follows the reference control voltage. To overcome this issue, the loop bandwidth must be selected much less than the frequency of the RHP zero. As can be seen implicitly in (2.6), the inductance L should be minimized to keep the RHP zero ω_{zv_RHP} at high frequency to increase the bandwidth of closed-loop, resulting in better dynamic response performance.

Owning to the occurrence of RHP zero, the IBC suffers a non-minimum phase problem [33]. Due to the problem, it is difficult for a conventional proportional-integral-derivative (PID) controller to perform a desirable performance under dynamic transient load. To overcome the drawback of the traditional PID controller, in this paper, type-III controller is applied for the dual-loop control scheme to achieve a better dynamic response [34]. Generally, a type-III controller is a lead-lead controller with a pole at the origin, which is expressed in Equation (14):

$$C_{typeIII}(s) = K_{C\_III}\frac{(s+2\pi\cdot f_{z_1})(s+2\pi\cdot f_{z_2})}{s(s+2\pi\cdot f_{p_1})(s+2\pi\cdot f_{p_2})} \tag{14}$$

In Equation (14), K_{C_III} is control gain, f_{z_1} and f_{z_2} are frequencies of two zeros (i.e., $z_1 = 2\pi\cdot f_{z_1}$ and $z_2 = 2\pi\cdot f_{z_2}$), respectively, f_{p_1} and f_{p_2} are frequencies of two poles (i.e., $p_1 = 2\pi f_{p_1}$ and $p_2 = 2\pi f_{p_2}$), respectively. When two zeros, two poles are identical at double frequencies ($f_z = f_{z_1} = f_{z_2}$, and $f_p = f_{p_1} = f_{p_2}$), respectively, Equation (14) becomes Equation (15):

$$C_{typeIII}(s) = K_{C\_III}\frac{(s+2\pi\cdot f_z)^2}{s(s+2\pi\cdot f_p)^2} \tag{15}$$

Conventionally, the double-pole frequency f_p and double-zero frequency f_z can be determined through the 'k-factor' method considering Equation (16) – Equation (19) where $\phi_{boost(III)}$ is the phase boost of the controller, f_c is the cut-off frequency of controller, $\left|T(s)\right|$ is the magnitude of open-loop gain determined at the cut-off frequency f_c:

$$K_{boost(III)} = \tan\left(45^o + \frac{\phi_{boost(III)}}{4}\right) \tag{16}$$

$$f_z = \frac{f_c}{K_{boost(III)}} \tag{17}$$

$$f_p = f_c\cdot K_{boost(III)} \tag{18}$$

$$K_{C\_III} = \left|\frac{1}{T(s)}\right|_{f=f_{c(III)}} \tag{19}$$

In the literature, several researchers have adopted PSO [35,36] and the queen-bee genetic algorithm (QBGA) [34] for tuning the control parameters. However, in their research, the controller has been treated independently with the power conversion design. In this paper, the control parameters are simultaneously optimized together with the power conversion design in a holistic codesign framework as explained in the next section. For the sake of performance comparison, the 'k-factor' based design is considered as a benchmark to be compared with the optimized design.

3. Proposed Simultaneous Codesign Optimization Framework

Considering the selected structure of power conversion and controller stages as discussed previously, this section presents the development of the proposed COF through four sub-sections. The high-abstract level of the multi-objective optimization (MOO) problem and the definition of codesign variable vector are presented in Section 3.1. Besides, the analytical derivations of objective functions are provided in Section 3.2. The holistic optimization workflow is developed in Section 3.3 to solve the MOO problem, following by the optimal solution in Section 3.4.

3.1. Principle and Flow Chart of Simultaneous Codesign Optimization

Figure 2 shows the block diagram of the power conversion structure coupling with the dual-loop controller architecture and the selected design variables of two stages.

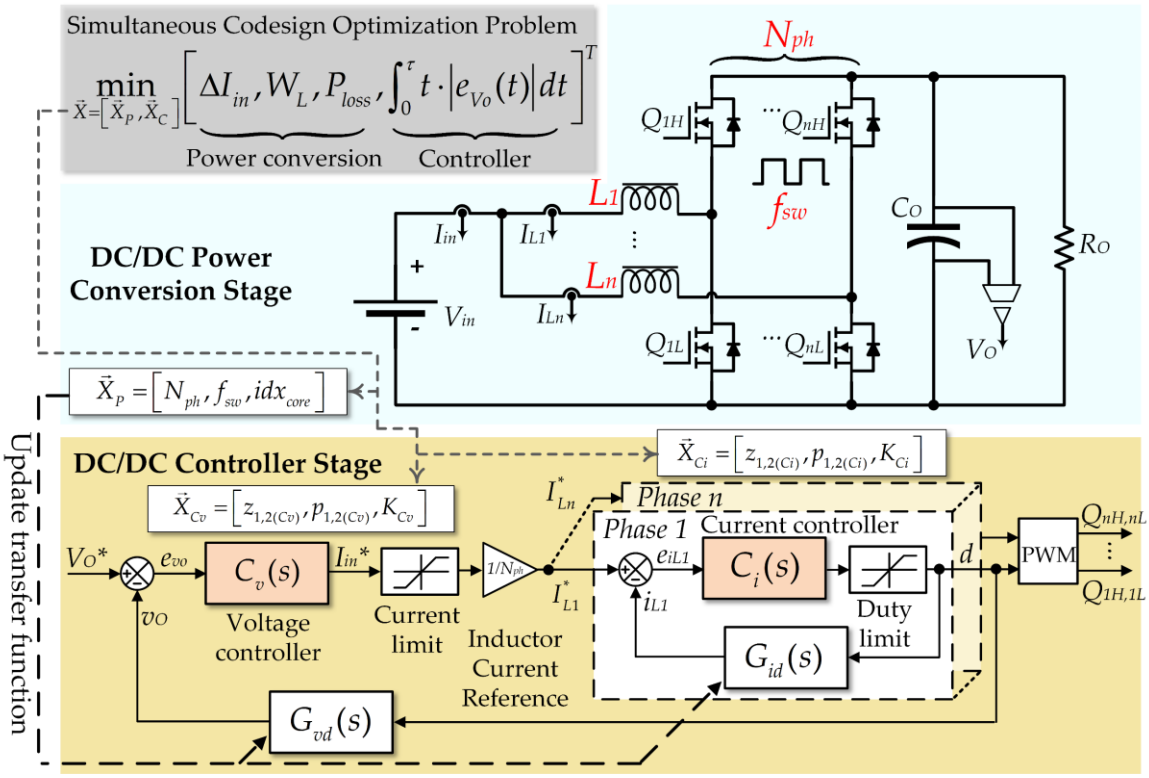


Figure 2. Block diagram of DC/DC power conversion stage and dual-loop control architecture.

In this research, four objective functions (*ObjFcn*) have been selected for the proposed COF. Regarding the power conversion stage, $ObjFcn_1(\vec{X})$ represents the total input ripple current ΔI_{in} [A], whereas, $ObjFcn_2(\vec{X})$ estimates the total weight of inductors W_L [kg], and $ObjFcn_3(\vec{X})$ determines the total power losses P_{loss} [W]. Regarding the controller stage, $ObjFcn_4(\vec{X})$ examines the performance of the closed-loop controller through the dynamic response of output voltage by using suitable control criteria. The multi-objective functions are mathematically described as Equation (20):

$$MulObjFnc(\vec{X}) = \begin{bmatrix} ObjFnc_1(\vec{X}) \\ ObjFnc_2(\vec{X}) \\ ObjFnc_3(\vec{X}) \\ ObjFnc_4(\vec{X}) \end{bmatrix} \quad (20)$$

where $\vec{X} = \left[\vec{X}_P, \vec{X}_C\right]$ denotes the codesign-variable vector consisting of 13 design variables. $\vec{X}_P = \left[N_{ph}, f_{sw}, idx_{core}\right]$ is the variable vector of the power conversion stage. Specifically, N_{ph} is a number of phases, f_{sw} is the switching frequency, and idx_{core} is the core index representing the core geometry parameters extracted from a core database. Besides, $\vec{X}_C = \left[\vec{X}_{Ci}, \vec{X}_{Cv}\right]$ is the design variable vector of the controller stage. Specifically, $\vec{X}_{Ci} = \left[z_{1,2(Ci)}, p_{1,2(Ci)}, K_{Ci}\right]$ and $\vec{X}_{Cv} = \left[z_{1,2(Cv)}, p_{1,2(Cv)}, K_{Cv}\right]$ are the vectors of design variables of the type-III current and voltage controllers that have the transfer functions as in Equation (21) and Equation (22), respectively. In more detail, $z_{1,2(Ci)}$, $p_{1,2(Ci)}$ and K_{Ci}

denotes two zeros, two poles, and the gain coefficient of the current controller $C_i(s)$. Similarly, $z_{1,2(Cv)}$, $p_{1,2(Cv)}$ and K_{Cv} denotes two zeros, two poles, and the gain coefficient of the voltage controller $C_v(s)$:

$$C_i(s) = K_{Ci}\frac{(s+z_{1(Ci)})(s+z_{2(Ci)})}{s(s+p_{1(Ci)})(s+p_{2(Ci)})} \tag{21}$$

$$C_v(s) = K_{Cv}\frac{(s+z_{1(Cv)})(s+z_{2(Cv)})}{s(s+p_{1(Cv)})(s+p_{2(Cv)})} \tag{22}$$

The multi-objective optimization problem subjecting to constraints is presented at a highly abstract level in Equation (23) and Equation (24):

$$\min_{\substack{\vec{X}=[\vec{X}_P,\vec{X}_C]\in\Omega \\ \vec{X}_P=[N_{ph},f_{sw},ind_{core}] \\ \vec{X}_C=[\vec{X}_{Ci},\vec{X}_{Cv}]}} \begin{cases} ObjFnc_1(\vec{X}) = \Delta I_{in}(\vec{X}_P) \\ ObjFnc_2(\vec{X}) = W_L(\vec{X}_P) \\ ObjFnc_3(\vec{X}) = P_{loss}(\vec{X}_P) \\ ObjFnc_4(\vec{X}) = ITAE(\vec{X}_P,\vec{X}_C) \end{cases} \tag{23}$$

$$s.t.\ g_i(\vec{X}) \le 0, i = 1,\dots m \tag{24}$$

The optimization constraints g_i are listed in Table 3. As N_{ph} and idx_{core} are integer numbers whereas other variables are continuous, Equation (23) is a mixed-integer optimization problem. Table 4 shows qualitatively the impact of the increases in design variables on objective functions. To cope with the conflicting objective functions, a flow chart using optimization algorithms is proposed to quantify the design variables. In this paper, the multi-objective optimization approach, which relies on mathematical models combined with data of components in the database, is taken into consideration. To simplify the optimization problem, it is assumed that the output capacitor is constant and not involved in the optimization process.

Table 3. Constraint description.

Constraints	Description
$1 \le N_{ph} \le 6$	Limitation for the number of phases
10 kHz $\le f_{sw} \le$ 100 kHz	Switching frequency range
$\Delta I_{in} \le 7.5\%\ I_{in}$	Maximum for the input current ripple
$W_L \le 5$ kg	Maximum for the total weight of inductors
$T_{j(MOS)} < 150$ °C	Maximum junction temperature of MOSFET
$T_{core} < 100$ °C	Maximum temperature rising of inductor core
$\tau_{Cv} < 0.03s$	Maximum settling time for voltage controller
$\tau_{Ci} < 0.003s$	Maximum settling time for current controller

Table 4. Impact of design variables on objective functions.

Objective Functions	$\nearrow \vec{X}_P$		
	$\nearrow N_{ph}$	$\nearrow f_{sw}$	$\nearrow idx_{core}$
$ObjFnc_1(\vec{X}) = \Delta I_{in}(\vec{X}_P)$	$\searrow$	$\searrow$	$\searrow$
$ObjFnc_2(\vec{X}) = W_L(\vec{X}_P)$	$\nearrow$	$\searrow$	$\nearrow$
$ObjFnc_3(\vec{X}) = P_{loss}(\vec{X}_P)$	$\nearrow$		$\nearrow$
$ObjFnc_4(\vec{X}) = ITAE(\vec{X}_P,\vec{X}_C)$	$\searrow$	-	$\nearrow$

3.2. Objective Functions

This subsection elaborates on the closed-form mathematical models incorporated in the objective functions which are defined in Equation (23).

3.2.1. Objective Function 1: Total Input Current Ripple

The first objective function $ObjFnc_1$ evaluates the total input current ripple ΔI_{in} which should be minimized because it has a detrimental impact on the long-term performance degradation of the battery pack connecting to an IBC [37]. Through electrochemical impedance spectroscopy techniques [37], undesired high switching frequency noises and current ripples (i.e., DC-current coupling with AC-current) can increase the capacity face and impedance of battery cells, resulting in differential current flowing into cells and heat generation within the battery pack. If the underlying causality is not properly managed, the battery life will be reduced, degrading vehicle reliability. Hence, it is imperative to minimize the total input current ripple by employing the multiple phases and interleaving technique for the IBC.

The analytical equation of $ObjFnc_1$ is shown in Equation (25) which is a function of variables N_{ph}, f_{sw}, and L:

$$ObjFnc_1 = \Delta I_{in}(\vec{X}_P) = \frac{V_O\left(D - \frac{k}{N_{ph}}\right)}{L \cdot f_{sw}}\left[1 - N_{ph}\left(D - \frac{k}{N_{ph}}\right)\right] \tag{25}$$

$$\begin{cases} 1 - \frac{V_{\max}}{V_O} < D < 1 - \frac{V_{\min}}{V_O} \\ k \in \left[0, N_{ph} - 1\right] \end{cases} \tag{26}$$

where D is the nominal duty cycle. The calculation of inductance value L will be explained in the next objective function.

3.2.2. Objective Function 2: Total Inductor Weights

The second objective function $ObjFnc_2$ evaluates the total inductor weights W_L as given in Equation (27) which is proportional to the number of phases N_{ph} and the weight of a single inductor. An inductor weight mainly composes of a winding weight $W_{winding}$ and a core weight W_{core}:

$$ObjFnc_2 = W_L(\vec{X}_P) = N_{ph}(W_{winding} + W_{core}) \tag{27}$$

Traditionally, an inductor can be designed using either K_g or A_P procedures [38]. In the K_g and A_P approaches, a core is selected to meet predefined requirements such as limited current ripple and desired inductor losses. In an iteration loop, a checking condition related to the temperature rising in the inductor core is used to evaluate the selected core. If the temperature condition is not satisfied, another core owning a higher value of A_P will be re-selected. The K_g and A_P methods are straight forward. However, they lack the optimality regarding the minimization of inductor losses.

To be distinguished from conventional inductor design, in this paper, the core area product A_P represented by the design variable idx_{core} is decided by the NSGA-II optimization loop to minimize multi-objective functions in Equation (23). In this paper, a database of different amorphous cores is prepared. Each inductor core is labeled by an integer number idx_{core} including main core parameters (the window area W_a [mm^2], the net cross-sectional area A_C [mm^2], the core area product $A_P = W_a \cdot A_C$ [mm^4], the saturation flux density $B_{\max}$ [T], the core window utilization factor K_u, and the core weight W_{core} [kg]). Once a specific idx_{core} is picked up by the NSGA-II, its characterized parameters are fetched and cast into Equation (28) (see Appendix C) to obtain an

attainable inductance value L[μH]. It is noted that the inductance value should be a real root of the second-order polynomial equation (28):

$$L^2 I_{L(crit)}^2 + L \cdot \left[\frac{I_{L(crit)}(1 - D_{\max}) D_{\max}}{f_{sw}} - K_u \cdot J_{wire} \cdot B_{\max} \cdot (W_a \cdot A_C) \right] + \left[\frac{V_O(1 - D_{\max}) D_{\max}}{2 \cdot f_{sw}} \right]^2 = 0 \quad (28)$$

As can be seen in Equation (28), the inductance value is determined under the critical condition of boost operation. The critical condition occurs when the input voltage reduces to the minimum voltage $V_{in(\min)}$. As a consequence, the duty cycle increases to a maximum value $D_{\max}$ to maintain a fixed output voltage V_O. Furthermore, in the critical condition, the core (with a saturation flux density $B_{\max}$) needs to be not saturated when the inductor current reaches the peak value $I_{L(crit,pk)} = I_{L(crit)} + \frac{1}{2} \frac{V_O(1-D_{\max})D_{\max}}{f_{sw} \cdot L}$. In the critical condition, the average inductor current is given as $I_{L(crit)} = \frac{P_{\max}}{N_{ph} \cdot V_O(1-D_{\max})}$.

Based on the inductance value, the number of turns N_{turn} and air-gap length l_{gap} are calculated as Equation (29) and Equation (30), respectively. The air-gap length l_{gap} [mm] is added to prevent the core saturation:

$$N_{turn} = round\left(\frac{L \cdot I_{L(crit,pk)}}{A_C \cdot B_{\max}} \right) \quad (29)$$

$$l_{gap} = N_{turn} \frac{\mu_0 \cdot I_{L(crit,pk)}}{B_{\max}} \quad (30)$$

where $\mu_0 = 4\pi.10^{-7}$ [H/m] is the vacuum magnetic permeability. Based on the number of turns and core geometries, once the winding length is estimated, the winding weight $W_{winding}$ can be calculated considering the winding weight density [kg/m] of the Litz wire. Therefore, the $ObjFnc_2$ in Equation (27) can be completely determined.

3.2.3. Objective Function 3: Total Converter Losses

The third objective function $ObjFnc_3$ evaluates the total converter losses P_{loss}. Accordingly, optimization-oriented and analytical equations representing the governing losses of components (i.e., SiC HB modules and inductors) with their nonlinearities are developed to estimate the power loss distribution. The total converter losses are mainly governed by the MOSFET losses $P_{loss(MOSFET)}$, the diode losses $P_{loss(DIODE)}$, and the inductor losses $P_{loss(L)}$ as shown in Equation (31):

$$ObjFnc_3 = P_{loss}(\vec{X}_P) = N_{ph}\left(P_{loss(MOSFET)} + P_{loss(DIODE)} + P_{loss(L)} \right) \quad (31)$$

Semiconductor Losses

As this paper focuses on high power converter applications, only critical and major losses will be considered for the loss model of semiconductors. It is noted that MOSFET and diodes are operated as switches, taking on various static and dynamic states in cycles. Individual power losses of switches can be broken down into static losses (i.e., on-state/conduction loss and blocking loss), switching losses (i.e., turn-on loss, turn-off loss, output parasitic capacitor loss, and gate driver loss). The accurate losses model of SiC power modules can be found in [39]. However, in this paper, several simplifications for the converter loss calculation can be conducted to facilitate the optimization process as follows:

(i) Dead-times loss is neglected,
(ii) The output capacitor loss owning to its equivalent series resistance (ESR) is neglected,
(iii) Junction temperatures are in time constant at 150 °C for the sake of conservative calculation, and the converter operates at the nominal rating power,
(iv) Gate driver loss are neglected because they are considered only for low-power, low-voltage MOSFET applications with very high frequency,

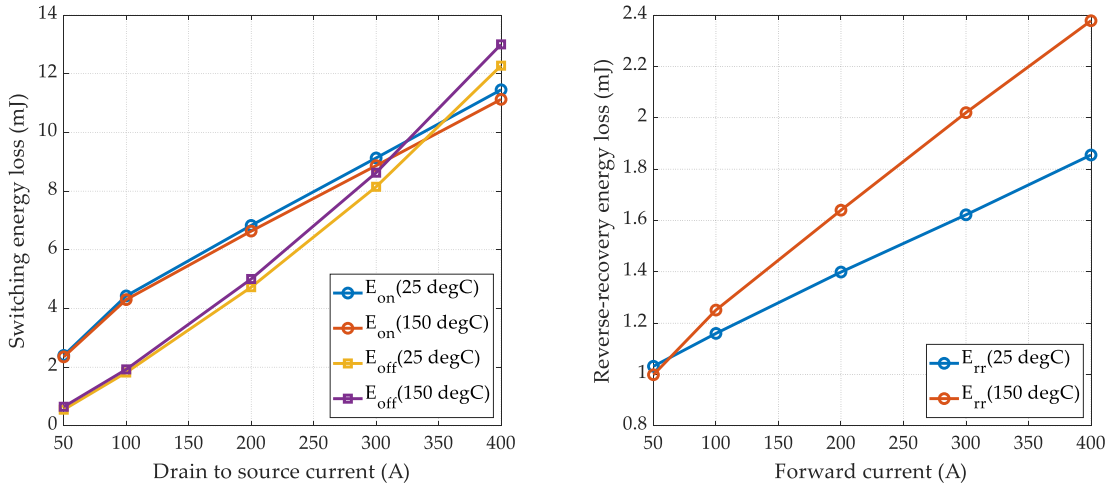
(v) Loss owning to discharging parasitic output capacitor, forward-blocking losses can be neglected in the high-power applications since they only account for a small share of the total power dissipation [40]. In case of high blocking voltages (>1000 V) and/or high operating temperatures (>150 °C), blocking losses may gain importance and may even result in thermal runaway owing to the exponentially rising reverse currents.

The MOSFET losses in Equation (32) can be broken down into the conduction loss $P_{cond(MOS)}$ and switching losses $P_{sw(MOS)}$ (i.e., turn-on and turn-off losses). Similarly, the diode losses in Equation (33) can be broken down into the conduction loss and reverse recovery losses:

$$\begin{aligned} P_{loss(MOSFET)} &= P_{cond(MOS)} + P_{sw(MOS)} \\ &= R_{DS(on)} \cdot I^2_{DS(rms)} + \frac{V_O}{V_{DS(ref)}} \cdot \frac{I_{DS(rms)}}{I_{DS(ref)}} \cdot f_{sw} \cdot \left(E_{on(@I_{DS(on)})} + E_{off(@I_{DS(off)})} \right) \end{aligned} \tag{32}$$

$$P_{loss(DIODE)} = R_F \cdot I^2_{D(rms)} + \frac{V_O}{V_{DS(ref)}} \cdot \frac{I_{D(rms)}}{I_{F(ref)}} \cdot f_{sw} \cdot \left[E_{rr(@I_{D(avg)})} \right] \tag{33}$$

From the manufacturer's datasheet, the characteristics of the SiC HB module are stored in look-up tables to interpolate the switching losses in different operating currents. Figure 3 shows the switching energy dissipations (i.e., E_{on}, E_{off}) of MOSFET and the reverse recovery energy loss (E_{rr}) of the diode, which are measured under the double-pulse test for given DC-bus voltage $V_{DS(ref)}$ and drain-to-source current $I_{DS(ref)}$ at 25 °C and 150 °C. In this regard, the estimated losses of MOSFET and diode can be scaled up or down according to the variations of design variables during the optimization process. Moreover, the currents $I_{DS(on)}$, $I_{DS(off)}$, $I_{DS(rms)}$, $I_{D(rms)}$, $I_{D(avg)}$ need to be determined to find the energy losses in Equation (32) and Equation (33).



(**a**) (**b**)

Figure 3. Semiconductor characteristics (**a**) switching energy dissipation of SiC MOSFET, (**b**) reverse recovery energy dissipation of diode.

Table 5 shows the calculations of those currents for the MOSFET and the diode. It is noted that in the boost operation, the bottom MOSFET of a phase leg conducts the inductor current during its on-period and the anti-parallel diode of the top MOSFET takes over the inductor current during the off-time of bottom MOSFET.

Table 5. Current calculation for MOSFET (lower side) and diode (upper side) in boost operation with an average inductor current $I_L = \frac{P_{nom}}{V_{in} \cdot N_{ph}}$, the inductor current ripple $\Delta I_L = \frac{D_{nom} \cdot V_{in}}{L \cdot f_{sw}}$, and the nominal duty cycle $D_{nom} = 1 - \frac{V_{in}}{V_O}$.

	MOSFET		Diode	
Turn-off current	$I_{DS(off)} = I_{DS(avg)} + \Delta I_L/2$	(34)		
Turn-on current	$I_{DS(on)} = I_{DS(avg)} - \Delta I_L/2$	(35)		
Average current	$I_{DS(avg)} = D_{nom} \cdot I_L$	(36)	$I_{D(avg)} = (1 - D_{nom}) \cdot I_L$	(37)
Root Mean Square (RMS) current	$I_{DS(rms)} = \sqrt{D_{nom}} \cdot I_L$	(38)	$I_{D(rms)} = \sqrt{1 - D_{nom}} \cdot I_L$	(39)

Inductor Losses

The inductor losses $P_{loss(L)}$ mainly consist of winding losses $P_{winding(L)}$ as in Equation (40), core losses $P_{core(L)}$ as in Equation (44), and air-gap losses $P_{gap(L)}$ as in Equation (46). The winding losses $P_{winding(L)}$ can be further classified as AC-winding loss $P_{ac(L)}$ and DC-winding loss $P_{dc(L)}$. The DC-winding loss as in Equation (41), known as a resistive loss, can be estimated by a DC-resistance $R_{dc(L)}$ and RMS current $I_{L(rms)}$ flowing through the designated inductor. The DC-resistance $R_{dc(L)}$ as in Equation (43) can be determined by copper resistivity $\rho_{res(copper)} = 16.78 \times 10^{-9}$ [Ω.m], total winding length $l_{winding}$, and conductor cross-sectional area A_{wire}. The AC-winding losses $P_{ac(L)}$ from the skin depth effect and the proximity effect can be neglected ($P_{ac(L)} = 0$) because the Litz-wire is utilized:

$$P_{winding(L)} = P_{dc(L)} + P_{ac(L)} \tag{40}$$

$$P_{dc(L)} = R_{dc(L)} \cdot I^2_{L(rms)} \tag{41}$$

$$I_{L(rms)} = \sqrt{I_L^2 + \frac{(\Delta I_L)^2}{12}} \tag{42}$$

$$R_{dc(L)} = \rho_{res(copper)} \frac{l_{winding}}{A_{wire}} \tag{43}$$

The core losses $P_{core(L)}$ are estimated in Equation (44). This equation is a modified version of the Steinmetz equation with a correction factor for the non-sinusoidal excitation in which the unidirectional flux density ripple B_{ac} [T] is proportional to the inductor current ripple ΔI_L where W_{core} [kg] is the weight of the core, coefficients $K_{core} = 6.5$, $\alpha_f = 1.51$, $\beta_B = 1.74$ are given in the manufacturer datasheet [41], ΔI_L is the inductor current ripple, and l_{gap} [cm] is the length of the air-gap:

$$P_{core(L)} = W_{core} \cdot \left(K_{core} \cdot f_{sw}^{\alpha_f} \cdot B_{ac}^{\beta_B} \right) \tag{44}$$

$$B_{ac} = \frac{0.4 \cdot \pi \cdot N_t \cdot \Delta I_L \cdot 10^{-4}}{l_{gap}} \tag{45}$$

The prediction of air-gap loss $P_{gap(L)}$ expressed in Equation (46) is a power function [42] of the total gap length l_{gap}, core lamination width D_{core}, frequency f_{sw}, and given peak AC-flux density $B_{ac(peak)}$, where k_g, k_{l_g}, k_D, k_f, $k_{B_{ac}}$ are numerical coefficients provided by the core manufacturer. In this paper, as the inductor core has a high permeability based on its finely laminated structure, the fringing effect is relatively small at air-gap, which can be neglected:

$$P_{gap(L)} = k_g \cdot l_{gap}^{k_{l_g}} \cdot D_{core}^{k_D} \cdot f^{k_f} \cdot B_{ac(peak)}^{k_{B_{ac}}} \tag{46}$$

3.2.4. Objective Function 4: Integral of Time-weighted Absolute Error for Output Voltage Control

In the EV drivetrain, the main purpose of the IBC is to maintain a fixed DC-link voltage regardless of battery voltage variation and output load disturbances. In this regard, the fourth objective function $ObjFnc_4$ evaluates the performance of output voltage control via the dynamic response of closed-loop. The objective of the controller is to minimize the dynamic error signal $e(t)$ during the transient time when the load changes. Some control criterion can be considered for the $ObjFnc_4$ as following: integral of squared error ($ISE = \int_0^\tau e^2(t)dt$), integral of absolute error ($IAE = \int_0^\tau \left|e(t)\right|dt$), integral of time-weighted absolute error ($ITAE = \int_0^\tau t\left|e(t)\right|dt$), integral of time-weighted squared error ($ITSE = \int_0^\tau te^2(t)dt$), integral of the time-squared weighted squared error ($IT^2SE = \int_0^\tau t^2e^2(t)dt$), and integral of the time-squared weighted absolute error ($IT^2AE = \int_0^\tau t^2\left|e(t)\right|dt$). An upper limit τ is chosen as a steady-state value.

As can be seen, the ISE and IAE treat the error signal $e(t)$ equally at any time instance. In contrast, the ITAE penalizes the error signal $e(t)$ along with a long duration transient, that leads to the error signal being forced to reduce to zero as soon as possible. Moreover, the ITAE generally produces less overshoots and oscillations compared to other criterion [33]. Therefore, in this paper, the ITAE is selected to evaluate the controller performance. The ITAE of the output voltage is mathematically expressed in Equation (47):

$$ObjFnc_4 = ITAE_{V_O}\left(\vec{X}_P, \vec{X}_C\right) = \int_0^\tau t\left|e_{V_O}(t)\right|dt \tag{47}$$

As recognized previously, the inductance value L influences the RHP zero and the bandwidth of the closed-loop system. Physically, L is also dependent on the idx_{core} which is a design variable in the vector $\vec{X}_P$. Therefore, $ObjFnc_4$ is a function of both $\vec{X}_P$ and $\vec{X}_C$. In the control design process, the $ObjFnc_4$ is evaluated from the step response of the voltage controller $C_v(s)$ considering the plant transfer function $G_v(s)$ in Equation (3).

3.3. Principle of Simultaneous Codesign Optimization

Four considered objective functions have been derived in analytical equations that are implicitly composed of design variables. This section explains how to incorporate the optimization algorithms to solve those objective functions, creating a holistic COF.

Figure 4 elaborates on the flow chart of the proposed COF. In this research, the NSGA-II [43] and average ranking (AR) [44] are combined to solve the mix-integer, highly nonlinear, and non-convex multi-objective optimization problem in Equation (23) under the list of constraints given in Equation (24). The NSGA-II was developed by Deb et al. [43]. In NSGA-II, the genetic algorithm (GA) plays as a searching kernel with two new additional functions to achieve better multi-objective optimization. These two added concepts are 'fast nondominated sorting' and 'crowding distance assignment'. NSGA-II uses a Pareto-front hierarchy and adopts an elitism mechanism to retain the best solutions generated during the search. By using the discrete value of design variable idx_{core}, the optimization process fetches individual parameters in the core database to calculate each objective function.

The NSGA-II algorithm starts by initializing the parent population randomly. Each of the four objective values is evaluated accordingly. The population is made up of 50 individuals (population size) that are characterized by a vector consisting of a codesign variable $\vec{X} = \left[\vec{X}_P, \vec{X}_C\right]$, objective values $\{ObjFnc_1; ...; ObjFnc_4\}$, overall fitness value, and neighborhood diversity value. For each generation, the individuals from parent and offspring populations are classified on several fronts by considering the non-dominance. It is called 'fast nondominated sorting' which uses a ranking concept to assign a fitness value to each solution, facilitating the selection process in the GA. The first front contains all non-dominated solutions (rank 1). The second front sorts the solutions (rank 2) dominated by only one solution. The third front has solutions (rank 3) dominated by two other solutions. This process

continues until no solution is left. To maintain the diversity of solutions in case of the same front, the additional sort called 'crowding distance assignment' is performed. The crowding distance algorithm calculates how far away the neighbors of a given solution are. In the next step, an 'elitism selection operator' uses a binary tournament to select individuals of the lower front (or lower rank) and the solution with greater crowding distance in case of the same front. New populations are generated by 'genetic operations' such as simulated binary crossover and polynomial mutation.

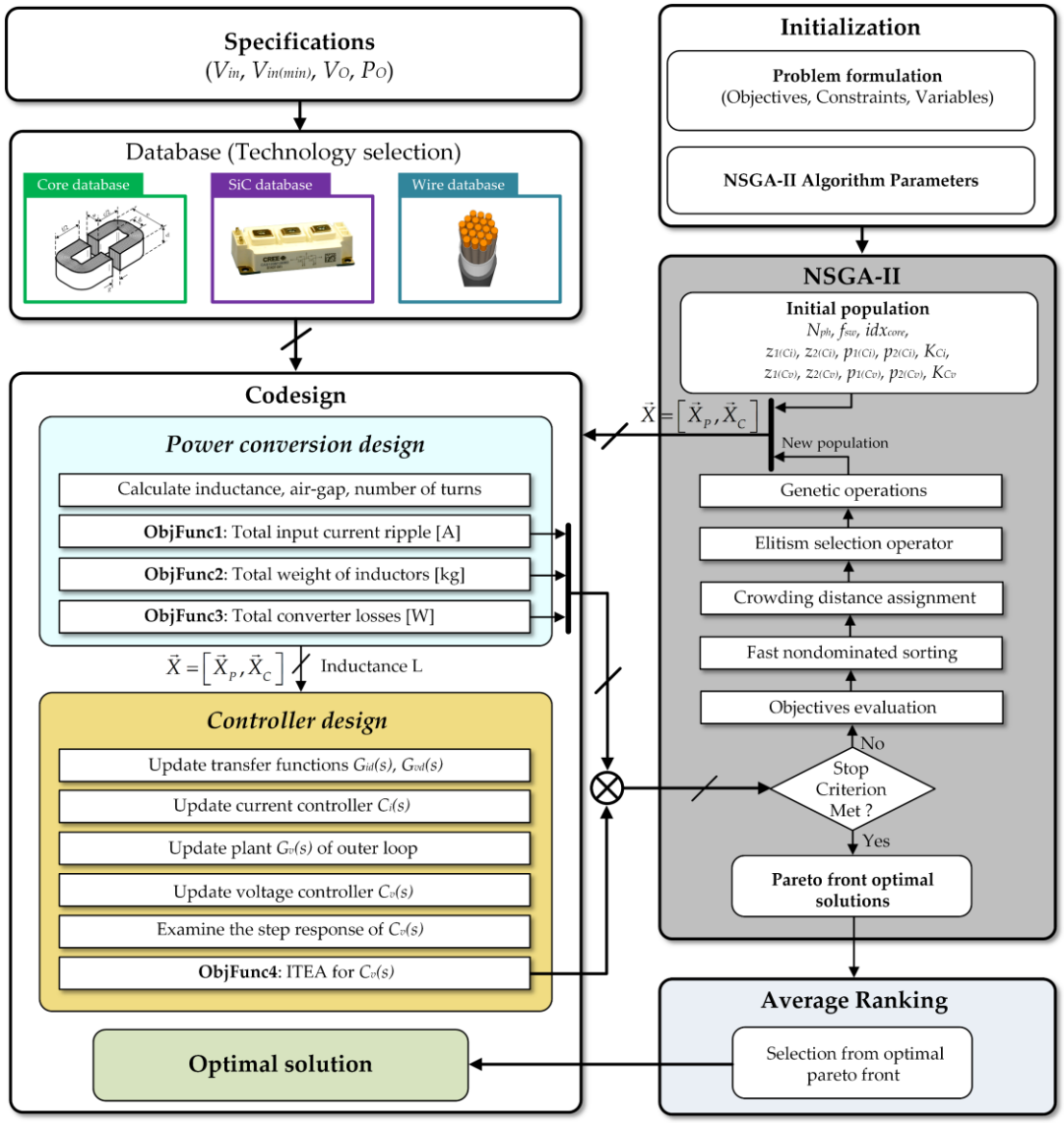


Figure 4. Proposed simultaneous codesign optimization framework.

The NSGA-II is terminated when the maximum generation of 200 is reached. A set of design solutions found is returned as the Pareto-front in which no other solutions are superior to those in its set when all objectives are considered. In other words, in the Pareto-front, each candidate solution can be considered equally good. A common post-processing approach is that the designer with their preference and design experience could select a compromised solution from amongst Pareto front solutions. This approach is dependent on the designer's decision, which may fail to find a truly optimum. Therefore, in this paper, the AR [44] as a decision-making step is added to pick up an optimal solution from the Pareto-front.

Basically, the AR calculates a score for each candidate solution s_i by summing the ranks of s_i for each objective function. If s_i, for example, is the first, second, third, and fourth best on the $ObjFnc_1$,

$ObjFnc_2$, $ObjFnc_3$, $ObjFnc_4$, respectively, the AR score of s_i will be 1 + 2 + 3 + 4 = 10. The s_i having the lowest score is chosen for the optimal solution.

3.4. Optimal Solution

As shown in Figure 5, the optimal solution at the low right corner of its data tip popup is highlighted in the 3-dimension (3D) Pareto-front. The total inductor weight ($ObjFnc_2$) is 2.4 kg, the input current ripple ($ObjFnc_1$) is 3.6 A, and the converter losses ($ObjFnc_3$) are 440 W meaning that the converter can theoretically achieve an efficiency of 98.5% at 30 kW. The optimal design solutions for the power conversion stage and the controller stage are summarized in Table 6.

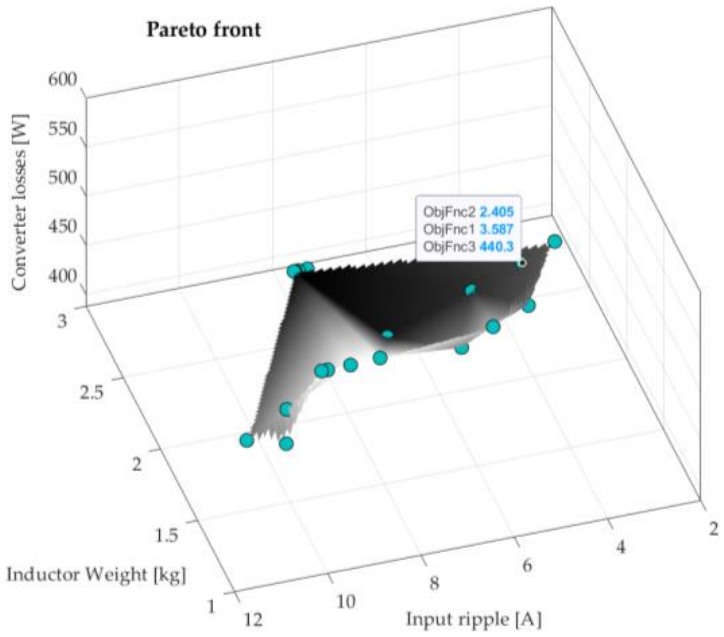


Figure 5. 3D Pareto-front (non-dominated optimal solutions) obtained by NSGA-II and the optimal solution determined by AR.

Table 6. Optimal solution for battery port in MPC.

	Power Conversion Stage
Switching frequency	60 kHz
Number of phases	3 phases
Inductance	175 µH
• Inductor core	AMCC50
• Number of turns	17 turns
• Airgap length	1.6 mm
	Controller stage
Current controller	$C_{i(opt)}(s) = 3341.6\frac{(s+1641)(s+1608)}{s(s+48140)(s+55810)}$
Voltage controller	$C_{v(opt)}(s) = 12799\frac{(s+1180)(s+1147)}{s(s+4567)(s+4703)}$

To verify the performance of optimized control, an IBC model for time-domain simulation is developed in the Matlab Simulink using SimPowerSystems. The output voltage is regulated at a fixed voltage of 400 V. At t = 0.05 s, the output load current modeled as a current source increases from 75 A to 150 A and decreases from 150 A to 75 A at t = 0.1 s. The type-III current- and voltage-controllers based on the 'k-factor' approach are designed as a benchmark.

Figure 6 shows the simulation responses of output voltage, input current, and inductor current when the load current changes. The optimized type-III controllers exhibit faster dynamics in both

current and voltage loop in comparison with the 'k-factor' based controllers, resulting in reductions in undershoot (−25%) and overshoot (−45%) for the output voltage. Compared to the 'k-factor' approach, the settling time for the optimized controller can be reduced from 25 ms to 10 ms.

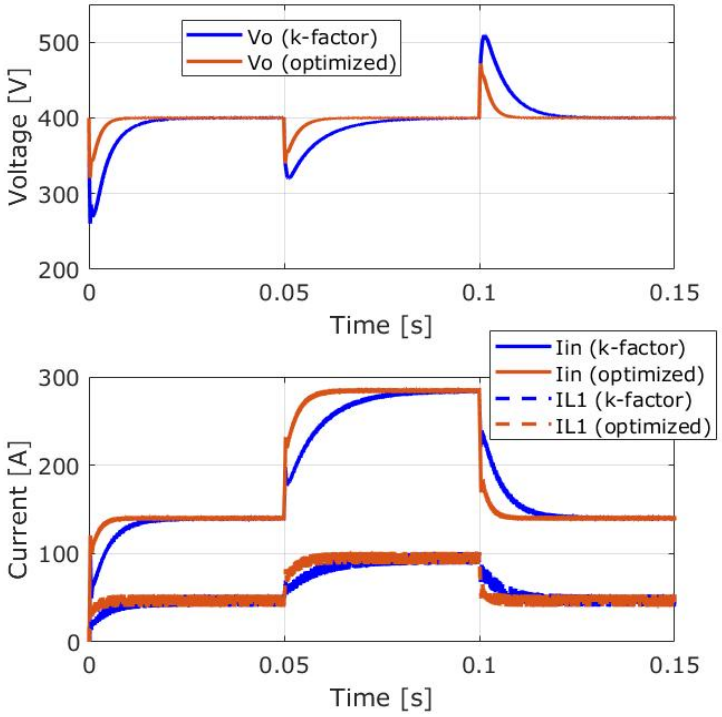
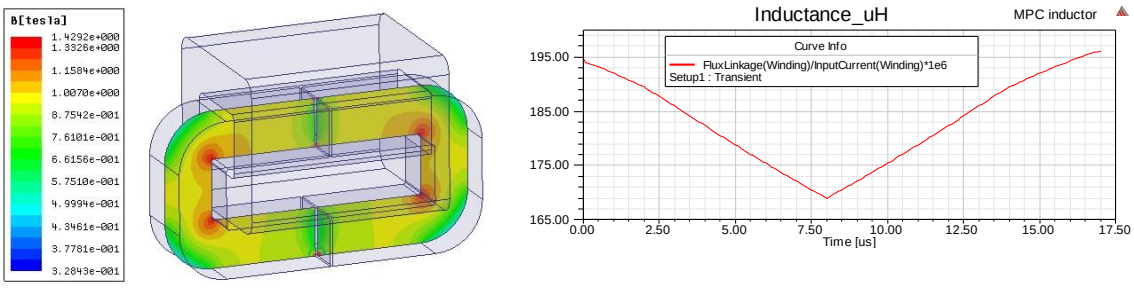


Figure 6. Comparative simulation results for the output voltage, input current and inductor current of conventional 'k-factor' based- and optimal- type-III controllers.

4. Inductor Design

This section presents detailed inductor design using the optimal parameters obtained from the previous sections. Computer-aid-design (CAD) and FEA tools are used to verify the inductance value and its temperature rise, which supports to avoid the trial-and-error iteration in the practical design.

Figure 7a,b show FEA results attained from ANSYS Maxwell for the inductor using the optimal parameters in Table 6. It is noted that the inductor simulation uses a lumped copper foil model because it is impractical to draw a model of Litz-wire. Besides, the modeling of individual laminations (18 µm thickness) inside the core is not considered feasible. Hence, the inductor core can be modeled by a solid continuum. However, the FEA inductor model can preserve the anisotropic properties of the laminated structure utilizing a homogenized approach [42].



(**a**) (**b**)

Figure 7. ANSYS Maxwell simulation results for (**a**) flux distribution inside inductor core; (**b**) inductance value during one switching period (f_{sw} = 60 kHz).

In the ANSYS Maxwell, the mesh size is 3mm and the excitation current flowing through the winding is a triangular DC-biased current (55 A average DC-current and 3.8 A current ripple). As can be seen in Figure 7a, the maximum flux density of 1.4 T is obtained at the corners of the window area, whereas the average flux density is about 1T through the mean path length of the inductor core. The flux density values are lower than the saturation flux (1.56 T) of the selected amorphous core. As can be seen in Figure 7b, the average inductance value of 175 μH is achieved with 17 turns and 1.6 mm air-gap.

Figure 8 illustrates the FEA thermal distribution of an inductor. The inductor winding which generates power losses of 6 W is selected as a heat source. Due to free convective heat transfer, the temperature rise on the surface of the inductor core is predicted about 68 °C.

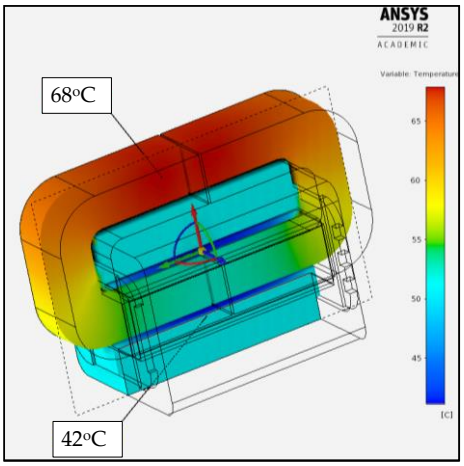
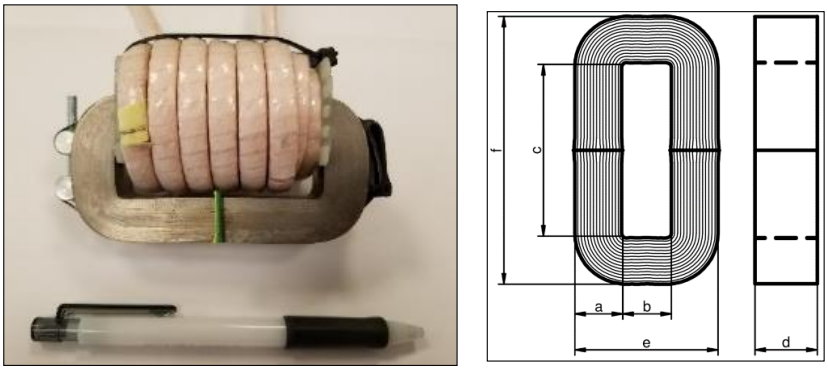


Figure 8. ANSYS AIM simulation for the thermal distribution of an inductor.

An inductor prototype is demonstrated in Figure 9a while the core dimension is shown in Figure 9b. Inductor prototypes are designed using the amorphous core AMCC50 from Metglas, rectangular Litz-wire from Von Roll Isola (Belfort, France, 0.2 kg/m, 2600 strands, the strand diameter is 0.1 mm, and RMS rating current is 60 A), and nylon bobbin. The three materials allow operating temperatures higher than 200 °C. The weight of an inductor is 1 kg due to additional screws and metal strip fastener. As the air gap lengths and winding lengths of inductors are not identical, the measured inductance of three phases are 175.7 μH, 173.5 μH, and 175.4 μH, respectively, which are slightly deviated from the desired value 175 μH. The unbalanced inductor currents due to the inductance deviation can be compensated by the closed-loop controllers.



(**a**) (**b**)

Figure 9. (**a**) Inductor prototype; (**b**) Dimensions of AMCC50 core: core build a = 16 mm; window width b = 20 mm; window length c = 70 mm; core height d = 25 mm; core width e = 52 mm; core length f = 102mm; core weight m_{core} = 586 g. Calculated specification: mean magnetic path length l_m = 24.4 cm; net cross-sectional area A_c = 3.3 cm^2; window area W_a = 14 cm^2; area product A_p = 45.9 cm^4.

5. Prototype Demonstration and Experimental Results

This section depicts a full-scale converter prototype in comparison with other published prototypes available in the literature. Besides, this section presents the FPGA implementation of digital controller before showing the verified experimental results.

5.1. Proposed Hardware Prototype and Comparison

As mentioned in the introduction, the MPC consists of two separate ports (30 kW/port) that can employ the same IBC topology for the sake of simplicity and modularity. It is noted that the proposed COF has been demonstrated above only for the IBC connecting to the battery port. Similarly, the proposed codesign methodology can be applied for the IBC of the SC port with the input voltage range of 200 V~400 V. The optimal inductance for the SC port is 145 µH which can be realized by using the same AMCC50 core and Litz wire as described in Figure 9b, except for a 15 turns winding. In this regard, a 60 kW MPC prototype has been fabricated to demonstrate the feasibility of the proposed COF.

Figure 10a shows the CAD model of a custom-made cold plate using liquid-cooling to ensure the peak junction temperature of the SiC MOSFET modules in the safe operation. Figure 10b depicts the actual implementation of SiC HB modules mounting on the top side of the cold plate. Laminated busbar which comprises two parallel aluminum plates separated by dielectric materials are designed to reduce the stray parasitic inductance of the DC-link. A heat exchanger with a pump is connected to the cold plate to circulate the coolant with the volumetric fluid flow rate of 4 L/min.

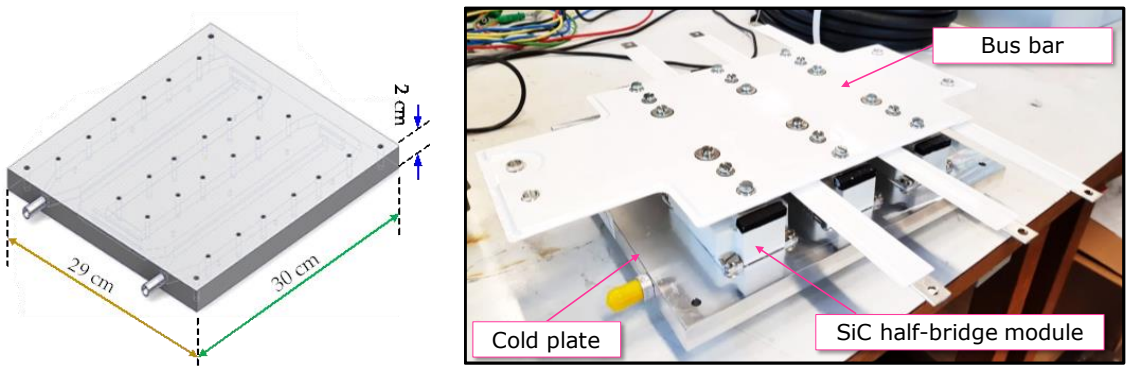
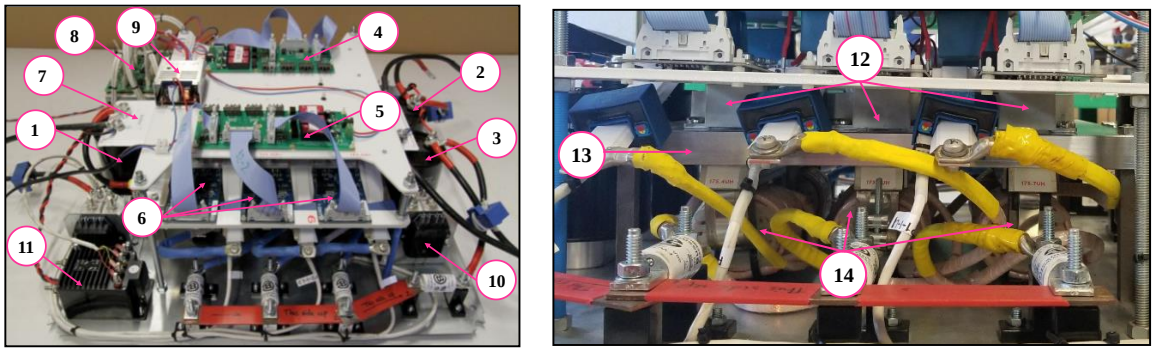


Figure 10. (**a**) CAD model of liquid-cooling cold plate, (**b**) placement of SiC half-bridge modules and a bus bar on top side of the cold plate.

Figure 11a,b show the overview and side-view layout of functional subsystems. Six SiC HB modules are mounted on the top of the cold plate, whereas six inductors are attached to its bottom side. In case, by leveraging the automated reconfigurable concept with the aid of controlled relays, the two ports based on two three-phase IBCs can be converted to a single six-phase IBC, increasing power capability. This approach enhances the scalability and modularity for the entire converter system, reducing the total cost of ownership.

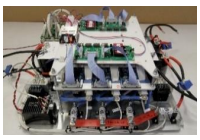
Table 7 compares the system specifications between the proposed prototype and different multiphase DC/DC prototypes including a battery charger [45], a railway traction converter [3], and a multidevice interleaved boost converter (MDIBC) [4] which are available in the literature. The published converters with amorphous cores are selected for the sake of a fair comparison. Several comments can be made as follows. First, it should be highlighted that by increasing switching frequency, inductor size can be reduced for the proposed SiC-based converter, resulting in overall reductions in weight and volume by 40% and 35%, respectively, compared to the Si-based IGBT MDIBC.



(**a**) (**b**)

Figure 11. Proposed hardware prototype (**a**) overview, and (**b**) side-view (①: output capacitor; ②-③: input capacitors of port 1 and port 2, respectively; ④–⑤: receiver boards; ⑥: gate driver boards; ⑦: bus bar; ⑧: measurement board; ⑨: power supply module; ⑩: precharge module; ⑪: voltage sensor; ⑫: half-bridge modules; ⑬: cold plate; ⑭: inductors).

Table 7. Overall comparison of multiphase DC/DC prototypes.

Specifications	DC/DC Battery Charger [45]	Railway Traction DC/DC Converter [3]	Multi-Device Interleaved Boost Converter [4]	Proposed Prototype (with 2 Ports)
Overview				
Dimension	350 × 300 × 250 mm	565 × 240 × 90 mm (only for inductors)	350 × 300 × 200 mm	300 × 300 × 150 mm
Power rating	100 kW	225 kW	30 kW	30 kW/port → 60 kW
Number of phases	4 phases	8 phases	4 phases	3 phases/port
Cooling method	Air-forced cooling	Air-forced cooling	Air-forced cooling	Liquid cooling
Power device	SiC MOSFET (discrete TO-247)	SiC MOSFET (HB module package 62 mm)	Si IGBT (HB module package 62 mm)	SiC MOSFET (HB module package 62 mm)
Switching frequency	60 kHz	30 kHz	20 kHz	60 kHz
Maximum efficiency	97%	98%	97%	98.4%
DC-link voltage	540 V	800 V	400 V	400 V
Volume	26.25 L	12.2 L (only for inductors)	21 L	13.5 L [(1)]
Weight	7.5 kg	-	15 kg	9 kg [(2)]
Volumetric power density	3.8 kW/L	-	1.4 kW/L	4.4 kW/L
Gravimetric power density	13.3 kW/kg	-	2 kW/kg	6.7 kW/kg

[(1)] The volume of the liquid-cycling system (pumps, radiator, compressor, and chiller) is not included. [(2)] The weight of the liquid-cycling system (pumps, radiator, compressor, and chiller) is not included.

Second, as the discrete TO-247 packages offer lighter weights compared to the 62 mm HB packaging, the discrete-based design in [45] has a gravimetric power density higher than the proposed prototype. However, in the converter using discrete TO-247 packages, some challenges for gate driver design should be taken into account to avoid unbalanced currents and cross-talk between parallelized MOSFETs. The main purpose of this paper is to demonstrate the feasibility of the codesign methodology involving

both hardware and controller optimization. There is still room for the optimization of component arrangement and thermal management to achieve higher power density, which is considered as our future work.

5.2. FPGA Digital Control Implementation

In this paper, the digital controller is implemented based on a digital redesign approach. Once the transfer functions of the controllers $C_i(s)$ and $C_v(s)$ are obtained in the s-domain, they are discretized using the Tustin transformation ($s \Leftrightarrow \frac{2}{T_{sampling}} \cdot \frac{z-1}{z+1}$). The Tustin transformation provides a good agreement in the frequency domain between the continuous- and discrete- transfer functions [46]. Typically, a good choice for the discretized sampling period $T_{sampling}$ is equal to the switching period T_{sw} ($= 1/f_{sw}$). Besides, in practice, the sampling period of the controller and the sampling period of analog-digital-converter (ADC) are the same. The sampling instants of the ADC are carefully selected when the bottom switch turns off to minimize errors induced by the switching noise.

In this paper, the standard form-I is adopted to implement the difference equation of the discrete transfer function thanks to its simplicity, configurability, and scalability [46]. Moreover, debugging is convenient as the error signal and the output reference signal can be followed independently in the difference equation. The discrete controller $C(z)$ in Equation (48) can be translated into the difference equation through the inverse z-transform as Equation (49) so that it can be implemented via a direct form-I:

$$C(s) \overset{s=\frac{2}{T_{sampling}} \cdot \frac{z-1}{z+1}}{\rightarrow} C(z) = \frac{u(z)}{e(z)} = \frac{\sum_{i=0}^{3} a_i \cdot z^{3-i}}{\sum_{i=0}^{3} b_i \cdot z^{3-i}} = \frac{\sum_{i=0}^{3} a_i \cdot z^{-i}}{\sum_{i=0}^{3} b_i \cdot z^{-i}} \tag{48}$$

$$u_k = \frac{1}{b_0} \cdot (a_0 \cdot e_k + a_1 \cdot e_{k-1} + a_2 \cdot e_{k-2} + a_3 \cdot e_{k-3} - b_1 \cdot u_{k-1} - b_2 \cdot u_{k-2} - b_3 \cdot u_{k-3}) \tag{49}$$

In Equation (48), $u(z)$ is the output control signal, $e(z)$ is the error between the reference signal and the measured signal. Where e_k, e_{k-1}, e_{k-2}, e_{k-3} is the present, one-sample period, two-sample period, three-sample period delayed values of the error signals, respectively. Similarly, u_k, u_{k-1}, u_{k-2}, u_{k-3} is the present, one-sample period, two-sample period, three-sample period delayed values of the output control signals, respectively. In the outer loop, the output voltage controller $C_v(z)$ generates $u(z)$ as the reference control signal of total inductor currents I_{ref} for the inner loop in which the current controller $C_i(s)$ generates the required duty cycle.

The discrete transfer functions in the z-domain of current- and voltage- digital controllers based on the optimized design and the 'k-factor' design are expressed in Equation (50)–Equation (53), respectively:

$$C_{i(opt)}(z) = \frac{0.044 \cdot z^{-1} - 0.064 \cdot z^{-2} + 0.0231 \cdot z^{-3}}{1 - 1.6074 \cdot z^{-1} + 0.6917 \cdot z^{-2} - 0.0843 \cdot z^{-3}} \tag{50}$$

$$C_{v(opt)}(z) = \frac{0.1985 \cdot z^{-1} - 0.3875 \cdot z^{-2} + 0.1891 \cdot z^{-3}}{1 - 2.8020 \cdot z^{-1} + 2.6137 \cdot z^{-2} - 0.8117 \cdot z^{-3}} \tag{51}$$

$$C_{i(kfac)}(z) = \frac{0.0168 \cdot z^{-1} - 0.0273 \cdot z^{-2} + 0.011 \cdot z^{-3}}{1 - 1.475 \cdot z^{-1} + 0.5308 \cdot z^{-2} - 0.0563 \cdot z^{-3}} \tag{52}$$

$$C_{v(kfac)}(z) = \frac{0.1348 \cdot z^{-1} - 0.2646 \cdot z^{-2} + 0.1298 \cdot z^{-3}}{1 - 2.732 \cdot z^{-1} + 2.482 \cdot z^{-2} - 0.75 \cdot z^{-3}} \tag{53}$$

Figure 12 shows a simplified block diagram of the digital control system. The control platform used in this paper is dSPACE MicroLabBox which includes two main boards (i.e., processor board DS1202 and FPGA board DS1302). The voltage reference setpoint and control coefficients can be set from the processor part which communicates with the FPGA board via local buses. The dual-loop control scheme is implemented on the FPGA board. The form-I digital implementation for type-III controller

based on Equation (49) is realized using Xilinx System Generator (XSG) blocksets such as adder, multiplier, registers. Additional configuration steps of the FPGA are needed to convert the XSG block program into the VHDL code. To this end, a VIVADO software version 17.2 provides an automatic synthesis and place-and-route tool to ultimately generate the bitstream file. The file can be downloaded into Xilinx Kintex-7 XC7K325T FPGA (10 ns period clock) embedded in the DS1302 board.

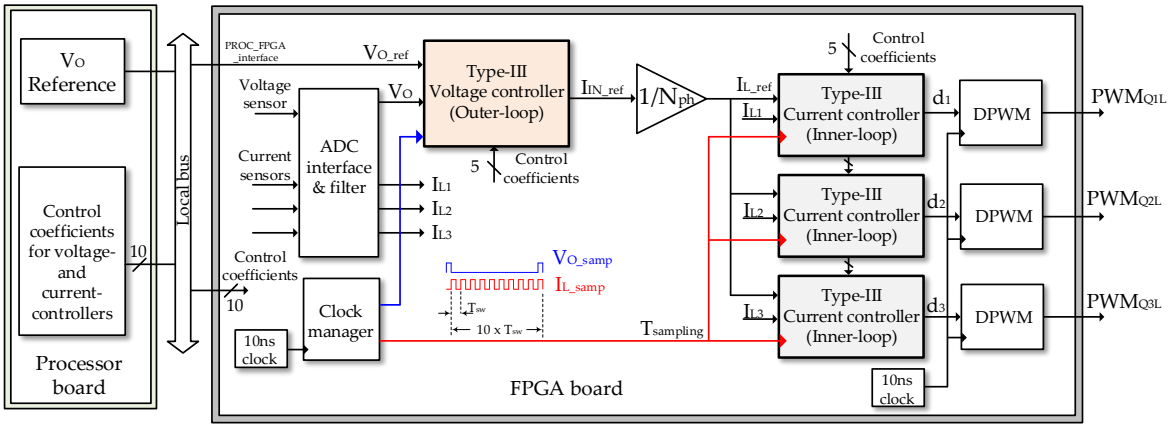


Figure 12. Block diagram of digital controller.

Figure 13a shows the principle of digital pulse width modulation (DPWM). A 16-bit count-limited counter is used to create a sawtooth carrier of the DPWM. As shown in Figure 13b, the period of the PWM is measured from zero to the limited counting value in the counter cycle. The phase-shift between each phase is realized by delay blocks.

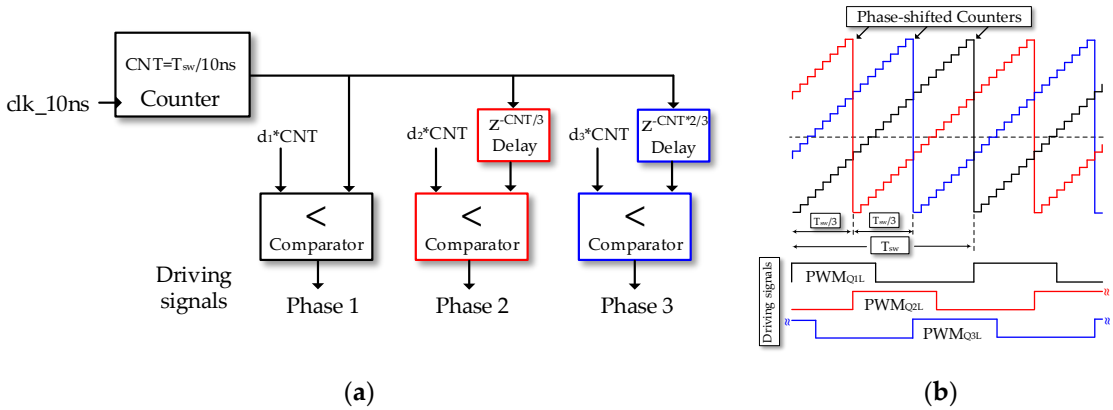


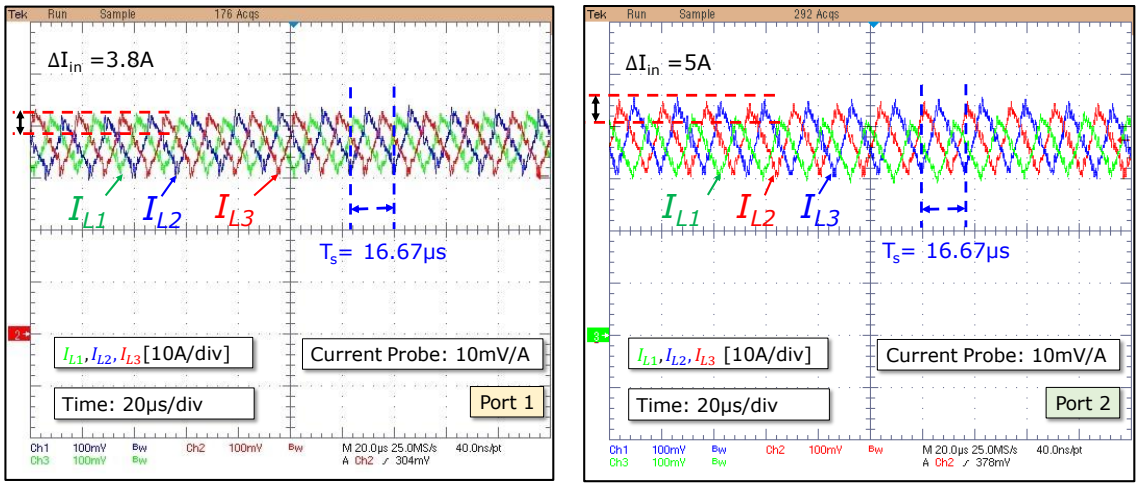
Figure 13. (**a**) Block diagram of digital PWM generator, (**b**) simplified phase-shifted operation for PWM driving signals.

5.3. Experimental Results

An experimental test bench was prepared in our laboratory. During the test procedure, a fixed input voltage is provided from a DC power supply. The output voltage is regulated at a constant voltage irrespective of output load disturbances. The experimental waveforms are measured and captured using a TDS5054B oscilloscope (Tektronix, Beaverton, OR, USA) with an accuracy of ±1%. The probing scales are 10 mV per 1 A for current probes and 5 mV per 1V for differential voltage probes.

Figure 14a,b show the experimental waveforms of three-phase interleaved inductor currents for the port 1 with 175 µH and the port 2 with 145 µH, respectively. The testing condition is at input voltage 250 V, output voltage 395 V, output power 27 kW. The inductor currents are balanced and shifted 120 degrees between phase-to-phase, confirming the developed control-oriented models in Table 2 and the proposed dual-loop control strategy. It can also be observed that at the same switching

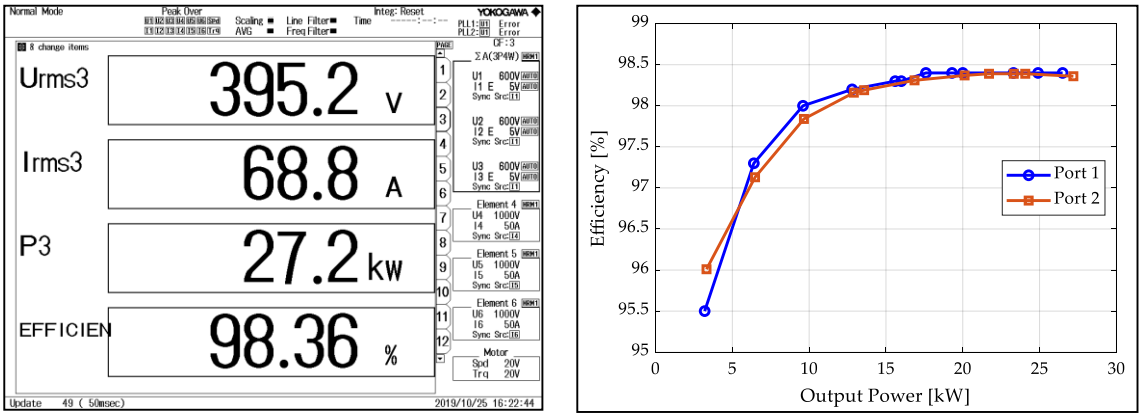
frequency 60 kHz (T_s = 16.67 µs), the input current ripple of 3.8 A at port 1 is less than that of 5 A at port 2. The experimental results are all in close agreement with the analytical model of the total input current ripple as selected for the $ObjFnc_1$.



(**a**) (**b**)

Figure 14. Experimental waveforms of three-phase interleaved inductor currents at 27 kW (V_{in} = 250 V, V_O = 395 V) (**a**) port 1 with L = 175 µH; (**b**) port 2 with L = 145 µH.

Figure 15a shows the efficiency obtained from YOKOGAWA WT1806E precision power analyzer (basic power accuracy 0.02%). It is noted that the IBC employing SiC technology can obtain a high efficiency of 98.4% at 27.2 kW. The experimental result achieves a high degree of accuracy with the theoretical model of the total converter losses as developed for the $ObjFnc_3$. Figure 15b plots the measured efficiency curves of two ports over the load range from 3.5 kW to 27 kW at fixed input voltage 250 V and output voltage 395 V.



(**a**) (**b**)

Figure 15. (**a**) IBC efficiency measured from YOKOGAWA power analyzer; (**b**) efficiency of two ports (V_{in} = 250 V, V_O = 395 V) with 2% error band of sensors and measuring.

Figure 16 shows the temperature distribution of port 1 measured by a FLIR thermal camera (2% accuracy). The temperature of the inductor core is 62 °C, which is in agreement with the FEA simulation result. The temperature of the HB module is about 45 °C.

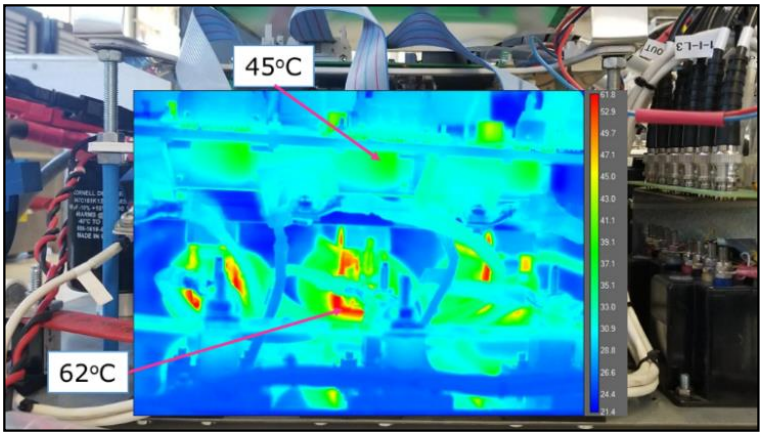
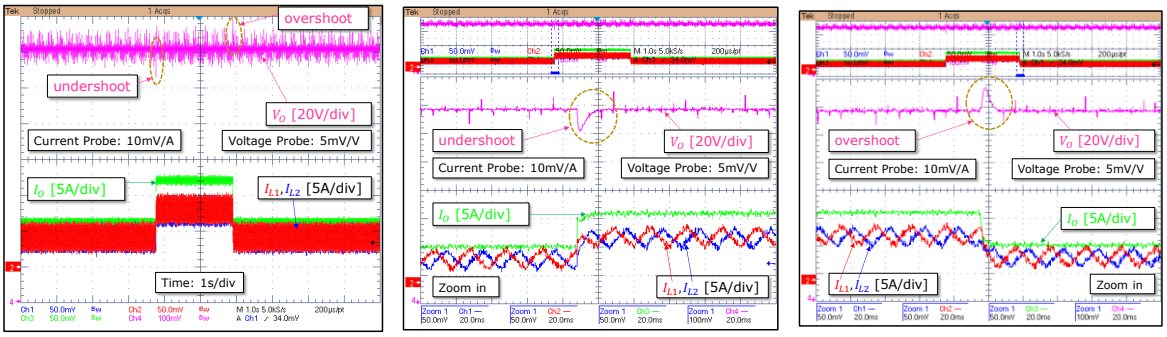


Figure 16. Inductor core temperature (62 °C) and half-bridge module temperature (45 °C) measured from FLIR thermal camera.

Figures 17a and 18a show overall dynamic behaviors (including output voltage, output current, inductor currents) for the classical 'k-factor' based controller and the optimized type-III controller, respectively. When the input voltage is 70 V, the output voltage is 140 V, and the step load is instantaneously varied between 25 Ω and 12.5 Ω. The zoom-in waveforms during the transient time are provided in Figure 17b,c for the 'k-factor' design while in Figure 18b,c for the optimized design. Compared to the conventional 'k-factor' design, the optimized controller exhibits better performance, providing smaller undershoot/overshoot (reduction of 37%) and faster settling time in the output voltage (reduction of 42%).

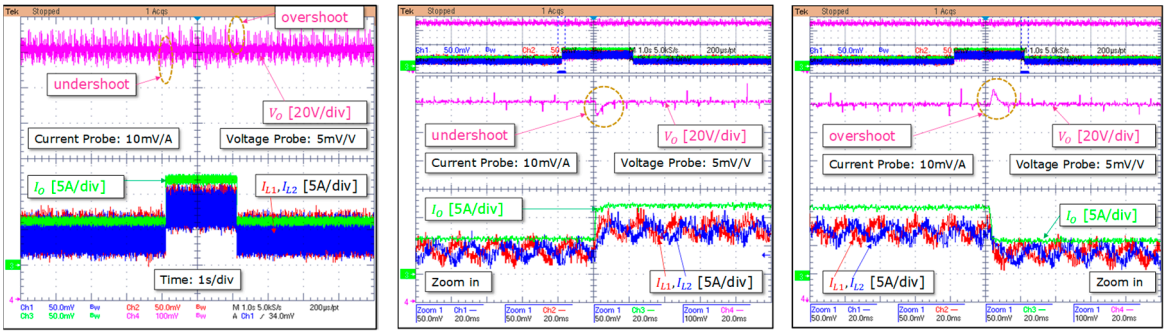


(**a**) (**b**) (**c**)

Figure 17. Experimental waveforms for 'k-factor' based controllers at V_{in} = 70 V, V_O = 140 V, R_O = 25 Ω/12.5 Ω, (**a**) overview when 100% load change, (**b**) zoom-in waveforms for positive load change, (**c**) zoom-in waveforms for negative load change.

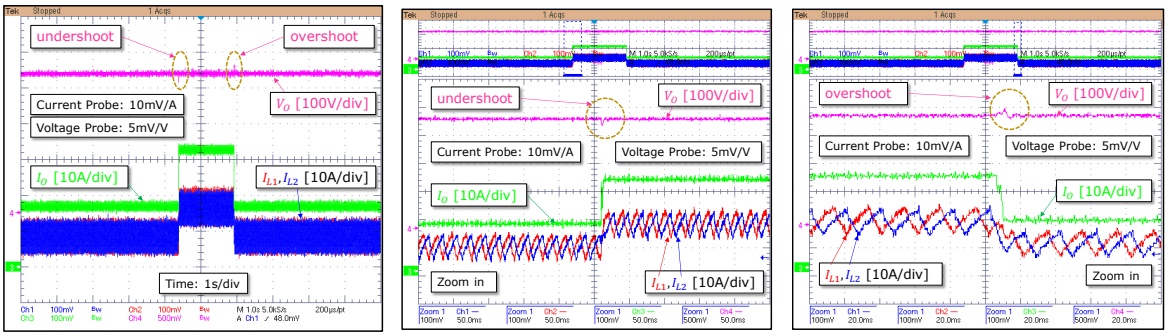
Similar experimental tests on load disturbances are conducted with V_{in} = 250 V, V_O = 385 V. The load R_O is changed between 25 Ω and 12.5 Ω, leading to the output power being varied between 6 kW and 12 kW. The dynamic behaviors regarding 'k-factor' based and optimized controllers are shown in Figures 19a and 20a, respectively. In this case, a maximum reduction of 33% in the amplitude of overshoot in the output voltage can be attained. With a reduction of 50% in the settling time, the optimized controller has a much better output voltage transient response, meaning that the optimized design requires less control energy to recover from the disturbance. As can be seen from two dynamic testing cases, the experimental results show a high degree of correlation with the simulation results as provided in Figure A1 in Appendix B. The closed-loop performances for the output voltage responses of two different approaches are quantified in Table 8 in terms of undershoot/overshoot (in the percentage of V_O) and settling time. The optimized controller has better disturbance rejection

capability and faster than the traditional 'k-factor' approach. This is the benefit of minimizing the control effort in the proposed COF.



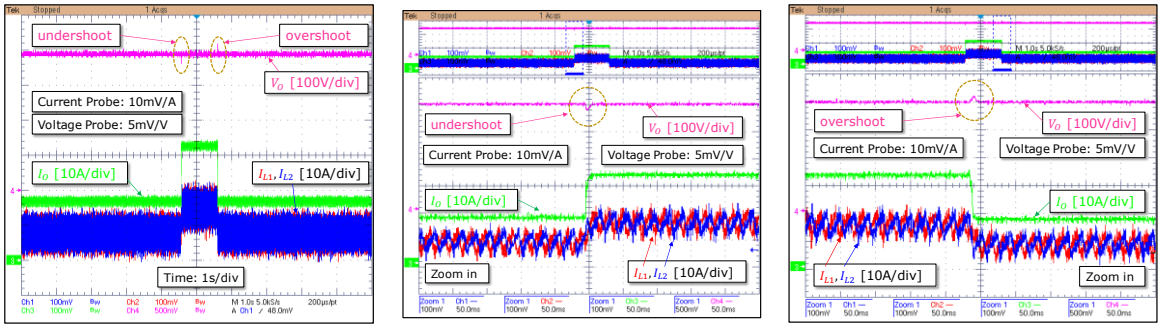
(**a**) (**b**) (**c**)

Figure 18. Experimental waveforms for optimized controllers at V_{in} = 70 V, V_O = 140 V, R_O = 25 Ω/12.5 Ω, (**a**) overview when 100% load change, (**b**) zoom-in waveforms for positive load change, (**c**) zoom-in waveforms for negative load change.



(**a**) (**b**) (**c**)

Figure 19. Experimental waveforms for 'k-factor' based controllers at V_{in} = 250 V, V_O = 385 V, R_O = 25 Ω/12.5 Ω, (**a**) overview when 100% load change, (**b**) zoom-in waveforms for positive load change, (**c**) zoom-in waveforms for negative load change.



(**a**) (**b**) (**c**)

Figure 20. Experimental waveforms for optimized controllers at V_{in} = 250 V, V_O = 385 V, R_O = 25 Ω/12.5 Ω, (**a**) overview when 100% load change, (**b**) zoom-in waveforms for positive load change, (**c**) zoom-in waveforms for negative load change.

Table 8. Comparative closed-loop performance for output voltage response of 'k-factor' based controller and optimal controller.

Case	Specifications	'k-Factor' Controller		Optimal Controller		Reduction in Experiment
		Simulation	Experiment	Simulation	Experiment	
Case 1: V_{in} = 70 V, V_O = 140 V, P_O = 0.8 kW →1.6 kW→0.8 kW	Maximum undershoot	9.3%·V_O (13 V)	11%·V_O (16 V)	7%·V_O (10 V)	7%·V_O (10 V)	−37%
	Maximum overshoot	10.7%·V_O (15 V)	11%·V_O (16 V)	7%·V_O (10 V)	7%·V_O (10 V)	−37%
	Maximum settling time	11 ms	12 ms	7 ms	7 ms	−42%
Case 2: V_{in} = 250V, V_O = 385V, P_O = 6 kW →12 kW→6 kW	Maximum undershoot	7.8%·V_O (30 V)	6.5%·V_O (25 V)	5.2%·V_O (20 V)	5.2%·V_O (20 V)	−20%
	Maximum overshoot	9.1%·V_O (35 V)	7.8%·V_O (30 V)	6.2%·V_O (24 V)	5.2%·V_O (20 V)	−33%
	Maximum settling time	15 ms	20 ms	10 ms	10 ms	−50%

6. Conclusions

In this paper, the simultaneous COF for both the power conversion and controller stages of the IBC has been proposed and demonstrated. Four contradictory objective functions (the total input current ripple, the total weight of inductors, the total power losses, and the integral of time-weighted absolute error for the output voltage) have been expressed properly in the analytical forms, which should be minimized simultaneously. The optimization process based on the NSGA-II and the AR entails the selection of number of phases, switching frequency, inductor sizing, and control parameters of type-III controllers embedded in the dual-loop control strategy.

The experimental results have confirmed the analytical models developed for objective functions. Under the design specifications V_{in} = 250 V and V_O = 395 V, the IBC can achieve high efficiency of 98.4% at 27.2 kW, which is well-matched with the calculated power losses. Besides, the proposed prototype yields the overall reduction in weight and volume by 40% and 35%, respectively, and the power density of 6.7 kW/kg, which is four times higher, compared to the Si-based IGBT MDIBC in [4]. Besides, regarding control validation, the optimized design of type-III controller has lower undershoot/overshoot (maximum 37% reduction) and faster dynamic response (the reduction up to 50% in the settling time) compared to the traditional 'k-factor' approach. Furthermore, a high degree of correlation has been achieved for closed-loop performance among simulation results and experimental testing.

Moreover, this paper provides not only a holistic analysis of power conversion and controller codesign, but also puts forward the emphasis and orientation of the future study. This will broaden relevant researchers' vision and promote the development of practical design with low cost and high performance for the multiphase DC/DC converters. The proposed COF reveals new directions for future research by integrating other considered aspects such as reliability factor, capital expenditure of components, and converter volume.

It should be pointed out that in this paper, some assumptions have been made for model simplifications and approximation to facilitate the optimization process. Therefore, there is still room for future development, which can involve improving the model fidelity and the component database. For example, the high-fidelity electro-thermal model can be adopted for the loss model of SiC MOSFET, or the fringing effect can be incorporated into the change of inductance value due to varying of a new design variable such as air-gap length. Moreover, in future work, core materials can be considered as design variables, which will be potentially optimized further considering different magnetic materials such as amorphous and nanocrystalline in the core database. As a result, the searching space will be expanded significantly, and new aspects of optimal solutions can be revealed.

Author Contributions: D.-D.T. has written the manuscript and presented the simultaneous codesign optimization methodology; S.C. analyzed multiport converter; Y.L. designed and analyzed the inductors, M.E.B. and O.H. reviewed and edited the manuscript and they also provided supervision guidance to this research. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Table A1. Commercially available SiC power modules.

Parameter	1200 V CREE CAS300H12BM2 62 × 106 × 30 [mm]		1200 V CREE CAS325M12HM2 65 × 110 × 10 [mm]		1200 V SEMIKRON SKM350MB120SCH17 62 × 106 × 30 [mm]		1200 V ROHM BSM300D12P2E001 62 × 152 × 17 [mm]		1200 V FUJI Elec 2CSI300CAS120 A-50 42 × 126 × 19 [mm]	
$V_{on}[V]$	0	0.825	0	0.833	0	1.05	0	0.705	0	0.72
$R_{on}[m\Omega]$	7.7	6.7	7.6	8	9.5	12	15	5.67	10.6	9.067
$E_{on}[mJ]$ (600 V 300 A)	5.8	-	5.6	-	8.65	-	9.5	-	4.3	-
$E_{off}[mJ]$ (600V 300 A)	6.1	-	3.7	-	7.98	-	10.5	-	10	-
$E_{rr}[mJ]$	-	0.64	-	0.86	-	0.088	-	0.7	-	2.57
$I_D[A]$	300		325		523		600		600	
$T_{j(\max)}[^OC]$	150		175		175		175		175	
$R_{th(j-c)}[^OC/W]$	0.075	0.076	0.115	0.127	0.045	0.18	0.08	0.11	0.098	0.098
Weight [g]	300		140		325		350		-	
Cost [€]	558		1306		473		668		-	

Table A2. Comparison of different magnetic materials.

Material Name	Manufacturer	Name	Saturation Flux Density (T)	Mass Density (g/cm^3)	Initial Relative Permeability	Core Loss @0.1 T, 20 kHz (kW/m^3)
Ferrite	Ferroxcube	3C93	0.5	4.8	1800	5
Iron-powder	Manetics	MPP60	0.75	8.2	60	45
Nanocrystalline	VAC	Vireoperm500F	1.2	7.3	15500	5
Amorphous	Metglas	2605SA1	1.56	7.18	1200	70
Silicon-steel	JFE	10JNHF600	1.87	7.53	800	150

Appendix B

In this appendix, comparative simulation results of the 'k-factor' based controller and the optimal controller are provided in Figure A1a,b for two cases, V_{in} = 70 V, V_O = 140 V and V_{in} = 250 V, V_O = 385 V, respectively. Compared to the measured waveforms in Figures 17–20, only a small deviation (<2%) between simulation and experimental results is recorded due to equipment error and uncertain noises, which is acceptable. Therefore, the experimental results show a high degree of correlation with the simulation results according to each case, which validates the optimal controller derived from the proposed COF.

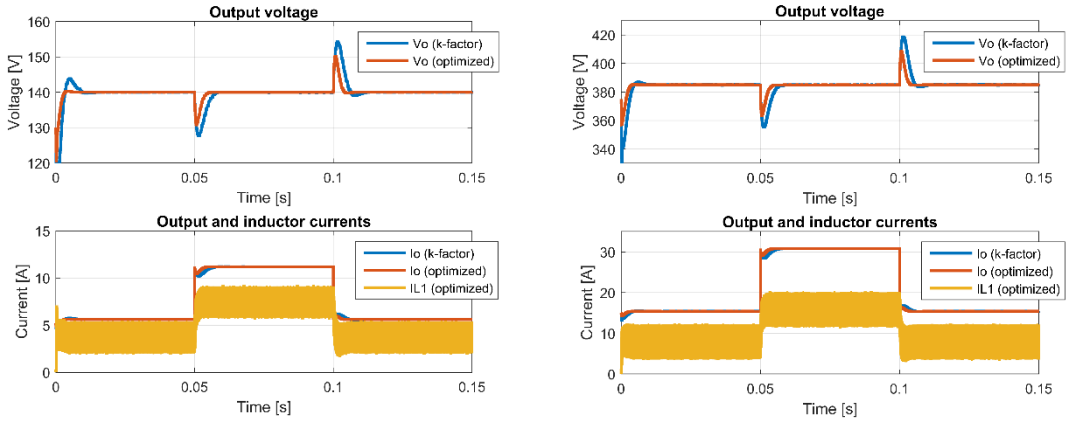

Figure A1. Comparative simulation results of 'k-factor' and optimal controller under positive/negative step load change 12.5 Ω/25 Ω when (**a**) V_{in} = 70 V and V_O = 140 V; (**b**) V_{in} = 250 V and V_O = 385 V.

Appendix C

This appendix explains step-by-step for the derivation of (28) in which the inductance value can be found based on a given core and design specification. The main steps are highlighted as follows.

Step 1:

The reluctance of the core can be neglected compared to that of the air gap, which results in Equation (A1).

$$N_{turn} \cdot i = \frac{\phi \cdot l_{gap}}{\mu_0 \cdot A_C} \tag{A1}$$

where N_{turn} is the number of turns, ϕ is the magnetic flux, l_{gap} is the air gap, μ_0 is the vacuum magnetic permeability, and A_C is the net cross-sectional area of the core. Given a peak winding current $I_{L(crit,pk)}$, it is desired to operate the core below the saturation flux density $B_{\max}$. Thus, Equation (A1) becomes Equation (A2).

$$N_{turn} \cdot I_{L(crit,pk)} = B_{\max} \cdot \frac{l_{gap}}{\mu_0} \tag{A2}$$

Step 2:

The inductance is related to the number of turns N_{turn} and the reluctance as shown in Equation (A3).

$$L = \frac{\mu_0 \cdot A_c \cdot N_{turn}^2}{l_{gap}} \tag{A3}$$

Step 3:

The wire must fit through the core window W_a. However, the wire does not pack perfectly which reduces the utilization factor K_u of the core window. Furthermore, insulation and the bobbin itself take some other place, which causes the utilization factor K_u to drop to values between 0.3 and 0.6. As a result, the number of turns in the core is limited by Equation (A4).

$$N_{turn} \cdot A_{wire} = K_u \cdot W_a \tag{A4}$$

where A_{wire} is the cross section of wire. The wire needs to carry the peak current as Equation (A5).

$$A_{wire} = \frac{I_{L(crit,pk)}}{J_w} \tag{A5}$$

By substituting Equation (A5) into Equation (A4) and then into Equation (A3), an expression of the maximum air-gap for the maximum number of turns can be derived in Equation (A6).

$$l_{gap} = \frac{K_u \cdot W_a \cdot J_w \cdot \mu_0}{B_{\max}} \tag{A6}$$

It is clear that Equation (A6) is a function of only the material and geometry of the core. It expresses the needed air gap to avoid the material saturates when the core window is filled with conductors. In standard design techniques, L is calculated based on the specifications on the ΔI_L. However, in this design algorithm, ΔI_L is a design variable, while the specification is set to ΔI_{in} that can be met with the phase interleaving. As a result, L becomes a design variable and it is related to the selected core. Moreover, it is worth expressing the peak inductor current explicitly in terms of the inductance L, as in Equation (A7).

$$I_{L(crit,pk)} = I_{L(crit)} + \frac{1}{2}\frac{V_O(1-D_{\max})D_{\max}}{f_{sw} \cdot L} \tag{A7}$$

where $I_{L(crit)}$ is given in Equation (A8).

$$I_{L(crit)} = \frac{P_{\max}}{N_{ph} \cdot V_O(1-D_{\max})} \tag{A8}$$

Step 4:

By substituting Equation (A7) and a version of Equation (A1) rearranged in N_{turn} into Equation (A2), a second-degree polynomial expression of L can be derived as below.

$$L^2 I_{L(crit)}^2 + L \cdot \left[\frac{I_{L(crit)}(1-D_{\max})D_{\max}}{f_{sw}} - K_u \cdot J_{wire} \cdot B_{\max} \cdot (W_a \cdot A_C) \right] + \left[\frac{V_O(1-D_{\max})D_{\max}}{2 \cdot f_{sw}} \right]^2 = 0$$

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