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DC Bus Voltage Control of Grid-Side Converter in Permanent Magnet Synchronous Generator Based on Improved Second-Order Linear Active Disturbance Rejection Control

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Abstract: In the permanent magnet synchronous generator (PMSG), the DC bus voltage fluctuates up and down under the influence of the load and power grid, which greatly affects the safe and reliable work of PMSG. In order to suppress the wide range fluctuation of DC bus voltage under disturbance and enhance its anti-disturbance performance, an optimized DC bus voltage control strategy is proposed by using the improved linear active disturbance rejection control (LADRC) in the voltage outer loop. By considering factors, such as load disturbance and grid voltage mutation as the total disturbance of the system, the improved reduced-order linear expansion state observer (RLSEO) is used to estimate and compensate the total disturbance, which greatly improves the stability of DC bus voltage. Firstly, the mathematical model of grid-side converter is established. On this basis, the LADRC control based on RLESO is designed, which reduces the phase lag of the linear extended state observer (LESO) and enhances the disturbance observation accuracy of the system. Then, a lead lag correction link is added to the total disturbance channel of RLESO to reduce the noise amplification effect of RLESO. Finally, the frequency domain characteristic analysis and stability proof of the improved LADRC control strategy are carried out. The simulation results show that the control strategy proposed in the article has a better control effect on the DC bus voltage.

Keywords: DC bus voltage; grid-side converter; linear active disturbance rejection control; reduced-order linear expansion state observer; correction link; frequency domain analysis

1. Introduction

A permanent magnet synchronous generator (PMSG) has the characteristics of a simple structure, low maintenance cost, low noise, and flexible operation control, which has attracted more and more attention of researchers both domestic and foreign [1,2]. PMSG usually uses a dual pulse width modulation (PWM) converter to realize grid-connected power generation [3]. Its topology is shown in Figure 1. The motor-side converter is mainly responsible for controlling the output power of the PMSG, so as to make full use of wind energy [4]. The grid-side converter is mainly responsible for the safe and stable grid connection of the PMSG system, and realizes the stable control of the DC bus voltage [5]. For the grid-side converter, the conventional double closed-loop control strategy cannot achieve a satisfactory control effect [6]. When the working state of the motor or grid voltage changes suddenly, the DC bus voltage will rise sharply, resulting in the degradation of the PMSG system's

performance [7]. Therefore, adopting a more effective control strategy to suppress the DC bus voltage fluctuation is the key to ensure that PMSG has better performance indicators [8].

Figure 1. Topological structure of the PMSG system.

At present, there are many control methods that can be used to enhance the transient performance of the DC bus voltage of the grid-side converter to resist sudden change of the grid voltage and load disturbance. In [9], the method of enlarging the capacitance of the DC bus can decrease the transient instability degree of the bus voltage, but this method not only increases the volume of the PMSG but also decreases the dynamic response of the system. In [10], the bus capacitance current is reconstructed by using the load information of the motor, which improves the anti-interference ability of the DC side voltage, but it is easily affected by the motor parameters and control strategies. the authors of [11] adopt master-slave control to ensure the power balance of the converters at both ends of DC bus. This modified method can enhance the stability of the DC link voltage in the case of a power network voltage disturbance. However, the control system of the grid-side converter and generator-side converter is coupled with each other, and the design of the system is complex. In [12], a direct control strategy of the DC link capacitance current is proposed. Based on the predictive effect of the differential, the DC link voltage can be tracked in real time more quickly, and the dynamic response of the system is enhanced. In [13], the control method of power feed-forward is adopted, and the active power is directly regulated by the current inner loop, which reduces the regulation time of the DC link voltage. However, when the motor load torque changes suddenly, its control effect on the DC link voltage is not obvious.

Active disturbance rejection control (ADRC) is a new control strategy proposed by Professor Han J.Q. It can make the internal and external disturbances, unmodeled dynamics, and other parts of the system equivalent, which are different from the integral series type into the total disturbance of the system [14], and the extended state observer (ESO) is used to estimate and compensate the total disturbance [15,16]. The authors of [17] apply ADRC to wind power inverters, which shows that it has a strong control effect for complex systems with strong coupling, both multivariable and nonlinear. The authors of [18] relate the controller parameters to the bandwidth and propose linear active disturbance rejection control (LADRC), which solves the problem of numerous parameters of traditional nonlinear ADRC. In [19,20], the known outputs of the system are deleted from the linear extended state observer (LESO), and an LADRC method based on the reduced-order linear extended state observer (RLESO) is proposed, which can reduce the phase lag of the system, and enhance the anti-interference rejection and robustness of the LADRC.

In this paper, the DC bus voltage is taken as the control object, and the LADRC control is constructed to replace the voltage outer loop. Because the DC bus voltage can be obtained by timely and accurate measurement in the measurement link, it is deleted from LESO, and a RLESO with

the error of the DC bus voltage differential and its observed value as the feedback is constructed. By introducing the correction link based on the lead lag on the total disturbance channel, the amplitude attenuation of the RLESO is increased, and its noise amplification effect is weakened. Frequency domain analysis shows that the anti-disturbance performance of the modified LADRC is better than that of the traditional LADRC. The simulation verifies that the modified LADRC control strategy can ensure that the DC bus voltage has a better control effect under a low-voltage ride through (LVRT) faults.

2. Mathematical Model of the Grid-Side Converter

The topological structure of the grid-side converter is shown in Figure 2. Where e_{ga} , e_{gb} , and e_{gc} are the power network voltages; i_{ga} , i_{gb} , and i_{gc} are the power network currents; u_{ga} , u_{gb} , and u_{gc} are the phase voltages' output by the grid-side inverter; U_{dc} is the DC bus capacitor voltage; i_s is the load current; R is the power network-side equivalent resistance; L is the power network-side filter inductor; and C is the DC bus capacitance.

Figure 2. Topological structure of the grid-side converter.

For the convenience of analysis, the following assumptions are made: The three-phase AC power supply of the grid is sinusoidal steady-state AC and three-phase symmetrical; the equivalent resistance and filter inductance of the power network side are all linear elements; and the switch is an ideal switch without conduction, shutdown delay, and loss. According to the structure shown in Figure 2 and Kirchhoff's law, the following formula can be obtained:

$$\begin{cases} \begin{bmatrix} e_{ga} \\ e_{gb} \\ e_{gc} \end{bmatrix} = \begin{bmatrix} u_{ga} \\ u_{gb} \\ u_{gc} \end{bmatrix} + R \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix}, \\ C \frac{dU_{dc}}{dt} = \sum_{k=a,b,c} S_k i_{gk} - i_s \end{cases} \quad (1)$$

where S_k represents the switching state of the switching device of the circuit bridge arm. When $S_k = 1$, it means that the switch of the upper bridge arm of the K phase is on; when $S_k = 0$, it means that the switch of the upper bridge arm of the K phase is off.

In Equation (1), although the physical meaning of the mathematical model is clear, since the parameters in the model are all sinusoidal time-varying parameters, this makes the design of the controller very difficult. Therefore, through park transformation, the mathematical model shown in Equation (1) is transformed into the d-q rotation coordinate system, which rotates synchronously with the fundamental voltage wave of the power grid, so as to realize decoupling control.

The matrix form of the Park transform expression is as follows [21]:

$$C_{3s/2r} = \frac{2}{3} \begin{bmatrix} \cos \omega t & \cos(\omega t - 2/3\pi) & \cos(\omega t + 2/3\pi) \\ -\sin \omega t & -\sin(\omega t - 2/3\pi) & -\sin(\omega t + 2/3\pi) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}, \quad (2)$$

where ω is the synchronous rotational angular velocity.

From the park transformation matrix, Equation (1) can be transformed into a d-q rotating coordinate system, and the following equation can be obtained:

$$\begin{cases} \begin{bmatrix} e_{gd} \\ e_{gq} \end{bmatrix} = \begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} + R \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} + \omega L \begin{bmatrix} -i_{gq} \\ i_{gd} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}, \\ C \frac{dU_{dc}}{dt} = \frac{3}{2} \sum_{x=d,q} S_x i_{gx} - i_s \end{cases} \quad (3)$$

where e_{gd} and e_{gq} represent the power network voltage in the d-q axis coordinate system, i_{gd} and i_{gq} represent the power network-side current in the d-q axis coordinate system, u_{gd} and u_{gq} represent the power network converter output phase voltage in the d-q axis coordinate system, and S_x represents the switching function in the d-q axis coordinate system.

In the process of coordinate transformation, the composite vector E of the grid voltage is pointed to the d-axis, that is, voltage vector directional control is adopted. Therefore, we can get $e_{gd} = |E|$, $e_{gq} = 0$. Then, Equation (3) can be reduced to Equation (4):

$$\begin{cases} Ri_{gd} + L \frac{di_{gd}}{dt} = e_{gd} + \omega Li_{gq} - u_{gd} \\ Ri_{gq} + L \frac{di_{gq}}{dt} = -\omega Li_{gd} - u_{gq} \end{cases} \quad (4)$$

In the d-q coordinate system, the instantaneous active power P_g and instantaneous reactive power Q_g of the grid-side converter can be obtained:

$$\begin{cases} P_g = e_{gd}i_{gd} + e_{gq}i_{gq} = e_{gd}i_{gd} \\ Q_g = e_{gd}i_{gq} - e_{gq}i_{gd} = -e_{gd}i_{gq} \end{cases} \quad (5)$$

According to Equation (5), i_{gd} and i_{gq} correspond to P_g and Q_g of the grid-side converter, respectively, that is, P_g can be controlled by controlling i_{gd} , and Q_g can be controlled by controlling i_{gq} . According to Equation (4), the d-axis and q-axis power network current are influenced by the power network voltage e_{gd} , e_{gq} and the cross-coupling terms ωLi_{gq} , and ωLi_{gd} , which is not conducive to the independent control of the current. To this end, feedforward decoupling control is introduced, and the following mathematical model can be obtained:

$$\begin{cases} u_{gd} = \left(K_{pi} + \frac{K_{ii}}{s} \right) (i_{gd}^* - i_{gd}) + \omega Li_{gq} + e_{gd} \\ u_{gq} = \left(K_{pi} + \frac{K_{ii}}{s} \right) (i_{gq}^* - i_{gq}) - \omega Li_{gd} + e_{gq} \end{cases} \quad (6)$$

where K_{pi} is the proportionality coefficient and K_{ii} is the integration coefficient.

According to Equations (4) and (6), the following mathematical models can be obtained:

$$\begin{cases} Ri_{gd} + L \frac{di_{gd}}{dt} = \left(K_{pi} + \frac{K_{ii}}{s} \right) (i_{gd}^* - i_{gd}) \\ Ri_{gq} + L \frac{di_{gq}}{dt} = \left(K_{pi} + \frac{K_{ii}}{s} \right) (i_{gq}^* - i_{gq}) \end{cases} \quad (7)$$

From Equation (7), the d-q axis power network current has been independently controlled due to the introduction of current feedforward decoupling. At the same time, the power network voltage is introduced as feed-forward compensation, which improves the PMSG's ability to resist sudden changes of the power network voltage to a certain extent. Figure 3 shows the principle block diagram of the corresponding current decoupling control. The decoupling process is actually used to inject the components containing other axis information into the proportional integral (PI) output of each axis current, and then the injected components cancel out the coupling quantity generated by the controlled object [22].

Figure 3. Schematic diagram of current decoupling control.

Figure 4 shows the overall control block diagram of the grid-side converter. The system control adopts reactive current $i_{gq}^* = 0$ control, sampling the three-phase grid voltage e_{ga}, e_{gb}, e_{gc} for phase locked, obtaining the voltage phase and frequency signals as the phase and frequency of the grid-connected current. At the same time, the three-phase grid-connected current is sampled, and the d-q-axis power network current is obtained through d-q coordinate transformation. PI adjustment is made with the q-axis current reference value i_{gq}^* given in the program and d-axis current reference value i_{gd}^* output by LADRC. After decoupling and grid voltage feedforward control, the PI results are transformed into V_α and V_β by $dq/\alpha\beta$ transformation. The duty cycle signal is obtained through the SVPWM operation to drive the switch to realize the grid-connected operation control of the unit power factor.

Figure 4. Overall control block diagram of the grid-side converter.

3. Design of the LADRC Controller

LADRC comprises the following three sections [23,24]: Linear tracking differentiator (LTD), LESO, and linear state error feedback (LSEF). Its structure diagram is shown in Figure 5. LTD can effectively filter out the high-order harmonic interference in the signal and enhance the robustness of the system. In addition to the differential function, the linear tracking differentiator also has an important function,

which is to arrange the transition of the input signal and balance the contradiction between overshoot and rapidity. Because LTD can easily cause system vibration, this paper does not use LTD. LESO can expand the disturbance that affects the output of the system into a new state variable, and then use the input and output of the system to observe the disturbance state variable. LSEF can linearly combine the obtained generalized errors, and finally obtain a more efficient control quantity.

Figure 5. Structure diagram of LADRC.

3.1. Design of LADRC Based on RLESO

In order to design the LADRC controller, Equation (4) can be transformed into a differential equation as follows:

$$\frac{d^2 U_{dc}}{dt^2} = \frac{3}{2} \sum_{k=d,q} S_k \left(\frac{e_{gk}}{CL} - \frac{u_{gk}}{CL} \right) - \frac{3S_d R i_{gd}}{2CL} - \frac{3\omega S_q i_{gd}}{2C} - \frac{1}{C} \frac{di_s}{dt}. \quad (8)$$

Equation (8) is a second-order differential equation. Therefore, a second-order LADRC is designed. Let $b_0 = 3/(2LC)$, record the internal parameter uncertainty, time variable, and external disturbance in the system (8) as the total disturbance, and then the total disturbance is as follows:

$$f = \frac{3}{2} \sum_{k=d,q} S_k \left(\frac{e_{gk}}{CL} - \frac{u_{gk}}{CL} \right) - \frac{3\omega S_q i_{gd}}{2C} - \frac{1}{C} \frac{di_s}{dt} + \left(-\frac{3S_d R}{2LC} - \frac{3}{2LC} \right) i_{gd} + w. \quad (9)$$

Let $U_{dc} = y$, $i_{gd} = i_{gd}^*$, $u = i_{gd}^*$, then Equation (8) can be transformed into the following mathematical model:

$$\ddot{y} = f + b_0 u. \quad (10)$$

Let $x_1 = y$, $x_2 = \dot{y}$, $x_3 = f$, then Equation (10) can be transformed into the following state space description:

$$\begin{cases} \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ b_0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} u \\ f \end{bmatrix} \\ y = x_1 \end{cases} \quad (11)$$

Therefore, the third-order continuous LESO corresponding to Equation (11) can be obtained:

$$\begin{cases} \dot{z}_1 = z_2 - l_1(z_1 - y) \\ \dot{z}_2 = z_3 + b_0 u - l_2(z_1 - y) \\ \dot{z}_3 = -l_3(z_1 - y) \end{cases} \quad (12)$$

In Equation (12), z_1 , z_2 , and z_3 are the observed values of y , $\dot{y}$, and f respectively; and l_1 , l_2 , and l_3 are the observer gains. Since the DC link voltage (y) can be observed at any time, the corresponding structure can be deleted from Equation (12), and the difference between the differential of the DC link

voltage and the corresponding state estimated by the observer can be corrected as feedback. Thus, the reduced-order linear extended state observer (RLESO) is obtained:

$$\begin{cases} \dot{z}_1 = z_2 + b_0 u - l_1(z_1 - \dot{y}) \\ \dot{z}_2 = -l_2(z_1 - \dot{y}) \end{cases}, \quad (13)$$

where z_1 is the observation value for $\dot{y}$, and z_2 is the observation value for f . Selecting the appropriate observer gain, the observer will be able to track $\dot{y}$ and f in real time.

The disturbance compensation and LSEF of RLESO are designed as follows:

$$u = \frac{K_p(r - y) - K_d z_1 - z_2}{b_0}, \quad (14)$$

where K_p and K_d are the parameters of the controller and r is the given value of the LADRC input. At this time, if the observation error of z_2 to f is ignored, the system (10) can be simplified as an integral series structure. Therefore, the expected transfer function of the controlled object is as follows:

$$G(s) = \frac{Y(s)}{R(s)} = \frac{K_p}{s^2 + 2K_d s + K_p}. \quad (15)$$

According to the pole assignment method in [25], the following pole assignment can be done for Equations (13) and (15):

$$l_1 = 2\omega_o, l_2 = \omega_o^2, \quad (16)$$

$$K_p = \omega_c^2, K_d = 2\omega_c, \quad (17)$$

where ω_o and ω_c are the bandwidth of the observer and controller, respectively.

According to Equations (13) and (14), the structure block diagram of LADRC based on RLESO is shown in Figure 6.

Figure 6. Structure diagram of LADRC based on RLESO.

3.2. Design of the Improved LADRC Structure

In LADRC, the total disturbance observation ability of LESO is an important factor affecting the control quality of LADRC. The stronger the observation ability, the better the robustness and anti-interference ability of LADRC. This section analyzes and improves RLESO in terms of the disturbance observation capabilities.

3.2.1. Characteristic Analysis of RLES0

From Equations (13) and (16), the transfer functions of z_1 and z_2 in RLES0 are obtained as follows:

$$\begin{cases} z_1 = \frac{2\omega_0 s^2 + \omega_0^2 s}{(s + \omega_0)^2} y + \frac{b_0 s}{(s + \omega_0)^2} u \\ z_2 = \frac{\omega_0^2 s^2}{(s + \omega_0)^2} y - \frac{\omega_0^2 b_0}{(s + \omega_0)^2} u \end{cases} \quad (18)$$

By Laplace transformation of Equation (10), the total disturbance f can be written as:

$$f = s^2 y - b_0 u. \quad (19)$$

According to Equations (18) and (19), the transfer function of the disturbance observation of RLES0 is as follows:

$$G_1(s) = \frac{z_2}{f} = \frac{\omega_0^2}{(s + \omega_0)^2}. \quad (20)$$

Figure 7 shows the comparison of the traditional LES0 and RLES0 disturbance observation capabilities. Compared with traditional LES0, the bandwidth of RLES0 is increased, and the disturbance observation ability of LES0 is improved. At the same time, the phase lag of RLES0 is reduced. However, the attenuation degree of its high-frequency band is reduced, which makes LES0 vulnerable to high-frequency noise.

Figure 7. Comparison of the disturbance observation capabilities between traditional LES0 and RLES0.

3.2.2. Design of the Improved RLES0

Although RLES0 improves the disturbance observation ability of the observer to a certain extent and reduces the phase lag of disturbance observation, it also enhances the noise amplification phenomenon. For this reason, referring to the classical control theory, a lead lag correction is added to the total disturbance. Therefore, following equation is obtained:

$$z_3 = \frac{T_e s + 1}{\alpha T_e s + 1} z_2, \quad (21)$$

where z_3 is the output of the correction link, T_e is the time constant of the lead lag correction link, and α is the coefficient greater than zero.

According to Equations (13) and (21), the state space expressions of the improved RLSEO is as follows:

$$\begin{cases} \dot{z}_1 = z_2 + b_0 u - l_1(z_1 - \dot{y}) \\ \dot{z}_2 = -l_2(z_1 - \dot{y}) \\ \dot{z}_3 = -\frac{1}{\alpha} l_2(z_1 - \dot{y}) + \frac{1}{\alpha T_e}(z_2 - z_3) \end{cases} \quad (22)$$

From Equations (20) and (21), the transfer function of the disturbance observation of the optimized RLESO is obtained as follows:

$$G_2(s) = \frac{z_3}{f} = \frac{(T_e s + 1)\omega_o^2}{(\alpha T_e s + 1)(s + \omega_o)^2}. \quad (23)$$

Figure 8 compares the disturbance observation capabilities of the improved RLESO and conventional RLESO. It can be seen that after adding the correction link, the high-frequency gain of RLESO is reduced, and the phase lag is basically unchanged. The noise amplification effect of RLSEO has been alleviated to some extent.

Figure 8. Comparison of the disturbance observation capabilities between RLESO and the improved RLESO.

The disturbance compensation and LSEF of the improved RLESO are designed as follows:

$$u = \frac{K_p(r - y) - K_d z_1 - z_3}{b_0}. \quad (24)$$

From Equations (22) and (24), the structure block diagram of the improved LADRC is shown in Figure 9.

Figure 9. Structure block diagram of the improved LADRC.

4. Analysis of the Frequency Domain Characteristics of Improved LADRC

4.1. Analysis of the Convergence and Estimation Error of Improved RLESO

Let the tracking error be $e_1 = z_1 - \dot{y}$, $e_2 = z_3 - f$. According to Equations (18) and (21), the observation error of the DC link voltage differential and total disturbance are as follows:

$$e_1 = \frac{-s^3 y + b_0 s u}{(s + \omega_o)^2}, \quad (25)$$

$$e_2 = \frac{(-s^3 y + b_0 s u)(\alpha T_e s^2 + (2\alpha T_e \omega_o + 1)s + \alpha T_e \omega_o^2 - T_e \omega_o^2 + 2\omega_o)}{(\alpha T_e s + 1)(s + \omega_o)^2}. \quad (26)$$

Let the output value y and the control quantity u both take the step signal of the amplitude K , then their Laplace transform formulas are $Y(s) = K/s$ and $U(s) = K/s$, respectively. Therefore, the steady-state errors of the DC link voltage differential and total disturbance are as follows:

$$\begin{cases} e_{1s} = \lim_{s \rightarrow 0} s e_1 = 0 \\ e_{2s} = \lim_{s \rightarrow 0} s e_2 = 0 \end{cases}. \quad (27)$$

The upper formula shows that under the condition of steady state, the improved RLESO can accurately track the actual value of the system and has good convergence.

4.2. Analysis of Anti-Interference Ability of Improved LADRC

According to Equations (18), (21), and (24), the transfer function of the control variable u is as follows:

$$u = \frac{N(s)}{G_3(s)b_0} \left(\omega_c^2 r - \frac{H(s)}{N(s)} y \right), \quad (28)$$

where:

$$\begin{aligned} N(s) &= (\alpha T_e s + 1)(s + \omega_o)^2 \\ G_3(s) &= \alpha T_e s^3 + (2\alpha T_e \omega_o + 2\alpha T_e \omega_c + 1)s^2 + (2\omega_o + 2\omega_c - T_e \omega_o^2 + \alpha T_e \omega_o^2)s \\ H(s) &= (T_e \omega_o^2 + 4\alpha T_e \omega_o \omega_c + \alpha T_e \omega_c^2)s^3 + (2\alpha T_e \omega_o^2 \omega_c + 2\alpha T_e \omega_o \omega_c^2 + \omega_o^2 + \omega_c^2 + 4\omega_o \omega_c)s^2 + \\ &\quad (\alpha T_e \omega_o^2 \omega_c^2 + 2\omega_o^2 \omega_c + 2\omega_o \omega_c^2)s + \omega_o^2 \omega_c^2 \end{aligned}$$

According to Equations (10) and (28), the simplified structure diagram of the improved LADRC is designed as follows:

From Figure 10, the closed-loop transfer function of the system is as follows:

$$y = \frac{N(s)\omega_c^2}{G_3(s)s^2+H(s)}r + \frac{G_3(s)}{G_3(s)s^2+H(s)}f = \frac{\omega_c^2}{s^2+2\omega_c s+\omega_c^2}r + \frac{G_3(s)}{G_3(s)s^2+H(s)}f \quad (29)$$

Figure 10. Simplified structure diagram of the improved LADRC.

If the total disturbance f can be fully estimated, the output of the power network-side converter is only related to the controller bandwidth ω_c . By adjusting ω_c , the system can track the given value r quickly and without overshoot.

Figure 11 shows the frequency domain characteristic curve of the disturbance term. Compared with LADRC based on RLES0, the gain of the system in the middle and low frequencies is reduced after adding the correction link, and the anti-disturbance performance of the improved LADRC in the middle- and low-frequency band is enhanced. At the same time, with the increase of T_e , the anti-interference performance of the system is gradually enhanced, and the degree of phase lag is gradually reduced.

Figure 11. Frequency domain characteristics of the disturbance term of the improved LADRC.

4.3. Analysis of the Anti-Disturbance Capability of the Improved LADRC in the PMSG System

The stability of the DC link voltage in PMSG is mainly affected by power network voltage mutation and load current disturbance [26]. In this article, the anti-interference ability of the DC link voltage to the load current is compared between the conventional LADRC and improved LADRC. Figure 12 is

the structure diagram of the power network-side converter controlled by LADRC. Thus, the transfer function of the DC link voltage of PMSG is as follows:

$$U_{dc} = \frac{K_c \omega_c^2 G_i N}{b_0 C G_i s + K_c G_i H} U_{dc}^* - \frac{G_3 b_0}{b_0 C G_i s + K_c G_i H} i_s \quad (30)$$

Figure 12. Equivalent control block diagram of the grid-side converter.

In Equation (30), $G_i(s)$ is the equivalent transfer function of the current inner loop, and K_c is the conversion link coefficient. It can be known from [27] that when the current inner loop adopts PI control, its equivalent transfer function $G_i(s) = 1/(3T + 1)$, where T is the time constant of the equivalent transfer function of the inner ring.

Figure 13 shows the comparison of the frequency domain characteristic curves of the improved LADRC and traditional LADRC. The anti-disturbance ability of the improved LADRC is better than that of the conventional LADRC in the middle- and low-frequency band; the two curves in the high-frequency band are roughly coincident, so the improved LADRC will not affect the high-frequency gain.

Figure 13. Frequency domain characteristics of improved LADRC and traditional LADRC.

4.4. Stability Analysis of the DC Bus Voltage of the Improved LADRC

From Equation (30), the closed-loop transfer function from the given value U_{dc}^* of the DC bus voltage to DC bus voltage U_{dc} can be simplified as follows:

$$U_{dc} = \frac{K_c \omega_c^2 (\alpha T_e s + 1) (s + \omega_o)^2}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} U_{dc}^*, \quad (31)$$

where:

$$\begin{aligned}
 a_5 &= 3C\alpha TT_e b_0 \\
 a_4 &= 3CTb_0 + C\alpha T_e b_0 + 6C\alpha TT_e(\omega_o + \omega_c)b_0 \\
 a_3 &= Cb_0 + K_c T_e \omega_o^2 + 6CT\omega_o b_0 + 6CT\omega_c b_0 + K_c \alpha T_e \omega_c^2 - 3CTT_e \omega_o^2 b_0 + 2C\alpha T_e \omega_o b_0 + \\
 &\quad 2C\alpha T_e \omega_c b_0 + 4K_c \alpha T_e \omega_o \omega_c + 3C\alpha TT_e \omega_o^2 b_0 \\
 a_2 &= K_c \omega_o^2 + K_c \omega_c^2 + 2C\omega_o b_0 + 2C\omega_c b_0 + 4K_c \omega_o \omega_c - CT_e \omega_o^2 b_0 + C\alpha T_e \omega_o^2 b_0 + \\
 &\quad 2K_c \alpha T_e \omega_o \omega_c^2 + 2K_c \alpha T_e \omega_o^2 \omega_c \\
 a_1 &= K_c \alpha T_e \omega_o^2 \omega_c^2 + 2K_c \omega_o \omega_c^2 + 2K_c \omega_o^2 \omega_c \\
 a_0 &= K_c \omega_o^2 \omega_c^2.
 \end{aligned}$$

Because ω_o , ω_c , T_e , T , K_c , b_0 , and α are all positive numbers, $a_i > 0$, $i = 0, 1, 2, 3, 4, 5$. Based on the Linard–Chipat stability criterion, the following algebraic relations can be obtained:

$$\begin{cases} \Delta_3 > 0 \\ \Delta_5 > 0 \end{cases}, \quad (32)$$

where:

$$\Delta_5 = \begin{vmatrix} a_1 & a_0 & 0 & 0 & 0 \\ a_3 & a_2 & a_1 & a_0 & 0 \\ a_5 & a_4 & a_3 & a_2 & a_1 \\ 0 & 0 & a_5 & a_4 & a_3 \\ 0 & 0 & 0 & 0 & a_5 \end{vmatrix}, \Delta_3 = \begin{vmatrix} a_1 & a_0 & 0 \\ a_3 & a_2 & a_1 \\ a_5 & a_4 & a_3 \end{vmatrix}.$$

Equation (32) represents a stable system. Through numerical simulation of Equation (32), it can be found that when the system controller gain b_0 is determined, when ω_o and ω_c are changed in a wide range, the stability of the DC link voltage of PMSG is not affected. In addition, under the condition that the system controller gain b_0 is uncertain, by reasonably configuring ω_o , ω_c , and b_0 , the bus voltage can still have a good stability margin.

5. Simulation Analysis

In order to verify the correctness of the above-mentioned improved LADRC theoretical analysis, a 1.5 MW PMSG model was built based on MATLAB simulation software. The voltage outer loop is an improved LADRC, and the current inner loop is a traditional PI regulation. The specific parameters of PMSG are shown in Table A1.

5.1. Parameter Tuning of Controller

The performance of the LADRC controller has a great relationship with the selection of parameters. If the parameters are not selected properly, the performance of the LADRC controller will be reduced, and then the control effect of the DC bus voltage will be affected. In order to achieve the best performance of LADRC, through a lot of simulation experience, the following parameter tuning rules are summarized as follows:

1. According to $b_0 = 3/(2LC)$, the control gain $b_0 = 52,083$ can be obtained.
2. The multiple relationship between the LESO bandwidth ω_o and the controller bandwidth ω_c is determined: $\omega_o = 1 \sim 3\omega_c$.
3. When a set of ω_o and ω_c is obtained, $l_1 \sim l_3$, K_p , and K_d are calculated according to the pole assignment equation of Equations (16) and (17).
4. Increase ω_o and ω_c proportionally until the noise cannot bear to cause the system output fluctuation or oscillation, and then appropriately reduce the value of ω_o and ω_c to take into account the dynamic performance and stability of the controlled object. Further, if necessary, independently

fine tune ω_o and ω_c until the dynamic response and anti-interference ability of the system meet the requirements.

5. Reduce l_1 and l_2 and increase l_3 appropriately until the dynamic characteristics of the controlled object can achieve the desired dynamic performance without overshoot. Record a set of parameters set at the current b_0 value. Adjust K_p and K_d according to the need to obtain a better dynamic performance.
6. Adjust b_0 appropriately, and then adjust it again according to the above steps, and get a set of optimal parameters by comparison

Through the above parameter tuning method, the parameters of the controller shown in Table A2 were obtained.

5.2. Comparative Simulation Analysis of the Anti-Disturbance Capability

In order to analyze the immunity ability of the DC link voltage under the improved LADRC strategy and the conventional LADRC strategy, the following four low-voltage rides through (LVRT) faults were established based on MATLAB simulation software:

- (i) The voltage of the power network has a symmetrical low-voltage ride through fault, and the drop amplitude is 0.3 p.u. and the duration is 0.3 s;
- (ii) The voltage of the power network has a symmetrical low-voltage ride through fault, and the drop amplitude is 0.6 p.u. and the duration is 0.3 s;
- (iii) The voltage of the power network has an asymmetric low-voltage ride through fault, and the drop amplitude is 0.3 p.u. and the duration is 0.3 s;
- (iv) The voltage of the power network has an asymmetrical low-voltage ride through fault, and the drop amplitude is 0.6 p.u. and the duration is 0.3 s.

Scenario 1

Figure 14 shows the power network voltage waveform and DC link voltage waveform when the power network voltage drops by 0.3 p.u. symmetrically. When it is set at 0.7 s, the power network voltage will fall symmetrically and return to normal after 0.3 s. At the moment of fault, the overshoot of DC link voltage controlled by conventional LADRC is about 0.01 p.u., and that of the improved LADRC is close to 0.006 p.u.; at the moment of fault recovery, the drop amplitude of DC link voltage controlled by the conventional LADRC is about 0.012 p.u., and that of the improved LADRC is close to 0.007 p.u.

Figure 14. Power network voltage waveform and DC link voltage waveform when the power network voltage drops by 0.3 p.u. symmetrically: (a) Waveform of the power network voltage; (b) Waveform of the DC link voltage.

Scenario 2

Figure 15 shows the power network voltage waveform and DC link voltage waveform when the power network voltage drops by 0.6 p.u. symmetrically. When it is set at 0.7 s, the grid voltage will fall symmetrically and return to normal after 0.3 s. At the moment of fault, the overshoot of the DC link voltage controlled by the conventional LADRC is about 0.03 p.u., and that of the improved LADRC is close to 0.015 p.u.; at the moment of fault recovery, the drop amplitude of the DC link voltage controlled by the conventional LADRC is about 0.03 p.u., and that of the improved LADRC is close to 0.017 p.u.

Figure 15. Power network voltage waveform and DC link voltage waveform when the power network voltage drops by 0.6 p.u. symmetrically: (a) Waveform of the power network voltage; (b) Waveform of the DC link voltage.

Scenario 3

Figure 16 shows the waveform of the power network voltage and DC link voltage when the power network voltage drops by 0.3 p.u. asymmetrically. When it is set at 0.7 s, the grid voltage asymmetrical drop fault occurs, and it returns to normal after 0.3 s. At the moment of fault, the overshoot of the DC link voltage controlled by the conventional LADRC is about 0.0061 p.u., and that of the improved LADRC is close to 0.0057 p.u.; during the fault period, the DC link voltage fluctuation range of the conventional LADRC control is about 0.9955~1.0049 p.u., and the DC link voltage fluctuation range of the improved LADRC control is close to 0.9965~1.0038 p.u.; at the moment of fault recovery, the DC bus voltage overshoot of the conventional LADRC control is about 0.0073 p.u., and that of the improved LADRC is close to 0.0065 p.u.

Figure 16. Power network voltage waveform and DC link voltage waveform when the power network voltage drops by 0.3 p.u. asymmetrically: (a) Waveform of the power network voltage; (b) Waveform of the DC link voltage.

Scenario 4

Figure 17 shows the waveform of the power network voltage and DC link voltage when the power network voltage drops by 0.6 p.u. asymmetrically. When it is set at 0.7 s, the grid voltage asymmetrical drop fault occurs, and it returns to normal after 0.3 s. At the moment of fault, the overshoot of the DC link voltage under conventional LADRC control and improved LADRC control is close to 0.011 p.u.; during the fault period, the fluctuation range of the DC link voltage controlled by the conventional LADRC is about 0.99~1.0099 p.u., and that of the improved LADRC is close to 0.9932~1.0078 p.u.; at the moment of fault recovery, the overshoot amplitude of the DC link voltage controlled by the conventional LADRC is about 0.0245 p.u., and that of the improved LADRC is close to 0.0194 p.u.

Figure 17. Power network voltage waveform and DC link voltage waveform when the power network voltage drops by 0.6 p.u. asymmetrically: (a) Waveform of the power network voltage; (b) Waveform of the DC link voltage.

The simulation results show that compared with the traditional LADRC, the improved LADRC has a better control effect on the DC link voltage in the case of the low-voltage ride through fault; that is, the improved LADRC can greatly enhance the anti-disturbance performance of PMSG.

6. Conclusions

The stability of DC bus voltage is key to safe and efficient operation of the PMSG system. In order to suppress the wide range of fluctuation of the DC bus voltage under disturbance, an LADRC based on an improved RLESO was proposed. The main contributions of this paper are as follows:

- (i) In order to reduce the phase lag and enhance the disturbance observation performance of the observer, an RLESO with a bus voltage differential and its observation error as feedback was designed. By introducing a lead lag correction in the total disturbance channel, the noise amplification phenomenon of the observer was enhanced, and the anti-disturbance performance of the improved LADRC was improved.
- (ii) The improved LADRC was applied to the voltage outer loop control of the power network-side converter of PMSG, which improved the stability of the DC bus voltage.
- (iii) The simulation results showed that under the condition of power network voltage symmetrical low-voltage ride through fault and asymmetrical low-voltage ride through fault, the control performance of the improved LADRC to DC bus voltage is better than that of the traditional LADRC.

The control strategy mentioned in this paper has proved its feasibility and effectiveness mainly through theoretical analysis and digital simulation, but it has not yet been applied to actual physical systems. Thus, our future research focus will be to verify the feasibility of the proposed control strategy through physical experiments.

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Abbreviations

Acronym	Definition
PMSG	Permanent magnet synchronous generator
DC	Direct current
AC	Alternating current
PI	Proportional integral
PID	Proportional integral differential
LADRC	Liner active disturbance rejection control
LESO	Linear extended state observer
LSEF	Linear state error feedback
SVPWM	Space Vector Pulse Width Modulation
PWM	Pulse width modulation
LVRT	Low voltage ride through

Appendix A

Table A1. Main parameters of PMSG.

Symbol	Description	Value
P_b	Base power	1.5 MW
V_b	Base voltage	690 V
f_b	Base frequency	50 Hz
U_{dc}	DC link voltage	1070 V
C	DC link capacitor	240 μ F
R	power network side equivalent resistance	0.942 Ω
L	power network side filter inductance	0.12 mH
T_e	Correction link time constant	0.004 s
α	Correction factor	0.2
T	Inner ring equivalent time constant	0.0025 s
K_c	Conversion link coefficient	0.85

Table A2. Controller parameters.

Symbol	Description	Value
ω_c	Controller bandwidth	500
ω_o	Observer bandwidth	2300
K_{pi}	Inner loop proportionality coefficient	0.9
K_{ii}	Inner loop integration coefficient	12

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