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A Selective Fault Clearing Scheme for a Hybrid VSC-LCC Multi-Terminal HVdc System

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Abstract: A selective fault clearing scheme is proposed for a hybrid voltage source converter (VSC)-line commutated converter (LCC) multi-terminal high voltage direct current (HVdc) transmission structure in which two small capacity VSC stations tap into the main transmission line of a high capacity LCC-HVdc link. The use of dc circuit breakers (dc CBs) on the branches connecting to VSCs at the tapping points is explored to minimize the impact of tapping on the reliability of the main LCC link. This arrangement allows clearing of temporary faults on the main LCC line as usual by force retardation of the LCC rectifier. The faults on the branches connecting to VSC stations can be cleared by blocking insulated gate bipolar transistors (IGBTs) and opening ac circuit breakers (ac CB), without affecting the main line's performance. A local voltage and current measurement based fault discrimination scheme is developed to identify the faulted sections and pole(s), and trigger appropriate fault recovery functions. This fault discrimination scheme is capable of detecting and discriminating short circuits and high resistances faults in any branch well before 2 ms. For the test grid considered, 6 kA, 2 ms dc CBs can easily facilitate the intended fault clearing functions and maintain the power transfer through healthy pole during single-pole faults.

Keywords: LCC-VSC hybrid HVdc transmission systems; hybrid multi-terminal HVdc grids; HVdc dc side fault recovery; dc fault detection and discrimination in HVdc grids

1. Introduction

In many cases, HVdc transmission lines are built with some spare capacity for future expansion or to meet other design requirements [1]. This situation exists on the present-day Bipoles I and II of Manitoba Hydro's HVdc transmission system. The potential renewable energy resources and new load centres can be integrated to the electricity grid with less cost using the spare capacity of the existing HVdc lines. However, high-power interfacing electronics are required for tapping into HVdc transmission lines. At present, the majority of existing bulk power HVdc transmission lines use line commutated converter (LCC) technology due to superior economics and proven technological performances [2]. On the other hand, the voltage source converter (VSC) offers a practical approach for tapping. VSCs also offer the ability to change the direction of power flow for meeting the instantaneous power balancing requirements [3]. The black start capability [4] and the ability to connect to weak ac systems [5] are very useful when integrating remote or isolated renewable power generation systems [6].

The two converter technologies can be combined in many different ways. A VSC can be combined in series with an LCC at each converter station as proposed in [7–9]. Different ways of implementing hybrid LCC-VSC two-terminal or multi-terminal HVdc (MT-HVdc) systems, where the individual

converter stations are based on different technologies, can be found in [10–20]. Two main classes of hybrid MT-HVdc systems are:

- A number of VSC rectifier stations, typically connected to offshore wind farms, linked to a large onshore LCC inverter station supplying one or more major load centres [10–12],
- One large LCC rectifier, typically connected to a large hydropower station, linked to a number of small VSC inverters supplying urban load stations [13–17].

In the first configuration, the advantages of VSC stations such as small footprint, ability to connect to a weak ac system are exploited in the offshore rectifiers, and the economy of LCC station in building large converter station is exploited in the onshore inverter. In the second configuration, the economy of LCC station is exploited in building a large rectifier station connected to a strong system and the advantage of the small footprint of VSC stations is exploited in building the converters supplying urban load centres. A real-world example for the second type is the Woudong hybrid three-terminal grid, which comprises an 8 GW LCC rectifier and two VSC inverters rated 5 GW and 3 GW [14]. This scheme is under construction and will be commissioned in the year 2022 [21]. In contrast, this paper considers tapping into an existing LCC link using VSC converters as described in [17–20].

Modern VSC stations are built using modular multilevel converter (MMC) technology using half-bridge sub-modules (HB-SM) or full-bridge sub-modules (FB-SM) [22]. Although the FB-SM option is more flexible and has the inherent DC fault current blocking capability, it is relatively expensive and currently not widely applied in practical systems. In contrast, HB-SM MMCs are more common and have been used in VSC based multi-terminal HVdc systems [23,24].

A fault clearing scheme for hybrid LCC-VSC MT-HVdc with HB-SM MMCs is proposed in [1]. The configuration proposed in [1] is depicted in Figure 1, and the method relies on ac CBs to interrupt fault currents from the VSC rectifier and employs a diode valve in series with the VSC inverters to block dc fault currents.

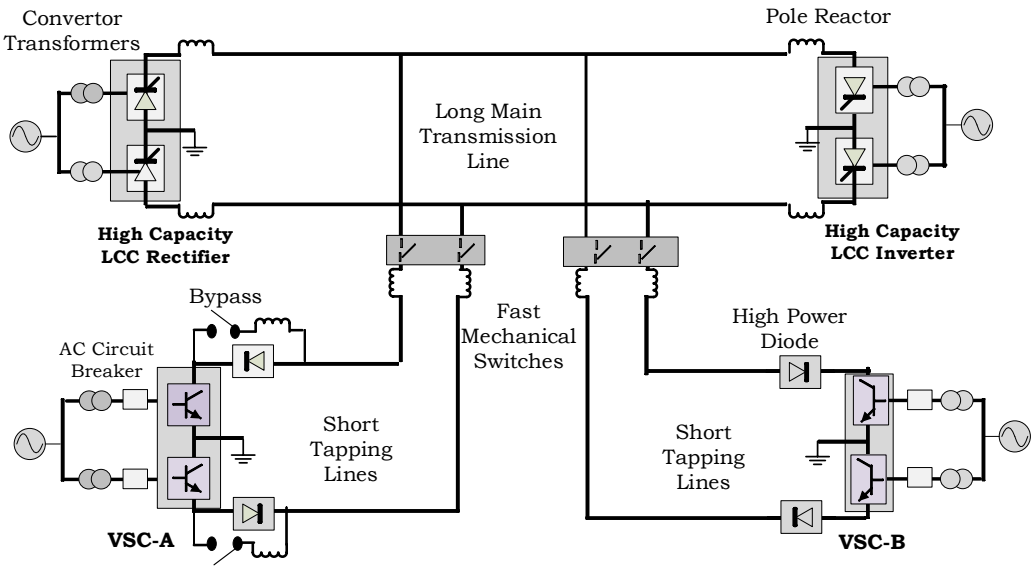


Figure 1. Proposed protection design for hybrid VSC-LCC system in [1].

VSC-A is assumed to be operated either as a rectifier or inverter. In contrast, VSC-B is assumed to be operated only in the inverter mode. To facilitate feeding power from VSC-A during rectifier operation, the diodes connected to VSC-A should be bypassed. Additionally, a series reactor is inserted for limiting the rate of rise of current injected by VSC-A during dc faults. A dc fault is cleared using the following sequence:

1. De-energize all VSC rectifiers by opening their ac CBs to avoid fault current injection from the ac side,

2. Apply force retardation at the LCC rectifier,
3. Open the fast mechanical switches when the current through them are sufficiently small.

Although this method works and can be implemented with the existing technologies, one of its drawbacks is the prolong time to extinguish arcing faults due to the long time taken to dissipate the stored energy in the VSC inductive elements and the transmission line, even after blocking the IGBTs. This is in contrast to LCC HVdc systems, which can quickly reduce dc fault currents by applying forced retardation procedure. Besides that, the series-connected high-power diode valve can be subjected up to 2 pu reverse voltage during the fault transients. Therefore, when a hybrid multi-terminal HVdc transmission system is created by connecting VSC based taps on an existing LCC HVdc link, and if the VSC rectifiers rely on ac side CBs to interrupt dc side fault currents [1], then the dc side fault clearing time increases in comparison to that of the original LCC HVdc link. The fault clearing performance and the reliability of the hybrid VSC-LCC MT-HVdc system proposed in [1] can be improved if high voltage dc circuit breakers (dc CBs) are employed for fast, selective fault isolation. Temporary faults due to flashover are very common in long open conductor overhead transmission lines used in HVdc transmission and therefore fast temporary fault recovery performance is essential [25]. Recent developments in high voltage dc CB technology include full-scale prototypes and field installations [24,26]. Technically viable commercial dc CB solutions are expected to emerge in the near future. An enhanced protection scheme having higher selectivity and higher security is developed in this paper to use in conjunction with strategically placed dc CBs.

Although selective fault clearing in purely VSC based MT-HVdc systems has been an active research area in recent years [27–29], the technology is not well established, especially for hybrid LCC-VSC MT-HVdc transmission systems that comprise of multiples zones, and gaps exist in the understanding. In contrast to the dc fault clearing approach proposed in [1], a selective fault clearing scheme needs a fault detection and discrimination scheme suitable for hybrid LCC-VSC multi-terminal systems having multiple protection zones.

In [30], a traveling wave-based fault location scheme is proposed for two-terminal HVdc links, and this concept is extended and applied for the protection of hybrid VSC-LCC HVdc systems in [31–35]. Most of the fault discrimination schemes presented for hybrid LCC-VSC HVdc transmission systems are proposed or evaluated for two-terminal HVdc systems [31–35], which typically have a single line protection zone. The traveling-wave protection (TWP) is reportedly considered for Wudongde three-terminal hybrid HVdc project for line protection [33]. A fault discrimination method is proposed in [36] for a hybrid LCC-VSC based MT- HVdc transmission system comprising of multiple zones. The method proposed in [36] uses the ratio of two voltage components at two different frequencies extracted from the fault transient as the fault indicator and claims to be capable of discriminating faults of up to 400 Ω fault resistance in a MT- HVdc system comprising of an LCC rectifier connected to two-VSC inverters. However, in [36] a fault clearing procedure is not discussed and the adequacy of the proposed scheme for successful fault clearing is not fully demonstrated.

Furthermore, without having a complete protection scheme that discriminates the faults in different zones, and a fault recovery scheme that invokes appropriate actions depending on the faulted zone and fault type, the potential fault recovery performances cannot be evaluated. The fault discrimination scheme should be capable of discriminating faults at each zone, up-to a fair value of fault resistance expected in a typical hybrid LCC-VSC based multi-terminal system. In addition, the fault discrimination method should be able to make decisions within a very short duration as dictated by the dc CB limitations. This is because a dc CB has to interrupt the rapidly rising fault currents before they exceed the maximum breakable current. The fault current injected through a VSC branch could reach its peak value within a few milliseconds. The fault discrimination speed of the scheme presented in [36], which needs 5 ms time window, may not be adequate with respect to the typical dc CB performance cited in the literature [24,26].

In contrast to the previously mentioned literature, this paper addresses the fault discrimination, fault clearing, and the post-fault recovery performance in a class of hybrid LCC-VSC MT-HVdc schemes

in a holistic manner. The configuration of the hybrid LCC-VSC MT-HVdc scheme considered is similar to the one shown in Figure 1 and the main contributions of the paper include (i) development of a complete protection scheme based on the local voltage and current measurements to identify the faulted segment and the conductors involved in the fault within a short time interval after a dc side fault, (ii) demonstration of the suitability of the fault discrimination scheme in terms of the capability of discriminating faults at the boundary of each zone for up to about 50 Ω of fault resistance with a speed that is adequate for meeting the breaking capability of the dc CB prototype presented in [26], (iii) development of a detailed fault recovery procedure that minimizes the extent of outages, and (iv) simulation-based analysis of the proposed algorithms under a variety of possible fault scenarios.

2. Proposed Protection Scheme

2.1. Key Components and Grid Layout

Figure 2 shows the considered hybrid LCC-VSC MT-HVdc grid layout and the essential elements of the proposed protection scheme.

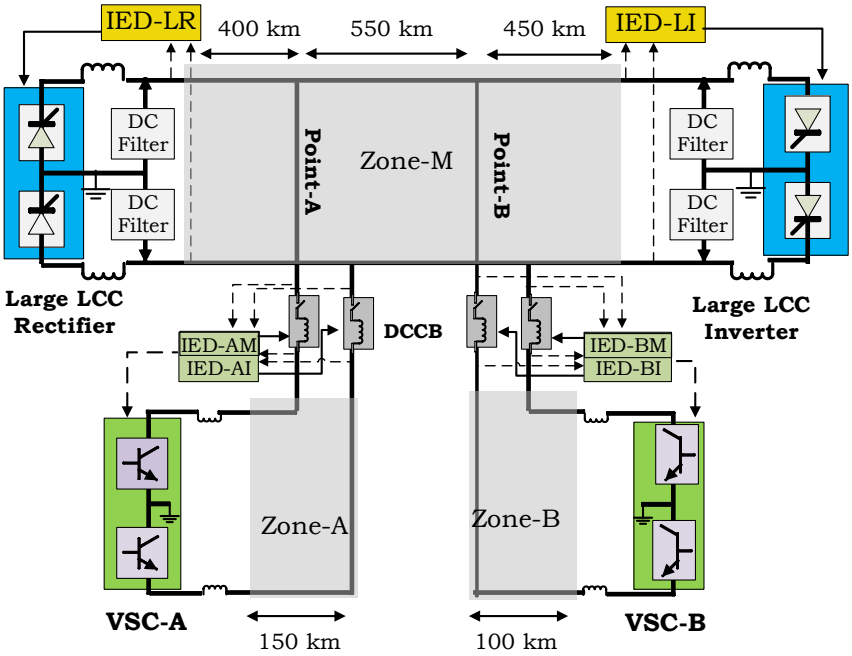


Figure 2. Hybrid VSC-LCC transmission system with two VSCs connected to an LCC-HVdc link.

Two VSC stations with a lower rating compared to the LCC stations are connected through two transmission lines, which are hereafter referred to as VSC branches, to a 1400 km long main transmission link. A bipole HVdc transmissions system without a dedicated metallic return wire similar to Manitoba Bipole-I and -II [37] is considered in this study. It is assumed that earth return mode is allowed for a short period for single-pole fault recovery. The VSC stations are based on more economical HB-SM technology.

A key requirement is to ensure that the reliability of the original LCC line is not degraded due to tapping. In order to minimize the fault clearing and recovery time for temporary dc faults, all HB-SM based MMCs on the affected pole(s) must be immediately disconnected from the dc network. Additionally, during all permanent faults on the VSC branches, the faulted line segment must be disconnected before the stability of the LCC link is affected. This is only possible by using dc CBs for selective fault isolation. In order to maximize the fault recovery performance with a minimum number of dc CBs (which are high-cost items), it is proposed to place a dc CB at each tapping point on the VSC branches. In this configuration, dc CBs perform two main roles:

1. For both temporary and permanent faults on VSC branches, they avoid the impact on the LCC link by promptly disconnecting faulty conductor(s) from the main LCC link.
2. For temporary faults on the main LCC link, they avoid the need for a complete shutdown and restarting of VSC stations by promptly disconnecting faulty conductor(s) from the VSCs. The VSCs that are connected to faulty pole(s) could be switched to static synchronous compensator (STATCOM) mode (i.e., no real power transfer) until the fault on the main transmission line is cleared.

It is necessary to have dc CBs on both poles to perform the above roles. With this arrangement, a VSC station is completely de-energized for faults on the line segment connecting it to the main LCC link. De-energization of a VSC during temporary faults can be avoided by providing additional dc CBs at the VSC terminals, but this is an expensive solution with only a marginal contribution to improve the reliability or safety of the system:

1. Because there is no alternative path for power transfer during a VSC branch fault in the considered layout, isolation of the faulty conductor to preserve the continuity of VSC operation does not offer any significant advantage.
2. Each VSC has its own low-level protection such as IGBT blocking upon fault detection and freewheeling diode protection by firing parallel thyristors [25].

The fault clearing process is initiated with the help of fault discrimination information provided by intelligent electronic devices (IEDs) installed on appropriate places as indicated in Figure 2. The forced retarding fault current blocking mechanism utilized on the LCC terminals is used for the proposed scheme as well. Based on the above reasoning, the dc CB placement shown in Figure 2 is considered as the arrangement that needs the least number of dc CBs for the proposed hybrid VSC-LCC multi-terminal HVdc topology, and it divides the dc network into three protection zones.

In this scheme, it is necessary to discriminate the faults on the main transmission line (Zone-M) from those on the branches connecting VSC-A (Zone-A), and VSC-B (Zone-B); and identify the pole(s) involved in the fault. An intelligent electronics device (IED) capable of the above tasks can be implemented at each tapping point as indicated on Figure 2 with the help of series di/dt limiting inductors, which are an integral part of dc CBs [26–28]. The protection IED-A at the tapping point-A comprises two functional units: one denoted as IED-AM to detect faults on the main transmission line, and the other denoted as IED-AI to detect faults on the line connecting the VSC. A similar protection IED is employed at the tapping point B as well.

The coordination of converter stations in this multi-terminal transmission system is important for stable normal operation and fault recovery. The centralized master power controller (MPC), proposed in [1] is considered in this study. Grid energization and co-ordination is carried as described in [6], in which the LCC inverter is operated in the constant extinction angle control mode, while VSC stations are operated in the constant power control mode during normal operation. The LCC rectifier is operated in the constant current control mode. The primary function of the MPC is to calculate the current order for the LCC rectifier to fulfil power demand at the LCC inverter while considering the instantaneous current injections from each VSC station. For example, the current order of the positive pole (P-pole) is calculated using Equation (1).

$$I_{O\_P} = S_{LIP}\left[\frac{K_{LI}\cdot P_{ref_{LIP}}}{V_{DCLIP} - V_{DCLIN}} + \frac{S_{VAP}\cdot K_{VA}\cdot P_{ref_{VAP}}}{V_{DCVAP} - V_{DCVAN}} + \frac{S_{VBP}\cdot K_{VB}\cdot P_{ref\_VBP}}{V_{DCVBP} - V_{DCVBN}}\right] \quad (1)$$

where P_{ref_LIP}, P_{ref_VAP}, P_{ref_VBP} are power reference values, and K_{LI}, K_{VA}, K_{VB} are power ramping rates of the LCC inverter, VSC-A, and VSC-B respectively. The binary signals S_{LIP}, S_{VAP}, and S_{VBP} are generated by a fault recovery supervisory function to reset the respective current component to zero after detecting a fault on P-pole conductor connected to the LCC inverter, VSC-A, and VSC-B respectively. V_{DCLIP}, V_{DCLIN}, V_{DCVAP}, V_{DCVAN}, V_{DCVAP}, and V_{DCVBN} are conditioned pole voltage measurements taken through the signal pre-processing arrangement shown in Figure 3.

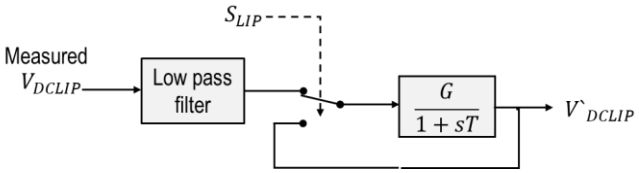


Figure 3. Dc voltage measurement conditioning (illustrated for LCC inverter P-pole).

This signal pre-processing arrangement includes a hold circuit which holds the pre-fault voltage measurement during the fault recovery period and a first-order filter with 200 ms time constant to avoid erratic current orders due to low dc voltages that may occur during faults. According to Equation (1), the current order is set to zero during a fault on Zone-M, by setting $S_{LIP} = 0$. During a fault on a VSC branch, the respective term is set to zero via S_{VAP} and S_{VBP}. During a single-pole fault, the healthy pole current order is frozen at the pre-fault value until the recovery. The current order for N-pole is calculated independently in the same manner.

2.2. DC Side Fault Clearing Strategy

The proposed dc fault clearing procedure is shown in Figure 4.

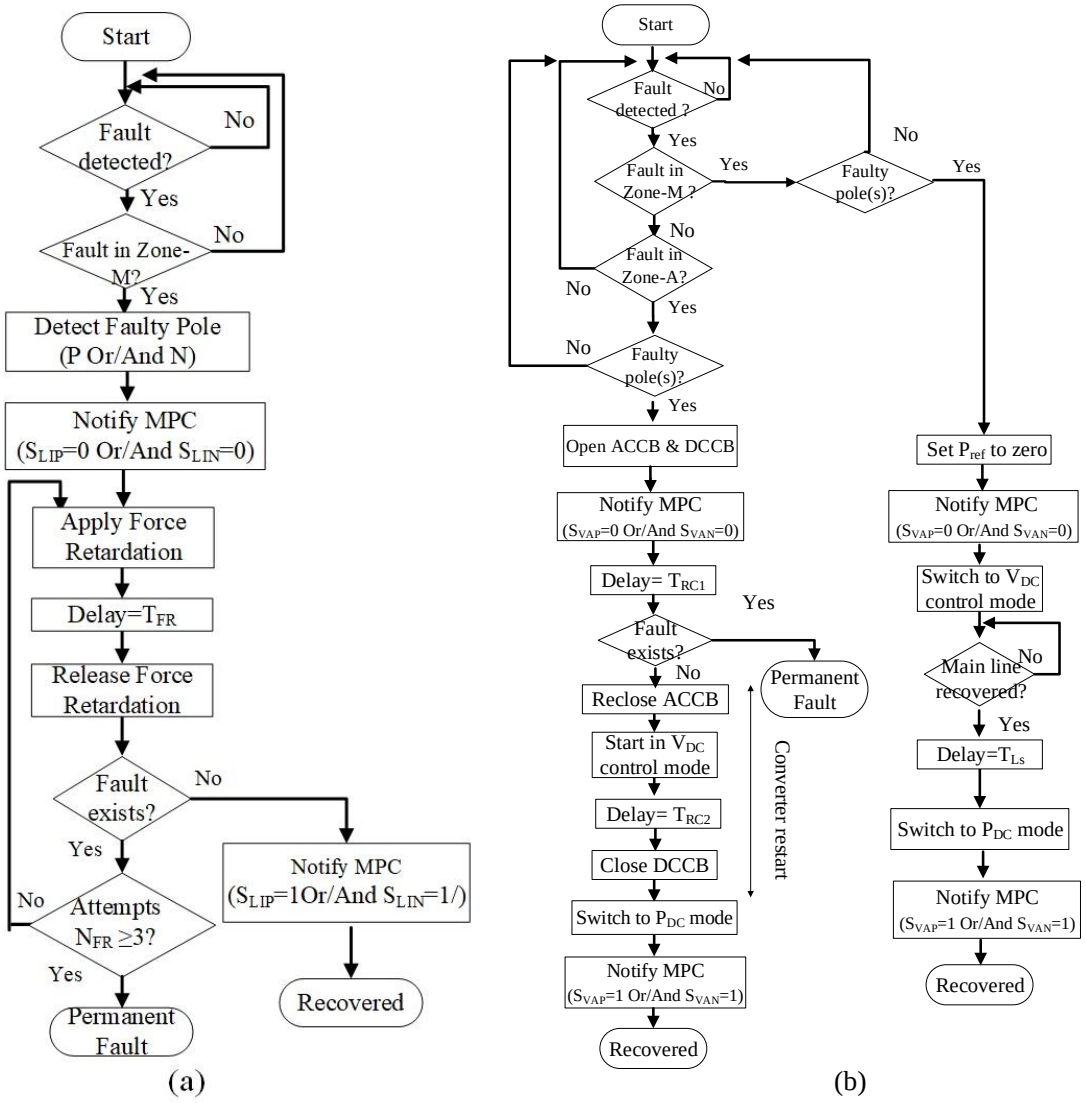


Figure 4. The fault recovery process, (**a**) at LCC rectifier station, (**b**) at VSC-A station (the same procedure is used at VSC-B station).

In order to preserve the operation of the healthy pole during single-pole-to-ground faults, the fault recovery process is applied independently for positive and negative poles. As depicted in Figure 4a, upon detecting a fault in Zone-M, force retardation is applied to the respective pole(s) of the LCC rectifier. For example, if only P-pole is involved in the fault, S_{LIP} in Equation (1) is reset ($S_{LIP} = 0$) to notify the MPC of cease of power transmission in P-pole. After a fixed time delay T_{FR}, which should be carefully selected by considering the worst case, the force retardation is released. If the voltage is recovering, S_{LIP} is set ($S_{LIP} = 1$) again and the firing angle of the LCC rectifier is gradually decreased to its pre-fault value. If the voltage does not recover in three attempts, the fault is declared as a permanent fault and the operation of LCC is stopped.

As depicted in Figure 4b, for a fault on the main transmission line, the dc CB of each faulted pole is disconnected immediately. Then the operating mode of the faulted poles of the VSC stations are changed to dc side voltage control mode till the fault is cleared. For a fault on a VSC branch, say on Zone-A as depicted in Figure 4b, the relevant dc CBs (dc CB on P-pole, N-pole, or both) are immediately opened to isolate the faulted pole(s) from the main transmission line. The IGBTs of the faulted pole of VSC-A (say P-pole) are immediately blocked by the converter internal protection. Subsequently, the faulted pole, P-pole in this case, is de-energized by opening the corresponding ac CB, and the MPC is notified about the de-energization by resetting S_{VAP} ($S_{VAP} = 0$).

Before enabling the reclose operation, a fixed delay of T_{RC1} is allowed to rule out the possibility that the fault is permanent because reclosing onto a fault is hazardous to converter IGBTs. This check may require communicating with protection IEDs [38–41]. Therefore communication delays should be taken into account in setting T_{RC1}. The approach of determining the presence of a fault will be discussed later in Section 3.2. If the fault has been cleared, ac CB is reclosed and the operating mode of the relevant pole of VSC-A is changed from STATCOM mode to voltage control mode. The dc CB is reclosed once the converter terminal voltage reaches the dc voltage at tapping Point-A. Thereafter, the MPC is notified by setting S_{VAP} ($S_{VAP} = 1$) back to its normal value. The operating mode of P-pole of VSC-A is changed to P_{DC} control mode and the pre-fault power reference is re-established. The same process is applied to N-pole or both poles of VSC-A depending on the fault type. The same procedure is applicable to VSC-B, for faults on Zone-B. More details of the grid energization procedure can be found in [6].

2.3. Fault Discrimination Strategy

As a breaker must isolate only the faulty pole(s) of the transmission line segment (protection zone) involved in the fault, a highly secure fault discrimination strategy is important to achieve the desired reliability improvement. The dc CBs separate the different protection zones and are associated with di/dt limiting inductors as shown in Figure 2. These inductors are referred to as the boundary inductors in this paper due to their location at the boundaries of adjacent protection zones. Due to the existence of a boundary inductor between the main transmission line and a VSC branch, during a fault on the main transmission line, the maximum rate of change of voltage (ROCOV) observed at any terminal of the main transmission line is significantly higher than the maximum ROCOV observed on any terminal of a VSC branch; the opposite is true during a fault on a VSC branch [27,38]. This enables discrimination of faults and therefore, maximum ROCOV is selected as the main fault indicator [27]. The sensitivity of the ROCOV based fault discrimination is improved by incorporating a directional logic as presented in [41] and using the aerial voltage components. The directional logic is employed only on IEDs -AM, -AI, -BM, and -BI. The directional logic is not relevant for IED-LR and IED-LI, since there are no other dc protection zones behind them. The faulty pole is identified using the logic described in [42]. The proposed fault discrimination algorithm with combined features is shown in Figure 5.

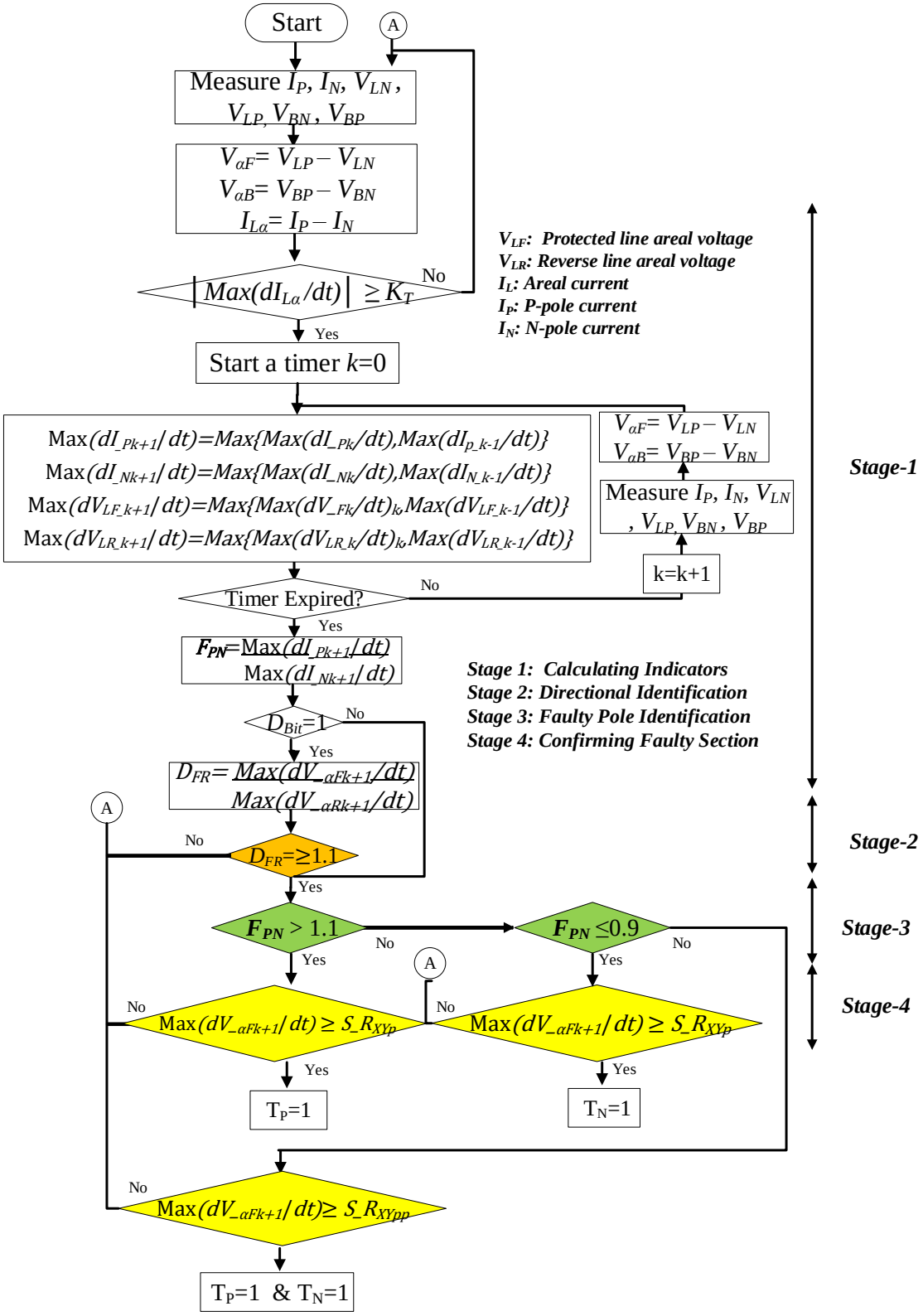


Figure 5. Fault discrimination algorithm.

The algorithm is run on an IED located at the boundary of a protected line. An IED takes voltage measurements at either side of the boundary inductors of P- and N-poles, and the currents through the inductors on both poles as inputs. V_{LN}, V_{LP}, are respectively N-pole and P-pole voltages on line side of the boundary inductors and V_{BN}, V_{BP} are N-pole and P-pole voltages of the bus side of the

boundary inductors. It then extracts the aerial components of the input voltages and the currents: $V_{L\alpha}(= V_{LP} - V_{LN})$, the aerial component of the voltages at the line side of boundary inductors, $V_{B\alpha}(= V_{BP} - V_{BN})$, the aerial component of the voltages at the bus side of the boundary inductors, and $I_{L\alpha}(= I_P - I_N)$, the aerial component of the current. The currents I_P and I_N are respectively the currents through the P-pole and the N-pole.

The algorithm is triggered when any of the observed rate of change of current (ROCOC) value is greater than the threshold K_T. The maximum values of ROCOV and ROCOC are tracked over a short time window, T_{w-max}, and the respective maximum values observed at the end of the time-window are sent to calculate the fault discrimination indices. Two indices, F_{PN} and D_{FR}, are calculated using Equations (2) and (3) using the maximum values of ROCOV and ROCOC.

$$D_{FR} = \frac{\text{Max}(dV_{L\alpha}/dt)}{\text{Max}(dV_{B\alpha}/dt)} \tag{2}$$

$$F_{PN} = \frac{\text{Max}(dI_P/dt)}{\text{Max}(dI_N/dt)} \tag{3}$$

If D_{FR} is greater than a preset threshold ($D_{FR} > 1 + \varepsilon$), the fault is declared to be on the forward side [41]. The faulty poles are identified by considering the fact that index F_{PN} is close to unity for pole-to-pole faults ($1 + \varepsilon > F_{PN} \geq 1 - \varepsilon$), considerably greater than unity for P-pole-to-ground faults ($F_{PN} > 1 + \varepsilon$), and considerably less than unity for N-pole-to-ground faults ($1 - \varepsilon > F_{PN}$) [42]. ε is a positive tolerance value. Once the fault type is identified, depending on whether the fault is a single-pole fault or a pole-to-pole fault, the maximum rate of change of V_F is compared with a threshold (S_R_{XYp} for pole-to-ground and S_R_{XYpp} for pole-to-pole) to determine whether the fault is within the protected line.

3. Test System Parameters and Settings

A detailed electromagnetic transient simulation model of the power system shown in Figure 2 was implemented on the PSCAD/EMTDC simulation software to validate the effectiveness of the proposed fault detection and clearance scheme.

3.1. Test System

The test system is adapted from [1]. The LCC scheme considered in this study is similar to a Bipole II of the Nelson River HVdc system [37], including the transmission line parameters. The line lengths are shown in Figure 2. Each pole of the LCC stations is assumed to consisting of twelve pulse converters. The principle converter parameters and transformer data are given in Tables 1 and 2 respectively.

Table 1. Test system details.

Parameter	Value	Units
Nominal dc Voltage	±500	kV
ac Sys. SCR LCC-Rectifier	2.9	
ac Sys. SCR LCC-Inverter	5.0	
ac Sys. SCR VSC-A/B	3.0	
Power ramping rate in LCC during fault recovery (per pole)	1000	MW/s
Power ramping rate in VSC during fault recovery (per pole)	300	MW/s
VSC Data		
MMC cell capacitance	2000	μF
MMC cell switch on resistance	0.2	Ω
Arm reactor	25	mH

Table 2. Transformer data.

Parameter	Value	Units
MVA-LCCs	600 × 2	MW/pole
MVA-VSC-A/B	300	MW/pole
Leakage Reactance-LCCs	0.15	pu
Leakage Reactance-VSCs	0.1	pu
Transformer Ratio LCCs	230 kV/209 kV	
Transformer Ratio VSCs	330 kV/315 kV	

A voltage-dependent current order limit (VDCOL) is implemented at the LCC inverter to protect its thyristor valves during ac side faults. The MMC cell capacitance is sized to achieve a ratio of 25 J/kVA [43] for the total capacitor stored energy in the converter to the rated power. The remaining parameters of the VSCs are given in [1]. A 60 mH inductor is placed at terminals of the VSC stations and in series with dc CBs. The dc CB operating delay and the maximum breaking current are assumed to be 2 ms and 6 kA. IGBTs are blocked when the current through any arm increased beyond 3 pu and for longer than 20 µs.

3.2. Protection Settings

In order to avoid false tripping, the single-pole ROCOV threshold setting S_R_{XYp} for the IED-XY should be set higher than the observed maximum ROCOV for a single-pole-to-ground short circuit fault in the forward direction, just outside the protected zone demarcated by the terminal inductor. This value is denoted by $ROCOV_{pMx\_A}$. Furthermore, in order to make sure far-end faults are detected, S_R_{XYp} should be set lower than the observed maximum ROCOV value for a high resistance single-pole-to-ground fault at the far-end of the protected transmission line, $ROCOV_{pMx\_B}$. The expected maximum fault resistance to be detected should be selected by considering the constraint $ROCOV_{pMx\_B} > ROCOV_{pMx\_A}$. Therefore, to compromise the sensitivity and the reliability requirements, the single-pole-to-ground fault ROCOV threshold setting for IED-XY is calculated with Equation (4).

$$S\_R_{XYp} = \frac{1}{2}\left(ROCOV_{pMx\_A} + ROCOV_{pMx\_B}\right) \quad (4)$$

The pole-to-pole settings are calculated in a similar manner by considering the pole-to-pole faults instead of the single-pole-to-ground faults. The setting S_R_{XYpp} for pole-to-pole faults is greater than the threshold settings for single-pole faults, S_R_{XYp}. Table 3 shows the maximum ROCOV values used to determine the settings S_R_{XYpp} and S_R_{XYp}. The maximum ROCOV settings of protection IEDs, S_R_{XYpp} and S_R_{XYp}, are given in Table 4.

Table 3. Maximum ROCOV values used with Equation (4).

IED	$ROCOV_{ppMx\_A}$ (kV/ms)	$ROCOV_{ppMx\_B}$ (kV/ms)	$ROCOV_{pMx\_A}$ (kV/ms)	$ROCOV_{pMx\_B}$ (kV/ms)
IED-LR	2230	3028	971	1077
IED-LI	1413	2903	586	1068
IED-AM	1394	3759	538	1346
IED-BM	2019	3932	875	1538

Table 4. Relay settings.

IED	S_R_{XYpp} (kV/ms)	S_R_{XYp} (kV/ms)	IED	S_R_{XYp} (kV/ms)	S_R_{XYpp} (kV/ms)
IED-LR	2630	1023	IED-BM	2975	1206
IED-LI	2158	827	IED-AI	8518	3542
IED-AM	2576	942	IED-BI	8838	3663

The threshold settings for the directional discrimination index, D_{FR}, and the faulty pole(s) identification index, F_{PN}, were selected considering a 10% tolerance and common for all IEDs. The ideal value for these two indices is 1, and the 10% tolerance provides an added security. Based on the simulation studies, the fault detection threshold parameter K_T is set to 2 kA/ms and the time window for computing the maximum ROCOC and ROCOV values, T_{w-max}, was set to 0.5 ms. This is the expiry time of the timer shown in Figure 5.

When selecting the time delay, T_{RC1}, the expected maximum fault clearing time and the time to run an appropriate checking mechanism to determine whether a fault on a VSC branch is permanent or temporary should be considered. The discrimination between a temporary arc fault and a permanent fault can be done in two ways in this application. The extinction of a temporary arc can be confirmed by looking at the reflected wave after injecting an active signal with the help of VSC, as proposed in [44,45]. Alternatively, the temporary faults can be discriminated from the permanent faults with the help of residual voltage characteristics of dc CBs at the tapping point as proposed in [38–41]. According to [38,41], the temporary faults can be discriminated from the permanent faults within a several tens of milliseconds. Assuming that the confirmation of extinction of fault is done at the dc CB, the time required to assess and inform the converter station are considered. The communication delay is estimated assuming that the velocity of signal propagation is 150 km/ms. The time delay, T_{del}, for communication between two entities separated by l km distance, is approximated by Equation (5).

$$T_{del} = \frac{l}{150} + 1\ ms \tag{5}$$

The time delay T_{RC1} shown in Figure 4b is set to 362 ms by considering a 330 ms duration for extinction of the temporary fault, a 30 ms worst-case delay for confirmation of the extinction of the temporary fault, and 2 ms communication delay. The time delay T_{FR} shown in Figure 4a is set to 150 ms. The delay T_{RC2} is the time delay to settle the VSC-A terminal voltage once it is re-started in DC voltage control mode by de-blocking the IGBT after re-closing AC circuit breakers. T_{RC2} is set to 50 ms.

4. Results

4.1. Fault Discrimination

Determination of the fault direction using the calculated value of D_{FR} at IED-AM is demonstrated in Figure 6 for faults inside Zone-M and Zone-A.

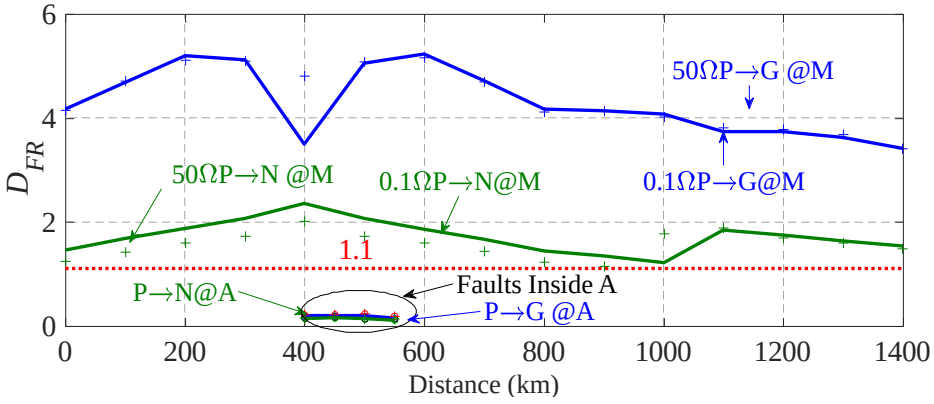


Figure 6. Calculated D_{FR} for faults inside Zone-M and Zone-A at IED-AM.

To avoid the ambiguity of having two curves for the same location, the distance to a fault is measured from the LCC rectifier end. The label 0.1ΩP→G@M indicates a P-pole-to-ground fault inside Zone-M simulated with a 0.1 Ω fault resistance and 0.1ΩP→N@M indicates a P-pole-to-N-pole fault with a 0.1 Ω fault resistance. The same convention is used for 50 Ω faults. The respective threshold is

also indicated on each graph. As depicted in Figure 6, the minimum calculated D_{FR} for the faults inside Zone-M is 1.2 whereas the highest calculated value of D_{FR} for faults inside Zone-A is 0.24. Therefore, as per the directional criterion depicted in Figure 6, any fault inside Zone-A is discriminated as a reverse fault at IED-AM while any fault inside Zone-M is declared as a fault in the forward direction. As depicted in Figure 7a,b, pole(s) involved in the fault can be recognized with the help of faulty pole(s) identification criterion respectively at IED-LR at the LCC rectifier and IED-AM at the tapping point-A.

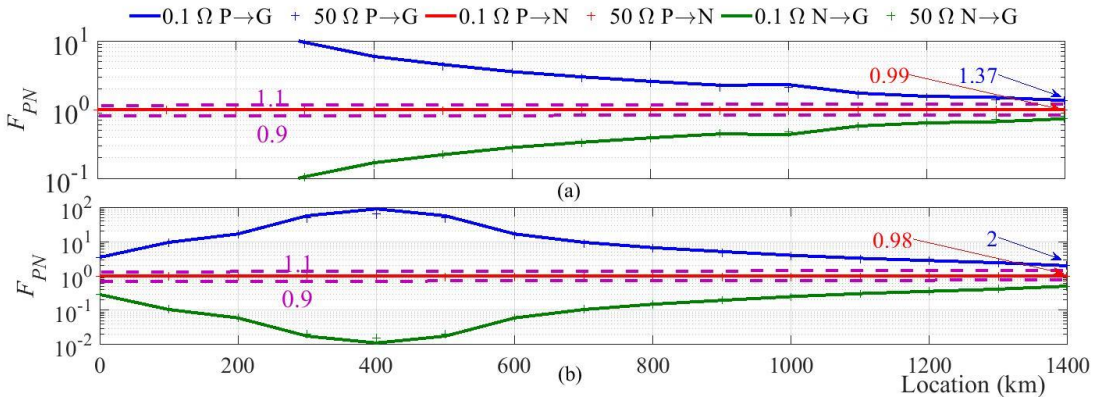


Figure 7. Calculated F_{PN} for faults in Zone-M (**a**) At IED-LR, (**b**) At IED-AM.

All P-pole-to-N-pole faults result in F_{PN} values between the thresholds 0.9 and 1.1; F_{PN} values for all P-pole-to-ground faults are above 1.1; and F_{PN} values for all N-pole-to-ground faults are below 0.9. Similar observations were made for the protection IEDs located near the LCC inverter and Point-B. The minimum margin of discrimination of faulty pole(s) at IED-A is 82%, and despite the extreme line length, IED-LR manages to recognize the faulty pole even for remote faults. As depicted in Figure 8a,b, the maximum ROCOV is greater than the respective thresholds up to a fault resistance of 50 Ω.

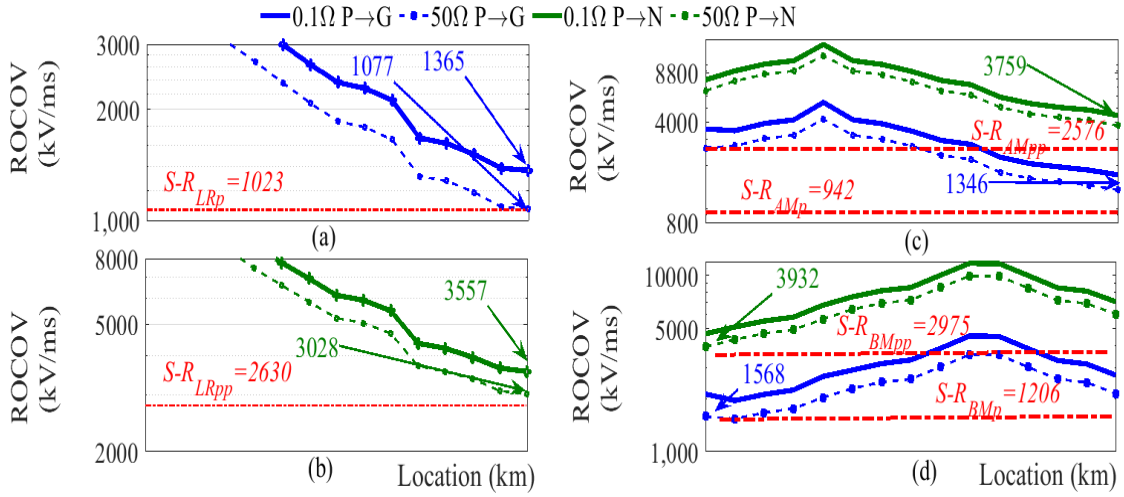


Figure 8. Calculated maximum ROCOV values (**a**) At IED-LR for P-pole-to-ground faults, (**b**) At IED-LR for P-pole-to-N-pole faults, (**c**) At IED-AM, (**d**) At IED-BM.

The discrimination margin for end of line faults is higher for pole-to-pole faults (15%) when compared with the single pole-to-ground faults (5%). If a higher margin is desired for single-pole-to-ground faults, the fault resistance considered in measurement of $ROCOV_{pMx\_B}$ that is used in Equation (4) can be lowered, leaving the end of line high resistance faults to be dealt using a transfer trip scheme or a line differential type backup protection scheme. Clearing time is not critical for such faults as the current rises slower and the peak fault current is lower for remote high

resistance faults. As depicted in Figure 7, pole(s) involved in the fault can be identified using F_{PN} with an adequate margin even though the line is very long. Similar observations were made for the protection IED located near the LCC inverter. Furthermore, as depicted in Figure 8c, the faulty section can be identified using the maximum ROCOV criterion with ample margin for both pole-to-pole (46%) and single-pole-to-ground (43%) faults at IED-AM. The variation of maximum ROCOV for N-pole-to-ground faults is similar to that of P-pole-to-ground faults.

Therefore, the results presented in Figures 6–8 confirm the ability of protection IEDs located at LCC stations and tapping points to identify any fault in Zone-M having a resistance up to 50 Ω, and the pole(s) involved. Furthermore, settings calculated using Equation (4) avoids false tripping for any fault in the forward direction beyond the protected zones.

The results shown in Table 5 confirm the capability of IED at the tapping point-A to detect and discriminate the faults on Zone-A using the proposed fault discrimination criteria. In Table 5, distance to the fault is measured from the IED. The third and fourth columns indicate the maximum ROCOV value for a metallic fault and for a 50 Ω fault at the specified location.

Table 5. Identifying faults in Zone-A at R_{AI}.

Loc. (km)	Fault Type	$ROCOV_{Max1}$ (kV/ms)	$ROCOV_{Max2}$ (kV/ms)	D_{FR}	F_{PN}
100	P→G	7393	5797	9.5	11.9
50	P→G	8518	6682	10.4	56.6
100	P→N	19,035	16,030	9.4	1
50	P→N	22,053	18,718	10.4	1

4.2. Clearing Temporary Faults on the Main Line

In the following simulation studies, a temporary metallic fault was considered and the fault is assumed to be self-cleared when the current through the fault falls below 0.1 kA.

4.2.1. Pole-to-Pole Faults

Figures 9 and 10 show the dc voltages and currents observed at the VSC and LCC stations during a P-pole-to-N-pole fault on the main transmission line, 100 km away from the LCC rectifier.

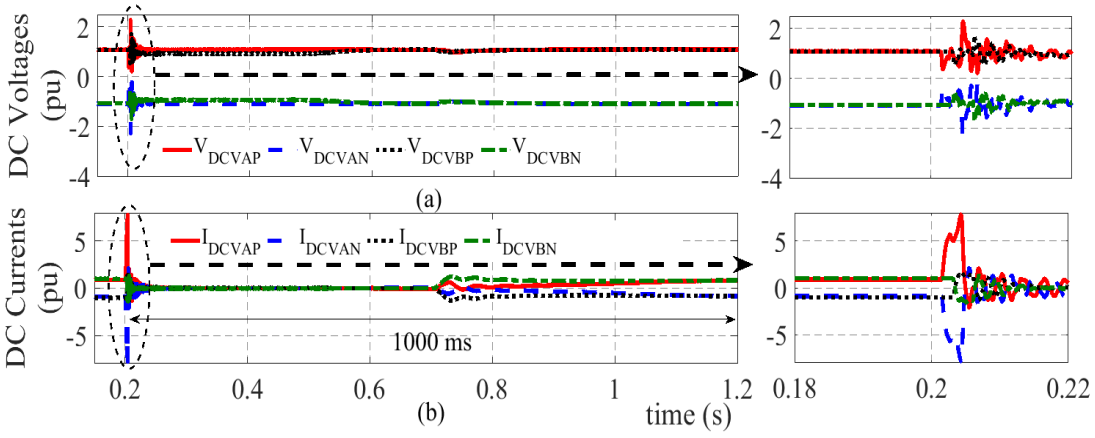


Figure 9. DC side measurements at VSC stations for a P-Pole-to-N-Pole fault on the main transmission line (**a**) voltages, (**b**) currents.

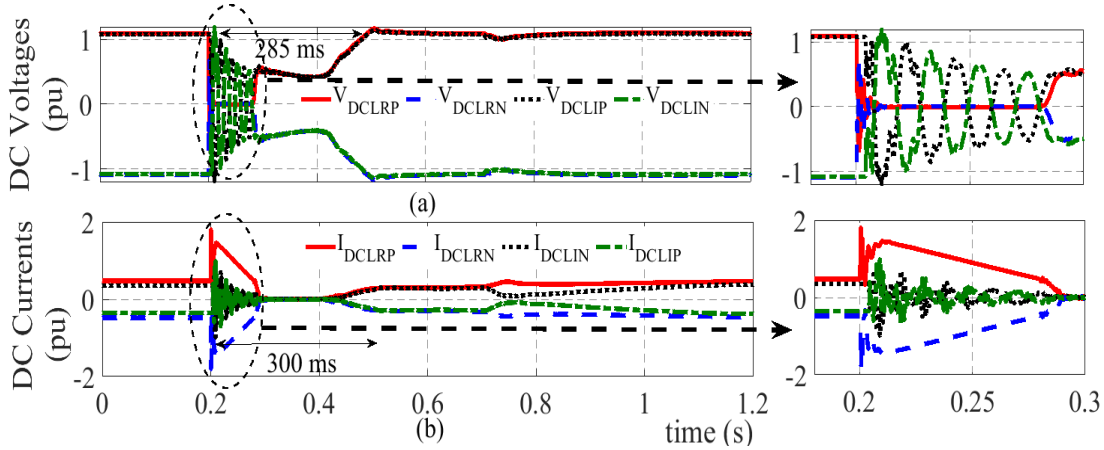


Figure 10. DC side measurements at LCC stations for a P-Pole-to-N-Pole fault on the main transmission line (**a**) voltages, (**b**) currents. Shown to the right of each plot is a zoomed view of the initial transient period.

According to Figure 9, the fault currents through the VSC rectifiers rapidly rose after the fault, until the dc CBs are opened as per the procedure described in the flowchart of Figure 4. Operation of the dc CBs quickly eliminated the fault current contributions from the VSCs, and enabled clearing of this temporary fault through force retardation of LCCs. This can be seen from Figure 10.

Moreover, Figure 9 shows that both VSCs managed to hold the dc voltage operating in the dc voltage control mode, fulfilling the requirement 2 listed in Section 2, and then quickly reconnect to the main transmission line after its restoration. As depicted in Figure 11, only the ac system connected to the LCC rectifier is noticeably affected by the fault.

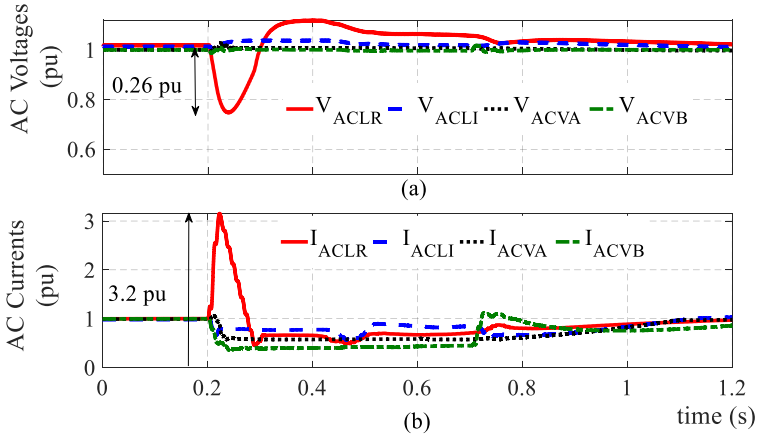


Figure 11. AC side measurements during P-Pole-to-N-Pole fault on the main transmission line (**a**) voltages, (**b**) currents.

In contrast to the topology without dc CB studied in [1], the ac system connected to the VSC rectifier was not affected by the fault. A 0.26 pu drop in ac voltage at LCC rectifier was due to 3.2 pu rise in ac current during the fault.

According to Figure 10, the fault clearing time, voltage recovery time, and the pre-fault state recovery times for the LCC link are 120 ms, 285 ms, and 300 ms. These figures are much shorter than those achievable with the topology without dc CB proposed in [1], i.e., 300 ms, 700 ms, and 1000 ms respectively. Without dc CBs, the VSC rectifier injects fault currents for several ac cycles until the ac CB opens and interrupts the VSC [1]. Furthermore, the VSC rectifier needs restarting and regaining control to restore the pre-fault power level of VSC stations, and this complete process required about 1000 ms as per [1].

4.2.2. Pole-to-Ground Faults

The single-pole-to-ground fault recovery performance was studied considering a metallic P-pole-to-ground fault on the main transmission line, 700 km away from the LCC rectifier. As per the results shown in Figures 12 and 13, strong transients are visible in healthy pole voltages and currents observed at both LCC and VSC stations.

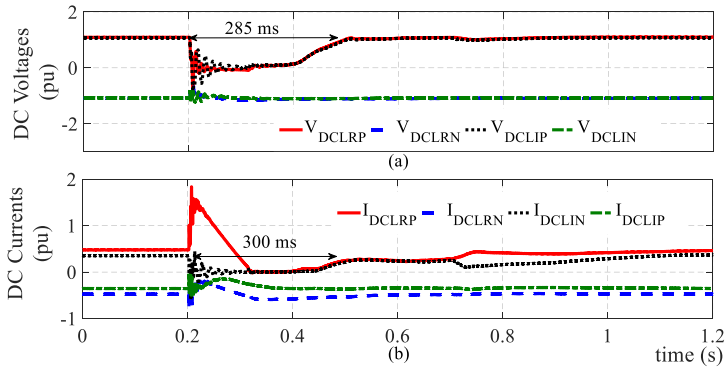


Figure 12. DC measurements at LCC stations for a P-Pole-to-ground fault on main transmission line (**a**) voltages, (**b**) currents.

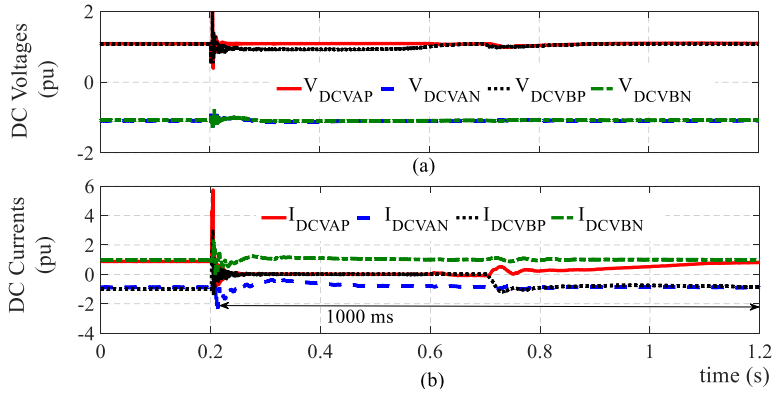


Figure 13. DC measurements at VSC stations for a P-Pole-to-ground fault on main transmission line (**a**) voltages, (**b**) currents.

After applying the fault recovery process in Figure 4, the voltages and currents of the healthy pole become stable within about 200 ms. As visible in Figure 14, the drop in ac side voltage of the LCC rectifier is smaller than that for the pole-to-pole fault.

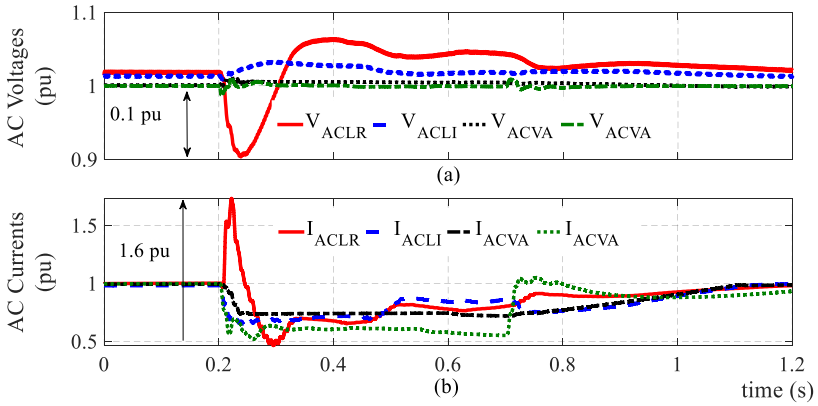


Figure 14. AC side measurements for a P-Pole-to-ground fault on the main transmission line (**a**) voltages, (**b**) currents.

Therefore, as depicted in Figure 15, power can be transferred through the healthy pole during a single-pole-to-ground fault. In addition to the recovery speed, the capability of transferring power through the healthy pole of VSC stations is another advantage of the proposed scheme when compared with the scheme without dc CB in [1].

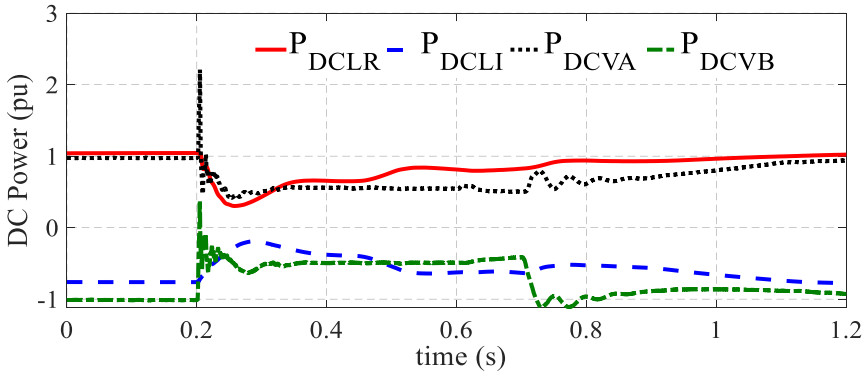


Figure 15. DC power for a P-Pole-to-ground fault on the main transmission line.

4.3. Clearing Temporary Faults on a VSC Branch

4.3.1. Pole-to-Pole Faults

Figures 16 and 17 show the dc side measurements at converter stations for a metallic pole-to-pole fault on VSC branch-A, 50 km away from VSC-A (in Zone-A).

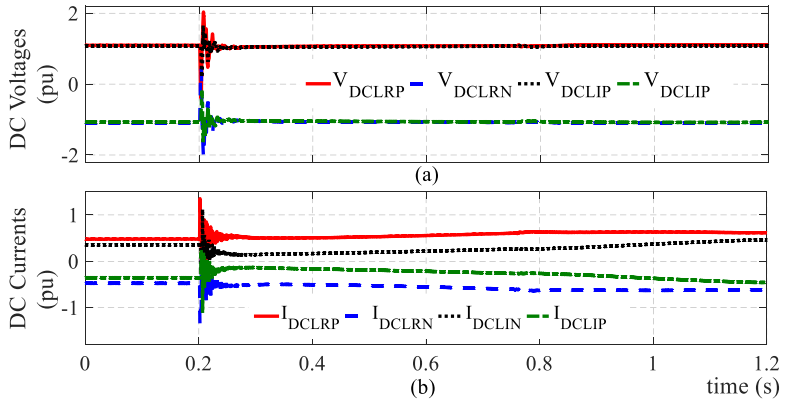


Figure 16. DC side measurements at LCC stations for a P-Pole-to-N-Pole fault on VSC branch-A (**a**) voltages, (**b**) currents.

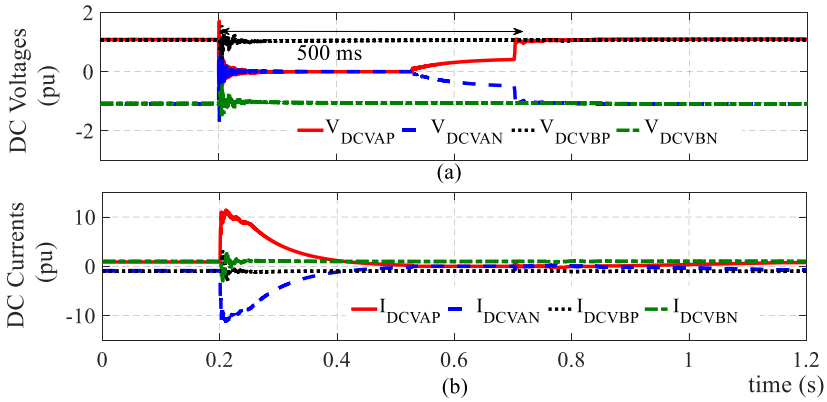


Figure 17. DC side measurements at VSC stations for a P-Pole-to-N-Pole fault on VSC branch-A (**a**) voltages, (**b**) currents.

According to Figure 16, the LCC link was not impacted and the requirement 1 listed in Section 2.1 was fulfilled. The fault recovery process of VSC-A is depicted in Figure 17. Note that this momentary peak fault current of 10.5 kA fed by VSC-A is shared by all three arms of the VSC. It took about 1000 ms to restore the pre-fault state. The only significant effect on the LCC link was the reduction of power received to LCC inverter due to the sudden disconnection of VSC-A (rectifier). However, the amount of power delivered to the LCC inverter was restored to the pre-fault level within 1000 ms.

4.3.2. Pole-to-Ground Faults

Recovering from asymmetrical faults is more challenging. However, the successful application of the fault recovery procedure proposed in Figure 4 to recover from a single-pole-to-ground fault on VSC branch-A (Zone-A) is depicted in Figures 18 and 19. The healthy pole of VSC-A is capable of continuing the power transfer with ground return mode till the fault is recovered.

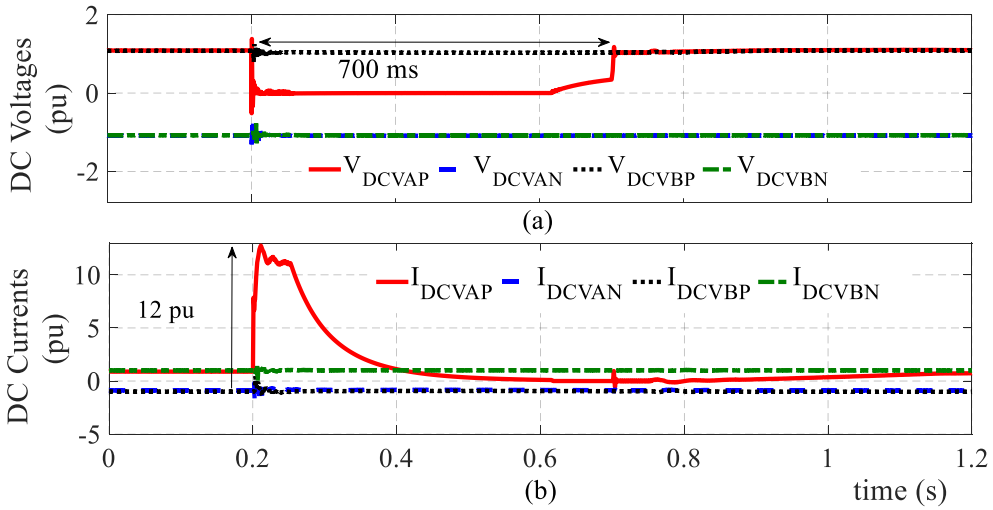


Figure 18. DC side measurements at VSC stations during a P-Pole-to-ground fault on VSC branch-A (**a**) voltages, (**b**) currents.

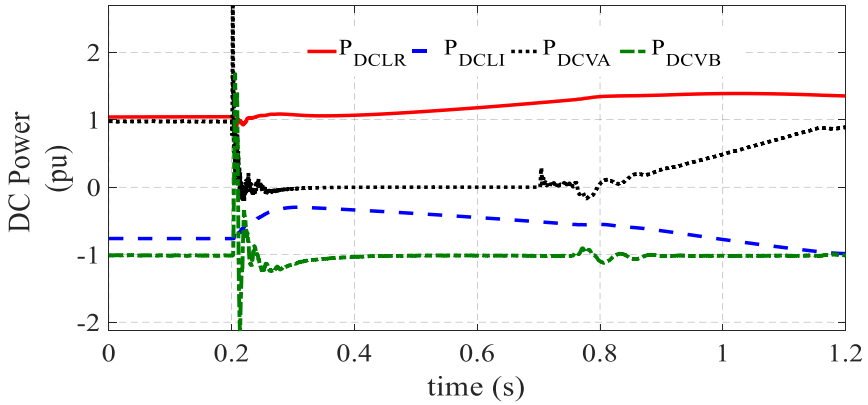


Figure 19. DC power measurements during a P-Pole-to-ground fault on VSC branch-A.

4.4. Fault Recovery Delays, Fault Detection Speed, and Breaker Rating

The observed recovery times for four-fault scenarios are tabulated in Table 6. The first and second columns show respectively the fault zone and fault type. The third and the fourth columns show the time taken to regain the pre-fault power level for the LCC link and for the VSC station connected to the faulted VSC branch.

Table 6. Fault recovery times.

F. Loc.	Type	T_{LPR} (ms)	T_{VPR} (ms)
Tap	P→N	0	1000
Tap	P→G	0	1000
Main	P→N	300	1000
Main	P→G	300	1000

As depicted in Figure 20a, any metallic fault can be detected within 1.09 ms. The pole-to-pole faults on the main transmission line are detected a little faster than single pole-to-ground faults, and this is more desirable. Figure 20b shows the observed maximum fault current through the dc CBs, 2 ms after the fault. Accordingly, a dc CB capable of interrupting 6 kA within 2 ms is adequate for the considered hybrid HVdc system.

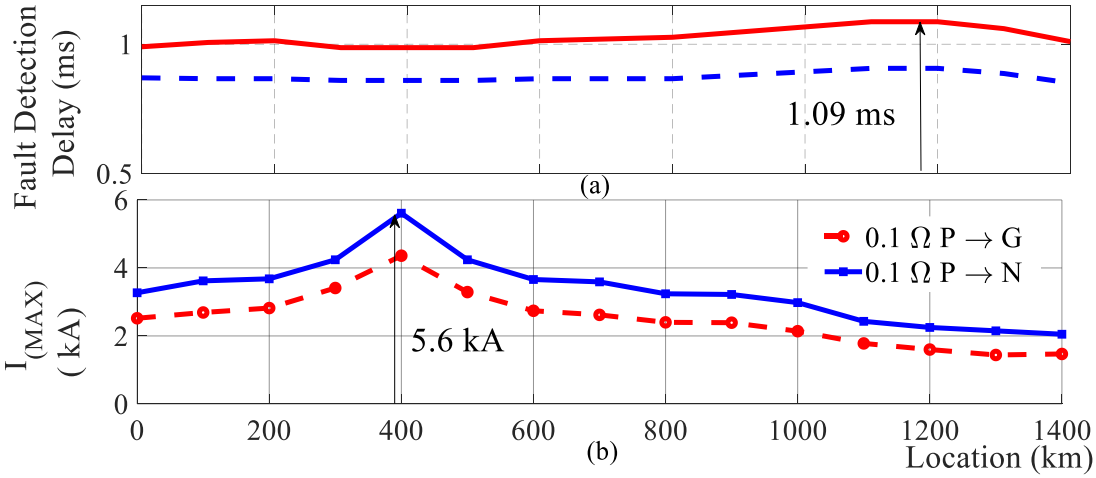


Figure 20. DC CB requirement (**a**) Fault detection speed, (**b**) Maximum dc CB current.

5. Conclusions

A selective fault clearing scheme is proposed for a possible hybrid VSC-LCC multi-terminal HVdc transmission structure in which the spare capacity of an LCC transmission line is shared with a smaller VSC scheme. This situation exists on the present-day Bipoles I and II of Manitoba Hydro's HVdc transmission system. The proposed fault discrimination and fault clearing procedure allow tapping of the main LCC link without significant degradation of the fault recovery performances. This is achieved with an optimal way by placing a dc CB on each VSC branch at the point of interconnection to the main transmission line. The detailed simulations with a test system confirmed (i) the ability of successfully discriminating faults at different sections at a speed fast enough for successful fault recovery, (ii) the ability to identify the faulted pole(s) to enable single-pole operation during the single-pole-to-ground faults, (iii) the successful recovery from temporary faults at various locations, and (iv) the requirements are within the capability of a 6 kA, 2 ms dc CB, for the test system considered.

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