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High Threshold Voltage Normally off Ultra-Thin-Barrier GaN MISHEMT with MOCVD-Regrown Ohmics and Si-Rich LPCVD-SiN_x Gate Insulator

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Abstract: A high threshold voltage (V_{TH}) normally off GaN MISHEMTs with a uniform threshold voltage distribution ($V_{TH} = 4.25 \pm 0.1$ V at $I_{DS} = 1$ μ A/mm) were demonstrated by the selective area ohmic regrowth technique together with an Si-rich LPCVD-SiN_x gate insulator. In the conventional GaN MOSFET structure, the carriers were induced by the inversion channel at a high positive gate voltage. However, this design sacrifices the channel mobility and reliability because a huge number of carriers are beneath the gate insulator directly during operation. In this study, a 3-nm ultra-thin Al_{0.25}Ga_{0.75}N barrier was adopted to provide a two-dimensional electron gas (2DEG) channel underneath the gate terminal and selective area MOCVD-regrowth layer to improve the ohmic contact resistivity. An Si-rich LPCVD-SiN_x gate insulator was employed to absorb trace oxygen contamination on the GaN surface and to improve the insulator/GaN interface quality. Based on the breakdown voltage, current density, and dynamic R_{ON} measured results, the proposed LPCVD-MISHEMT provides a potential candidate solution for switching power electronics.

Keywords: normally off; MISHEMT; MOCVD-regrowth; leakage current; dynamic R_{ON}

1. Introduction

In recent years, GaN-based normally off high-electron-mobility transistors (HEMTs) have been implemented for switching power electronics due to their wide energy bandgap, high electron mobility, and high current density [1–3]. In order to achieve the normally off operation of the GaN HEMT structure, many papers have reported a recessed gate (e.g., fully removed AlGaN barrier beneath the gate region) and metal-insulator-semiconductor (MIS) gate structure process [4–7]. By controlling the etching depth and profile aspect ratio, a stable positive threshold voltage (V_{TH}) can thus be obtained. In addition, the MIS gate structure also offers high thermal stability of V_{TH} and a large forward gate-voltage operating range [8]. However, the deep level traps were generated on AlGaN or GaN surfaces by plasma bombardment damages, which caused the serious V_{TH} variation and reliability issue [9]. To overcome the etching damages and V_{TH} uniformity issues of the gate-recess-type normally off GaN HEMT, ultra-thin-barrier (UTB) AlGaN/GaN heterostructures with an MIS gate architecture were also proposed [10–12]. All of these previous studies adopted PEALD (plasma-enhanced atomic layer deposition) as the gate insulator to minimize the plasma-induced damage during gate insulator

deposition. However, the PEALD-grown Al_2O_3 is very sensitive to the subsequent process temperature. C. Mizue et al. observed that the as-deposited ALD- Al_2O_3 thin film performed an amorphous-phase structure and the thin film also achieved a uniform thickness at this stage, owing to its deposition mechanism. During the ohmic contact formation process, the 850–900 °C annealing temperature leads to the formation of a microcrystallized Al_2O_3 layer, resulting in an obvious increase in the leakage current of the $\text{Al}_2\text{O}_3/\text{GaN}$ structure [13,14]. In this study, we proposed an Si-rich SiN_x gate insulator grown by LPCVD (low-pressure chemical vapor deposition system) to absorb the oxygen atom on the native AlGaN barrier layer surface and thus narrow the oxygen contamination region between $\text{SiN}_x/\text{AlGaN}$ interfaces. To further improve the ohmic contact resistivity, the MOCVE-regrown AlGaN drain/source regions were also adopted to demonstrate a low on-resistance (R_{ON}) ultra-thin barrier (UTB) GaN MISHEMT with a large positive V_{TH} performance.

2. Device Fabrication

The devices were fabricated using an AlGaN/GaN heterostructure, grown by metal-organic-chemical vapor deposition (MOCVD) on a conductive 6-inch Si (111) p-type substrate. As shown in Figure 1, a 4- μm -thick AlN transition layer and C-doped buffer layer were first grown on an Si substrate for high breakdown voltage consideration. Then, an undoped 300-nm GaN channel layer was deposited on a 50-nm-thick low Al mole fraction ($A\% = 5\%$), AlGaN back barrier layer, and a 3-nm-thick undoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ ultra-thin barrier layer were sandwiched into a 1-nm GaN cap layer and GaN channel. The GaN cap was used to suppress the oxidation of the $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ thin barrier and the cap layer at the regrowth region was removed. As to the device fabrication, the device started with the AlGaN regrowth region formation. Prior to the regrowth process, a 100-nm-thick dense SiO_2 layer was deposited on the GaN wafer as a regrowth mask by PECVD and the regrowth region was patterned using diluted HF wet etching solution. Then, the 1-nm GaN cap layer was removed by low-damage $\text{SF}_6 + \text{BCl}_3$ mixtures in a dry etching process with a very low DC power condition and the sample was loaded into MOCVD without a queue time. Different from the published regrowth method with ohmic recess [15,16], the additional 20 nm of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ was selectively grown on the exposed 3-nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer surface. The Al composition of the regrown $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ layer was also 25% to achieve a high-quality regrowth interface and good contact resistance with the initial barrier layer. This structure exhibited a sheet charge density of $1.05 \times 10^{13} \text{ cm}^{-2}$ and electron mobility of $1570 \text{ cm}^2/\text{V}\cdot\text{s}$ at 300 K together with an epitaxial sheet resistance of $420 \Omega/\square$ measured by Hall measurement. The first step in determining carrier mobility is to measure the Hall voltage by forcing both a magnetic field perpendicular to the sample and a current through the sample. The resistivity can be determined using either a four-point probe on GaN test samples. The PECVD SiO_2 in the gate region was then selectively removed using diluted HF wet etching. Afterward, the active region was protected by a photoresist and the mesa isolation region was removed in a reactive ion etching (RIE) chamber using $\text{BCl}_3 + \text{Cl}_2$ mixed-gas plasma. As to the gate dielectric layer, a 32-nm-thick layer of Si-rich LPCVD-grown SiN_x measured by transmission electron microscopy (TEM) was deposited on the 1-nm GaN cap layer. The SiH_2Cl_2 (dichlorosilane) flow rate was 150 sccm together with the mixture gas flow ratio ($\text{SiH}_2\text{Cl}_2:\text{NH}_3$) of 5:1 to reach an Si-rich content in SiN_x at 800 °C, 180 m torr environment, and the deposition rate was around 2.2 nm/min. For comparison, the device with a 30-nm PECVD-grown SiN_x gate dielectric was also fabricated. The ohmic contacts for the drain and source contacts were deposited by the electron beam evaporation of a multi-layer Ti/Al/Ni/Au (30 nm/125 nm/50 nm/200 nm) sequence, followed by rapid thermal annealing at 550 °C for 20 min in a nitrogen-rich ambient. Finally, the electron-beam evaporated Ni/Au was deposited as gate metal. Compared to the conventional gate recessed-type E-mode HEMT process, the barrier layer in this study eliminated the plasma bombardment by dry etching during the device fabrication process. Figure 1 shows the cross-sectional structure and scanning electron microscope (SEM) images of the fabricated UTB GaN MISHEMT with the device dimension $L_{\text{GS}}/L_{\text{G}}/L_{\text{GD}}/L_{\text{FP}}$ of 2/1.5/10/4 μm , respectively. According to the atomic force microscope (AFM) images shown in Figure 2, the root mean square roughness of the GaN/ $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ /GaN heterostructure

beneath the gate metal area is 0.37 nm and this value is 0.43 nm of the regrown $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ ohmic contact area. The ohmic contact resistance measured by the transmission line method (TLM) was improved from $2.2 \times 10^{-5} \Omega\text{-cm}^2$ to $1.6 \times 10^{-6} \Omega\text{-cm}^2$ by adopting the AlGaN-regrown method owing to its totally 23-nm AlGaN barrier-induced high 2-DEG density.

Figure 1. The layer structure and cross-sectional SEM images of Si-rich LPCVD-SiN_x MISHEMT with a selective area ohmic regrowth layer.

Figure 2. The AFM images gate trench profile before and after selective area ohmic regrowth.

3. Results and Discussion

Figure 3 presents the energy dispersive spectrometer (EDS) vertical line scanning analysis for the PECVD- and LPCVD-SiN_x passivated UTB MISHEMT. Obviously, a narrow oxygen-contaminated layer was found on the AlGaIn surface, which was primarily due to the native AlGaIn oxidation compounds with environment moisture. However, with Si-rich LPCVD passivation at high temperature, the oxygen atoms were collected into the SiN layer and the oxygen-contaminated layer for LPCVD-MISHEMT was eliminated [17]. Therefore, Si-rich LPCVD-grown SiN_x film passivates the dangling bonds on the Ga(Al)-terminated AlGaIn surface, and thus lowers the interface traps in LPCVD-grown SiN_x passivated UTB MISHEMTs.

Figure 3. The EDX vertical line scanning images for PECVD- and LPCVD-SiN_x passivated UTB MISHEMT.

Figure 4a displays the three-terminal off-state breakdown voltages (V_{BR}) of devices with a wide gate-to-drain spacing (10 μm), which was evaluated by the Agilent B1505A measurement system and the Si substrate was grounded bias during the measurement. In this study, V_{BR} is defined as the voltage when the drain leakage current between the source and the drain contacts reaches 1 mA/mm at a V_{GS} of 0 V. The drain (I_{DS}) leakage current of PECVD-MISHEMT increases rapidly with the increase of V_{DS} and its V_{BR} is 680 V. Referring to the gate (I_{GS}) leakage current in Figure 4b, obviously, the I_{DS} leakage current was one order of magnitude high than the I_{GS} leakage current. Thus, the three-terminal leakage current not only contributed by the gate terminal when $V_{DS} > 50$ V and the surface hopping leakage current also appeared in the breakdown mechanism of PECVD- MISHEMT [7]. The gate leakage current of LPCVD-MISHEMT is negligible and the drain-to-source leakage current dominated the breakdown mechanism in these devices, significantly improving the V_{BR} values to 750 V. Based on

the leakage current shown in Figure 4, the Si-rich high-quality LPCVD gate insulator suppressed the surface native oxidation layer and prevented electrons' surface hopping-induced leakage current at a high drain voltage [17].

Figure 4. (a) the three-terminal off-state breakdown voltages and (b) I_{GS} - V_{GS} characteristics for PECVD- and LPCVD-SiN_x passivated UTB MISHEMT.

Figure 5 displays the I_{DS} - V_{DS} outputs and log-scale I_{DS} - V_{GS} transfer characteristics of two devices at a V_{DS} of 10 V. The V_{TH} values of the PECVD- and the LPCVD-MISHEMT were both 4.25 V (defined by $I_{DS} = 1$ mA/mm). The corresponding maximum drain current density (I_{Dmax}) values were 276.26 and 361.71 mA/mm, respectively. The I_{Dmax} value of the LPCVD-MISHEMT was 30.9% higher than that of the PECVD-MISHEMT because the capability of the gate modulation-induced current was not limited by the gate leakage current, which appeared in PECVD-MISHEMT. Thus, the static R_{on} of the LPCVD-MISHEMT was improved to 19.85 Ω ·mm, which corresponds to a specific on-resistance ($R_{on} \cdot A$) of 1.98 m Ω ·cm² at a V_{GS} value of 16 V. These values of the PECVD-MISHEMT were 26.78 Ω ·mm and 2.67 m Ω ·cm², respectively. For the LPCVD-MISHEMT, the suppression in the off-state I_{DS} leakage current improved the on/off drain current ratio by approximately one order of magnitude and the subthreshold swing slope (S.S.) was improved from 155 to 150 mV/dec compared with that of the LPCVD-MISHEMT. Owing to the good interface between SiN_x and the ultra-thin AlGaIn barrier of the LPCVD-MISHEMT, contributing to improve the V_{TH} uniformity and controllability. A standard deviation of 0.1 V was obtained by measuring 50 samples across the 6-inch wafer, as shown in the inset of Figure 4b.

The quasi-static C-V characterization was adopted to capture the carrier filling process of the deep interface states at the MIS gate structure interface of both devices, as shown in Figure 6, which was performed on the MIS gate structure of both devices. The second plateau in the C-V characteristics of the MIS diodes depicts the response of the insulator/thin AlGaIn interface states. The interface trap density (D_{it}) values with τ between 10⁻⁶ and 10⁻⁴ s ($0.34 < E_C - E_T < 0.42$ eV) from 5.3×10^{10} cm⁻² to 1.2×10^{11} cm⁻² eV⁻¹ for LPCVD-MISHEMT were lower than 6.8×10^{10} cm⁻² to 2.5×10^{11} cm⁻² eV⁻¹ for PECVD-MISHEMT.

Figure 5. (a) The I_{DS} - V_{DS} characteristics (b) Log-scale I_{DS} - V_{GS} and V_{th} distribution of both devices.

Figure 6. The quasi-static C-V characterization and D_{it} versus $E_C - E_T$ of the PECVD- and LPCVD-MISHEMT.

To further analyze the trapping/detrapping effect, the dynamic R_{on} ratio of the PECVD- and LPCVD-MISHEMT was measured using a pulse width of 2 μs and period of 200 μs . In this work,

there were five bias conditions, which are pulse voltage (V_{GS} , V_{DS}) and quiescent voltage (V_{GSQ} , V_{DSQ}). However, the drain lag is due to the carriers during switching being trapped near the surface, which is in the SiN_x /thin AlGaIn interface. Furthermore, the trapping phenomenon also leads to a carrier density reduction and then an increase of the resistance. As the result, the V_{DSQ} for both devices was swept from 0 to 600 V with an increment of 100 V, respectively. Clearly, the LPCVD-MISHEMT exhibits a superior dynamic R_{on} than the PECVD-MISHEMT because the dynamic R_{on} ratio improved from 2.6 to 1.9 times at $V_{DSQ} = 600$ V, as indicated in Figure 7. In addition, a higher V_{DSQ} was applied because of a lower trap density in the MIS-gate interface. The oxygen vacancies in the $\text{AlGaIn}/\text{GaIn}$ interface can lead to serious trapping behavior during high switching operation [18].

Figure 7. The dynamic R_{on} ratio of the PECVD- and LPCVD-MISHEMT.

4. Conclusions

In this work, we developed and investigated the electrical properties of a normally off GaN-based switching device by using a high-temperature Si-rich LPCVD- SiN_x gate insulator and selective area ohmic regrowth technique. Based on the EDX analysis, Si-rich LPCVD- SiN_x mitigated the native oxygen contamination of the GaN surface, thus the interface D_{it} was improved. In addition, the selective area ohmic regrowth AlGaIn layer improved the 2-DEG density at the access region, thus the device R_{ON} was reduced. The low D_{it} high temperature Si-rich LPCVD- SiN_x gate insulator achieved a large positive threshold voltage together with a low leakage current and high I_{ON}/I_{OFF} ratio. Moreover, the low dynamic R_{ON} also indicated that the proposed device provides great promise in achieving a high-performance normally off GaN power electronics device.

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References

- Chen, K.J.; Haberlen, O.; Lidow, A.; Tsai, C.L.; Ueda, T.; Uemoto, Y.; Wu, Y. GaN-on-Si Power Technology: Devices and Applications. *IEEE Trans. Electron Devices* **2017**, *64*, 779–795. [\[CrossRef\]](#)
- Uemoto, Y.; Hikita, M.; Matsuo, H.; Ishida, H.; Yanagihara, M.; Ueno, H.; Ueda, T.; Tanaka, T.; Ueda, D. Gate Injection Transistor (GIT)—A Normally-Off AlGaIn/GaN Power Transistor Using Conductivity Modulation. *IEEE Trans. Electron Devices* **2007**, *54*, 3393–3399. [\[CrossRef\]](#)
- Marcon, D.; Saripalli, Y.N.; Decoutere, S. 200mm GaN-on-Si epitaxy and e-mode device technology. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 1621–1624. [\[CrossRef\]](#)
- Oka, T.; Nozawa, T. AlGaIn/GaN Recessed MIS-Gate HFET with High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications. *IEEE Electron Device Lett.* **2008**, *29*, 668–670. [\[CrossRef\]](#)
- Wang, Y.; Wang, M.; Xie, B.; Wen, C.P.; Wang, J.; Hao, Y.; Wu, W.; Chen, K.J.; Shen, B. High-performance normally-Off Al₂O₃/GaN MOSFET using a wet etching-based gate recess technique. *IEEE Electron Device Lett.* **2013**, *34*, 1370–1372. [\[CrossRef\]](#)
- Wang, H.; Wang, J.; Li, M.; Cao, Q.; Yu, M.; He, Y.; Wu, W. 823-mA/mm Drain Current Density and 945-MW/cm² Baliga's Figure-of-Merit Enhancement-Mode GaN MISFETs with a Novel PEALD-AlN/LPCVD-Si₃N₄ Dual-Gate Dielectric. *IEEE Electron Device Lett.* **2018**, *39*, 1888–1891. [\[CrossRef\]](#)
- Huang, S.; Jiang, Q.; Wei, K.; Liu, G.; Wang, X.; Zheng, Y.; Sun, B.; Zhao, C.; Liu, H.; Jin, Z.; et al. High-temperature low-damage gate recess technique and ozone-assisted ALD-grown Al₂O₃ gate dielectric for high-performance normally-off GaN MIS-HEMTs. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014; pp. 1741–1744. [\[CrossRef\]](#)
- Tang, Z.; Jiang, Q.; Lu, Y.; Huang, S.; Yang, S.; Tang, X.; Chen, K.J. 600-V Normally Off SiN_xSiN_x/AlGaIn/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse. *IEEE Electron Device Lett.* **2013**, *34*, 1373–1375. [\[CrossRef\]](#)
- Imada, T.; Motoyoshi, K.; Kanamura, M.; Kikkawa, T. Reliability analysis of enhancement-mode GaN MIS-HEMT with gate-recess structure for power supplies. In Proceedings of the 2011 IEEE International Integrated Reliability Workshop Final Report, South Lake Tahoe, CA, USA, 16–20 October 2011; pp. 38–41. [\[CrossRef\]](#)
- Anderson, T.; Wheeler, V.D.; Shahin, D.I.; Tadjer, M.J.; Koehler, A.D.; Hobart, K.D.; Christou, A.; Kub, F.J.; Eddy, C.R. Enhancement mode AlGaIn/GaN MOS high-electron-mobility transistors with ZrO₂ gate dielectric deposited by atomic layer deposition. *Appl. Phys. Express* **2016**, *9*, 71003. [\[CrossRef\]](#)
- Huang, S.; Liu, X.; Wang, X.; Kang, X.; Zhang, J.; Bao, Q.; Wei, K.; Zheng, Y.; Zhao, C.; Gao, H.; et al. High Uniformity Normally-OFF GaN MIS-HEMTs Fabricated on Ultra-Thin-Barrier AlGaIn/GaN Heterostructure. *IEEE Electron Device Lett.* **2016**, *37*, 1617–1620. [\[CrossRef\]](#)
- Han, P.-C.; Yan, Z.-Z.; Wu, C.-H.; Chang, E.Y.; Ho, Y.-H. Recess-Free Normally-off GaN MIS-HEMT Fabricated on Ultra-Thin-Barrier AlGaIn/GaN Heterostructure. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 427–430. [\[CrossRef\]](#)
- Mizue, C.; Hori, Y.; Miczek, M.; Hashizume, T. Capacitance-voltage characteristics of Al₂O₃/AlGaIn/GaN structures and state density distribution at Al₂O₃/AlGaIn interface. *Jpn. J. Appl. Phys.* **2011**, *50*, 021001-1-7.
- Toyoda, S.; Shinohara, T.; Kumigashira, H.; Oshima, M.; Kato, Y. Significant increase in conduction band discontinuity due to solid phase epitaxy of Al₂O₃ gate insulator films on GaN semiconductor. *Appl. Phys. Lett.* **2012**, *101*, 231607. [\[CrossRef\]](#)
- Huang, T.; Zhu, X.; Lau, K.M. Enhancement-Mode AlN/GaN MOSHFETs on Si Substrate with Regrown Source/Drain by MOCVD. *IEEE Electron Device Lett.* **2012**, *33*, 1123–1125. [\[CrossRef\]](#)
- Lu, X.; Ma, J.; Jiang, H.; Liu, C.; Xu, P.; Lau, K.M. Fabrication and Characterization of Gate-Last Self-Aligned AlN/GaN MISHEMTs With In Situ SiN_x Gate Dielectric. *IEEE Trans. Electron Devices* **2015**, *62*, 1862–1869. [\[CrossRef\]](#)

17. Huang, T.; Axelsson, O.; Malmros, A.; Bergsten, J.; Gustafsson, S.; Thorsell, M.; Rorsman, N. Low-Pressure-Chemical-Vapor-Deposition SiNx passivated AlGaIn/GaN HEMTs for power amplifier application. In Proceedings of the 2015 Asia-Pacific Microwave Conference (APMC), 6–9 December 2015; Institute of Electrical and Electronics Engineers (IEEE): Piscataway, NJ, USA, 2015; Volume 3, pp. 1–3.
18. Fleetwood, D.M.; Roy, T.; Shen, X.; Puzyrev, Y.S.; Zhang, E.X.; Schrimpf, R.D.; Pantelides, S.T. Oxygen-related border traps in MOS and GaN devices. In Proceedings of the 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology, Xi'an, China, 29 October–1 November 2012; Institute of Electrical and Electronics Engineers (IEEE): Piscataway, NJ, USA, 2012; pp. 1–4.

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