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Design Considerations of Series-Connected Devices Based LLC Converter

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Abstract: This paper describes the design of a Series-Connected Device based on a fixed–frequency LLC resonant converter (SCDLLC). Isolation of the dc-dc converter like the LLC resonant converter is used for the stability of the high voltage system such as a solid-state-transformer (SST). The series-connected devices driving method is one of the methods applicable to a high voltage system. When driving series-connected devices, an auxiliary circuit for voltage balancing between series-connected devices is required, which can be simply implemented using a passive element. In this paper, LLC converter design with balancing circuits configured in parallel with a device is provided, and both the simulations and experiments were performed.

Keywords: solid-state-transformer (SST); isolation dc-dc converter; LLC resonant converter; series-connected devices

1. Introduction

Recently, with new technologies such as smart grid and DC distribution, SST have emerged. SST connects directly to the grid instead of the traditional transformers to perform a variety of roles such as power factor correction and DC distribution. Therefore, SST should be able to cope with the high voltage of the grid, so that the various studies can be conducted [1–8]. To cope with high voltage, a multi-module converter (MMC) or a series-connected switching devices method has been studied. Figure 1 shows the difference between MMC and the series-connected device method.

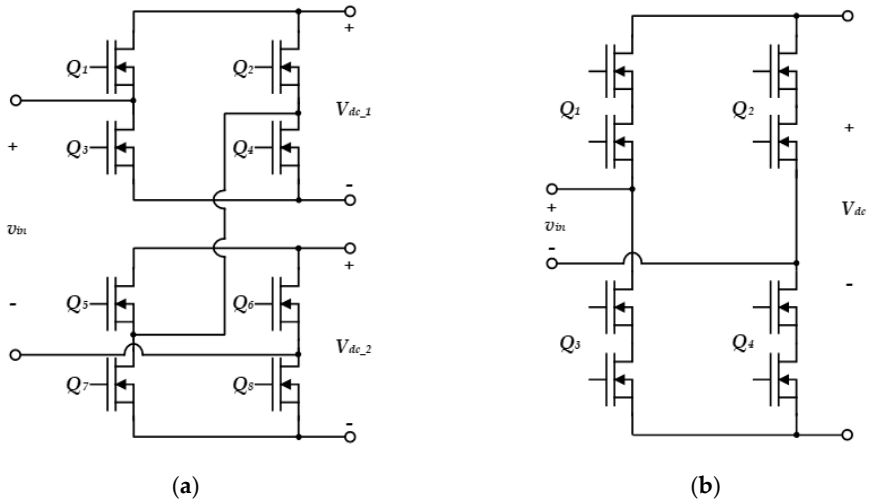


Figure 1. Comparison structure between MMC and the series-connected devices-based converter. (**a**) MMC; (**b**) series-connected devices-based converter.

MMC is a structure that increases the front of the circuit by stacking the circuit in series, which is relatively easy to expand, and has the advantage of reducing filter size by increasing the Power Conversion System (PCS) voltage level. But, since there is a separated DC link voltage, it is necessary to control and balance the separated DC link voltage. In addition, all individual devices should be controlled as the number of modules increases, which requires a digital computing device with many Pulse Width Modulation (PWM) channels. On the other hand, the series-connected devices behave like a single device, so even if many devices are connected in series, no digital computing device with many PWM channels is required. Furthermore, due to the series-connected devices, PCS does not have the separated DC link voltage. No additional control method is needed for DC link voltage balancing. On the other hand, because the output voltage level of series-connected devices based on PCS decreases, the filter size is larger than the MMC method. In addition, there is an issue with a switch voltage imbalance between the series-connected switches.

According to References [9–16], there are various reasons for causing a voltage imbalance. The first reason is the error of the gate driver. The gate driver is composed of various passive components and semiconductor devices like Negative, Positive, Negative (NPN) and Positive, Negative, Positive (PNP) transistors. Errors in devices of the gate driver cause an unbalance in the gate signal, which causes an imbalance in the voltage across the series-connected devices. The second reason is the error of parasitic components of the device itself. The error of the output capacitor of devices affects the switching speed and causes a voltage imbalance. The third reason is the parasitic capacitor from gate to ground of each device.

To solve voltage imbalance, various studies have been conducted [9–16]. In Reference [9], Active Gate Driver using Field Programmable Gate Array (FPGA) with RCD (Resistor, Capacitor and Diode) snubbers across each device method for balancing was proposed and tested. In the documents, the three-phase half-bridge inverter was built in 12-series connected Insulated Gage Bipolar Transistor (IGBT) and verified at a rated current within ±10 kV DC-link. In Reference [12], an active gate driver using a current mirror with a steady-state balancing resistor was proposed and performed. The steady-state voltage imbalance is reduced by the balancing resistor, and the transient imbalance was solved by the analog gate controller used a current mirror. In Reference [14], the voltage balancing method with only passive components using a single gate driver unit was proposed. In the documents, experimental verifications were applied to the DC circuit breaker with a 1.2 kV bus voltage. It was confirmed that it is possible to cope with the high voltage system by using a series connection element applied to various methods.

In a high voltage system, like SST, isolated converters are needed to increase the stability of the system and grid. Isolated converters are one of the necessary converters for SST regardless of MMC or series-connected devices. There are many types of isolated converters such as Dual-Active-Bridge (DAB), Quad-Active-Bridge (QAB), and LLC Converter. A fixed-frequency resonant converter conducts zero voltage switching (ZVS) over a wide frequency range and provides the advantages of high efficiency and high-power density.

In this paper, fixed-frequency LLC resonant converter-based series-connected devices is proposed. In order to cope with a high voltage, a series-connected device based on PCS was applied and an R-C snubber was applied to solve the voltage imbalance between series-connected devices. In conclusion, this paper examined the effect of R-C snubber applied to the LLC converter to solve the voltage imbalance. The proposed converter consists of a full-bridge inverter. Unlike the usual full-bridge converter, the proposed converter consists of eight devices, as shown in Figure 1b. The operation of the SCDLLC converter with a balancing circuit is described. This paper is structured as follows. In Section 2, imbalance factors of series-connected devices are described and a balancing method using passive elements is expressed. In Section 3, a configuration method of the LLC converter considering series-connected devices is explained. In Sections 4 and 5, a 3-kW prototype model is manufactured to verify the usefulness of the proposed system and the simulations and experiments are performed. Lastly, in Section 6, we discuss experimental results and conclude the paper.

2. Design of Series-Connected Devices Balancing Circuit

Figure 2 depicts the series-connected device with various factors that cause a voltage imbalance. Gate signal mismatch can occur due to an error of the device's parasitic capacitor, unbalance of the gate signal due to a gate pattern, and an error of the parasitic capacitor from gate to ground, which causes an unbalance of voltage across the device. Furthermore, the voltage imbalance of devices increases the stress and can cause damage to the device. In this section, in order to prevent damage to the device, the voltage balancing method of the series-connected devices was analyzed using passive components.

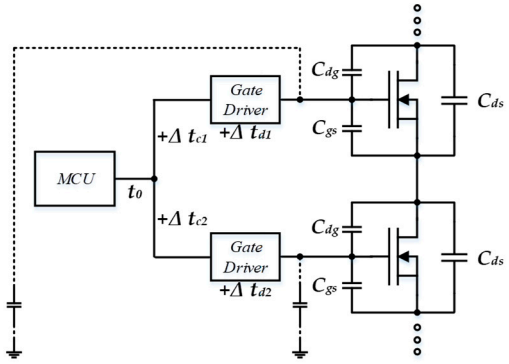


Figure 2. Voltage imbalance factors in series-connected devices.

Passive snubbers implemented by passive devices (C, RC, RCD, etc.) are used for voltage balancing circuits. Voltage imbalance of devices is somewhat limited by placing the passive snubber circuit between drain to source. The use of passive snubber circuits reduces the switching speed of devices and the voltage imbalance due to a gate signal imbalance. Figure 3 shows series-connected devices with passive balancing circuits. The snubber circuit composed of a steady-state balancing resistor (R_{bal}) and a transient state balancing capacitor (C_{snub}, R_{damp}).

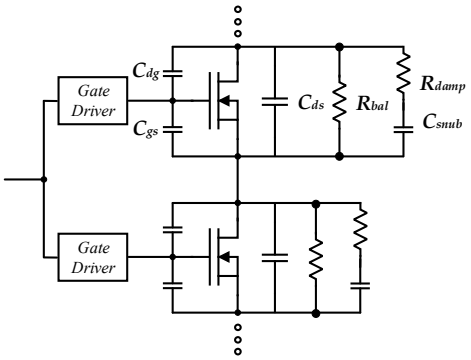


Figure 3. Structure of voltage balancing circuits in series-connected devices.

The steady-state balancing resistors operate when the switch is fully turned-off. If the steady-state balancing resistors are small, the devices are well balanced. However, the power dissipation of balancing resistors increased, which requires the use of higher-rated resistors. Conversely, If the balancing resistors are big, the power dissipation of balancing resistors decrease. However, there is a high probability that voltage balancing between series-connected devices will fail. Therefore, when designing the balancing resistor, the leakage current of the device should be considered. Steady-state resistance are calculated below.

$$\frac{v_{ds}}{10 \times i_{leakage\_max}} < R_{bal} < \frac{v_{ds}}{10 \times i_{leakage\_min}} \quad (1)$$

The transient state balancing circuit (C_{snub}, R_{damp}) operates when the switch is a turn-on state and a turn-off state. C_{snub} is selected considering the parasitic capacitor of the device. To avoid imbalance by parasitic capacitor errors of the devices, attach a balancing capacitor with negligible parasitic capacitors of a device. If snubber capacitance is big, voltage unbalance during the transient will be stabilized, but switching speed will decrease and switching loss will increase. If the snubber capacitance is small, the snubber capacitors cannot perform proper balancing. R_{snub} works as a damping resistor. The inrush current of the snubber capacitor at the switching state is limited by R_{snub}. Therefore, R_{snub} is selected by the current rating of the snubber capacitor. In addition, when calculating the R_{snub} value, a time constant ($\tau = RC$) and switching frequency (f_{sw}) should be considered. A large time constant reduces the switching speed, increases switching losses, and also hinders soft switching of the LLC converter.

3. Design of LLC Converter

Figure 4 depicts the series-connected SiC MOSFETs LLC Converter with voltage balancing circuits. Generally, the output capacitance of the switching device should be considered in the design process. However, in this case, Snubber capacitors are added in parallel with the series-connected devices for voltage balancing. The output capacitor should be discharged during deadtime for a sufficient Zero Voltage Switching (ZVS) effect. Therefore, the snubber capacitor should be considered when designing an LLC converter. Except for the snubber capacitor, the others process of the designed LLC converter are followed by the general LLC converter design process in References [17,18].

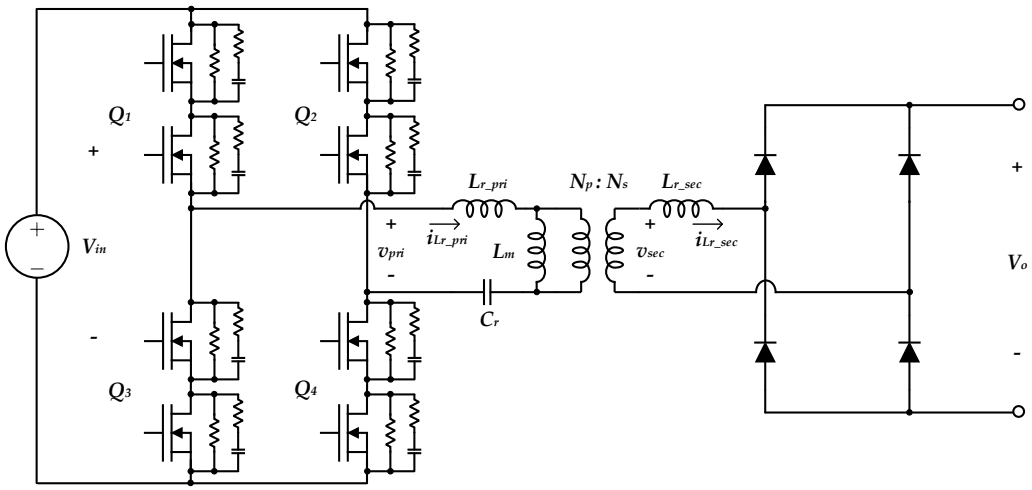


Figure 4. Series-connected devices-based LLC Converter with a voltage balancing circuit.

Figure 5 shows theoretical waveforms of the conventional LLC converter. For simplifying it to analyze, some assumptions are made as follows.

- There is no error of parasitic elements of a switching device;
- Gate drivers are all ideal, and there is no time delay between series-connected devices due to the gate driver.

The gate signals of devices are off during the deadtime (t_{dead}) interval. The magnetizing current and resonant current become the same during the deadtime. During the deadtime, inductor current flows through the antiparallel diode of the switch and discharges the parasitic output capacitor of the switch. Then, the switch turns on after zero voltage is formed by the discharged output capacitor so that soft switching is possible. The equation of minimum deadtime and magnetizing inductance for soft switching is calculated below.

$$t_{dead} \geq 16 C_{oss} f_{sw} L_m \quad (2)$$

Equation (2) represents that the ZVS is related to the magnetizing inductance of the high frequency transformer (HF transformer) and the output capacitance of the switch. As mentioned in the previous section, Snubber capacitors are required for voltage balance between series-connected devices. Therefore, when manufacturing the LLC converter with balancing circuits that are connected in parallel to each device, balancing circuits should be considered. This is not a parasitic component of the switch. After that, the rest process design of an LLC converter follows the conventional design process.

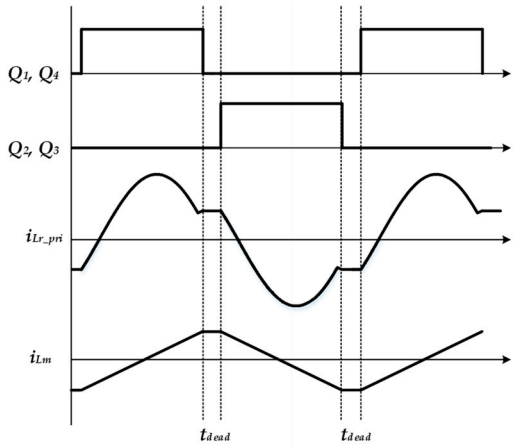


Figure 5. Switching state and resonant (i_{Lr_pri}), magnetizing current (i_{Lm}) of the transformer.

Figure 6 shows the equivalent circuit of an LLC converter. To design LLC, the converter is described as follows [3–9].

$$n = \frac{N_p}{N_s} \tag{3}$$

$$m = \frac{L_r + L_m}{L_r} \tag{4}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{5}$$

$$F_x = \frac{f_{sw}}{f_r} \tag{6}$$

$$R_{ac,\,min} = \frac{8}{\pi^2}\cdot\frac{N_p^2}{N_s^2}\cdot R_o \tag{7}$$

$$Q_{max} = \frac{\sqrt{L_r/C_r}}{R_{ac,min}} \tag{8}$$

where N_p and N_s means the turn ratio of the transformer and R_o is the load resistance. Furthermore, f_{sw} is the switching frequency, f_r is the resonant frequency, and the R_{ac} is the reflected load resistance. Therefore, the voltage gain of the resonant tank is defined below.

$$K = \left|\frac{V_{o\_ac}(s)}{V_{in_{ac}}(s)}\right| = \frac{F_x^2(m-1)}{\sqrt{\left(m\cdot F_x^2 - 1\right)^2 + Fx^2\left(F_x^2-1\right)^2(m-1)^2Q^2}} \tag{9}$$

where V_{o_ac} (s), V_{in_ac} (s), Q, m, and F_x are the v_{in_ac}, v_{o_ac}, the quality factor, the ratio of the total primary inductance to resonant inductance, and the normalized switching frequency, respectively. Figure 7 shows voltage gain according to different m and Q factors. In the figure, as the m factor decreases, the voltage conversion ratio is extended. However, according to Equation (4), a low m factor requires low magnetizing inductance L_m. Thus, magnetizing current increases. It means that the conduction loss of magnetic components is increased. In terms of the Q factor, the Q factor is related to the load. The high

Q value means heavy load conditions and the low Q value means light load conditions. Therefore, it is important to set the Q value at the rated load. Thus, a voltage gain of an LLC converter is related to m and Q factors.

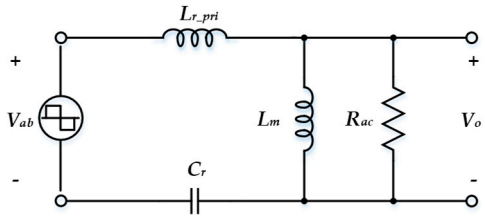


Figure 6. Equivalent circuit of the LLC resonant tank.

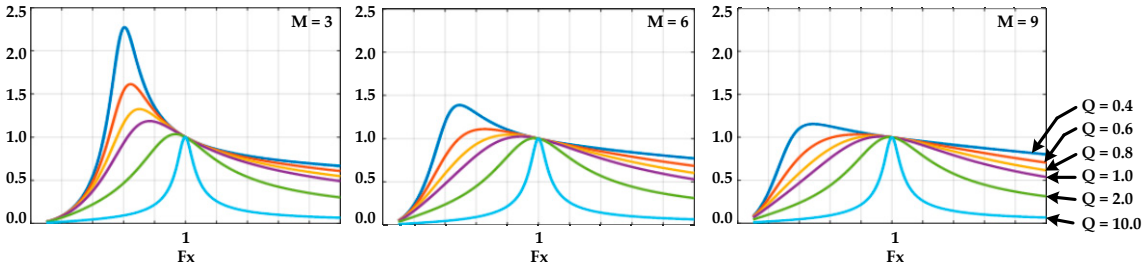


Figure 7. Voltage gain according to different m and Q factors.

4. Simulations and Simulation Results

In order to verify the series-connected devices-based LLC converter, simulation was conducted by Power Sim (PSIM) and Linear Technology spice (LTspice).

4.1. Voltage Balancing Simulation

Figure 8 shows the simulation circuit of voltage balancing. Table 1 shows the parasitic value of components of experiment setup and Table 2 shows the parasitic value of device itself. Voltage balancing simulation was performed by LTspice. Parasitic values of devices were added arbitrarily, and voltage balancing simulation was performed depending on whether the snubber circuit was used.

Table 1. Parameters of the voltage balance test circuit.

Parameters	Values
Input voltage (V_{IN})	1000 V
Gate driver parasitic inductance (L_{g1})	1 pH
Gate driver parasitic inductance (L_{g2})	1.2 pH
Parasitic output capacitance (C_{oss_1})	170 pF
Parasitic output capacitance (C_{oss_2})	100 pF
Inductor (L)	3 mH
Voltage balancing resistor (R_{bal})	1 MΩ
Damping resistor (R_{snub})	5 Ω
Voltage balancing circuits capacitor (C_{snub})	1 nF

Table 2. Parameter of the selected device (C2M0040120D).

Parameters	Minimum	Type	Maximum
Leakage current	x	1 μA	100 μA
Output capacitance		150 pF	

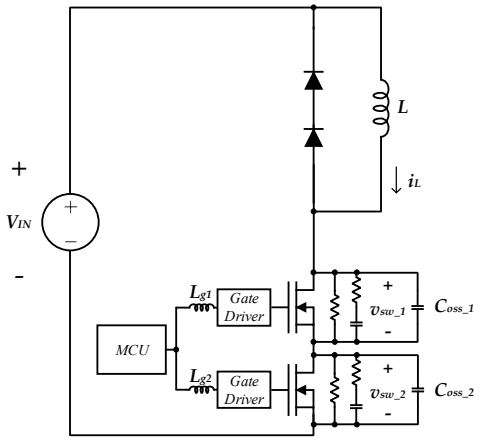


Figure 8. Multi-pulse test circuit for voltage balancing simulation.

Figure 9 shows the simulation results with and without balancing circuits. Without balancing circuits, simulation results show that the voltage balancing between series devices did not converge, and the voltage imbalance increased as the inductor current increased. On the other hand, with balancing circuits, voltage imbalance is somewhat reduced, and the imbalance range is maintained even with the increased inductor current.

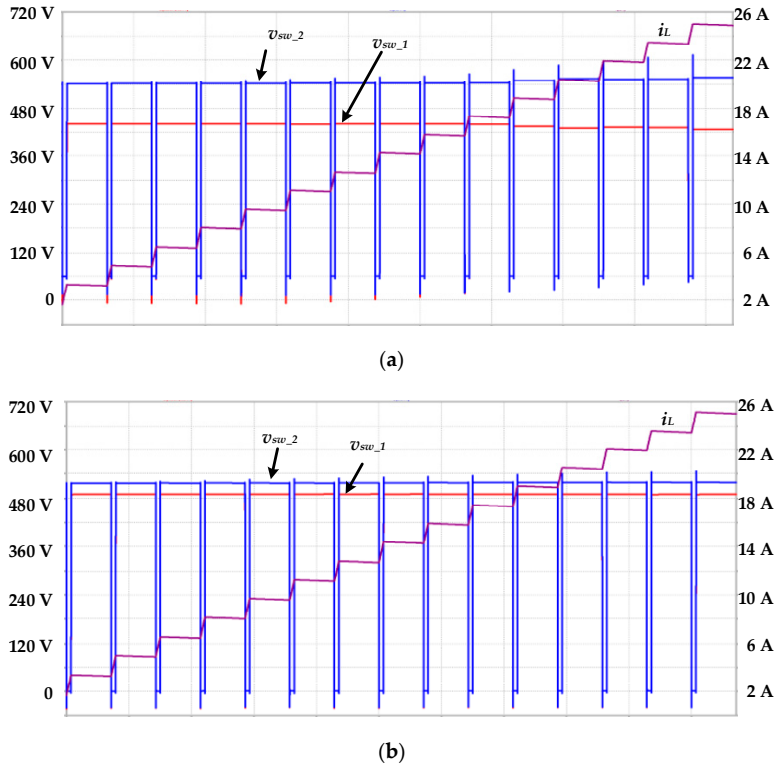


Figure 9. Multi-pulse test simulation result: (**a**) without balancing circuits and (**b**) with balancing circuits.

4.2. LLC Converter Simulation

The LLC converter simulation was conducted on the assumption that voltage imbalance did not occur. The simulation model is shown in Figure 10. Table 3 gives the parameters of the system. An isolated HF transformer can be described as an ideal transformer, magnetizing inductance, and leakage inductance in simulation. In Figure 10, the model of the HF transformer of the LLC converter consists of magnetizing leakage inductance and an ideal transformer, which has a 10:4 transfer ratio. L_m means the magnetizing inductance of the fabricated HF transformer. L_{r_sec} means the secondary

side leakage inductance of the HF transformer. L_{r_pri} means the primary side leakage inductance of the HF transformer, which is the sum of the leakage inductance of the HF transformer itself and the added inductance on the outside. In addition, C_r means the resonant capacitor. Resonant capacitors work as a resonant tank with L_{r_pri}. Therefore, the resonant frequency of the LLC converter is determined by the resonant capacitor and the primary leakage inductance of the transformer. Figure 11 shows the voltage gain curve according to the load of the proposed converter.

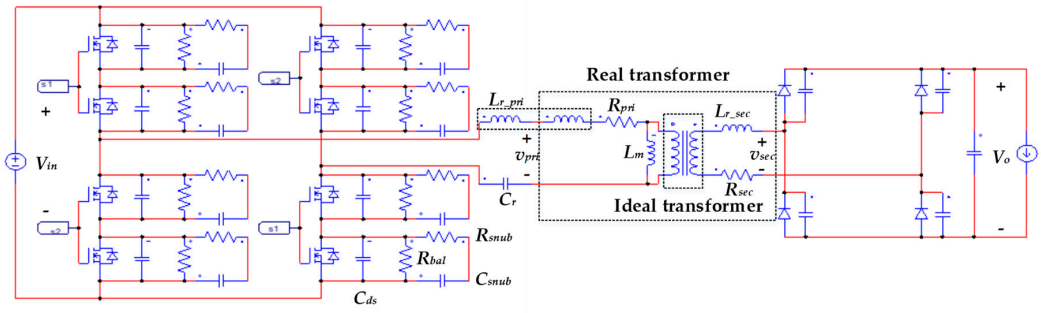


Figure 10. Simulation circuit of series-connected devices based on the LLC converter with a voltage balancing circuit.

Table 3. Parameters of simulation.

Parameters	Values
Input voltage (V_i)	1000 V
Output voltage (V_o)	400 V
Power	3000 W
Resonant frequency (f_r)	100 kHz
Switching frequency (f_{sw})	100 kHz
HF transformer turn ratio (primary: secondary)	10:4
Primary leakage inductance (L_{r_pri})	129 µH
Primary resonant capacitor (C_r)	20 nF
Magnetizing inductance (L_m)	302 µH
Secondary leakage inductance (L_{r_sec})	2.598 µH
Primary resistance (R_{pri})	0.135 Ω
Secondary resistance (R_{sec})	0.110 Ω
Deadtime	500 ns

Figures 12 and 13 show the simulation results of the LLC converter. Figure 12 shows the switching voltage and channel current of the MOSFETs. In the figure, v_{ds_Q1}, v_{ds_Q2}, v_{ds_Q3}, and v_{ds_Q4} represents the drain to source voltages and i_{Q1}, i_{Q2}, i_{Q3}, and i_{Q4} represents the current of devices. In the figure, the channel currents increase after the devices are fully turned on. It means ZVS is achieved. Figure 13 shows the input/output voltage and the current of the HF transformer.

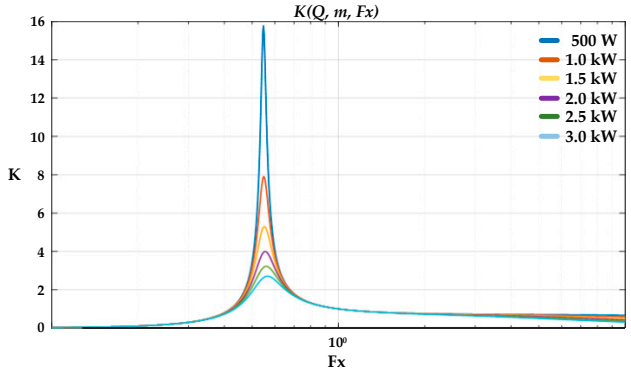


Figure 11. Voltage gain graph of the LLC converter according to a different load.

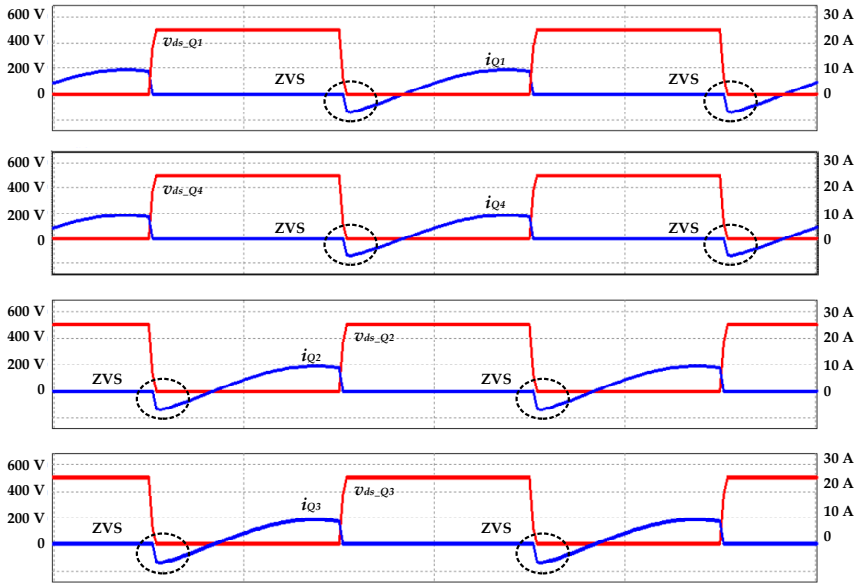


Figure 12. Switching waveform of the drain-source voltage and MOSFET current of the LLC converter.

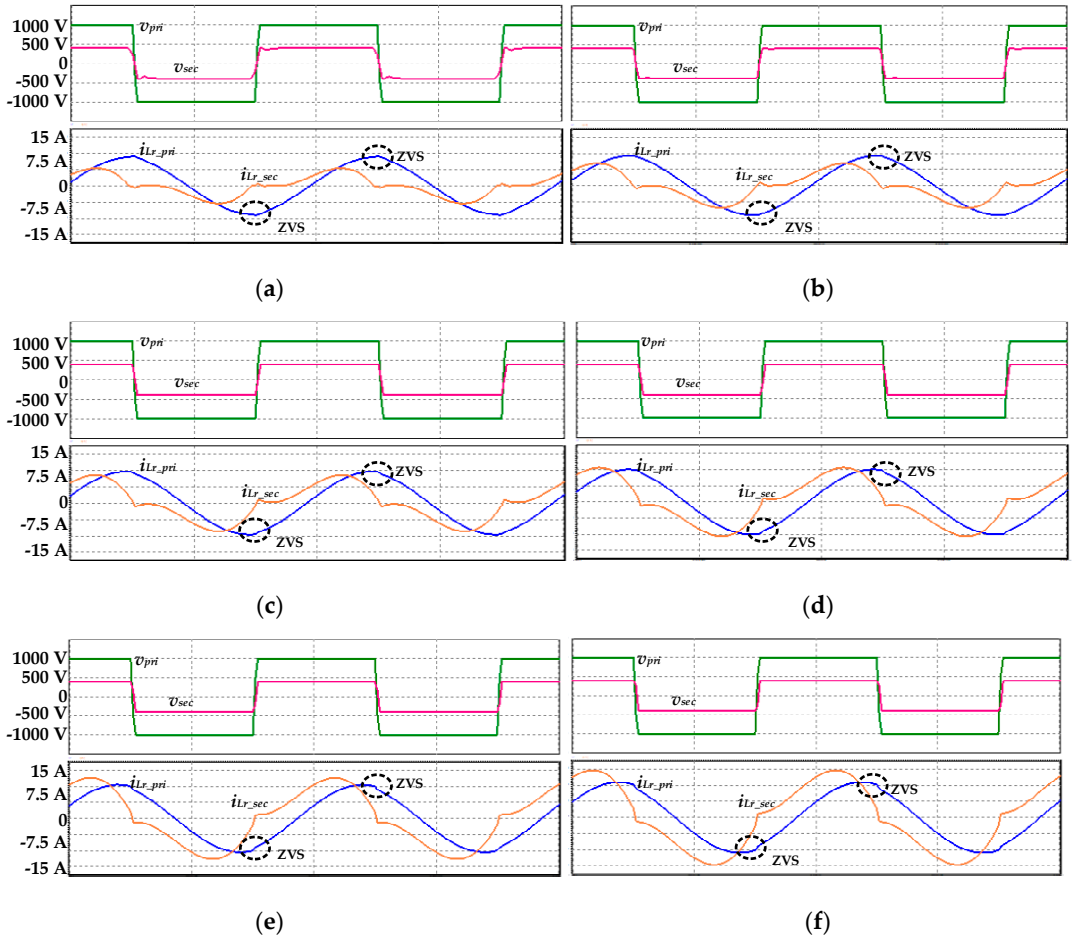


Figure 13. Simulation results of the input voltage v_{pri} and output voltage v_{sec} of the transformer and resonant current of the primary side i_{Lr_pri} and secondary side i_{Lr_sec}: (**a**) simulation at 500 W, (**b**) simulation at 1000 W, (**c**) simulation at 1500 W, (**d**) simulation at 2000 W, (**e**) simulation at 2500 W, and (**f**) simulation at 3000 W.

5. Experiments and Experimental Results

The proposed circuit verified by simulation was tested through experiments. Figure 14 shows the experimental configuration of the proposed LLC converter using a 1200-V SiC MOSFET (C2M0040120D, Cree) and 1200-V SiC Schottky Diode (C4D20120D, Cree). Experimental specifications are shown in Table 3. Before the verification of series-connected devices based on an LLC converter, a multi-pulse test is conducted to verify voltage balancing between series-connected devices.

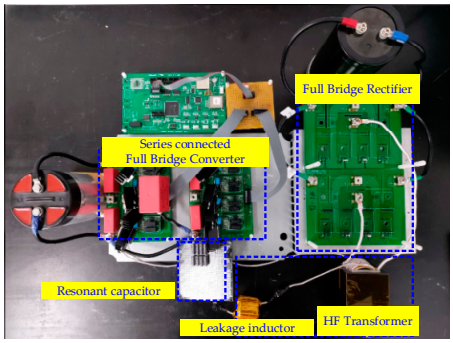
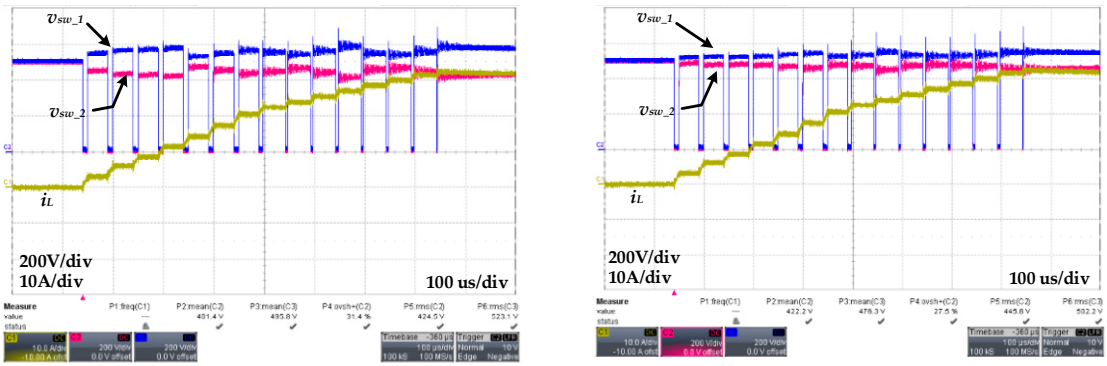


Figure 14. Hardware configuration for a series-connected LLC converter.

5.1. Voltage Balancing Experiment

Voltage imbalance was tested through a multi-pulse test. The experimental setup is shown in Figure 8. The experiment parameters are represented in Table 1.

Figure 15 shows the experimental results without balancing circuits and with balancing circuits. Compared with the simulation results, the trend tends to be different. In the simulation, the factor of voltage imbalance reflects the unbalance of the device's parasitic and the delay of the gate signal. However, according to Reference [12], the parasitic capacitor from gate to ground one of the important factors contribute to a voltage imbalance. In addition, this factor was not reflected in the simulation. Although practical experiments, with the parasitic capacitors considered from gate to ground, the voltage imbalance converges to a steady state through snubber circuits selected by simulation. It means that, if the unbalance voltage does not exceed the rated voltage of the switch, the switch can be regarded as a stable operation with selected balancing circuits by simulation.



(**a**) (**b**)

Figure 15. Experimental results of the voltage imbalance test: (**a**) without balancing circuits and (**b**) with balancing circuits.

5.2. Double Pulse Test

As mentioned in the previous section, an added snubber circuit for voltage balancing slows down switching speed and increases switching loss. In this section, a Double Pulse Test (DPT) was conducted

to analyze switching losses with and without snubber circuits. The experimental setup is shown in Figure 16 and parameters are shown in Table 4. Balancing snubber parameters are shown in Table 1.

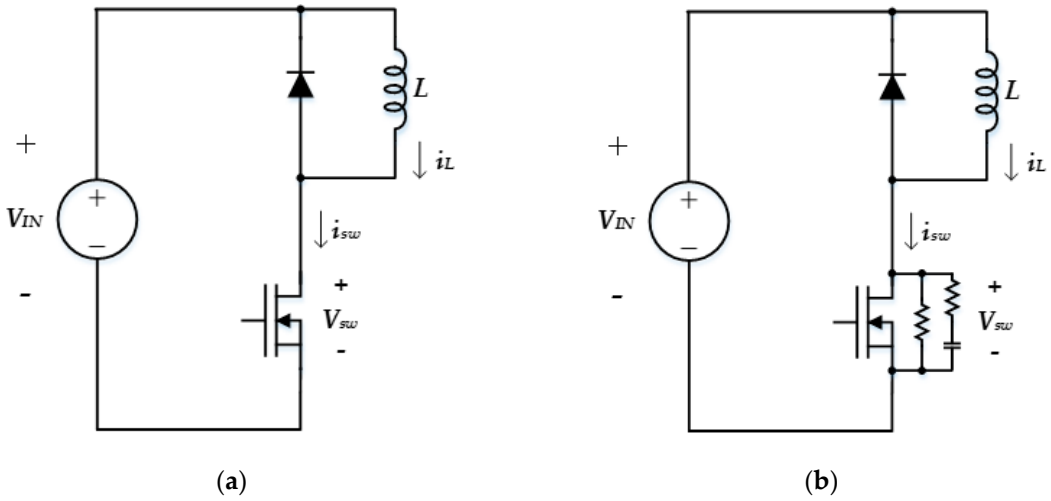


Figure 16. Double pulse test circuits: (**a**) without balancing circuits and (**b**) with balancing circuits.

Table 4. Parameters of the double pulse test.

Parameters	Values
Input voltage (V_{IN})	500 V
Inductor (L)	1.5 mH

DPT was conducted when the DC-link is 500 V. Figure 17 shows DPT results. According to Figure 17, both turn-on and turn-off losses increased with snubber circuits. However, the proposed LLC converter operates ZVS turn-on at all loads. The turn-on loss can be negligible.

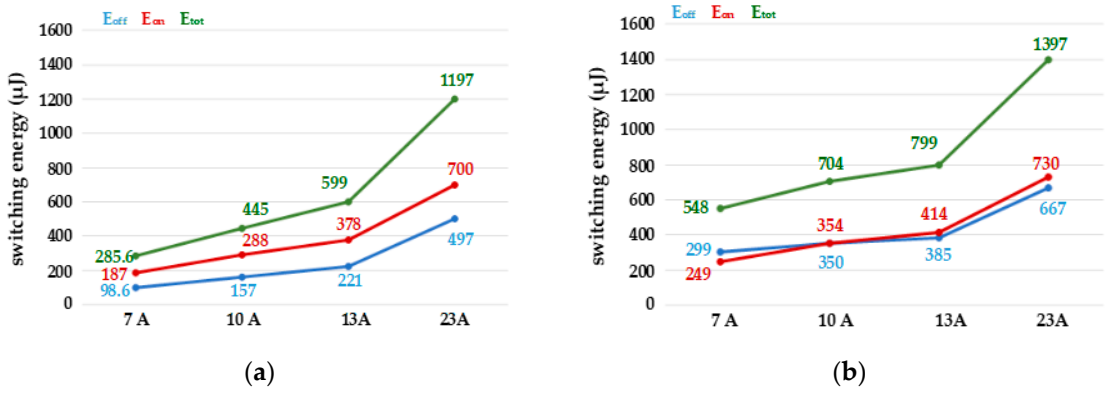


Figure 17. Switching loss comparison according to the switch current: (**a**) without balancing circuits and (**b**) with balancing circuits.

5.3. LLC Converter Experiment

Based on the balancing circuit's value selected through simulations and a multi-pulse test, the series-connected devices based on the LLC converter experiment was conducted. Figure 18 shows the main waveforms of the proposed LLC converter according to the load. In the figure, v_{pri} and v_{sec} represent input/output voltage of the HF transformer, i_{Lr_pri} and i_{Lr_sec} represent input/output current of the HF transformer, according to the load. As shown in the previous section, experimental results were well matched with simulation results.

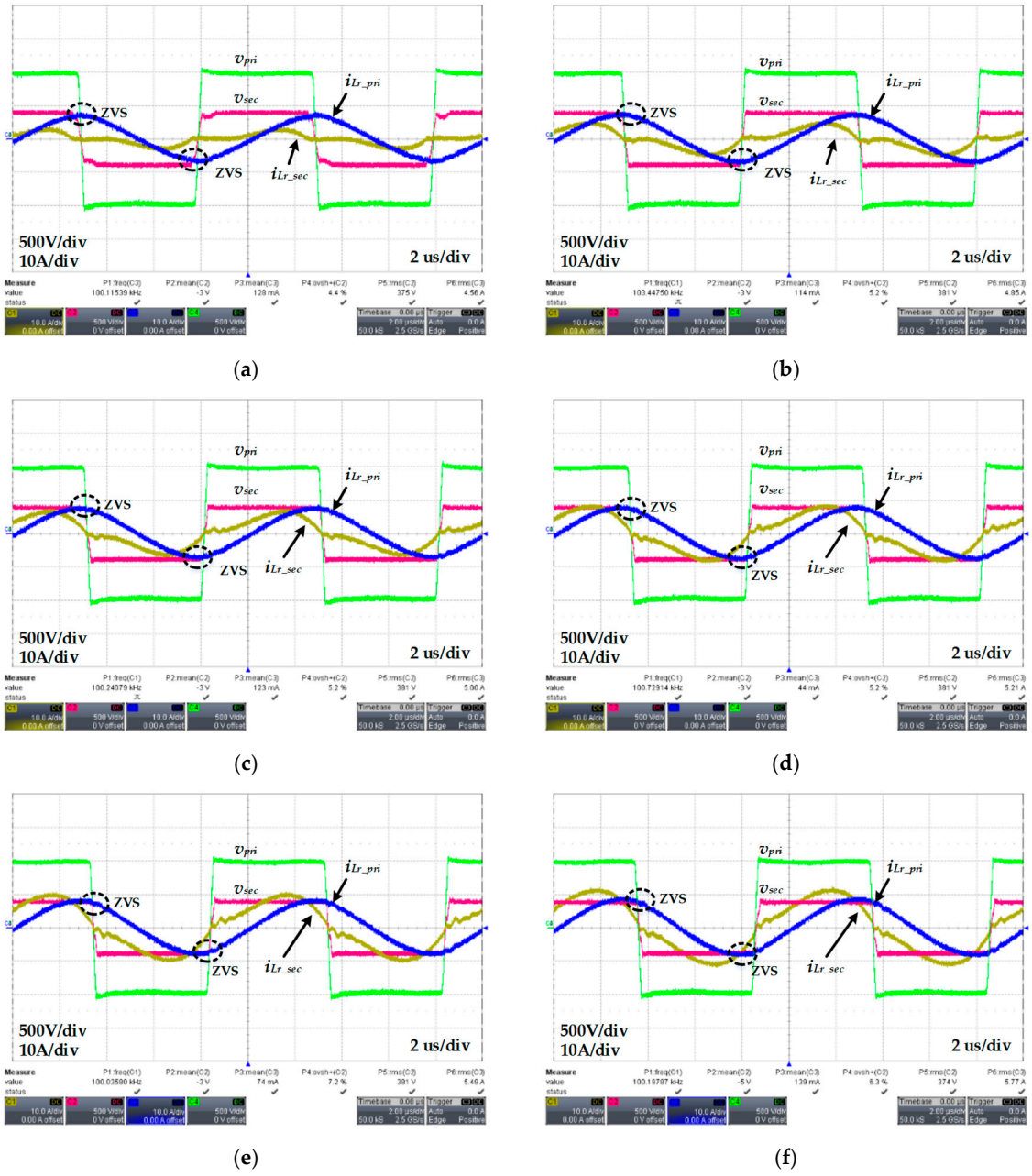


Figure 18. Experimental results of the input voltage v_{pri} and output voltage v_{sec} of transformer and resonant current of the primary side i_{Lr_pri} and the secondary side i_{Lr_sec}. (**a**) Simulation at 500 W, (**b**) simulation at 1000 W, (**c**) simulation at 1500 W, (**d**) simulation at 2000 W, (**e**) simulation at 2500 W, and (**f**) simulation at 3000 W.

Figure 19 shows v_{qs_1}, v_{qs_2}, and v_{gs} at the rated power. v_{qs_1}, v_{qs_2} represent the drain to source voltage of each device connected in series at the rated power. Voltage balancing between series-connected devices did not diverge, and both switches connected in series had achieved ZVS operation. Figure 20 shows the efficiency of series-connected devices-based LLC converter. The maximum efficiency was measured at the rated load.

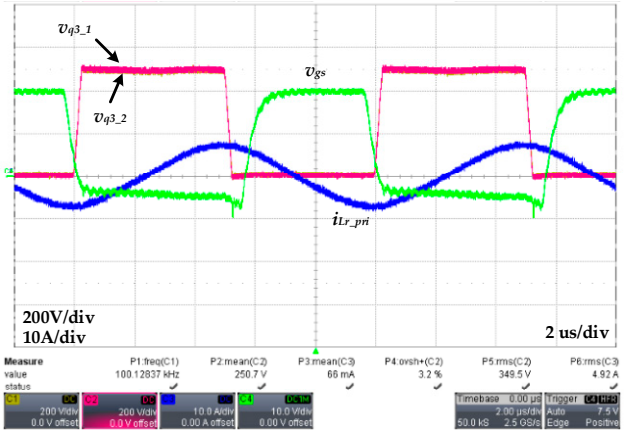


Figure 19. Experimental results of series-connected devices voltage v_{q3_1}, v_{q3_2}, and v_{gs} at the rated load.

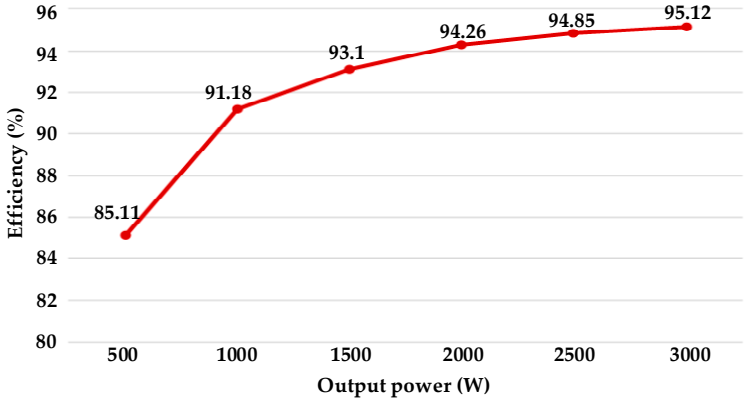


Figure 20. Efficiency of series-connected devices-based LLC converter.

6. Conclusions

This paper describes the design consideration of the fixed frequency LLC converter considered balancing circuit of series-connected devices circuit. In the introduction, the reason for the imbalance voltage across the series-connected devices was described and discussed the need of an LLC converter. The proposed converter consists of a series-connected devices-based LLC converter.

In order to verify the proposed converter, a series-connected devices-based voltage balancing experiment and the series-connected devices-based LLC converter was performed. The snubber circuit, which is the simplest method among the various methods for voltage balancing, was applied and the switching loss comparison and voltage balancing test was performed according to snubber circuits. Furthermore, based on the snubber circuits-designed simulation and experiments, 3 kW series-connected devices-based LLC converter was fabricated and verified. Through the experiments, the voltage balancing between series-connected devices and soft switching operation of the proposed converter are verified. The efficiency of a fabricated converter was measured 95.12% at 3 kW load. When the series-connected based LLC converter is fabricated with balancing snubber circuits, it is confirmed that the LLC converter design is necessary considering the balancing snubber, and the experimental results confirm that the consideration is valid.

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