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Five-Level T-type Cascade Converter for Rooftop Grid-Connected Photovoltaic Systems

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Abstract: Multilevel converters are widely considered to be the most suitable configurations for renewable energy sources. Their high-power quality, efficiency and performance make them interesting for PV applications. In low-power applications such as rooftop grid-connected PV systems, power converters with high efficiency and reliability are required. For this reason, multilevel converters based on parallel and cascaded configurations have been proposed and commercialized in the industry. Motivated by the features of multilevel converters based on cascaded configurations, this work presents the modulation and control of a rooftop single-phase grid-connected photovoltaic multilevel system. The configuration has a symmetrical cascade connection of two three-level T-type neutral point clamped power legs, which creates a five-level converter with two independent string connections. The proposed topology merges the benefits of multi-string PV and symmetrical cascade multilevel inverters. The switching operation principle, modulation technique and control scheme under an unbalanced power operation among the cell are addressed. Simulation and experimental validation results in a reduced-scale power single-phase converter prototype under variable conditions at different set points for both PV strings are presented. Finally, a comparative numerical analysis between other T-type configurations to highlight the advantages of the studied configuration is included.

Keywords: grid-connected photovoltaic systems; cascade multilevel converters; multistring converters; T-type converters

1. Introduction

Rooftop photovoltaic (PV) energy conversion systems (less than 20 kW), have become a well-established technology in the industry. The most common configurations for single-phase grid-connected PV systems commercially found are the string, multistring and ac-module integrated topologies. Central and string inverters have been widely applied to manage and control PV energy systems [1]. Among the string topologies, the transformerless H5, H6, HERIC, neutral point clamped (NPC) and T-type NPC converters have been successfully commercialized [2]. In fact, multilevel inverters (MLI) are designed to produce a stepped voltage waveform by reducing the Total Harmonic Distortion (THD) and the voltage stress across semiconductor devices. Secondly, reduction of the

output filter size and power footprint also permit an important improvement in terms of costs, weight and efficiency [3]. These technical features have led to the massive adoption of MLI over the last thirty years for high-power medium voltage (MV) motor drive applications. In the last years, three-level neutral point clamped (3L-NPC) converters have been used for interfacing PV systems into the grid, where a higher PV incorporation has brought substantial concerns on power efficiency, power quality and grid code compliance [1] as well as power grid services [4].

T-type neutral point clamped inverters (3L-TNPC), also known as neutral point piloted converters (3L-NPP), [5] have gained a wide presence in the industry sector due to several advantages as symmetrical loss distribution, higher overall efficiency, small footprints [6] and low harmonic injection in relation to the conventional 3L-NPC [7]. In fact, many manufactures such as Fuji, On Semiconductor, Mitsubishi and Semikron have commercial T-type legs used in central PV inverters and motor drive applications [8–10]. For the three-level inverter, based on the T-type leg, was presented thirty-five years ago for motor drives, with the bidirectional medium switch being realized with thyristors and improved with GTO-thyristors [11]. After some years, many configurations based on the well-known three-level T-type NPC leg can be found in the literature [12]. In [13] a five-level TNPC (5L-TNPC) was introduced, which corresponds to the parallel connection of two 3L-TNPC legs [14,15]. Furthermore, a variation of this configuration with reduced switches, also known as five-level hybrid T-type NPC (5L-HTNPC), was presented in the recent literature [16]. This topological variation is built with a 3L-TNPC leg and a two-level leg inverter, forming a five-stepped voltage waveform in the AC terminals.

In the literature there are two main possibilities for increasing the number of levels in the power converter field, which is by increasing the internal DC capacitors connected to a single DC source or by connecting several converters in the series at the AC side, in which each converter has an independent DC source. Focusing on the second alternative, cascade MLI can be developed by using symmetrical or asymmetrical voltage levels and by using different type of topologies such as: Full H-Bridge, 3L-TNPC converters or by performing a hybrid configuration [17]. Note that symmetrical cascade configurations have had a more industrial presence as the case of Cascade H-Bridge (CHB) converters [3] due to modulation and control simplicity compared with asymmetrical configurations [18]. In fact, in [19] a symmetrical nine-level T-type converter (9L-TNPC) is presented for motor drive applications, which is based on the cascade connection of two 5L-TNPC converters. The same number of levels can be generated with advanced hybrid topologies as presented in [6,12].

Considering the advantages and features previously presented regarding the 3L-TNPC and symmetrical cascaded configurations, this paper described and validated the 5L-CTNPC topology for rooftop PV applications by using a cascaded connection of two 3L-TNPC legs which was firstly introduced in [20] as a cascade 3L-TNPC converter. Thus, the advantages of symmetrical cascade configurations with multistring inputs are merged. Each 3L-TNPC converter can interface a dedicated DC bus, and consequently two separate maximum power point tracking (MPPT) algorithms are allowed to obtain the maximum power of each PV string. Note that the PV string of each module can be sized to handle half the entire PV string in the conventional 3L-TNPC converter, providing better MPPT efficiency since less modules are combined in a series per string. The main contribution of this paper is the experimental validation of a simplified control scheme to alleviate the power unbalancing mismatch between 3L-TNPC modules and to compensate capacitor voltage variations per each converter, which was presented earlier in [20]. Furthermore, a brief comparison between five-level voltage waveform converters based on the conventional 3L-TNPC is performed as a second contribution in terms of the main electrical features.

The rest of the document is organized as follows. In Section 2, a hardware description of the proposed converter, switching states and implemented modulation is presented. In Section 3, a simple stationary reference-frame voltage-oriented control and a voltage control loop to compensate a possible power unbalance operation are included. Then, in Section 4, simulation results and experimental verification of the proposed multilevel converter and its control system behavior are

added. Furthermore, a brief comparison with the 5L-TNPC and 5L-HTNPC is performed to highlight the main advantages of the proposed configuration. Finally, in Section 5, the conclusions of the paper summarize the work done.

2. The 5L-CTNPC Converter Topology

The power topology of the analyzed cascade 5L-CTNPC for a rooftop grid-connected PV system is depicted in Figure 1. The configuration is composed of a series connection of two 3L-TNPC legs, where each of them is built with two conventional IGBTs and one bidirectional switch. This bidirectional switch could be formed either by two conventional IGBTs in common-emitter or by a common-collector and reverse blocking IGBT connection. Actually, a classical IGBT semiconductor structure could be replaced by a reverse blocking MOSFETs for a high-voltage [21] and high-switching frequency operation [22]. Although more than two cells in a series connection are conceptually feasible, for the sake of simplicity, two-cell 3L-TNPC converters have been introduced as a proof-of-concept applied to conventional string rooftop PV applications.

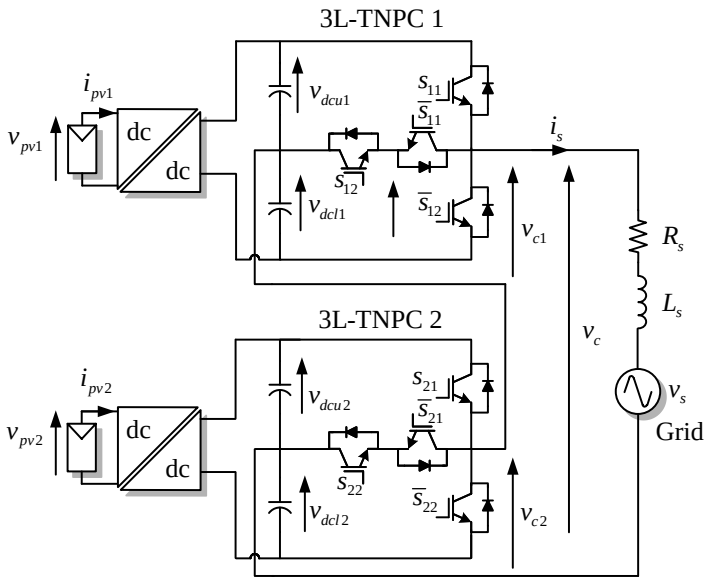

Figure 1. Proposed 5L-CTNPC power topology.

Each 3L-TNPC leg operates as a string inverter connected to a single potential-induced degradation converter which is fed by one PV string. This potential-induced degradation stage can be designed to boost the DC voltage and perform the MPPT. Furthermore, it could be isolated [23] to avoid leakage currents due to the PV aluminium metallic frame grounded [1]. To reduce leakage currents paths and avoid high-frequency transformers there are three successful options well-documented in the literature: Changing the modulation stage to avoid switched common mode [16], by reducing surface conductivity of PV modules to avoid potential-induced degradation (PID) and by including extra switches between the PV array and the inverter, also well-known as transformerless inverters [24]. Although, a potential-induced degradation stage is desired to provide an independent DC voltage control, in this work, the validation of the proposed configuration does not integrate a potential-induced degradation stage, giving place to the worst case scenario under study where the MPPT control is fulfilled directly from each 3L-TNPC power cell, instead of using a high frequency galvanic isolated converter with its appropriate MPPT control. Thus, the overall control loops are more challenging since the voltage fluctuations in the PV panel is directly presented in the DC-side of each 3L-TNPC module, i.e., $v_{dck} = v_{pvk}$, where $k = \{1, 2\}$ is given by the number of cell. Furthermore, in order to extract the maximum power from the PV panels, an integration of an external

MPPT algorithm is required so as to define the appropriate DC voltage reference in each cell. Note that the proposed topology is modeled without affecting the basic control objectives.

2.1. Fundamental Principle of the 5L-CTNPC

The 3L-TNPC provides three-output voltage levels: $v_{dck}/2$, 0 and $-v_{dck}/2$, where k is the cell or module number. These voltage steps are generated by connecting the AC terminals to the positive, neutral and negative pole of the DC-link terminals. Although, the 3L-TNPC configuration gives rise to four switching states, in order to avoid a short-circuit to the DC side there are only three of them possible. The cascade connection of two 3L-TNPC cells permits the generation of five voltage steps, where the zero level is combined into just one at the AC converter output voltage v_c. According to the switching states presented in Table 1, the output voltage in the 5L-CTNPC can be modeled as:

$$v_c = \underbrace{(S_{11} + S_{12} - 1)\frac{v_{dc1}}{2}}_{v_{c1}} + \underbrace{(S_{21} + S_{22} - 1)\frac{v_{dc2}}{2}}_{v_{c2}}, \tag{1}$$

where v_c is the addition of the converter voltages of both modules, S_{1k} and S_{2k} are the switching states of the k-th 3L-TNPC unit and $v_{dck}/2$ is the total DC-link voltage of each cell. Furthermore, the dynamic model of the AC current in terms of the output voltage is governed by the next expression:

$$v_c = i_s R_s + L_s \frac{di_s}{dt} + v_s, \tag{2}$$

with v_s as the grid voltage measured at the point of common coupling (PCC), i_s as the grid current, L_s the grid filter inductance and R_s is the filter resistance included for modeling purposes. According to Table 1, the switching states are able to generate nine voltage levels in the output voltage v_c where each state has an associated voltage level in function to the DC-link v_{dc1} and v_{dc2}. Note that in this rooftop PV application both strings will be considered to work with similar DC-link voltages, i.e., $v_{dc1} \approx v_{dc2} = v_{dc}$. By doing this, the output voltage v_c can be reduced just to $\pm v_{dc}$, $\pm v_{dc}/2$ and 0. This assumption leads to five switching states with similar output voltage steps between two consecutive levels [20]. The redundant switching states will be used to balance the voltage in the DC-link capacitors by adjusting the power mismatch between the converter cells. The computed peak amplitude of the converter output voltage $\hat{v}_c$ is equal to $v_{pv1}/2 + v_{pv2}/2$, i.e., each power cell has a DC-link equal to the maximum level of the converter voltage. Therefore, for a proper grid current regulation, each PV string must be designed to satisfy $v_{pv1} \approx v_{pv2} > v_s$. In fact, this aspect is a practical advantage of cascaded configurations, since the overall DC-link voltage of the central configuration is split among power cells, thus reducing the string size.

Table 1. Switching states and output voltage in the AC terminals.

State	S_{11}	S_{12}	S_{21}	S_{22}	v_c
1	1	1	1	1	$v_{dc1}/2 + v_{dc2}/2$
2	1	1	0	1	$v_{dc1}/2$
3	0	1	1	1	$v_{dc2}/2$
4	1	1	0	0	
5	0	0	1	1	0
6	0	1	0	1	
7	0	1	0	0	$-v_{dc1}/2$
8	0	0	0	1	$-v_{dc2}/2$
9	0	0	0	0	$-v_{dc1}/2 - v_{dc2}/2$

2.2. Proposed Hybrid LS-PWM and PS-PWM Modulation Scheme for 5L-CTNPC Converter

The proposed modulation scheme for the 5L-CTNPC is based on two well-known carriers based on the sinusoidal PWM methods. The first is the Sinusoidal Level-Shifted Pulse Width Modulator (LS-PWM), used in 3L-NPC three-phase converters [25] and the single 3L-TNPC legs [20]. This modulation strategy requires two carrier signals in phase, to generate the three voltage levels in the output terminals of each cell. One carrier signal has a positive polarity (0 to 1) and the other has a negative polarity (–1 to 0). Furthermore, the LS-PWM is merged with the Sinusoidal Phase-Shifted PWM (PS-PWM) conventionally used in cascaded H-bridge power converters [26]. In the PS-PWM modulation, a phase shift between the carrier signals of each series connected to a power cell is introduced to increase the number of voltage levels, giving rise to a five-level stepped voltage waveform. The operation principle of this hybrid modulation technique is illustrated in Figure 2, where m^*_{ck} and v_{ck} are the modulation signal and the output voltage in the k-th cell, respectively. Note that each cell uses two carrier signals defined as v_{cr1} and v_{cr2}. Thus, the stacked connection of both cells creates the converter voltage v_c, which is commanded by its reference v^*_c. The combination of both methods is simpler in respect to the space vector modulation (SVM) [27]. Finally, the implementation of this modulation technique is depicted in the block diagram of Figure 3, where simple comparators and two carrier signals are required to implement the proposed technique.

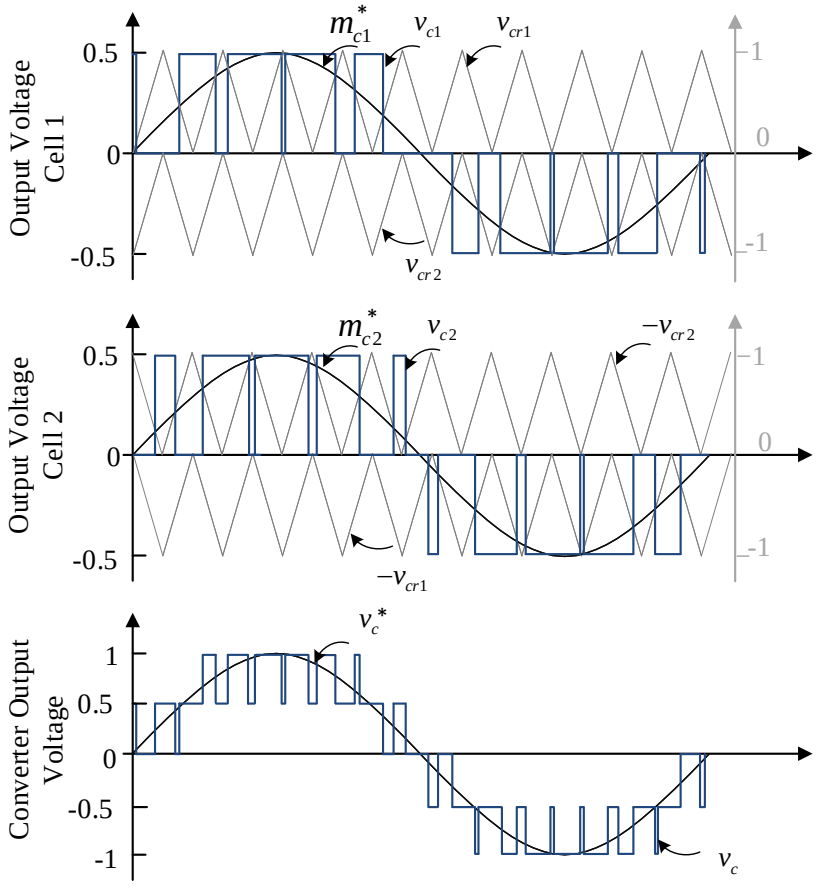

Figure 2. Proposed modulation scheme for 5L-CTNPC based on the hybrid LS-PWM and PS-PWM.

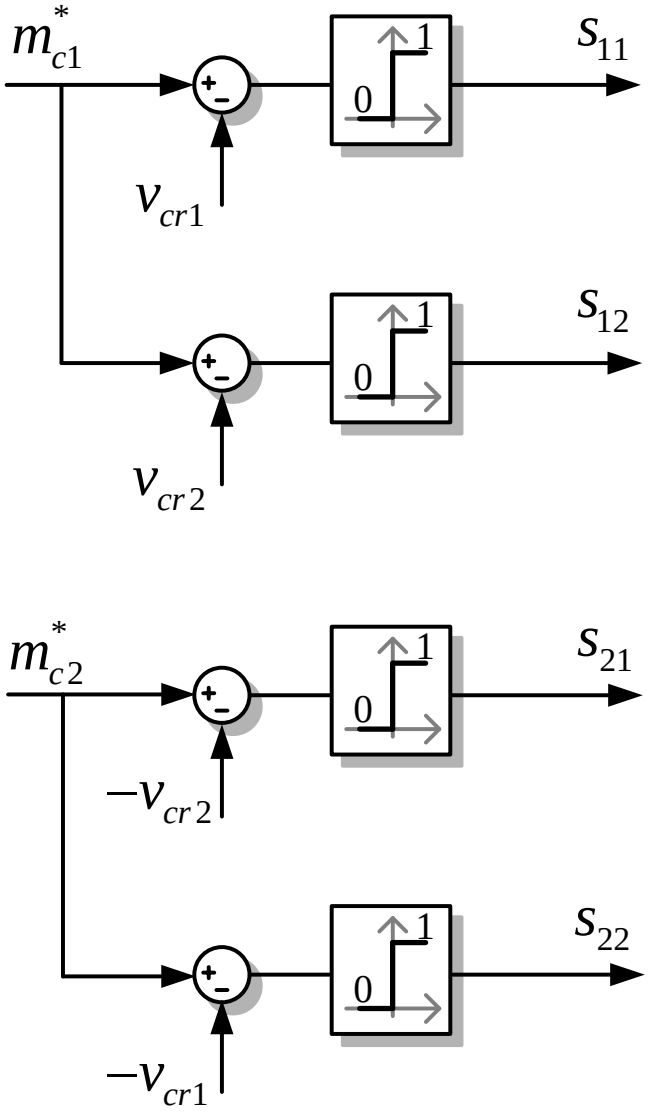

Figure 3. Straightforward implementation of hybrid LS-PWM and PS-PWM modulation for a 5L-CTNPC converter.

3. Overall Control Strategy

In this work three decoupled control stages are programmed to regulate the current injected into the grid, the power generated by each PV string and the power mismatch between cells. The first one is the MPPT, which set the DC-link voltage reference for both cells and is optionally included to extract the maximum power from the PV panels in case of direct connection to the 3L-TNPC modules. This control stage is complemented with the total DC-link control loop based on the energy interchange between the power cells. The second control stage is the single-phase voltage-oriented control loop, which has an embedded stationary current control loop implemented with Proportional Multi-Resonant (PMR) controllers. The last control loop is in charge of attenuating the DC-link voltage differences to compensate power mismatch issues among each cell of the converter. The overall control scheme is presented in Figure 4, where v_{pvk}, i_{pvk}, v_{dck} and s_{ok} are the PV voltage, PV current, DC-link voltage measurement and gating pulses of each k-th module.

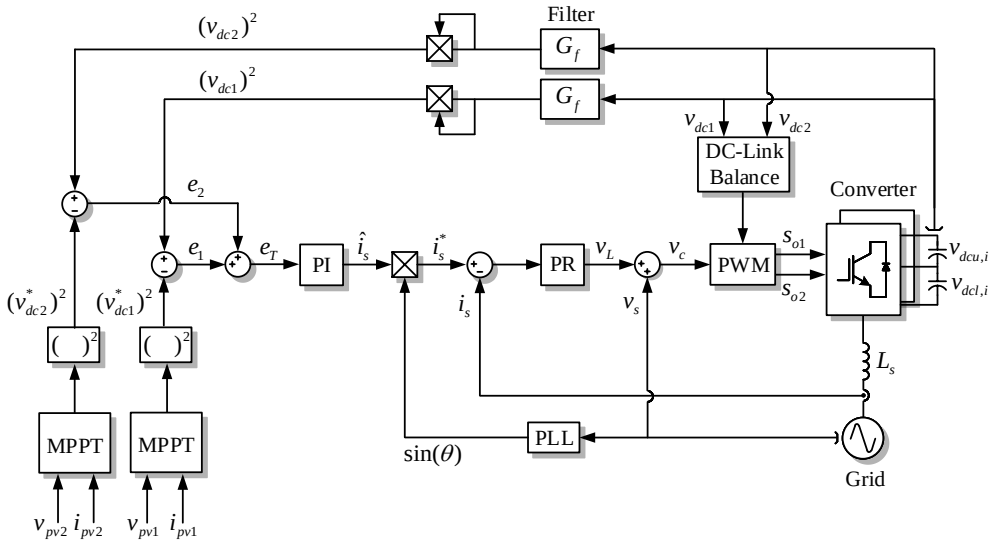

Figure 4. Single-phase voltage-oriented control strategy for the proposed 5L-CTNPC converter.

3.1. MPPT and Outer DC-Link Controller

The well-known Perturb and Observe (P&O) MPPT routine has been implemented for simplicity in this application. As the analyzed power configuration features two separate DC-links or PV string connections, two independent MPPT algorithms are required to obtain its full power operation. The MPPT routines compute the voltage reference for each DC-link v_{dc1}^* and v_{dc2}^*, as illustrated in Figure 4. Then, the DC-link control loop is designed to manage the total energy of the system through the difference between the voltage reference and the voltage measured, i.e., $e_T = e_1 + e_2$. This total energy is governed by using a proportional-integral (PI) controller, which generates the amplitude of the injected grid current $\hat{i}_s$. Note that the DC-link voltage measurements are acquired and processed with a notch filter G_f to eliminate the second harmonic ripple $2\omega_s$ presented in the DC-link capacitors by the rectification of a single-phase grid voltage. In fact, not filtering this harmonic voltage component will generate an undesired third harmonic $3\omega_s$ component in the grid current reference. The MPPT parameters such as voltage step Δv_{pv} and time period T_k are designed according with conventional commercial values. In experimental results, the voltage step $\Delta v_{pv} = 6$ V and the time period $T_k = 2$ s, whereas in simulation results, $\Delta v_{pv} = 6$ V and the time period is ten times smaller than the experimental results. Furthermore, the DC-link compensator has been designed by using a DC-link control bandwidth of 14Hz. Major details about the outer control design can be found in [20].

3.2. PMR Current Control Scheme

The grid current reference is generated by multiplying the amplitude of the injected grid current $\hat{i}_s$ with a unitary sinusoidal signal synchronized to the grid voltage. To avoid voltage measurement noise and low frequency harmonic components, a second order generalized integrator (SOGI) with a synchronous reference frame phase lock loop (SRF-PLL) is implemented to set the synchronous angle. Then, the grid current reference i_s^* is compared with the current measured value i_s, giving rise to a current error which is regulated by using a PMR control scheme. The structure of the implemented controller is included in Figure 5 and expressed as following:

$$C_i(s) = k_p + \sum_{h=1,3,5} \frac{2k_{ih}s}{s^2 + h^2\omega_s^2} \tag{3}$$

where k_p is the proportional gain and k_{ih} is the resonant gain at each selected h-th harmonic. Note that the above resonant controllers have been considered to achieve selective harmonic impedance enhancement at 3st and 5th components. The resonant frequency at ω_s is equal to the grid frequency,

hence the compensator $C_i(s)$ has infinite gain at ω_s, providing perfect sinusoidal tracking with zero steady-state error. The PMR compensator in Figure 5 has been designed by a simple pole placement with a crossover frequency of 270 Hz, which corresponds to a rate twenty times faster than the outer control loop. This control scheme is currently adopted for grid-connected PV systems where the grid voltage has important low-frequency harmonics [28].

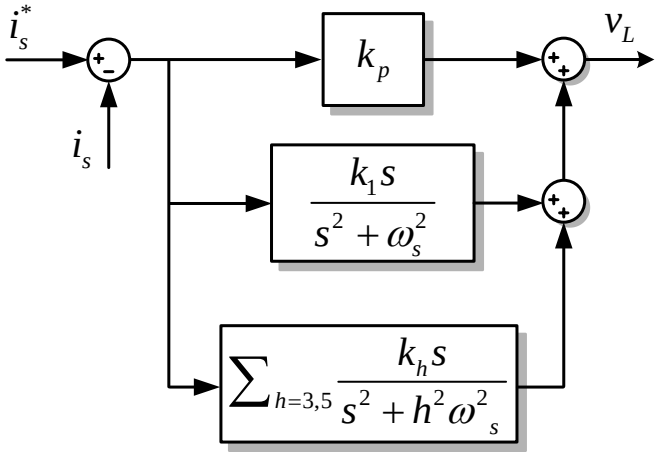

Figure 5. Stationary current control loop implemented with PMR controllers.

The output of the current control loop set the voltage reference across the grid inductor v_L^*. Neglecting the voltage drop in the resistance R_s, the converter voltage is equal to $v_c = v_L + v_s$. Commonly, the obtained inverter voltage reference v_c would be directly connected to the modulation block stage to generate the firing pulses in each semiconductor device. Since the current i_s is the same for both series connected 3L-TNPC converters, the voltage references for each power unit must be modified in advance to allow different power inputs. This important control requirement is performed by including an internal DC-link voltage balance stage, which enables the voltage balancing between capacitors in the DC-link and the power unbalance operation between both cells. In fact, the voltage balancing operation is performed by the DC-link voltage references v_{dc1}^* and v_{dc2}^* naturally delivered by the MPPT algorithm.

3.3. Voltage Balancing Control and Power Balance Scheme

As mentioned, correct power distribution between both cells and a control strategy to avoid voltage unbalancing in the DC-link capacitors is required to provide full operation in the 5L-CTNPC. The compensation block shown in Figure 6 is separated into two parts. The first one is the DC-link balancing control between cells, whose purpose is to regulate the power mismatch by increasing or decreasing the general modulation index amplitude, also referred to as the normalized inverter voltage v_c delivered from the current controller. In this control loop, the DC voltage error is regulated by using a PI controller and then the voltage compensator Δm_c is multiplied by the normalized inverter voltage reference v_c [29]. Therefore, the cell with higher power will increase its modulation amplitude, as the cell with lower power reduces its modulation amplitude. The second part of the control loop is given by the voltage balancing between the internal capacitors in the DC-link, where the voltage error is controlled using another PI controller. The output signal of this compensator Δm_d is added to the modulation index provided by the cell voltage control by moving in the vertical axis the modulation index for capacitor balancing purposes. Both PI controllers have been designed by a pole placement strategy, using a bandwidth of 5 Hz. This dynamic has been imposed to avoid fast disturbances into the modulation signal. Note that the proposed balancing control scheme does not need extra measurements, since they are previously accessible from the outer control stage.

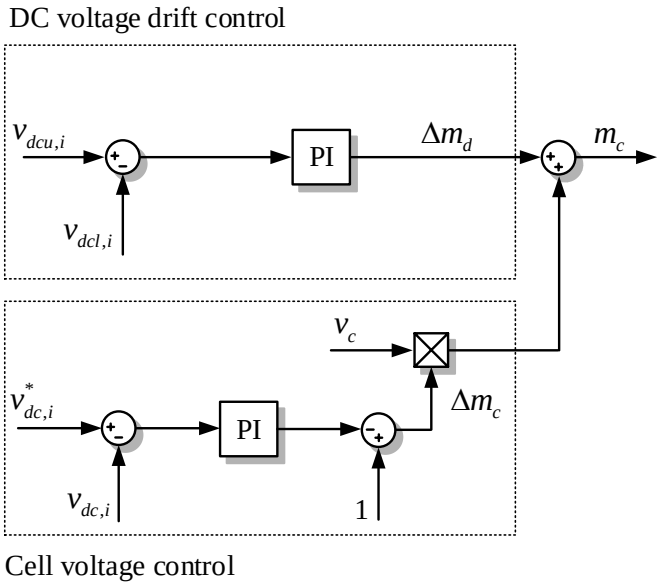

Figure 6. Implemented voltage balancing control strategy per 3L-TNPC cell.

4. Results

Simulation and experimental results of the proposed configuration are presented in this section. The simulation analysis has been performed through MatLab/Simulink for control purposes, while PLECS were used for modelling the modulation stage, power converter, grid voltage and PV strings. The analysis was completed by using the same scenarios of the experimental set-up just to improve the concept verification. The key simulation and experimental parameters are identified in Table 2. It is important to highlight that simulation parameters have been selected according to the reduced power experimental prototype.

Table 2. Simulation and experimental parameters.

Symbol	Parameter	Simulation Value	Experimental Value
Grid Parameters			
$\hat{v}_s$	Peak grid voltage	80 (V)	80 (V)
f_s	Grid frequency	50 (Hz)	50 (Hz)
Converter Parameters			
C_{dc}	DC-link capacitors	1950 (µF)	1950 (µF)
f_{cr}	Carrier frequency	2000 (kHz)	2083 (kHz)
L_s	Grid inductance	5 (mH)	5 (mH)
R_s	Grid resistance	0.01 (Ω)	1 (Ω)
Control Parameters			
T_s	Sample period	10 (µs)	15 (µs)
BW_{vdc}	DC-link control bandwidth	14 (Hz)	14 (Hz)
BW_{is}	Current control bandwidth	270 (Hz)	270 (Hz)
BW_{dv}	Balancing control bandwidth	5 (Hz)	5 (Hz)
MPPT Parameters			
T_k	P&O period	0.24 (s)	2.1 (s)
Δv_{pv}	P&O voltage step	6 (V)	6 (V)
PV String Parameters			
P_{mp}	Maximum power	106 (W)	106 (W)
v_{mp}	Voltage at maximum power	48.4 (V)	48.4 (V)
v_{oc}	Open-circuit voltage	65.0 (V)	65.0 (V)
i_{mp}	Current at maximum power	2.2 (A)	2.2 (A)
i_{sc}	Short-circuit current	2.6 (A)	2.6 (A)

4.1. Simulation Results

The first simulation result presented the injected grid current i_s with reference i_s^* and both capacitor voltages for each power cell under steady-state operation. In Figure 7, it is possible to appreciate the good regulation and synchronization in respect to the grid voltage v_s performed by the grid current control and the synchronization control loop. Furthermore, in Figure 8, the voltage balancing control is demonstrated, where the upper $v_{dcu,k}$ and lower $v_{dcl,k}$ voltage capacitors for each k-th power cell are well balanced.

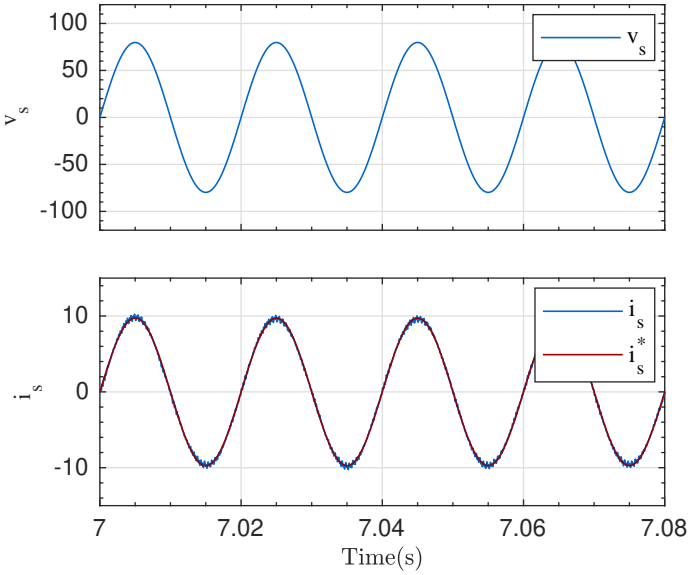

Figure 7. Steady-state operation of the grid current PMR control.

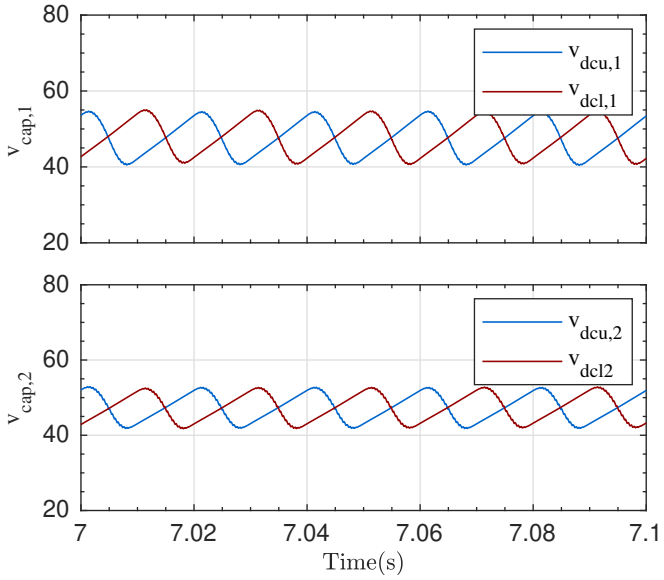

Figure 8. Steady-state operation of capacitor voltages for each power cell.

The second simulation results present a dynamic operation under two different scenarios. An irradiation step from 1 kW/m^2 to 0.8 kW/m^2 was applied to the lower cell, maintaining 1 kW/m^2 of irradiation in the PV string connected to the upper cell. After the irradiation step took place, a temperature step changes was performed from 25 °C to 18 °C to the upper cell, generating an increase in the power. The irradiation and temperature changes were introduced in a simplified PV model provided by PLECS. Figure 9 shows the dynamic operation of the DC-link voltage v_{dck} and the

power at DC-side $P_{ck} = v_{dck} \cdot i_{pvk}$ for each k-th cell. It is possible to appreciate how the irradiation step at t = 3.5 s only affected to the lower module, producing a voltage perturbation and a power reduction in P_{c2}. Since the reference voltage is provided by the P&O algorithm, the stepped voltage was required to maintain the maximum power operation. In the second scenario, the temperature decreased at t = 8 s and the DC voltage as well as the power in the upper module increased. The three-level voltage v_{ck} of each converter cell, and the overall five-level voltage v_c are depicted in Figure 10 under unbalance operation. Additionally, it is possible to appreciate how the power reduction in the lower arm affects the modulation indexes m_{ck}, creating signals with different magnitudes.

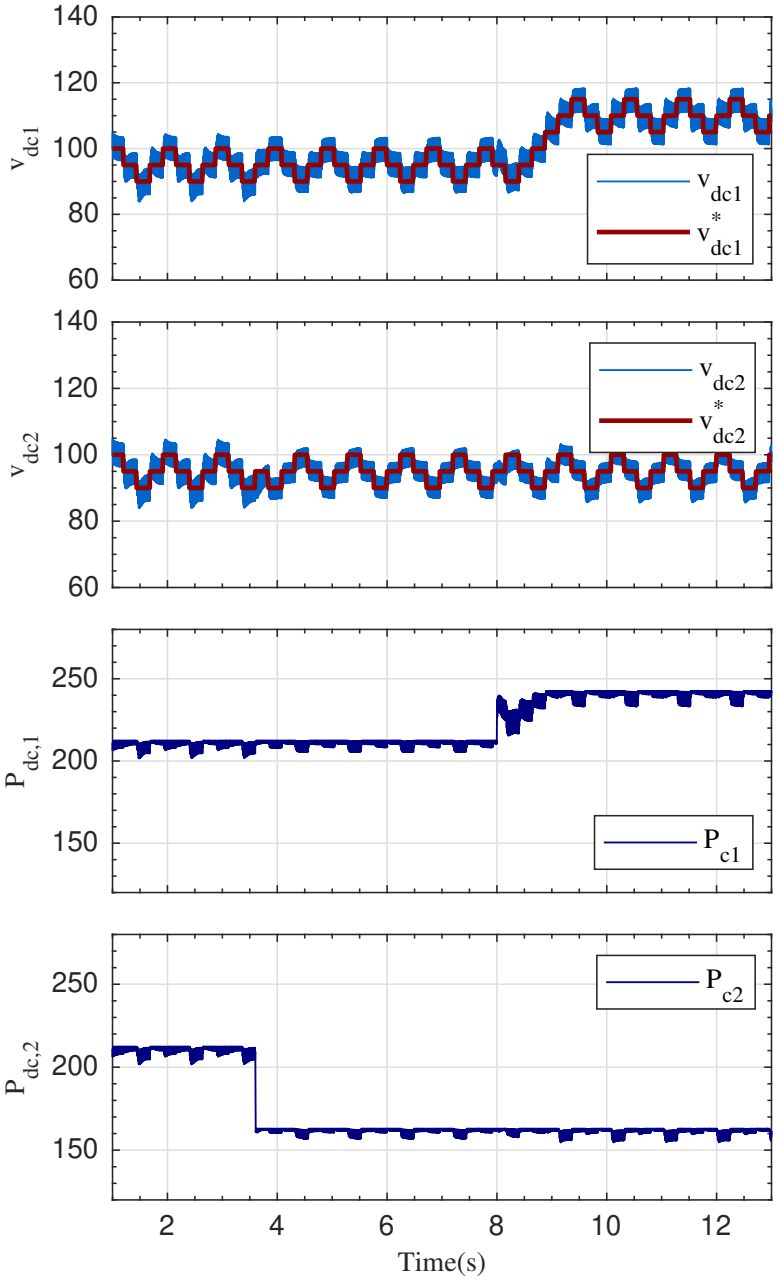

Figure 9. Dynamic operation of DC-link and power on the DC-side under unbalanced power per string.

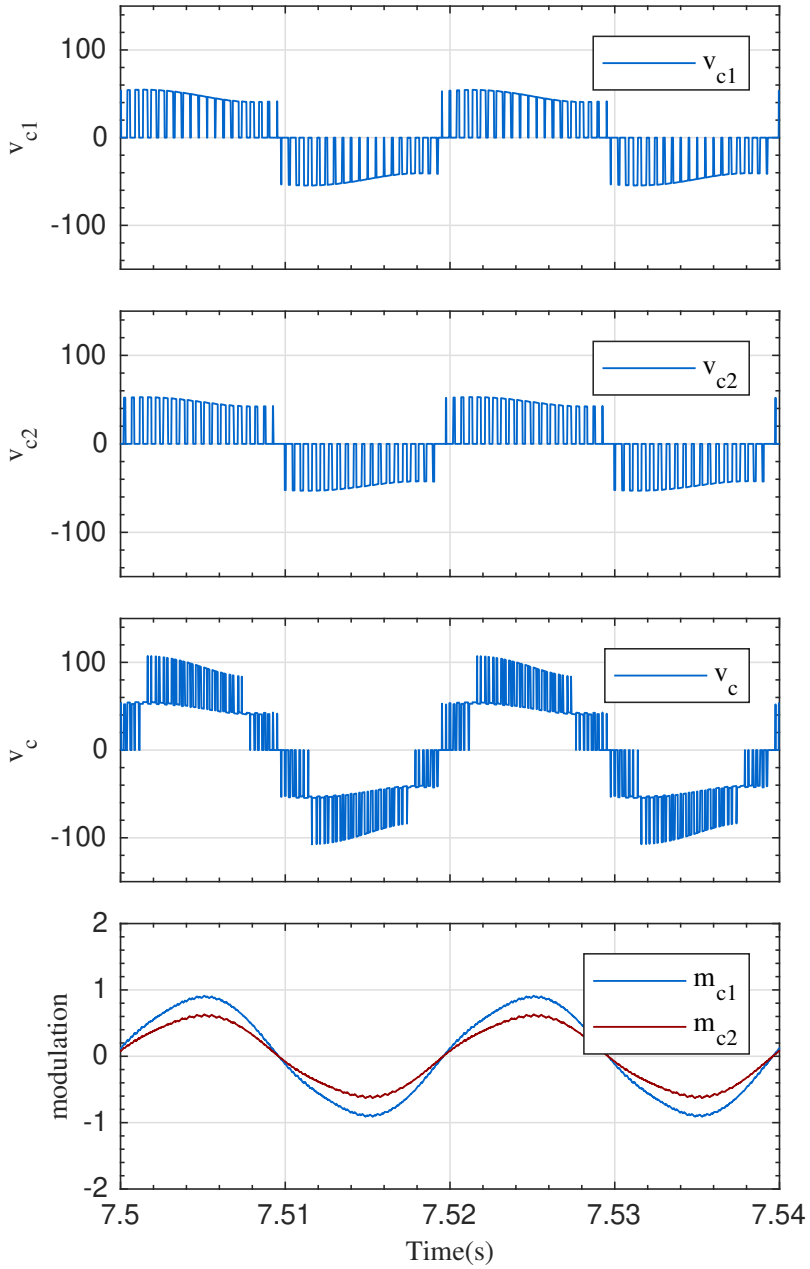

Figure 10. Steady-state converter output voltage performance under unbalanced power per string.

4.2. Experimental Results

The experimental PV system comprises of two 3L-TNPC power cells without isolation and were fed directly by one PV string. Each string was composed by two PV modules emulated with the Agilent E4360 solar array simulator, which enabled a total control of the temperature and irradiation parameters. Each simulator has two output channels connected in series to emulate the PV string generator. The parameters such as maximum power P_m, current at maximum power i_{mp}, short-circuit current i_{sc}, voltage at maximum power v_{mp} and open-circuit voltage v_{oc} are listed in Table 2. The simplified layout of the experimental small-scale setup is depicted in Figure 11. The control algorithm is fully programmed in C code by using a dSPACE 1103 digital control platform running at 15 µs. The modulation stage and dead-time generation is implemented by using a FPGA Spartan3. To experimentally validate the proposed control scheme, three different operation points are evaluated. A steady-state operation, and two dynamic operation under an irradiation and a temperature step.

The first experimental results shown in Figures 12 and 13 are analyzed during steady-state operation. The grid-side variables i.e., grid current and voltage waveforms are presented in Figure 12, where the unitary power factor operation is achieved. Furthermore, Figure 13 captures the output voltage of each cell and the total voltage composed by a five-level waveform. Similar to the simulation results, the steady-state performance of the capacitor voltage balancing in Figure 14 is included.

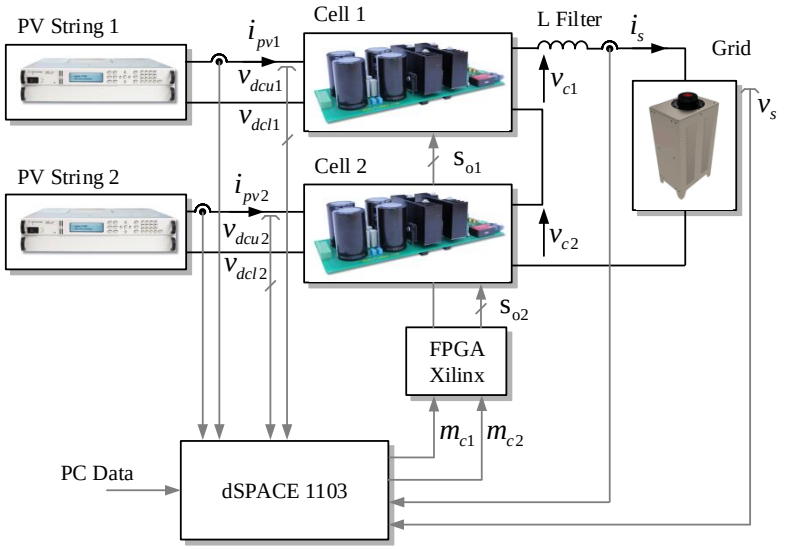

Figure 11. Simplified diagram of implemented experimental setup.

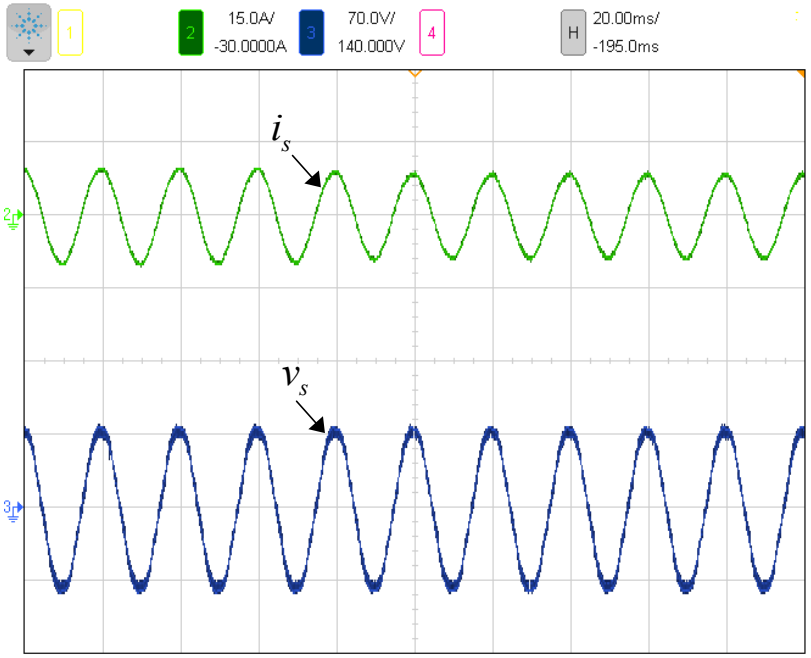

Figure 12. Steady-state experimental results at grid-side variables: Grid current and voltage waveforms.

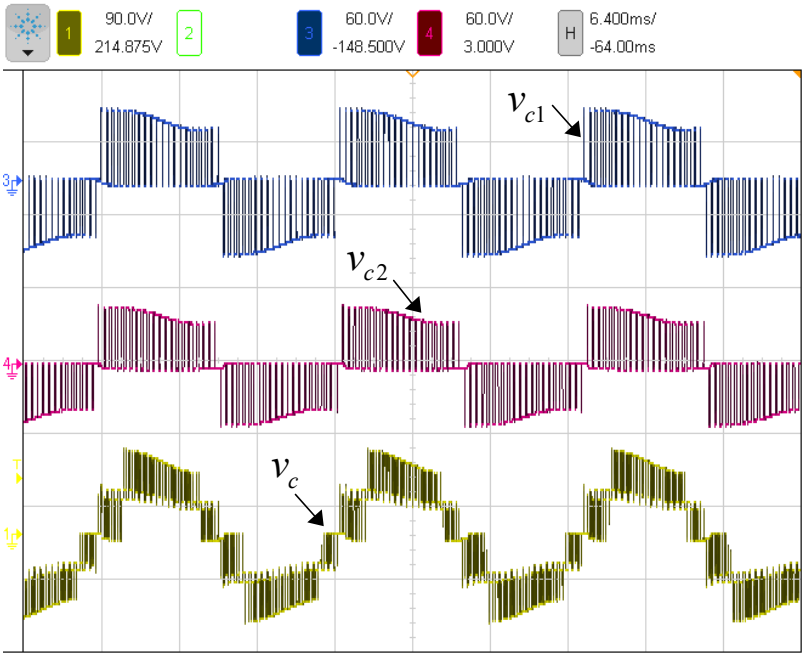

Figure 13. Steady-state experimental results at converter-side variables: Output voltage for each cell and total output voltage.

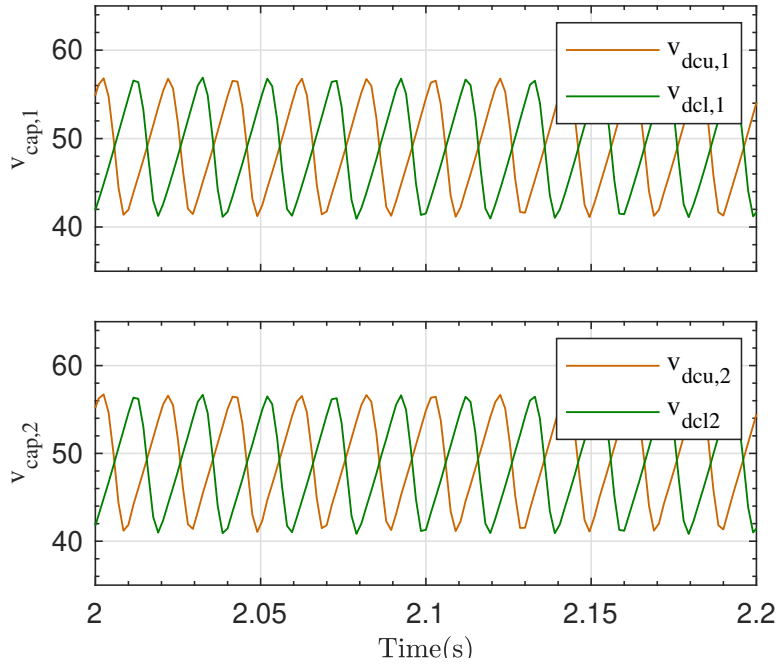

Figure 14. Steady-state experimental results of capacitor voltage across each 3L-TNPC cell.

The second set of experimental results during dynamic operation is shown in Figures 15 and 16. Firstly, an irradiation step from 1 kW/m^2 to 0.8 kW/m^2 was applied to the second PV cell (lower cell operating at reduced power), while the first array irradiation level was retained. After this irradiance step variation, a temperature step change was tested from 25 °C to 18 °C and applied to the first PV cell (upper cell operating at increased power). Under the above conditions, the input voltages generate a three-level waveform signal due to the use of the conventional P&O MPPT method. Note that under both scenarios, the coupling effects from one cell to each other is fully avoided, ensuring a decoupled operation between power cells.

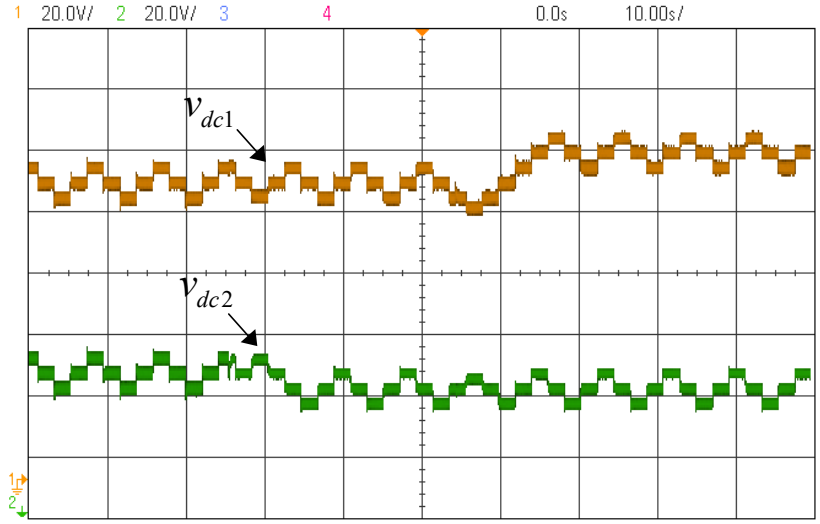

Figure 15. Experimental dynamic operation of DC-link voltage under unbalanced power per string due to solar irradiation and temperature changes.

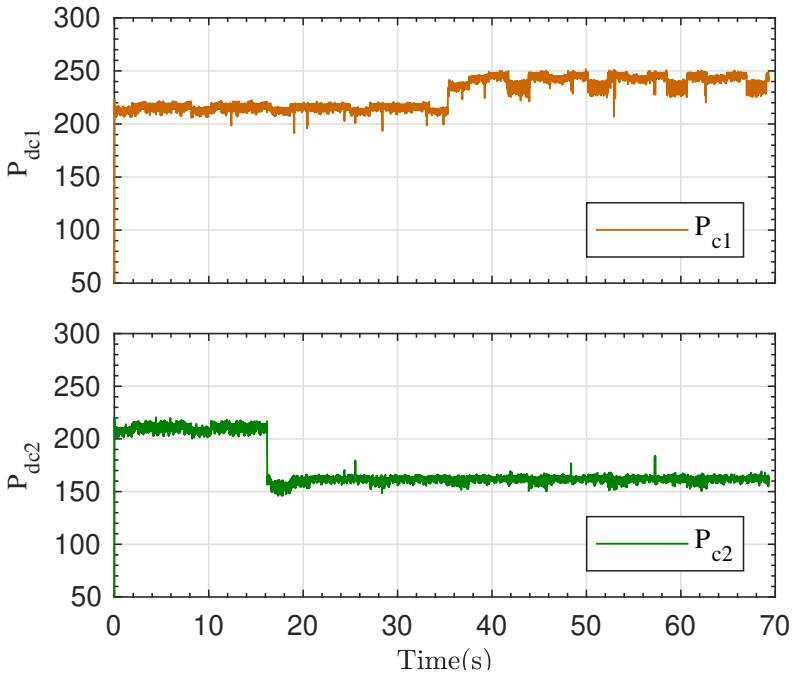

Figure 16. Experimental dynamic operation of DC power under unbalanced power per string due to solar irradiation and temperature changes.

4.3. Brief Comparison with Other Five-Level T-type Converters

A comprehensive comparison between three different five-level T-type converters have been presented in Table 3. The studied topologies are the proposed 5L-CTNPC, the hybrid version 5L-HTNPC and the conventional 5L-TNPC. Each topology presents the same features of the one described in simulation and experimental results. To evaluate the power efficiency of each converter, switching and conduction losses is required in respect to the power operation point for each cell. Semiconductor device losses are included with a thermal model library developed in PLECS, based on the manufacturer datasheet [30]. The resulting efficiency evaluation is depicted in Figure 17, where the obtained efficiency of the proposed configuration 5L-CTNPC is equal to the conventional 5L-TNPC. Due to the fact that there is a reduced number of switches at the second parallel leg in the 5L-HTNPC

a slightly higher efficiency was achieved. This analysis is corroborated by counting the number of semiconductor devices used for each evaluated topology, which is summarized in Table 3.

The symmetrical topology configuration and the multiple MPPT possibilities are the main advantages of the studied topology in respect to the rest power converters. Finally, in Figure 18 the current spectrum for each evaluated converter topology is computed. The current THD obtained with the proposed topology is similar to the conventional 5L-TNPC power topology, while the worst value (over 4.9%) was reached in the 5L-HTNPC configuration. In fact, the apparent switching frequency of this topology was equal to the carrier frequency, while in the proposed 5L-CTNPC and 5L-TNPC the apparent switching frequency was twice the switching frequency.

Table 3. Brief comparison between five-level T-type topologies.

Parameter	5L-CTNPC	5L-HTNPC	5L-TNPC
DC-link voltage	v_{dc}	v_{dc}	v_{dc}
IGBT blocking voltage	$4 \times v_{dc}, 4 \times v_{dc}/2$	$4 \times v_{dc}, 2 \times v_{dc}/2$	$4 \times v_{dc}, 4 \times v_{dc}/2$
IGBT switching freq.	8×2 (kHz)	4×2 (kHz), 2×50 (Hz)	8×2 [kHz]
Apparent output voltage Ffreq.	4 (kHz)	2 (kHz)	4 [kHz]
Grid current THD	2.83%	4.91%	2.53%
Switching losses	0.087%	0.078%	0.087%
Cond. losses	1.467%	1.409%	1.469%
Converter efficiency	98.43%	98.51%	98.44%
MPPT efficiency	+++	++	++
Topology configure	Symmetrical	Asymmetrical	Symmetrical
Advantages	2 MPPT High energy yield High power quality	1 voltage control loop Good power quality	1 voltage control loop High power quality
Disadvantages	2 voltage control loops High cond. losses	1 MPPT only DC-voltage offsets	1 MPPT only High cond. losses

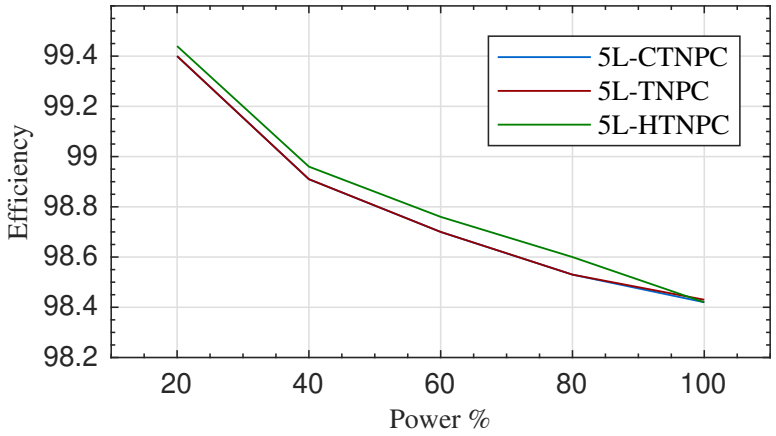

Figure 17. Efficiency comparison between 5L-CTNPC, 5L-HTNPC and 5L-TNPC inverter topologies respect to the power operation.

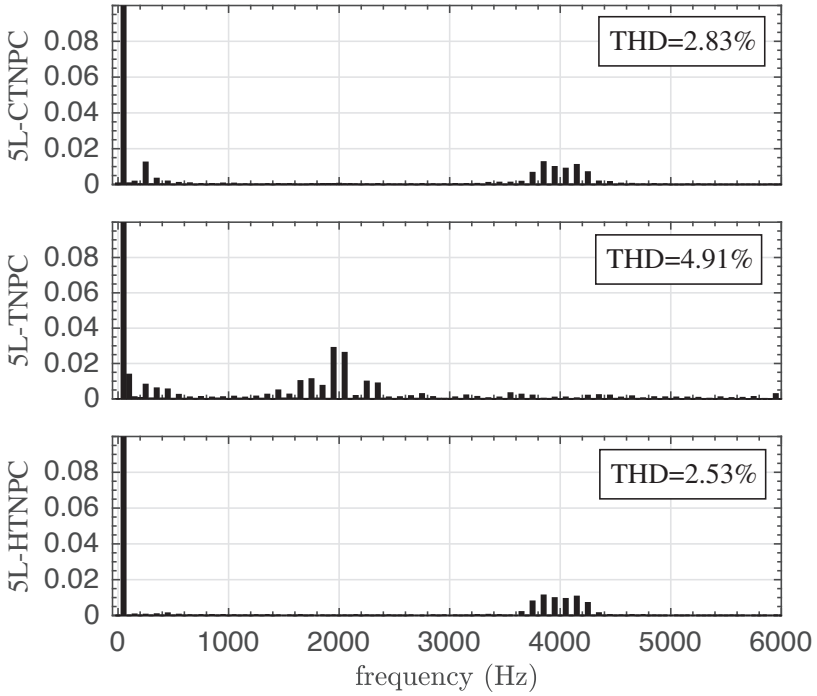

Figure 18. Grid current FFT comparison between 5L-CTNPC, 5L-HTNPC and 5L-TNPC inverter topologies.

5. Conclusions

In this work a grid-tied PV system configuration based on a series connection of three-level T-type inverter cells was described and validated. The proposed power topology merged the benefits of multistring configurations with more than one independent MPPT capability and the benefits of cascade H-bridge converters, generating a five-level output voltage waveform in the AC terminals. The proposed topology, modulation and control scheme were validated experimentally in a reduced scale power prototype with a straightforward implementation. Additionally, the proposed control strategy was evaluated under steady-state and unbalanced power conditions, ensuring a decoupled operation between both power cells. Finally, a brief comparison for key merit figures was included, where the main advantages of the proposed topology among other T configurations were highlighted, giving rise to the possibility of enhancing the power extraction from the PV side due to the multi-string configuration.

Author Contributions: C.V. conceived, designed and performed the experimental evaluations; S.K. provided insight on the power topology and conceptual solution, and was responsible of supervision throughout the work; C.A.R. wrote the manuscript and was part of the development team of the experimental test-bench, M.A.P. was responsible for the guidance during the prototype design stage, T.M. and M.M. provided relevant key theoretical and technical suggestions.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
DC	Direct Current
PV	Photovoltaic
NPC	Neutral Point Clamped
MLI	Multi Level Inverter
THD	Total Harmonic Distortion
MV	Medium-Voltage
3L-NPC	Three-Level Neutral Point Clamped
3L-TNPC	Three-Level T-type Neutral Point Clamped
3L-NPP	Three-Level Neutral Point Piloted
5L-TNPC	Five-Level T-type Neutral Point Clamped
5L-HTNPC	Five-Level Hybrid T-type Neutral Point Clamped
CHB	Cascade H-Bridge
9L-TNPC	Nine-Level T-type Neutral Point Clamped
5L-CTNPC	Five-Level Cascade T-type Neutral Point Clamped
IGBT	Isolated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
PID	Potential-Induced Degradation
PWM	Pulse Width Modulation
LS-PWM	Level-Shifted Pulse Width Modulation
PS-PWM	Phase-Shifted Pulse Width Modulation
SVM	Space Vector Modulation
PMR	Proportional Multiresonant
P&O	Perturb and Observe
PI	Proportional-Integral
SOGI	Second Order Generalized Integrator
SRF-PLL	Synchronous Reference Frame Phase Lock Loop

Nomenclature

The following variable nomenclature is used along figures and tables of this manuscript:

v_s	Grid voltage
i_s	Grid current
L_s	Filter inductor
R_s	Filter resistor for modelling purposes
v_c	Total converter voltage
v_{ck}	Converter voltage per cell
C_{dc}	Capacitance per cell
S_{k1}, S_{k2}	Switching signals per cell
$v_{dcu,k}$, $v_{dcl,k}$	Upper and lower capacitor voltages per cell
$v_{dc,k}$	DC-link voltage per cell
v_{dck^*}	DC-link voltage reference per cell
$v_{pv,k}$	PV voltage per cell
$i_{pv,k}$	PV current per cell
m_{ck}	Modulation reference signal per cell
v_{cr1}, v_{cr2}	Carrier signals
v_c^*	Per-unit converter voltage reference
e_k	Energy error per cell
e_T	Total error energy
$\hat{i}_s$	Reference current magnitude
ω_s	Angular grid frequency
θ	Grid angle
f_s	Grid frequency

G_f	Notch filter
Δv_{pv}	MPPT voltage step
T_k	MPPT time step
i_s^*	Current reference
$C_i(s)$	Current controller
k_p	Proportional gain of the PMR controller
k_{ih}	Integral gain of the PMR controller for each h-th frequency component
h	Grid harmonic
v_L	Inductor voltage
v_L^*	Inductor voltage reference
f_{cr}	Carrier frequency
T_s	Sampling period
BW_{vdc}	DC-link control bandwidth
BW_{is}	Current control bandwidth
BW_{dv}	Balancing control bandwidth
P_{mp}	Maximum power
v_{mp}	Voltage at maximum power
v_{oc}	Open-circuit voltage
i_{mp}	Current at maximum power
i_{sc}	Short-circuit current
Δm_d	Voltage drift modulation component
Δm_c	Cell voltage control
P_{ck}	Power per cell

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