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A Gate Driver Based on Variable Voltage and Resistance for Suppressing Overcurrent and Overvoltage of SiC MOSFETs

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Abstract: A SiC MOSFET is a suitable replacement for a Si MOSFET due to its lower on-state resistance, faster switching speed, and higher breakdown voltage. However, due to the parasitic parameters and the low damping in the circuit, the turn-on overcurrent and turn-off overvoltage of a SiC MOSFET become more severe as the switching speed increases. These effects limit higher frequency applications of SiC MOSFET. Based on the causes of overcurrent and overvoltage of SiC MOSFET, a novel gate driver with the variable driving voltage and variable gate resistance is proposed in this paper to suppress the overcurrent and overvoltage of SiC MOSFETs. The proposed gate driver can realize the variation in driving voltage and gate resistance during switching transitions. It not only suppresses the overcurrent and overvoltage of SiC MOSFETs, but also has little effect on switching loss. The working principle of the proposed gate driver is analyzed in this paper. Finally, experimental verification on a double-pulse test platform is performed to verify the effectiveness of the proposed gate driver.

Keywords: SiC MOSFET; overvoltage; overcurrent; switching loss; gate driver

1. Introduction

Silicon carbide (SiC) MOSFETs have the advantages of high breakdown electric field, fast drift saturation of carriers, good thermal stability, and high thermal conductivity [1–5]. These advantages of SiC MOSFETs can improve the performance of electronic converters. The switching frequency of power electronic converters based on SiC MOSFETs can even reach MHz, and the power density has been greatly improved because of the good switching characteristics of SiC MOSFETs [6–9]. However, the turn-on overcurrent and turn-off overvoltage of SiC MOSFETs become more severe as the switching speed increases due to the parasitic parameters and the low damping in the circuit, which limits the switching frequency of SiC MOSFETs and even damages the devices [7–14]. Therefore, it is necessary to reduce the turn-on overcurrent and turn-off overvoltage of SiC MOSFETs. At present, there are three methods to reduce the turn-on overcurrent and turn-off overvoltage of SiC MOSFETs. The first method is adding an RCD snubber circuit in the switching device or the main power loop [15,16]. This method of increasing an RCD snubber circuit can suppress the turn-off overvoltage effectively, but the energy stored in the external capacitor will be released through the device channel when the device is turned on, which could increase the turn-on overcurrent and turn-on loss. The second method is the use of a DC-side snubber, this method can decouple a portion of parasitic inductance from the power loop by paralleling a decoupling capacitor in the bridge circuit. However, the parasitic inductance will resonate with the high-frequency decoupling capacitor if the decoupling capacitor is not large enough. The suppression effect is not good when the high-frequency decoupling capacitor is large enough to

avoid low-frequency oscillation [14]. The third method to suppress the overvoltage and overcurrent is increasing the gate resistor for slowing the switching speed, but switching loss is greatly increased as a result [1,17,18]. Therefore, a two-stage gate driver based on a variable resistor is proposed in the literature [19]. However, a two-stage gate driver only based on a variable resistor cannot achieve lower switching loss. Additionally, a multilevel gate driver based on a switched voltage is proposed [20]; its principle is based on a monotonic gate voltage. The multilevel gate driver can suppress the overvoltage and overcurrent, but the switching loss increases greatly.

A novel gate driving circuit based on variable driving voltage and variable gate resistance topology is proposed in this paper to suppress the overvoltage and overcurrent of SiC. The proposed gate driver can not only suppress the overvoltage and overcurrent of SiC MOSFETs, but also reduce the switching loss when compared with gate drivers presented in the literature. The causes of overvoltage and overcurrent of SiC MOSFETs are analyzed in detail in Section 2. Section 3 provides the topology and operation principle of the proposed gate driver. A double-pulse test platform based on the proposed gate driver is set up in Section 4 to verify the correctness and effectiveness of the proposed gate driver.

2. Overvoltage and Overcurrent of SiC MOSFETs

Figure 1 shows a double-pulse circuit considering the parasitic parameters. The circuit shown in Figure 1 can also be used to analyze the switching characteristics of Buck, Boost, Buck-Boost, Half Bridge, and Full Bridge circuits. In Figure 1, the input voltage V_{DC} and the output current I_o are constant. Q_1 is a SiC MOSFET. The parasitic parameters are the gate-source junction capacitance C_{GS} , gate-drain junction capacitance C_{GD} , drain-source junction capacitance C_{DS} , gate parasitic inductance L_G , common-source parasitic inductance L_{CS} and internal gate resistance R_{G1} . R_{G2} is the external gate resistor and v_p is the driving signal of Q_1 .

Figure 1. Double-pulse circuit considering the parasitic elements.

The freewheeling diode D uses a SiC JBS diode. The parasitic parameters inside the package are: junction capacitance C_F and its on-resistance R_F . L_C , L_D , L_G , and L_{BUS} represent the parasitic inductance of the branches where they are located (including parasitic inductances on the package and PCB connection lines).

Figure 2 shows the switching waveforms of Q_1 : the gate-source voltage v_{GS} , the drain current i_D , the drain-source voltage v_{DS} , and the switching waveform of freewheeling diode voltage v_F . The switching waveforms of a switching cycle can be divided into ten stages. The turn-on transient includes: Stage 1 (turn-on delay stage), Stage 2 (current-rising stage), Stage 3 (turn-on overcurrent stage), and Stage 4 (current-oscillating stage). The turn-off transient includes: Stage 6 (turn-off delay stage), Stage 7 (voltage-rising stage), Stage 8 (turn-off overvoltage stage), and Stage 9 (voltage-oscillating stage). Stage 5 and Stage 10 are the stable stages after the switching transient. Since this paper mainly analyzes the

causes of the overcurrent and overvoltage of SiC MOSFETs, the section only analyzes Stage 3, Stage 4, Stage 8, and Stage 9 in detail.

Figure 2. Switching waveforms of a SiC MOSFET and a freewheeling diode.

2.1. Causes of Turn-On Overcurrent

Stage 3, Turn-on overcurrent stage. When the i_D of the SiC MOSFET is equal to I_o , the freewheeling diode D is able to block the voltage. The junction capacitance C_F is charged, and the charging current flows through Q_1 and causes i_D to have an overcurrent. Meanwhile, the junction capacitances C_{GS} and C_{DS} of the SiC MOSFET are discharged, the discharge current flows through its channel, and the channel current i_{CH} also appears overcurrent. The equivalent circuit at this stage is shown in Figure 3a. The junction capacitance C_F , C_{GS} , and C_{DS} are equivalent to current sources, and the Q_1 channel is equivalent to a controlled current source.

Figure 3. Equivalent circuit of (a) Stage 3, (b) Stage 4, (c) Stage 8, (d) Stage 9.

The overcurrent of i_D is shown in Equation (1), and the overcurrent of i_{CH} is shown in Equation (2).

$$\Delta i_D = C_F \frac{dv_F}{dt} \quad (1)$$

$$\Delta i_{CH} = C_F \frac{dv_F}{dt} - C_{GD} \frac{dv_{DS}}{dt} - C_{DS} \frac{dv_{DS}}{dt} \quad (2)$$

In the above Equation, dv_F/dt is the voltage variation rate of v_F , and dv_{DS}/dt is the voltage variation rate of dv_{DS} . According to Equation (1) and Equation (2), the overcurrent of Q_1 is mainly determined by dv_F/dt and dv_{DS}/dt , and the relationship shown in Equation (3) exists at this stage.

$$\frac{dv_F}{dt} \approx -\frac{dv_{DS}}{dt} \approx \frac{V_{GS} - V_{mil}}{(R_{G1} + R_{G2})C_{GD}} \quad (3)$$

In Equation (3), V_{mil} is the Miller voltage of Q_1 . Since the voltage V_{GS} changes slightly at this stage, it can be considered as a constant. The turn-on overcurrent can be reduced by reducing the turn-on driving voltage V_{GS} and increasing the external gate resistance R_{G2} according to Equation (3).

Stage 4, Current-oscillating stage. After the diode voltage v_F reaches the input voltage V_{DC} , the SiC MOSFET can be equivalent to the on-state resistance R_{DS} . The junction capacitance C_F oscillates with the parasitic inductance of the power loop L_{BUS} to consume the energy stored in C_{GS} , C_{DS} , C_F before time t_2 . The equivalent circuit at this stage is shown in Figure 3b.

2.2. Causes of Turn-Off Overvoltage

Stage 8, Turn-off overvoltage stage. After the drain-source voltage v_{DS} is equal to V_{DC} , D turns on. Q_1 and D commutate, the rapid di_D/dt creates a voltage drop in the parasitic inductance L_P . The voltage drop is superimposed on the drain-source of Q_1 and a turn-off overvoltage appears. The equivalent circuit of this stage is shown in Figure 3c, and the overvoltage can be calculated by Equation (4). At this stage, i_D is approximately equal to i_{CH} . Equation (5) can be derived according to the transconductance relationship of the SiC MOSFET.

$$\Delta v_{DS} = L_P \frac{di_D}{dt} \quad (4)$$

$$\frac{di_D}{dt} \approx \frac{di_{CH}}{dt} = g_f \frac{dv_{GS}}{dt} \quad (5)$$

where $L_P = L_{BUS} L_C + L_D + L_{CS}$, and g_f is the transconductance of Q_1 .

Stage 9, Voltage-oscillating stage. When the i_D drops to 0, the channel of the Q_1 is turned off. The C_{GD} and C_{DS} oscillate with the parasitic inductance L_P to consume the energy stored in L_P before time t_8 . The equivalent circuit in this stage is shown in Figure 3d.

Based on the above analysis, the parasitic inductance L_P , transconductance g_f , and dv_{GS}/dt can determine the turn-off overvoltage. g_f is a device parameter and it is not easy to change. Reducing the turn-off driving voltage amplitude $-V_{SS}$ and increasing the external gate resistance R_G at this stage can suppress the turn-off overvoltage.

3. Proposed Gate Driving Circuit

Based on the analysis in Section 2, the turn-on overcurrent and turn-off overvoltage can be suppressed by reducing the driving voltage amplitude v_p and increasing the external gate resistance R_G . However, when this method is applied to the entire switching cycle, it will slow down switching speed in each stage. The switching loss will increase as a result.

Therefore, a novel gate driver based on the variable driving voltage and variable gate resistance topology for SiC MOSFETs is proposed in this paper. This proposed gate driver adopts different driving voltage and gate resistance during different switching stages. It can not only suppress the turn-on overcurrent and turn-off overvoltage but can also avoid serious switching loss.

faster turn-off speed to reduce turn-off loss during these two stages, the turn-off voltage can be set to a negative voltage (<0 V, >-10 V), and a small gate resistance should be set.

4) *Turn-off overvoltage and voltage-oscillating stages*. In order to reduce di_D/dt , the turn-off driving voltage no longer uses a negative voltage and a larger gate resistance should be set.

3.2. Working Principle of the Proposed Gate Driving Circuit

The working modes of the proposed driving circuit are as follows. Table 1 shows the driving voltage and gate resistor in each mode of the proposed driving circuit.

Table 1. Driving voltage and gate resistor in each mode.

Working Modes	Switching Stages	Driving Voltage	Gate Resistance
Mode 1	Stages 1-2 [t_1 - t_3]	V_{GS}	$R_{G1} + R_{G4}$
Mode 2	Stages 3-5 [t_3 - t_6]	$V_{GS} + V_{SS}$	$R_{G1} + R_{G3} + R_{G5}$
Mode 3	Stages 6-7 [t_6 - t_8]	V_{SS}	$R_{G1} + R_{G3}$
Mode 4	Stages 8-10 [t_8 - t_{11}]	0 V	$R_{G1} + R_{G4} + R_{G6}$

We assume that the driving circuit is in a stable state before time t_1 , S_3 and S_4 are in the on-state, the gate resistance is $R_{G1} + R_{G4} + R_{G6}$, Q_1 is in the off-state, and the freewheeling diode D freewheels.

Mode 1: At time t_1 , S_1 , S_4 , and S_{A1} are turned on and S_3 is turned off. The driving signal v_P of Q_1 changes from 0 V to V_{GS} , and the gate resistance becomes $R_{G1} + R_{G4}$. The smaller the R_{G4} , the faster the speed of these two stages. Therefore, R_{G4} can choose a 10 Ω resistor. At time t_3 , i_D rises to I_o , freewheeling diode D turns off, and this mode ends. The equivalent circuit of this mode is shown in Figure 6a. In this mode, the turn-on delay time and current-rise time of the Q_1 are shortened.

Mode 2: At time t_3 , S_1 and S_2 are turned on, S_4 and S_{A1} are turned off; the driving signal v_P of Q_1 becomes $V_{GS} + V_{SS}$, and the gate resistance becomes $R_{G1} + R_{G3} + R_{G5}$. During these two stages, $V_{GS} + V_{SS}$ depends on V_{GS} and V_{SS} and cannot be changed. The larger the R_{G5} , the lower the turn-on overcurrent of Q_1 . However, the turn-off process does not end completely, and the turn-off loss will increase as R_{G5} increases. Therefore, the value of R_{G5} should be a tradeoff between the turn-on overcurrent and turn-on loss. At time t_6 , the turn-off signal of Q_1 arrives and this mode ends. The equivalent circuit is shown in Figure 6b. In this mode, the turn-on overcurrent and oscillation of Q_1 are suppressed.

Mode 3: S_2 , S_3 , and S_{A3} are turned on and S_1 is turned off at time t_6 . The driving signal v_P of Q_1 changes from 0 V to V_{SS} , and the gate resistance becomes $R_{G1} + R_{G3}$. The smaller the R_{G3} , the faster the speed of these two stages, and a 10 Ω resistor can be chosen as R_{G3} . At time t_8 , v_{DS} rises to V_{DC} , freewheeling diode D conducts, and this mode ends. The equivalent circuit of this mode is shown in Figure 6c. In this mode, the turn-off delay time and voltage-rising time of the Q_1 are shortened, and the turn-off loss decreases as a result.

Mode 4: At time t_6 , S_3 and S_4 are turned on, and S_2 and S_{A3} are turned off. The driving signal v_P of Q_1 becomes 0 V, and the gate resistance becomes $R_{G1} + R_{G4} + R_{G6}$. The larger the R_{G6} , the lower the turn-off overvoltage of Q_1 . However, the turn-off process does not end completely, the turn-off loss will increase as R_{G6} increases. Therefore, the value of R_{G6} should be a tradeoff between the turn-off overvoltage and turn-off loss. At t_9 , the turn-on signal of Q_1 arrives and this mode ends. This mode equivalent circuit is shown in Figure 6d. In this mode, the turn-off overvoltage and oscillation of Q_1 are suppressed.

Figure 6. Equivalent circuit of each working mode: (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

4. Experimental Verification

In order to verify the advantages of the gate driving circuit proposed in this paper, a double-pulse test platform based on the proposed gate driver was built.

4.1. Design of the Double-Pulse Test Platform

Figure 7 shows the double-pulse test platform based on the proposed gate driver. The double-pulse test platform is composed of a double-pulse circuit, a digital controller and the proposed gate driver. In the double-pulse circuit, the SiC MOSFET and diode are C2M0080120D and C4D20120A produced by Cree. Coaxial shunt produced by T & M Researcher is adopted to ensure the accuracy of current measurement.

Figure 7. Double-pulse test platform based on the proposed gate driver.

Considering that the maximum turn-on driving voltage of the SiC MOSFET is 25 V and the maximum turn-off driving voltage is -10 V, the recommended driving voltage is 20 V to -5 V. Therefore, the proposed drive circuit has a V_{GS} of 24 V and a V_{SS} of -5 V. This not only meets the requirements of the proposed driver, but also ensures that the on-state resistance of the SiC MOSFET is small during the conducting stage. In the driving loop, gate parasitic inductance L_G , common-source parasitic inductance L_{CS} , gate-source junction capacitance C_{GS} and external gate resistance R_G form an LCR resonant circuit, as shown in Figure 8. The overvoltage and oscillation may occur in the gate-source voltage v_{GS} . The gate-source voltage v_{GS} can be calculated according to the Equation (6).

$$(L_G + L_{CS})C_{GS} \frac{d^2 v_{GS}}{dt^2} + R_G C_{GS} \frac{dv_{GS}}{dt} + v_{GS} = V_G \quad (6)$$

Figure 8. Gate drive considering parasitic parameters.

In order to avoid gate-source voltage oscillation, the external gate resistance R_G needs to satisfy inequality (7). The sum of L_{CS} and L_G of the double-pulse circuit is approximately 25 nH, C_{GS} of a C2M0080120D is about 1.2 nF. Therefore, 10 Ω resistor is selected for R_{G3} and R_{G4}

$$R_G \geq 2 \sqrt{\frac{L_G + L_{CS}}{C_{GS}}} \quad (7)$$

In the proposed gate driver, a larger resistor should be selected for R_{G5} and R_{G6} to reduce the overshoot of the SiC MOSFET in Stage 3 and Stage 8. However, the larger R_{G5} and R_{G6} are, the larger the switching loss is. Therefore, it is necessary to balance the overshoot and turn-on loss to select R_{G5} and R_{G6} , a 50 Ω resistor are selected for R_{G5} and R_{G6} . The driving parameters of the proposed gate driver are shown in Table 2.

Table 2. Driving parameters of the proposed gate driver.

Name	Parameters
Main circuit	Input voltage
	400 V/500 V/600 V
Proposed gate driver	Output current
	11 A/16 A/21 A
	V_{GS}
	24 V
	V_{SS}
	−5 V
	R_{G3}
	10 Ω
	R_{G4}
	50 Ω
	R_{G5}
	10 Ω
	R_{G6}
	50 Ω

In order to verify the effectiveness of the proposed gate driver, this paper gives the results of a comparative test performed between the proposed gate driver and traditional gate drivers. The traditional gate driver used different driving parameters, as shown in Table 3.

Table 3. Driving parameters of traditional gate drivers.

Traditional Gate Drivers	Turn-On Stages		Turn-Off Stages	
	Driving Voltage	Gate Resistance	Driving Voltage	Gate Resistance
Driver ¹	24 V	10 Ω	−5 V	10 Ω
Driver ²	19 V	50 Ω	0 V	50 Ω

The PCB of the proposed gate driver is shown in Figure 9. Six nonisolated driver chips (UCC27531) produced by TI were selected as S_1 – S_4 and S_{A1} – S_{A2} . Two isolation chips (ISO7230M) produced by TI are used to ensure effective isolation between the control circuit and the main power circuit. V_{GS} and $-V_{SS}$ are provided by the auxiliary power WRE0512S-3WR2 and WRF0505S-3WR2, respectively. To reduce the space, the SMD resistors of 0603 package are selected as gate resistance. The driving signals for S_1 – S_4 and S_{A1} – S_{A2} are provided by a TMS320F28335 digital signal processor.

Figure 9. Printed circuit board (PCB) of the proposed gate driver.

When using the proposed gate driver, the time of Stage 1–2 and Stage 6–7 must be solved to determine the switching points in Figure 5. The time of these four stages can be obtained by the LTspice simulation or the datasheet of the SiC MOSFET provided by the manufacturer. However, the double-pulse test is the most accurate method to solve the time. This paper used the double-pulse test to solve the time of these four stages. In order to achieve faster switching speed, the proposed gate driver and traditional gate driver have the same driving parameters during these four stages.

Therefore, when the double-pulse test adopts the traditional gate driver, the time of these four stages can be easily measured. Table 4 gives the time of the four stages with traditional driver ¹.

Table 4. Time of Stage 1, Stage 2, Stage 3, Stage 4 with traditional driver.

Switching Stages	Time/ns
Stag 1	18
Stag 2	24
Stag 6	24
Stag 7	20

Table 5 shows the test equipment used for the double-pulse test platform.

Table 5. Test equipment for the double-pulse test platform.

Name	Type	Bandwidth/MHz
Oscilloscope	Tektronix DPO4054B	500
Differential Voltage probe	Tektronix P6139B	500
Passive Voltage probe	Tektronix P2220	200
Coaxial shunt	SSDN-414-025	2500

4.2. Test Results of the Turn-on Process

The turn-on waveforms of the gate-source voltage v_{GS} , drain current i_D , drain-source voltage v_{DS} , and switching loss based on different gate drivers are given in Figure 10, and the experiment was conducted under an input voltage of 600 V and an output current of 21 A.

Figure 10. Switching waveforms based on different gate drivers: (a) Turn-on current waveforms, (b) Turn-on voltage waveforms, (c) Gate driving waveforms, and (d) Turn-on loss waveforms.

The experimental comparison results of the turn-on process are shown in Table 6.

Table 6. Experimental results of the turn-on process based on different gate drivers.

Turn-on Parameters	Driver ¹ (24 V/10 Ω)	Driver ² (19 V/50 Ω)	Proposed Gate Driver
Current spike	32 A	22.7 A	26.6 A
Delay time	18 ns	60 ns	19 ns
Current-rising time	24 ns	164 ns	24 ns
Voltage-dropping time	60 ns	350 ns	129 ns
Turn-on loss	0.203 mJ	2.031 mJ	0.494 mJ

When using a traditional driver with driving parameters of 24 V/10 Ω , the SiC MOSFET has the fastest turn-on speed and the lowest turn-on loss but the highest current spike. When using a traditional driver with driving parameters of 19 V/50 Ω , the turn-on current spike of the SiC MOSFET is reduced by 9.3 A, but the turn-on loss increases by 1.828 mJ. When using the novel drive circuit, the turn-on current spike is reduced by 5.4 A and the turn-on loss is only increased by 0.291 mJ.

4.3. Test Results of the Turn-Off Process

The turn-off waveforms based on different gate drivers are given in Figure 11.

Figure 11. Switching waveforms based on different gate drivers: (a) Turn-off current waveforms, (b) Turn-off voltage waveforms, (c) Gate driving waveforms, and (d) Turn-off loss waveforms.

The experimental comparison results of the turn-off process are shown in Table 7. When using traditional driver with the driving parameter of 24 V/10 Ω , the SiC MOSFET has the fastest turn-off speed, the lowest turn-off loss, but the largest voltage spike. The turn-off voltage spike of the SiC MOSFET is reduced by 145 V when the traditional driver adopts the driving parameter of 19 V/50 Ω , but the turn-off loss increases by 1.496 mJ. When using the proposed gate driver, the turn-off voltage spike is reduced by 105 V and the turn-off loss is only increased by 0.078 mJ.

Table 7. Experimental results of turn-off process based on different gate drivers.

Turn-off Parameters	Driver ¹ (−5 V/10 Ω)	Driver ² (0 V/50 Ω)	Proposed Gate Driver
Voltage spike	765 V	620 V	660 V
Delay time	24 ns	400 ns	25 ns
Voltage-rising time	20 ns	220 ns	19 ns
Current-dropping time	20 ns	290 ns	45 ns
Turn-off loss	0.179 mJ	1.675 mJ	0.257mJ

4.4. Test Results under Different Working Conditions

Figure 12 shows the experimental test results with different gate drivers for respective input voltage and output current of 400 V/11 A, 500 V/16 A, 600 V/21 A. According to the test results, the traditional gate driver with the driving parameters 24 V/10 Ω and −5 V/10 Ω has the highest turn-on overcurrent, highest turn-off overvoltage, fastest switching speed, and lowest switching loss. Although the traditional gate driver with driving parameters 19 V/50 Ω and 0 V/50 Ω can suppress the turn-on overcurrent and turn-off overvoltage of the SiC MOSFET, the switching loss increases rapidly.

Figure 12. Experimental results under the different working conditions: (a) Overshoot current, (b) Overshoot voltage, (c) Turn-on loss, and (d) Turn-off loss.

By comparison, the proposed gate driver can suppress the turn-on overcurrent and turn-off overvoltage of the SiC MOSFET effectively and has little effect on switching loss.

5. Conclusions

This paper analyzed the causes of the turn-on overshoot current, turn-off overvoltage, and switching oscillation of SiC MOSFETs. The analysis results verified that the turn-on overcurrent and turn-off overvoltage can be suppressed by reducing the amplitude of the driving voltage v_p and increasing the external gate resistance. Based on the theoretical analysis, this paper proposed a novel gate driver based on the variable driving voltage and variable gate resistance topology for SiC MOSFETs. The proposed gate driver was tested under different working conditions to verify its suppression effect on the turn-on overcurrent and turn-off overvoltage of SiC MOSFETs. The

experimental test results show that the proposed gate driver can suppress the turn-on overcurrent and turn-off overvoltage of SiC MOSFETs effectively and has little effect on switching loss.

The proposed gate driver can effectively suppress the overvoltage and overcurrent of SiC MOSFETs when compared with the conventional gate drivers. However, it requires five additional digital signals to drive S_1 – S_4 and S_{A1} – S_{A2} . In the future, the manufacturer of the gate driver can integrate the proposed gate drive circuit into an integrated gate driver chip to achieve simple control of the proposed gate driver. This is of great significance to promote the wide use of SiC MOSFETs in high-frequency applications.

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