## Article

# A Single-Phase Buck and Boost AC-to-AC Converter with Bipolar Voltage Gain: Analysis, Design, and Implementation 

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Received: 24 January 2019; Accepted: 5 April 2019; Published: 10 April 2019


#### Abstract

In this research, a new single-phase direct AC-to-AC converter, operating in buck and boost mode, with a bipolar voltage gain, is proposed. The operation is accomplished through high frequency direct and indirect PWM control of a single switch with low voltage stresses. This reduces, not only the control effort, but also the switching losses. The low voltage stresses across the high frequency switches, reduce the $d v / d t$ problem significantly without any loss and bulky voltage snubber arrangement. The operation, in its all-operating modes, has a low inductor ripple current and switching current. The proposed converter may be employed as an AC voltage restorer in a power distribution system to cope with the voltage sag and swell issues. The detailed analysis of the proposed converter is carried out in order to compare its performance with the existing converters. The simulation results obtained using the MATLAB/Simulink environment are verified through experimental results.


Keywords: bipolar voltage gain; direct ac-to-ac converter; PWM control; voltage stresses; voltage sag and swell

## 1. Introduction

Traditionally, in variable AC power system, load voltage and frequency regulation are accomplished with indirect AC-to-AC power converters as reported in [1-3]. They are dual converters, having bulky DC linked capacitor to suppress the ripples in the output voltage of the first conversion stage. This arrangement generates harmonics in the input current, thus causing poor power quality. A filtering inductor filter is employed at the input side to mitigate the generated harmonics. Extra circuit elements (two inductors and capacitors) are employed in z-source arrangement [4] to solve the short problem of the second conversion stage. Indirect AC power converters are complex and have high conversion losses, thus causing poor efficiency. Their reliability is also low, due to an intermediate DC link capacitor [5].

In direct AC-to-AC power converters [6-8], the variable output voltage and the frequency are obtained through a single stage power conversion. These can be implemented as AC voltage
controllers and direct frequency changers (DFC). They offer many advantages, such as simple circuit implementation, easier control, small size, and low price. AC voltage controllers are used to control the dynamic voltage variation in AC power systems. Voltage sags and swells are major disturbances of the power system [9], which degrade the system's performance severely. The end users have to use power-conditioning units and controllers, as reported in [10], to cope with such problems for the safe and proper operation of their equipment. Dynamic voltage restorer (DVR), presented in [11,12], can also be used to solve this problem. They are voltage source inverters (VSI), and can mitigate the voltage sag problem, by injecting ac power through a series connected transformer. They only maintain the amplitude of the input voltage, thereby ignoring the problem of harmonic distortion and phase delay. Therefore, this approach is inefficient and has low reliability.

Single phase direct AC voltage controllers, as proposed in [13], are implemented with PWM control by using a DC-DC complement approach, where a bi-directional current conduction capability is achieved by using bi-directional controlled switches, instead of uni-directional switches. The converters realized with this approach in [14,15], only perform buck, and boost operations, respectively. They have a current commutation problem, due to the overlapping intervals caused by the complementary switches. The filtering capacitors or voltage sources get short-circuited during these intervals, causing a generation of voltage and current surges. This problem increases the power rating of the controlled switches and may cause their failure. The problems caused by the overlapping times are mitigated by inserting the dead-time in the gating sequences of the complementary switches. But this approach limits their switching speed, voltage gain, and hence degrades their power quality. It also makes the switching arrangement complex. The current commutation problems are also solved in [16], by using a coupled inductor approach. This approach only improves the current continuity without improving the voltage gain. This results in an increased power rating of the controlled and uncontrolled devices. The z-source and quasi-z-source converters in $[17,18]$ solve these problems caused by the current commutation. Z-source AC voltage controllers with buck-boost characteristics, as reported in $[19,20]$, mitigate the voltage sag problem up to $25 \%$ in depth. AC voltage controllers to mitigate the voltage sag up to $50 \%$ depth are developed by using inter-phase power conversion approach [21], where the power in faulty phase is injected from other two healthy phases with the help of series connected transformers. All z-source converters require extra circuit elements to solve the problem of current commutation.

The non-z-source AC voltage controllers, in [22-26], eliminate the extra circuit elements but their inverting buck-boost operation requires high voltage switching stresses, high inductor ripple current and high switching currents. This results in high switching, conduction, and filtering of the inductor's DCR resistance losses. High voltage switching stresses also result in high $d v / d t$ problem; so, it increases the voltage rating of the switching devices. Such devices have high internal resistances or forward voltage that also increase the conduction losses. Also, the operation in buck-boost mode has a high voltage and current ripples, thus causing high filtering losses. So, the overall conversion efficiency in these converters is low, due to high conduction and switching losses.

In this research, a novel AC voltage converter is proposed that has $50 \%$ low switching stresses across the high frequency switching devices, in the inverting buck and boost mode, with a duty ratio of 0.5. This results in $50 \%$ low switching losses. The other highlights of this research are no short through problem, caused by the complementary switching devices, low switching, and inductor ripple current. The control effort is reduced by controlling one switch as a direct PWM (DPWM) and the other one as an indirect PWM (IDPWM) control. A detailed analysis is carried out to compare the performance of the proposed topology with existing converters. A hardware setup is developed to validate the simulation results obtained by modelling of proposed converter in the MATLAB/Simulink environment.

## 2. The Proposed AC-to-AC Voltage Converter Circuit Configuration

The proposed converter's circuit consists of one filtering inductor, two capacitors, and eight MOSFET-diode series connected pairs (see Figure 1). All its operating modes are accomplished
through one high frequency DPWM control, one IDPWM control, and two low frequency switches. The remaining four switches are off throughout the operation of the converter. The DPWM switch controls the switching state of IDPWM switch. No voltage develops across the series connected diodes of DPWM control switch, due to the negative voltage at its cathode. So, the reverse voltage is developed across the MOSFET. In IDPWM control switch, as MOSFET remains in a conduction state to avoid the current interruption problem of the inductor, so its series connected diode has to withstand the reverse voltage. The proposed topology comes with the advantage that both the buck and the boost operating modes with non-inverting and inverting characteristics can be realized with the help of just changing the switching states mechanism. The series connection of diode, with MOSFET, eliminates the possible short through of input voltage, output voltage, and paralleling of input and output voltages. For example, the antiparallel arrangement of diodes $D_{S 2}, D_{S 3}$ and $D_{S 5}, D_{S 6}$, avoids the short circuiting of the input, and output voltage, respectively. In the same way, $D_{S 1}$ and $D_{S 4}$ avoid the paralleling of input and output voltages.


Figure 1. Proposed circuit topology.

### 2.1. Non-Inverting and Inverting Buck Operation

The non-inverting and inverting buck operation of the suggested topology is explored in modes ' $A$ ' to ' $D$ ' depending upon sequence of switching signals. The voltage gain is positive and negative in non-inverting and inverting operation respectively as demonstrated in PWM scheme shown in Figure 2. It also depicts their switching sequences for its various operating modes. For example, in non-inverting buck mode (see Figure 2a), the switching signals $g_{1}, g_{4}, g_{5}, g_{6}, g_{7}, g_{8}$ and $g_{2}, g_{3}$ are the low, and high frequency signals, respectively. Its inverting mode may be realized only by changing the connection of the gating signals to switching devices, as depicted in Figure 2b. The detail of its various operating modes is given below through the power transfer path.

### 2.1.1. Operating Mode A

In mode ' $A$ ', the output is non-inverted for a positive input voltage. Figure 2 a illustrates the switching signals to achieve the required target. During this operating mode, the switch $M_{2}$ is controlled in a high frequency PWM manner; the switching devices $M_{3}, M_{5}, M_{4}, D_{S 2}, D_{S 4}$, and $D_{S 5}$ are in on-state, while $M_{1}, M_{6}, M_{7}, M_{8}, D_{S 1}, D_{S 6}, D_{S 7}$, and $D_{S 8}$ are in off-state. The controlled switch $M_{3}$ cannot conduct, due to reverse biasing of its series connected diode $D_{S 3}$. During the turn-on interval of the switch $M_{2}$, the input power is delivered to load via the current conduction path, formed by the switching devices $M_{2}, D_{S 2}$, filtering inductor $L, M_{5}, D_{S 5}, M_{4}$ and $D_{S 4}$, as highlighted
in Figure 3a. In this period, the switching voltages across the DPWM and IDPWM switches are ' 0 ', and ' $V_{i}$ ', respectively. Once the switch $M_{2}$ turns off, the input power is removed from the load and the series-connected diode $D_{S 3}$ becomes forward biased. The energy stored in the inductor is now supplied to load through the current conduction path of the switching devices $M_{3}, M_{5}, M_{4}, D_{S 3}, D_{S 5}$, $D_{S 4}$, as exposed is Figure 3b. In this period, the switching voltage of the DPWM, and IDPWM switches are changed from ' 0 ', ' $V_{i}$ ' to ' $-V_{i}$ ', ' 0 ', respectively. The dynamic state equations of inductor voltage and capacitor current are framed in Equations (1) and (2) during turn-on and -off periods of the PWM control by, applying the KVL and KCL in Figure 3a,b as established in [23]. The duty ratio during switching on and off intervals are represented as $d$, and $d^{\prime}$, respectively.

$$
\begin{align*}
& \left\{\begin{array}{l}
L \frac{d i_{L}}{d t}=d\left(v_{i}-v_{0}\right) \\
C \frac{d v_{o}}{d t}=d\left(i_{L}-i_{0}\right)
\end{array}\right.  \tag{1}\\
& \left\{\begin{array}{l}
L \frac{d i_{L}}{d t}=-d^{\prime} v_{0} \\
C \frac{d v_{o}}{d t}=d^{\prime}\left(i_{L}-i_{0}\right)
\end{array}\right. \tag{2}
\end{align*}
$$

The PWM dynamic average behavior of these state equations is obtained in Equation (3) by adding the right side of Equations (1) and (2).

$$
\left\{\begin{array}{l}
L \frac{d i_{L}}{d t}=d\left(v_{i}-v_{o}\right)-d^{\prime} v_{o}  \tag{3}\\
C \frac{d v_{o}}{d t}=d\left(i_{L}-i_{o}\right)+d^{\prime}\left(i_{L}-i_{o}\right)
\end{array}\right.
$$



Figure 2. Gating sequences for: (a) buck operation for positive voltage gain; (b) buck operation for negative voltage gain.


Figure 3. Parts (a-d) and (e-h) represent the non-inverting and inverting buck operation respectively.

### 2.1.2. Operating Mode B

During the negative half cycle of the input voltage, the positive voltage gain is obtained by applying the high frequency PWM control signal to switch $M_{3}$. In its on interval, the switching devices $M_{6}, M_{1}, M_{2}, D_{S 6}, D_{S 1}$ turn on to connect load with the source as shown in the power flow path shown in Figure 3c. The switch $M_{2}$ remain off, as its series, connected diode $D_{S 2}$ is reverse bias by the ' $V_{i}$ ' volt. During the turn off period of its PWM control, the diode $D_{S 2}$ changes it operating state from off to on as the source voltage is isolated from the load and energy stored in the inductor is delivered to load through the current flow path formed by $M_{1}, M_{2}, M_{6}$, inductor, $D_{S 1}, D_{S 2}$ and $D_{S 6}$ as highlighted
in Figure 3d. The PWM dynamic averaging of this mode is developed in Equation (4) by repeating the steps of mode ' $A$ '.

$$
\left\{\begin{array}{l}
L \frac{d i_{L}}{d t}=d\left(v_{i}-v_{o}\right)-d^{\prime} v_{o}  \tag{4}\\
C \frac{d v_{o}}{d t}=d\left(i_{L}-i_{0}\right)+d^{\prime}\left(i_{L}-i_{o}\right)
\end{array}\right.
$$

The voltage and current transfer ratios of mode ' $A$ ' and ' $B$ ' are obtained in Equation (5) by ignoring the right side of Equations (3) and (4) as they have low variation at low fundamental frequency.

$$
\left\{\begin{array}{l}
\frac{v_{o}}{v_{i}}=d  \tag{5}\\
i_{L}=i_{0}
\end{array}\right.
$$

### 2.1.3. Operating Modes C and D

Similarly, these modes are employed to have a negative voltage gain with any polarity of the input voltage. It is implemented by simply swapping the low frequency control signals $g_{5}$ with $g_{6}$, and $g_{4}$ with $g_{7}$, and $g_{1}$ with $g_{8}$, as can be investigated in its PWM modulation control, as shown in Figure 2b. There is no change in its high frequency PWM signals, $g_{2}$ and $g_{3}$. The detail of switching and inductor voltage in these operating modes is explored with the help of power flow paths in Figure 3e-h, for positive, and negative, input voltage, respectively. Similarly, the PWM dynamic equation, and the voltage and current transfer ratio of these operating modes are expressed in Equations (6) and (7), respectively.

$$
\begin{gather*}
\left\{\begin{array}{l}
L \frac{d i_{L}}{d t}=d\left(v_{i}+v_{o}\right)+d^{\prime} v_{o} \\
C \frac{d v_{o}}{d t}=-d\left(i_{L}+i_{o}\right)-d^{\prime}\left(i_{L}+i_{o}\right) \\
\left\{\begin{array}{l}
\frac{v_{o}}{v_{i}}=-d \\
i_{L}=-i_{0}
\end{array}\right.
\end{array} .\right. \tag{6}
\end{gather*}
$$

The operation of the proposed converter in mode ' $A$ ', ' $B$ ' and ' $C$ ', ' $D$ ' may realize as non-inverting, and inverting, AC voltage compensator, respectively.

### 2.2. Non-Inverting and Inverting Boost Operation

The bipolar voltage gain characteristics of the proposed topology in boost operation is explored in mode ' $E$ ' to ' $F$ ', with respect to the polarity of the input voltage. Their PWM switching modulation strategy is shown in Figure $4 \mathrm{a}, \mathrm{b}$ for non-inverting, and inverting operation, respectively. It is clearly observed from these switching controls that boost operation can be obtained with the switching schemes, developed for the buck operation by changing the connection of the gating signals to the controlled switches. For example, the high frequency PWM signals $g_{2}$ and $g_{3}$ of non-inverting buck now become $g_{5}$, and $g_{6}$, of the none-inverting boost, respectively. The same is true for the reaming low frequency gating signals $g_{1}, g_{4}, g_{5}$, and $g_{6}$. The detail of operating modes with switching and inductor voltage, their corresponding dynamic averaging state equations, and voltage and current transfer ratio are realized in Figure 5, Tables 1 and 2 respectively.


Figure 4. Gating sequences: (a) boost operation for positive voltage gain; (b) boost operation for negative voltage gain.


Figure 5. Cont.


Figure 5. Parts (a-d) and (e-h) represent the non-inverting and inverting boost operation respectively.
Table 1. Operating modes in proposed circuit in boost mode.

| Mode Name | Operating Modes | Switching States |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Low <br> Frequency <br> Switches | OFF Switches | DPWM <br> Control <br> Switch | IDPWM <br> Control <br> Switch |
| $E$ | Non-Inverting <br> Boost with Positive <br> Input | $M_{2}, M_{4}$ | $M_{1}, M_{3}, M_{7}, M_{8}$ | $M_{6}$ | $M_{5}$ |
| $F$ | Non-Inverting <br> Boost with <br> Negative Input | $M_{1}, M_{3}$ | $M_{2}, M_{4}, M_{7}, M_{8}$ | $M_{5}$ | $M_{6}$ |
| $G$ | Inverting Boost <br> with Positive Input | $M_{2}, M_{7}$ | $M_{1}, M_{3}, M_{4}, M_{8}$ | $M_{5}$ | $M_{6}$ |
| $H$ | Inverting Boost <br> with Negative <br> Input | $M_{3}, M_{8}$ | $M_{1}, M_{2}, M_{4}, M_{7}$ | $M_{6}$ | $M_{5}$ |

Table 2. PWM switching average modelling and corresponding transfer ratio for boost operation.

| Non-Inverting Boost Operation | Inverting Boost Operation |
| :---: | :---: |
| $\left\{\begin{array}{l}L \frac{d i_{L}}{d t}=d v_{i}+d^{\prime}\left(v_{i}-v_{o}\right) \\ C \frac{d o_{o}}{d t}=-d i_{o}+d^{\prime}\left(i_{L}-i_{o}\right) \\ \frac{v_{o}}{v_{i}}=\frac{1}{d^{\prime}} \\ \frac{i_{o}}{i_{L}}=d^{\prime}\end{array}\right.$ | $\left\{\begin{array}{l}L \frac{d i_{L}}{d t}=d v_{i}+d^{\prime}\left(v_{i}+v_{o}\right) \\ C \frac{d v_{o}}{d t}=-d i_{o}-d^{\prime}\left(i_{L}+i_{o}\right)\end{array}\right.$ |
| $\frac{v_{0}}{v_{i}}=\frac{-1}{d^{\prime}}$ <br> $\frac{i_{o}}{i_{L}}=-d^{\prime}$ |  |

The AC voltage controller has non-inverting and inverting boost characteristics, which may be realized by operating the suggested converter in modes ' $E$ ', ' $F$ ', and ' $G^{\prime}$, ' $H$ ', respectively. The control of duty cycle regulates their voltage gains. The input current in boost operation is inherently continuous, having low THD than that of buck or buck-boost operation.

The controlling signals of Figures 2 and 4 depict the low control effort as only one switch at any time instant regulates the positive and negative voltage gains with buck and boost characteristics through PWM control. This control also governs the switching states of the IDPWM controlled switches indirectly as their series connected diodes become forward during the turning off periods of the DPWM switches. These switching characteristics simplify the control algorithms. The switching losses of the high frequency devices are lower at any instant of time, as only one switch is operated at low switching voltage and hence it improves the conversion efficiency.

## 3. Performance Evaluation with Existing Converters

The performance parameters of the proposed converter are computed to compare its performance evaluation with the existing converters in terms of voltage stresses, switching losses, inductor ripple and peak switching current as discussed below.

### 3.1. Voltage Stresses Across Switching Devices

Bipolar voltage gain in proposed converter is obtained through the high frequency switching action of $M_{2}, M_{3}$ for buck and $M_{5}, M_{6}$ for boost operation. The peak switching voltage across the high frequency-controlled switches operating in non-inverting and inverting buck and boost are given in Equation (8).

$$
\left\{\begin{array}{l}
V_{M 2, M 3(\text { peak })}=V_{D S 2, D S 3(\text { peak })}=\sqrt{2} V_{i}  \tag{8}\\
V_{M 5, M 6(\text { peak })}=V_{D S 5, D S 6(\text { peak })}=\sqrt{2} V_{o}
\end{array}\right.
$$

Similarly, the maximum voltage stresses of the high frequency-controlled switches in inverting buck-boost mode of [22] are computed in Equation (9).

$$
\begin{equation*}
V_{M 3, M 4(\text { peak })}=V_{D S 3, D S 4(\text { peak })}=\sqrt{2}\left(V_{i n}+V_{o}\right) \tag{9}
\end{equation*}
$$

As can be seen from Equations (8) and (9) that the proposed converter has $50 \%$ low switching stresses with voltage gain of 0.5 and 2 for inverting buck and boost mode respectively. So, the proposed converter has low voltage rating, low $d v / d t$ problem and low switching losses.

### 3.2. Inductor Ripple and Switching Currents

The comparison of inductor ripple and switching currents is carried for the voltage gain of 0.5 and 2 for buck and boost mode respectively.

$$
\begin{align*}
& \left\{\begin{array}{l}
\Delta i_{\text {Lpeak,proposed }(\text { Buck })}=0.25\left(\frac{\sqrt{2} V_{i, p e a k}}{L} T\right) \\
\Delta i_{\text {Lpeak,proposed }(\text { Boost })}=0.5\left(\frac{\sqrt{2} V_{i, \text { peak }}}{L} T\right)
\end{array}\right.  \tag{10}\\
& \left\{\begin{aligned}
\Delta i_{\text {Lpeak, }[22](\text { Buck })} & =0.333\left(\frac{\sqrt{2} V_{i, \text { peak }}}{L} T\right) \\
\Delta i_{\text {Lpeak, }[22](\text { Boost })} & =0.667\left(\frac{\sqrt{2} V_{i, \text { peak }}}{L} T\right)
\end{aligned}\right.  \tag{11}\\
& \left\{\begin{array}{l}
I_{S w(\text { peak })-\operatorname{proposed}(\text { Buck })}=\sqrt{2} \frac{P_{0}}{V_{o}} \\
I_{S w(\text { peak })-\operatorname{proposed}(\text { Boost })}=2 \sqrt{2} \frac{P_{0}}{V_{o}}
\end{array}\right.  \tag{12}\\
& \left\{\begin{array}{l}
I_{S w(\text { peak })-[22](\text { Buck })}=3 \frac{P_{0}}{\sqrt{2} V_{o}} \\
I_{S w(\text { peak })-[22](\text { Boost })}=3 \sqrt{2} \frac{P_{0}}{V_{o}}
\end{array}\right. \tag{13}
\end{align*}
$$

The analysis and comparison from Equations (10) to (13) explores that the proposed converter has low inductor ripple and switching current having low conduction losses and low losses in the DCR resistance of filtering inductor. These losses are proportional to the magnitude of the conducting currents. They also depend on their internal resistances and forward voltage drops. Low switching voltage devices have low on-state resistances and forward voltage drops. The proposed topology has low conduction losses due to low conduction current and switching voltage as can be observed from Equations (10) to (13). The quality of the output voltage depends on the ripple voltage that is improved due to low inductor ripple current. In addition, during the short through intervals, the output is distorted. Therefore, absence of short through problem and low ripples improve the power quality of the output voltage.

### 3.3. Switching Losses

The switching losses of a MOSFET depend on switching voltage, current, switching frequency, output capacitance, rise and fall time as reported in [23]. These losses in fast recovery diode depend on its reverse recovery characteristics as in [23]. They are also proportional to number of high-frequency switching devices and voltage gain. The switching losses of DPWM control switch only come from the switching of MOSFET as its series connected diode is forward biased due to negative reverse voltage. The switching losses of IDPWM controlled switch are only due to reverse biasing of diode as MOSFET is kept turned on to ensure the continuous conduction of inductor current.

The buck operation of the proposed circuit is implemented with high frequency PWM control of $M_{2}\left(M_{3}\right)$ and $D_{S 2}\left(D_{S 3}\right)$. The total switching losses of the proposed converter and the converter in [22] in inverting mode are computed by assuming same switching current and constant input voltage in Equations (14) and (15) respectively.

$$
\begin{gather*}
\left\{\begin{array}{c}
P_{s w-b u c k(\text { proposed })}=f_{s w}\left[\frac{1}{4}\left\{I_{L} V_{i}\left(t_{o n}+t_{o f f}\right)+C_{o s} V_{i}^{2}\right\}+\frac{2 Q_{R R}}{\pi} V_{i}\right] \\
P_{s w-b o o s t(\text { proposed })}=f_{s w}\left[\frac{1}{4}\left\{I_{L} G_{V} V_{i}\left(t_{o n}+t_{o f f}\right)+C_{o s}\left(G_{V} V_{i}\right)^{2}\right\}+\frac{2 Q_{R R}}{\pi} G_{V} V_{i}\right]
\end{array}\right.  \tag{14}\\
P_{s w-b u c k-b o o s t[21]}=f_{s w}\left[\frac{1}{4}\left\{I_{L} V_{i}\left(1+G_{V}\right)\left(t_{o n}+t_{o f f}\right)+C_{o s} V_{i}^{2}\left(1+G_{V}\right)^{2}\right\}+\frac{2 Q_{R R}}{\pi} V_{i}\left(1+G_{V}\right)\right] \tag{15}
\end{gather*}
$$

where $f_{s w}$ is switching frequency, $I_{L}$ is the switching current, $C_{o s}$ is output capacitance of MOSFET, $Q_{R R}$ is the reverse recovery charge of series connected fast recovery diode, $V_{i}$ is the input voltages, and $G_{V}$ is the voltage gain. The proposed converter has $50 \%$ low switching losses than that of converter in [22] during buck and boost operation with voltage gain of 0.5 and 2 respectively.

### 3.4. Conduction Losses

The conduction losses of a MOSFET-diode pair depend on their forward voltages and resistances. They also depend on their conduction currents. The conduction losses of the proposed topology and converter in [22] are realized in Equations (16) and (17) for voltage gain of '2' respectively, where $R_{T}$ and $R_{d}$ are on-state resistances of MOSFET and diode respectively whereas $V_{d}$ is the forward voltage of the diode.

$$
\begin{gather*}
P_{\text {Cod }(\text { proposed })}=\frac{12 V_{d} I_{o}}{\pi}+6 I_{o}^{2}\left(R_{T}+R_{d}\right)  \tag{16}\\
P_{\operatorname{Cod}([22])}=\frac{18 V_{d} I_{o}}{\pi}+13 I_{o}^{2}\left(R_{T}+R_{d}\right) \tag{17}
\end{gather*}
$$

The above comparison depicts that the proposed topology has low conduction losses.
In a summary, the comparison of the proposed topology with the existing converter in [22] is detailed in Tables 3 and 4 for buck and boost mode respectively. For the sake of making comparison simple, terms involving $C_{o s}$ are neglected.

Table 3. Comparison of performance parameters in buck mode.

| Inverting Buck Operation with Voltage Gain of 0.5 |  |  |  |
| :---: | :---: | :---: | :---: |
| Description | Proposed Converter | Converter in [22] | Comparision |
| Voltage stresses across high frequency switches | $\begin{gathered} V_{M 2, M 3(\text { peak })}=\sqrt{2} V_{i} \\ V_{D S 2, D S 3(\text { peak })}=\sqrt{2} V_{i} \end{gathered}$ | $\begin{gathered} V_{M 3, M 4(\text { peak })}=\frac{3 \sqrt{2} V_{i}}{2} \\ V_{D S 3, D S 4(\text { peak })}=\frac{3 \sqrt{2} V_{i}}{2} \end{gathered}$ |  |
| Peak inductor ripple current | $\begin{gathered} \Delta i_{\text {Lpeak }}= \\ 0.25\left(\frac{\sqrt{2} V_{i, \text { peak }}}{L} T\right) \end{gathered}$ | $\begin{gathered} \Delta i_{\text {Lpeak }}= \\ 0.334\left(\frac{\sqrt{2} V_{i_{\text {peak }}}}{L} T\right) \end{gathered}$ | $\frac{\Delta i_{\text {Lpeak }[22]}}{\Delta i_{\text {Lpeak }[\text { Proposed }]}}=\frac{0.334}{0.25}$ |
| Peak switching device current | $I_{S w(\text { peak })}=\sqrt{2} \frac{P_{0}}{V_{o}}$ | $I_{S w(\text { peak })}=2 \sqrt{2} \frac{P_{0}}{V_{0}}$ |  |
| Switching power losses | $\begin{gathered} P_{s w}= \\ f_{s w}\left[\begin{array}{c} \frac{1}{4}\left\{I_{L} V_{i}\left(t_{o n}+t_{o f f}\right)\right\} \\ +\frac{2 Q_{R R}}{\pi} V_{i} \end{array}\right. \end{gathered}$ | $\begin{gathered} P_{s w}= \\ ]^{\frac{3}{2} f_{s w}}\left[\begin{array}{c} \frac{1}{4}\left\{I_{L} V_{i}\left(t_{o n}+t_{o f f}\right)\right\} \\ +\frac{2 Q_{R R}}{\pi} V_{i} \end{array}\right] \end{gathered}$ | $\frac{P_{s v[2]]}}{P_{s v[\mid \text { Propsese] }}}=\frac{3}{2}$ |

Table 4. Comparison of performance parameters in boost mode.

| Inverting Boost Operation with Voltage Gain of 2 |  |  |  |
| :---: | :---: | :---: | :---: |
| Description | Proposed Converter | Converter in [22] | Comparision |
| Voltage stresses across high frequency switches | $\begin{gathered} V_{M 5, M 6(\text { peak })}=2 \sqrt{2} V_{i} \\ V_{D S 5, D S 6(\text { peak })}=2 \sqrt{2} V_{i} \end{gathered}$ | $\begin{gathered} V_{M 3, M 4(\text { peak })}=3 \sqrt{2} V_{i} \\ V_{D S 3, D S 4(\text { peak })}=3 \sqrt{2} V_{i} \end{gathered}$ | $\begin{aligned} & V_{M 3, M 4(\text { peak })}=\frac{3}{2} \\ & V_{D S 3,, 23(\text { peak })} \\ & V_{D(\text { peak })} \end{aligned}=\frac{3}{2}$ |
| Peak inductor ripple current | $\begin{gathered} \Delta i_{\text {Lpeak }}= \\ 0.5\left(\frac{\sqrt{2} V_{i \text { peak }}}{L} T\right) \end{gathered}$ | $\begin{gathered} \Delta i_{\text {Lpeak }}= \\ 0.667\left(\frac{\sqrt{2} V_{i \text { peakk }}}{L} T\right) \end{gathered}$ | $\frac{\Delta i_{L_{\text {peak }}[2]}}{\Delta i_{\text {Lpeak }} \mid \text { rroposecel] }}=\frac{0.667}{0.5}$ |
| Peak switching device current | $I_{S w(\text { peak })}=3 \frac{P_{0}}{\sqrt{2} V_{o}}$ | $I_{S w(\text { peak })}=3 \sqrt{2} \frac{P_{0}}{V_{0}}$ | $\frac{I_{s w(p e a k}[22]}{I_{S w(p e a k)}[\text { Proposeded] }}=\frac{3}{2}$ |
| Switching power losses | $\begin{gathered} P_{s w}= \\ 2 f_{s w}\left[\begin{array}{c} \frac{1}{4}\left\{I_{L} V_{i}\left(t_{o n}+t_{o f f}\right)\right\} \\ +\frac{2 Q_{R R}}{\pi} V_{i} \end{array}\right. \end{gathered}$ |  | $\frac{P_{s t([\mid 2]}}{P_{s w l}[\text { Proposed] }]}=\frac{3}{2}$ |

## 4. Simulation Results and Discussion

The validity of the proposed research is explored by modeling the proposed converter in MATLAB/Simulink environment to find the switching stresses across high frequency switching devices.

### 4.1. Voltage Stresses of Switching Devices

To find the voltage stresses across the high frequency switches in buck and boost modes with bipolar voltage gain, the proposed converter is simulated with peak input voltage, and frequency of 65 V , and 50 Hz respectively. In buck operation, the output voltage is half than the source voltage, both in non-inverting and inverting modes, as the duty cycle for PWM controlled switches is taken as 0.5. The situation is displayed in Figure 6a,b. Similarly, with duty ratio of 0.5 (thus, with voltage gain of 2) for boost operation, the output voltage becomes two times the input voltage as depicted in Figure $6 \mathrm{c}, \mathrm{d}$. This implies that output voltage is linearly related with the duty ratio. The output voltage is in phase and out of phase with the input voltage as voltage gain is positive and negative respectively.


Figure 6. Input (black) and output (red) voltage (a) non-inverting buck mode; (b) inverting buck mode; (c) non-inverting boost mode; (d) inverting boost mode.

In addition, from the analysis of Figure 7a-d, it is clear that voltage stresses in buck and boost modes are restricted to $V_{i}$, and $V_{o}$, respectively, as compared to the existing converters, which are $V_{i}+V_{o}$. The switching stresses are complementary, as when one switch operates as DPWM, the other as IDPWM. It ensures low switching losses and improved conversion efficiency.


Figure 7. Voltage stresses across (a) $M_{2}\left(D_{S 2}\right) ;$ (b) $M_{3}\left(D_{S 3}\right) ;$ (c) $M_{5}\left(D_{S 5}\right)$; (d) $M_{6}\left(D_{S 6}\right)$.

### 4.2. Conversion Losses and Efficiency

The total conversion losses of the proposed topology come from switching and conduction losses of the high and low frequency switching devices respectively. The conversion losses of the proposed converter, and converter in [22], are compared through the simulation results. The system parameters (taken from the datasheet) considered for the simulation purposes are the followings: $Q_{R R}=1 \mathrm{uC}$,
$V_{d}=1 \mathrm{~V}, R_{T}=0.08 \Omega, R_{d}=0.006 \Omega, t_{r}=30 \mathrm{~ns}, t_{f}=50 \mathrm{~ns}$, and $f_{s w}=50 \mathrm{kHz}$. Figure 8 depicts the comparison of conversion losses and efficiency.


Figure 8. Comparison for (a) switching losses; (b) conduction losses; (c) total power losses; (d) conversion efficiency.

The proposed topology comes with the advantages of low voltages and currents in the switching devices. It ensures low switching and conduction losses that result in improved conversion efficiency, as can be observed from the simulation results depicted in Figure 8.

## 5. Practical Validation

An experimental setup (see Figure 9) is built for further verification of the proposed converter. It includes eight power MOSFETs (IRF840), eight fast recovery diodes (RHRG3040), one filtering inductor of 1 mH , and two capacitors of $4.7 \mu \mathrm{~F}$, and $1 \mu \mathrm{~F}$ for output, and input filter respectively. A step-down $230 / 50 \mathrm{~V} 50 \mathrm{~Hz}$ transformer is used to bring the voltage at safe level for laboratory prototype. STM microcontroller generates the gating signals for the controlled switches. A zero-crossing detector synchronizes the gating signals with respect to the input voltage waveform. Six hybrid chips (EXB840), with six isolated DC supplies are used as gate drivers for MOSFETs. The input voltage is 65 V peak at supply frequency of 50 Hz for buck and boost operation. The duty cycle of the high frequency ( 50 kHz ) switches is maintained at $50 \%$ both for the buck and boost mode.


Figure 9. Hardware Setup.

## Buck and Boost Operation

The non-inverting and inverting buck and boost modes of the proposed converter are implemented, using two high and four low frequency switches, during a complete cycle of the source voltage. So only six control signals can implement all operating modes of the proposed converter just by changing their position to the controlled switches. Figure 10a-d illustrate the practically recorded waveforms of the output voltage in buck and boost mode with inverting and non-inverting characteristics. The in phase and out of phase output voltage depicts the positive and negative voltage gain respectively. Figure 11 shows the switching voltage across the high frequency switching devices.


Figure 10. Input (blue) and output (red) voltage (a) non-inverting buck mode; (b) inverting buck mode; (c) non-inverting boost mode; (d) inverting boost mode.


Figure 11. Voltage stresses across (a) $M_{2}\left(D_{S 2}\right) ;(\mathbf{b}) M_{3}\left(D_{S 3}\right) ;$ (c) $M_{5}\left(D_{S 5}\right) ;(\mathbf{d}) M_{6}\left(D_{S 6}\right)$.
As in the simulation results, the experimental results presented in Figure 11a-d confirm that the switching stresses, in the buck and boost operation, do not exceed the input, and output voltage, respectively. The inductor current in the boost mode is larger than that of its buck operation. It increases the voltage drops in the switching devices, thus causing lower output voltage and efficiency. In non-inverting and inverting boost mode, the inductor current is continuous with a low THD as it is conducted through the inductor and load in turn on and off intervals of switching period (see Figure 12). Therefore, these characteristics improve its power quality.


Figure 12. (a) Input current (blue) with reference of input voltage (red) in boost mode; (b) power quality analysis of the input current.

## 6. Conclusions

A novel AC voltage controller, operating in separate buck and boost mode, with a bipolar voltage gain, is proposed in this research. In all operating modes of the proposed topology, the voltage stresses across the high frequency switches, are reduced to $50 \%$, with the duty ratio of 0.5 . The high switching frequency control effort is also reduced by implementing all operating modes with one DPWM and one IDPWM control switch. Each operating mode requires the conduction of two low frequency switches having a low internal resistance and forward voltage. The proposed topology, not only offers less voltage stresses across the high frequency switches but also reduced peak inductor ripple current, peak switching device current, and conversion losses (switching and conduction power losses), thus improved efficiency compared to the other topology reported in literature. The devices with low voltage and current ratings can be utilized, due to the reduced voltage stresses. A low ripple in the output voltage and the absence of short through issues, improve the power quality of the output voltage. The hardware implementation of the proposed converter validates the simulation results obtained in the MATLAB/Simulink environment.

Author Contributions: N.A., T.I. and G.A. suggested the idea, performed the simulations and experiments. V.E.B., M.M.B., T.-C.L. and M.U.A assisted in the idea development and paper writing-review and editing. U.F. and J.G. managed the paper.
Funding: This research received no external funding.
Conflicts of Interest: The authors declare no conflict of interest.

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