

Article

Novel Step-Down DC–DC Converters Based on the Inductor–Diode and Inductor–Capacitor–Diode Structures in a Two-Stage Buck Converter

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Abstract: This paper explores and presents the application of the Inductor–Diode and Inductor–Capacitor–Diode structures in a DC–DC step-down configuration for systems that require voltage adjustments. DC micro/picogrids are becoming more popular nowadays and the study of power electronics converters to supply the load demand in different voltage levels is required. Multiple strategies to step-down voltages are proposed based on different approaches, e.g., high-frequency transformer and voltage multiplier/divider cells. The key question that motivates the research is the investigation of the aforementioned Inductor–Diode and Inductor–Capacitor–Diode, current multiplier/divider cells, in a step-down application. The two-stage buck converter is used as a study case to achieve the output voltage required. To extend the intermediate voltage level flexibility in the two-stage buck converter, a second switch was implemented replacing a diode, which gives an extra degree-of-freedom for the topology. Based on this modification, three regions of operation are theoretically defined, depending on the operational duty cycles δ_2 and δ_1 of switches S_2 and S_1 . The intermediate and output voltage levels are defined based on the choice of the region of operation and are mapped herein, summarizing the possible voltage levels achieved by each configuration. The paper presents the theoretical analysis, simulation, implementation and experimental validation of a converter with the following specifications; 48 V/12 V input-to-output voltage, different intermediate voltage levels, 100 W power rating, and switching frequency of 300 kHz. Comparisons between mathematical, simulation, and experimental results are made with the objective of validating the statements herein introduced.

Keywords: DC–DC converter; experimental verification; Inductor–Diode; Inductor–Capacitor–Diode; nonisolated; step-down; two-stage buck converter; voltage regulation

1. Introduction

In the last century, AC systems predominated as the most widespread method for energy generation, transmission, and distribution. For regular AC generation, large power plants, e.g., coal, hydro, and nuclear, have been used to centrally generate energy. Alternatives, such as wind and solar generation, are more frequently being installed to decentralize the energy production and lower the CO₂ emitted by the energy production [1,2].

Wind farms (AC generation) are more common in remote regions (on and off-shore) where the wind is conducive for generation. Solar (DC generation), on the other hand, started to become viable

for application in high populated areas where the sun irradiation is high enough to achieve maximum power generation. DC systems started to be developed and implemented in pilot projects and real applications because they have proved to be more efficient than AC systems in terms of transformation steps [3], costs [4], and power transfer capability [5]. Applications of DC system such as in micro- and nanogrids [6,7], datacenters [8,9], and aircrafts, where redundancy and backup is mandatory, are currently on the rise. DC system technology can also be implemented in isolated/remote/emerging regions [10]. In these systems, redundancy normally is indispensable in order to keep the system operational even if a component and/or a converter fails. Furthermore, DC loads are common especially in low voltage/low power applications, for instance, in computer and battery chargers, USB and USB-C ports, and LED lights. These type of loads are commonly found in offices and residences.

Discussions among the voltage levels that are implemented in these systems are extensively presented in the literature [11], for instance, with a voltage between 350 and 400 V for distribution in unipolar or bipolar [6,12,13] DC configurations to supply high power equipments. The 48 V level is [14,15] normally adopted as an intermediate bus stage to supply the low voltage/low power loads aforementioned. The 48 V level is also getting more common in battery systems for Electric Vehicles (EV), and it is considered for residential applications due to its user safety approach.

A DC picogrid, based on state-of-the-art architectures [3,6,16], is depicted in Figure 1, which emulates a building and/or residence with a DC grid implementation. In this grid, a bipolar DC network is realized (P0N poles), which has the possibility of injecting the energy generated by the panels in the AC grid or, alternatively, directly supply DC loads bypassing the DC-AC-DC transformation.

A lot of effort has been spent to propose new topologies and systems to interconnect PV generation in AC or DC grids with, respectively, microinverters [17–19] and microconverters (DC power optimizers) [20–24] which, in essence, are step-up converters since the PV panel output voltage is lower than the AC grid or DC bus voltages. The control aspects of this system and MPPT strategies are common subjects in the literature [20,25–27].

Different strategies to step-up the voltage have been studied and proposed in the literature, such as: isolated step-up topologies [17,21,28], coupled-inductor, nonisolated topologies [29–35], nonisolated topologies with Capacitor-Diode/switch structure [19,36–38], nonisolated topologies with Inductor-Diode/switch [39,40] and nonisolated topologies with Capacitor-Diode/switch and Inductor-Diode/switch structures [41,42]. These structures are known, respectively, as switched-capacitors and switched-inductors. An adaptation of the Inductor-Diode structure is proposed in [43], where a capacitor replaces one diode and changes the gain of the structure for step-up applications. Each of the above-mentioned strategies to step-up voltages has its advantages and disadvantages. For instance, isolated topologies and coupled inductor topologies have the flexibility of, based on the turns ratio of the magnetic device, select the suitable output voltage requirement, although it is known that these magnetic components are, together with heatsinks, the bulkiest components in a converter. Switched capacitor and switched inductors do not bring this flexibility once the gain is defined based on the operational duty cycle of the active switches. Inductors are more reliable components than capacitors, giving an advantage in terms of reliability, while capacitors are more compact and more suited for high power density applications.

In step-down conversion ratio converters, the Capacitor-Diode/switch structures are commonly used to improve the step-down ratio of the converters [44–46]. On the other hand, the implementation of an Inductor-Diode/switch and Inductor-Capacitor-Diode structures in the step-down conversion ratio is not extensively discussed in the literature, with few exceptions that explore both step-up and step-down structures [39]. The structures evaluated in this paper are shown in Figure 2. The Inductor-Diode structure shown in Figure 2 can offer a redundant path if one diode of the structure fails in open-circuit, as proposed in [47]. In steady-state, the inductors can be considered as current sources and, due to the structure operability discussed in Section 4, mitigate the implementation of current sensors for control purposes, since the current balance between the inductors is naturally

achieved without any control strategy (switched-inductor characteristic). The only sensor that might be considered for implementation is a voltage sensor, if the application requires a regulated and constant output voltage level for the entire load range of operation. For instance, a contraction technique was proposed to control a regular step-down converter [48].

With these considerations, the objective of this paper is to investigate the influence of the Inductor–Diode (ID) and Inductor–Capacitor–Diode (ICD) structures in the step-down conversion stage from 48 V to 12 V input-to-output voltage. The main contributions of this paper are (1) an analysis of the influence of the ID and ICD structures in a step-down conversion system; (2) the presentation of a full theoretical analysis of the converters generated; (3) applying the ID and ICD structures in a quadratic buck converter; (4) analyzing the intermediate voltage level behavior for different operational points, showing the intermediate voltage flexibility of the circuit, which is beneficial for a voltage regulation point of view; (5) creating a flexible test bench to be able to validate the proposed converters and; (6) experimentally validation with waveforms of the topologies studied in the paper.

The paper is organized as follows; Section 2 presents the analysis of the ID and ICD structure in a regular single-stage buck converter and its impact on the gain of the converter. Section 3 presents the two-stage buck converter, known as quadratic buck converter [49], to enable the converter applying the ID and ICD structures to achieve the required output voltage levels. The operational principle of the topologies generated by the proposed intra-exchangeability is explained in Section 4. Section 5 explores the simulation results of the proposed topologies, showing the intermediate and output voltage levels that are obtained for each possible configuration. Section 6 describes the experimental test bench built for further validation, showing experimental waveforms that validate the theoretical analysis presented in Sections 3 and 4. Section 7 presents the main conclusions and future work suggestions.

2. Impact of Inductor–Diode and Inductor–Capacitor–Diode Structures in a Step-Down Converter

This section has the objective of investigating the influence of the ID and ICD structure in a step-down buck converter. Inductor L , shown in Figure 3, is replaced by ID and ICD structures and the PWM modes are described herein. The main difference between the ID and ICD structures is that the capacitor of the ICD is also charged during the magnetization of the inductors. When discharging, the capacitor also discharges, providing energy to the load. The capacitor stores part of the energy that is delivered to the load, which helps decrease the size of the inductors, since less energy is stored in their magnetic field. Additionally, the capacitor changes the voltage applied across the inductors during demagnetization, which changes the gain of the structures, as described herein.

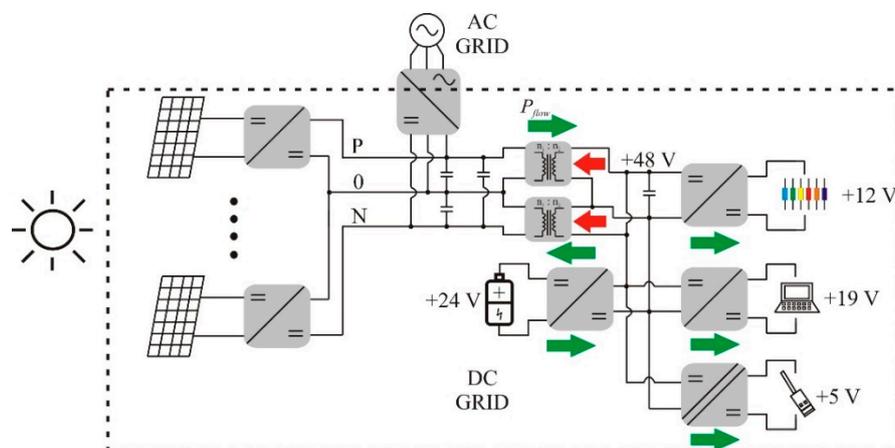


Figure 1. A basic DC picogrid, highlighting the PV generation and DC step-up conversion; the bipolar DC network (P0N); the battery energy storage system (BESS); and the DC loads supplied by DC–DC step-down converters.

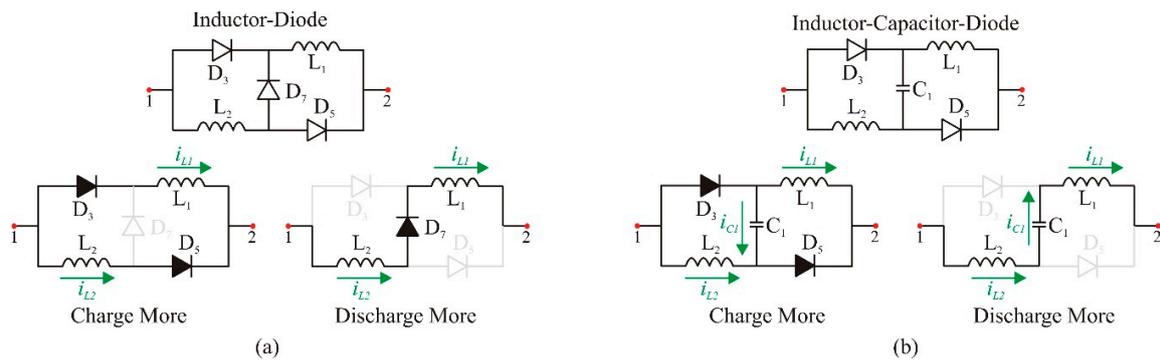


Figure 2. (a) Inductor–Diode (ID) structure and its charge and discharge modes and (b) Inductor–Capacitor–Diode (ICD) structure and its charge and discharge modes.

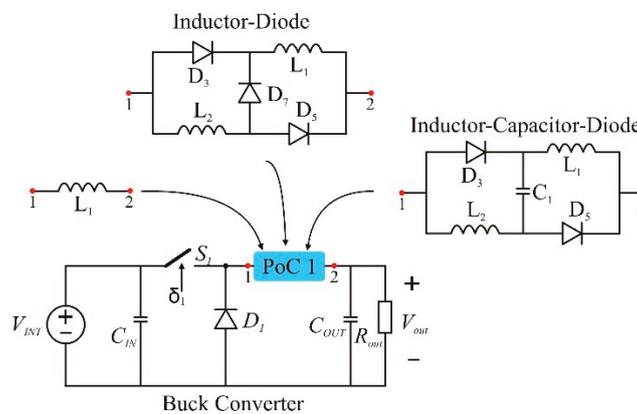


Figure 3. DC–DC Buck Converter with Point-of-Connection 1 (PoC1) to interchange inductor (I), Inductor–Diode (ID) and Inductor–Capacitor–Diode (ICD) structures.

2.1. PWM Mode 1

In this PWM mode, the switch S_1 commutates from ‘open’ to ‘close’, changing the equivalent circuit of the converter. The equivalent circuit for this mode is shown in Figure 4a,b for the ID and ICD applications in PoC1, respectively. During this mode, the voltage applied in the inductor terminals V_{L1} and V_{L2} is positive, due to the step-down mechanism, and energy is magnetically stored in the inductors during the process. The voltage applied across the inductors terminals has the same level (internally in ID and ICD structures), which leads to similar current level in the inductors of the structures. In the ID structure, the inductors store energy during this PWM Mode while in the ICD structure the inductors and the capacitor of the structure store energy.

2.2. PWM Mode 2

In this PWM mode, the switch S_1 commutates from ‘close’ to ‘open’. The equivalent circuit for this mode is shown in Figure 4c,d for the ID and ICD structures, respectively. During this PWM mode, the voltage applied across the inductors terminals V_{L1} and V_{L2} is negative, since diode D_1 is forward biased, leading to a demagnetization of these inductors. The current across both inductors is equal as these components are in series, which guarantees the same negative voltage level across the inductors of the structures during the demagnetization. The demagnetization mechanism for both structures is similar, since in both structures the inductors are connected in series and the same current flows through the passive components.

From the above PWM mode analysis, the theoretical voltage profile for all the inductors in both structures are presented in (1). These equations are applied in (2) to obtain the conversion gain of the structures, in steady-state.

$$\left\{ \begin{array}{l} V_{L1} = V_{L2} = V_{IN} - V_{OUT} \text{ during } \delta_1 \\ V_{L1} = V_{L2} = -\frac{V_{OUT}}{2} \text{ during } (1 - \delta_1) \end{array} \right. \quad \begin{array}{l} ID \\ ICD \end{array} \quad \left\{ \begin{array}{l} V_{L1} = V_{L2} = V_{C1} = V_{IN} - V_{OUT} \text{ during } \delta_1 \\ V_{L1} = V_{L2} = \frac{V_{IN}}{2} - V_{OUT} \text{ during } (1 - \delta_1) \end{array} \right. \quad (1)$$

$$\overline{V}_L = \int_0^{T_s} v_L dt = 0 \quad (2)$$

2.3. Theoretical Gain in Continuous Conduction Mode

To obtain the theoretical voltage gain profile of the topologies, operation in steady-state is considered, which allows the application of (1) in (2) to obtain the ideal gain of the structures. After some mathematical manipulation, the theoretical expression that represents the gain of the Inductor–Diode (ID) and Inductor–Capacitor–Diode (ICD) structures, respectively, is graphically represented in Figure 5. From Figure 5, it is noticed that the operational voltage range tackled in this paper cannot be realized with the ICD structure, since its gain range is, ideally, between [0.5 ; 1]. To overcome this, the quadratic buck converter—a nonlinear step-down converter generated by two buck converters connected in series with each other—as depicted in Figure 6, is the base topology used to generate the converters proposed in this paper. This converter presents an intermediate stage, giving an extra degree of freedom for implementation, since two voltage levels are generated in the same converter and both can be used to supply loads.

Only one switch is implemented on the power stage of the conventional quadratic buck, which has the benefit of control strategy simplification; and the intermediate voltage level is in the function of the duty cycle applied to switch S_1 . If a second switch is introduced in the power stage, the degree of freedom for voltage regulation in the intermediate stage is guaranteed by the duty cycle of the second switch S_2 , although the control strategy might increase in complexity, if applicable. Since the objective of the topologies is to improve the flexibility of the conversion ratio and the overall system, the quadratic buck with two switches is the converter that will be extensively explored in the next section, together with the intra-exchangeable PoC structures presented in Figure 3.

3. Double-Switch Two-Stage Quadratic Buck Converter for Voltage Regulation

As previously mentioned, the two-stage buck converter, most known as quadratic buck converter, is the base topology used for the intra-exchangeable methodology used herein for testing multiple configurations, based on the ID and ICD structures, applied for voltage regulation. Since a second stage is now implemented in the power circuit, the intra-exchangeability increases the amount of topologies that can be generated. More specifically, with three structures and two stages, the number of topologies generated is $3^2 = 9$, where only the conventional quadratic buck is already explored in the literature. Figure 6 exemplifies the possible configurations that can be obtained from the proposed intra-exchangeability between a regular inductor (I) and the ID and ICD structures. When an I structure is connected to PoC1 and PoC2, the regular quadratic buck is obtained. In total, nine topologies are generated from this method and, since two switches are implemented in the power stage with independent duty cycles, three regions of operation can be explored and will be briefly discussed herein. The regions of operation are highlighted in Figure 6, named as region 1, when duty cycle δ_2 is higher than duty cycle δ_1 ; region 2, when δ_1 is higher than δ_2 ; and region 3, when both duty cycles are equal. The switch realization is based on a MOSFET with an antiparallel diode, as shown in Figure 6.

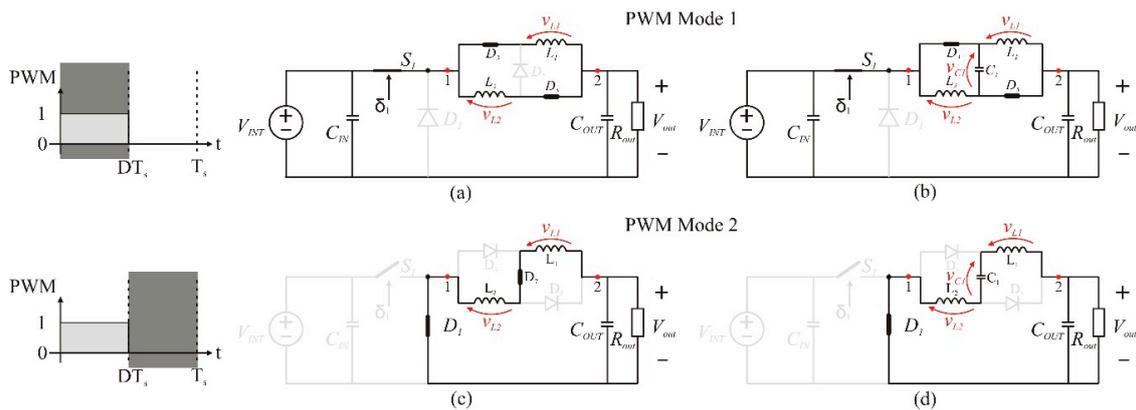


Figure 4. (a) PWM mode 1 for ID structure; (b) PWM mode 1 for ICD structure; (c) PWM mode 2 for ID structure, and (d) PWM mode 2 for ICD structure.

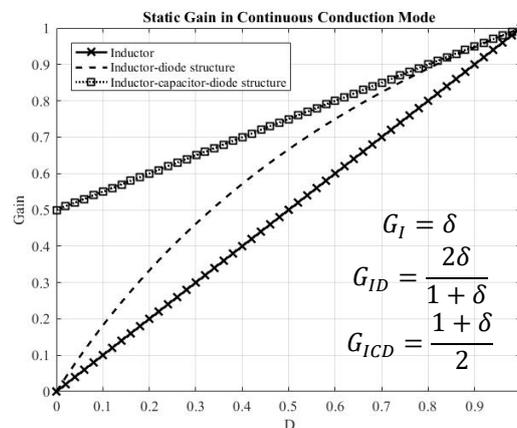


Figure 5. Continuous conduction mode graphical gain representation.

3.1. Region 1 ($\delta_2 > \delta_1$)

Operating in Region 1, the two stages of the quadratic buck structure operate independently, leading to intermediate and output voltages, depending on the duty cycles δ_2 and δ_1 . The intermediate voltage across capacitor C_{inter} depends on the structure connected in PoC2 and the duty cycle δ_2 to command switch S_2 . The output voltage, on the other hand, depends on both structures connected in PoC2 and PoC1, since the intermediate voltage level is the input voltage of the first stage. The equations presented in Figure 5 are reused to find the intermediate and output voltages generated by this integration. Table 1 summarizes the analysis, showing the theoretical gain profile of the intermediate stage and output stage in function of the input voltage of the circuit and the duty cycle of switches S_1 and S_2 . For instance, if the ID structure is applied in PoC1 and the I structure in PoC2, the intermediate and output voltages of the circuit are, respectively, related to equations δ_2 and $\delta_2 \frac{2\delta_1}{1+\delta_1}$, which means that the intermediate voltage is regulated by the nominal set point of the duty cycle applied in S_2 and the output voltage depends on the duty cycles applied to S_1 and S_2 . The analysis considers that the duty cycles are independent, and with no phase-shift between each other.

3.2. Region 2 ($\delta_2 < \delta_1$)

Operating in this region, the second stage of the quadratic buck depends on the first stage, since the duty cycle of switch S_1 is higher than the duty cycle of switch S_2 . Consequently, the intermediate capacitor continues to discharge even if the switch S_2 is in ‘off’-state (due to the antiparallel diode between drain-source points of S_2). In this operational region, the duty cycle δ_1 defines the intermediate

voltage level and the output voltage level. Table 2 summarizes the voltage levels in this region of operation.

3.3. Region 3 ($\delta_2 = \delta_1 = \delta$)

Region 3 is the region when both switches operate with the same duty cycle ($\delta_2 = \delta_1 = \delta$) and the duty cycles are in phase with each other. For this case, the intermediate and output voltages are subject to the operational duty cycle of the circuit. The theoretical analysis, shown in Section 4, is related to operation in Region 3. Table 3 summarize the voltage gain of the topologies generated by this intra-exchangeability.

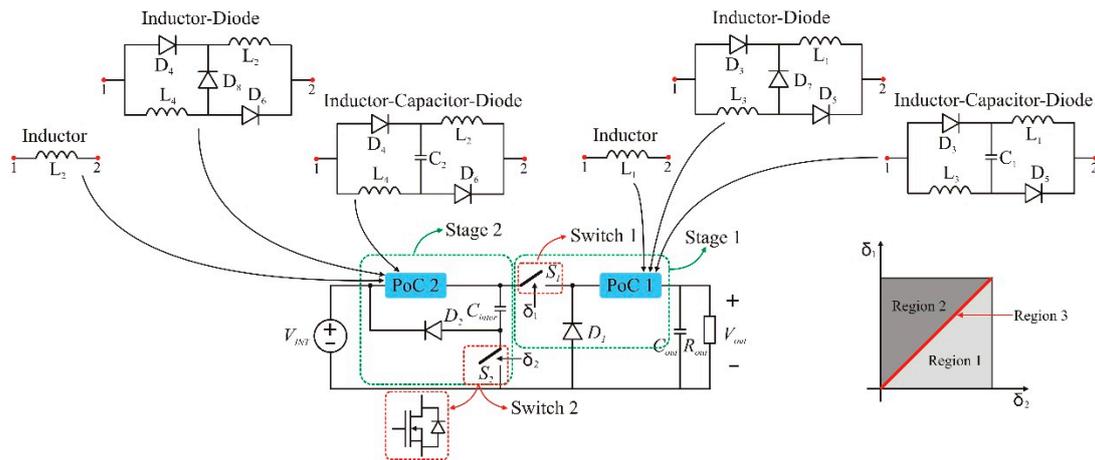


Figure 6. Quadratic Buck with two Point-of-Connections (PoCs) implemented and possible configurations achieved by the intra-exchangeability between I, ID, and ICD structures. Additionally, the operational regions for different duty cycle possibilities and switch realization.

Table 1. Theoretical Gain Analysis for all possible combinations between I, ID, and ICD structures in the quadratic buck configuration operating in Region 1. Intermediate and output voltage profiles in function of the input voltage of the circuit.

PoC2 \ PoC1	I		ID		ICD	
	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$
I	δ_2	$\delta_2 \delta_1$	δ_2	$\delta_2 \frac{2\delta_1}{1+\delta_1}$	δ_2	$\delta_2 \frac{1+\delta_1}{2}$
ID	$\frac{2\delta_2}{1+\delta_2}$	$\frac{2\delta_2}{1+\delta_2} \delta_1$	$\frac{2\delta_2}{1+\delta_2}$	$\frac{2\delta_2}{1+\delta_2} \frac{2\delta_1}{1+\delta_1}$	$\frac{2\delta_2}{1+\delta_2}$	$\frac{2\delta_2}{1+\delta_2} \frac{1+\delta_1}{2}$
ICD	$\frac{1+\delta_2}{2}$	$\frac{1+\delta_2}{2} \delta_1$	$\frac{1+\delta_2}{2}$	$\frac{1+\delta_2}{2} \frac{2\delta_1}{1+\delta_1}$	$\frac{1+\delta_2}{2}$	$\frac{1+\delta_2}{2} \frac{1+\delta_1}{2}$

where δ_2 and δ_1 are the duty cycle of switches S_2 and S_1 , respectively.

Table 2. Theoretical Gain Analysis for all possible combinations between I, ID, and ICD structures in the quadratic buck configuration operating in Region 2. Intermediate and output voltage profiles in function of the input voltage of the circuit.

PoC2 \ PoC1	I		ID		ICD	
	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$
I	δ_1	δ_1^2	δ_1	$\frac{2\delta_1^2}{1+\delta_1}$	δ_1	$\delta_1 \frac{1+\delta_1}{2}$
ID	$\frac{2\delta_1}{1+\delta_1}$	$\frac{2\delta_1^2}{1+\delta_1}$	$\frac{2\delta_1}{1+\delta_1}$	$\left(\frac{2\delta_1}{1+\delta_1}\right)^2$	$\frac{2\delta_1}{1+\delta_1}$	δ_1
ICD	$\frac{1+\delta_1}{2}$	$\frac{1+\delta_1}{2} \delta_1$	$\frac{1+\delta_1}{2}$	δ_1	$\frac{1+\delta_1}{2}$	$\left(\frac{1+\delta_1}{2}\right)^2$

Table 3. Theoretical Gain Analysis for all possible combinations between I, ID, and ICD structures in the quadratic buck configuration operating in Region 3. Intermediate and output voltage profiles in function of the input voltage of the circuit.

PoC2 \ PoC1	I		ID		ICD	
	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$	$\frac{V_{inter}}{V_{IN}}$	$\frac{V_{OUT}}{V_{IN}}$
I	δ	δ^2	δ	$\frac{2\delta}{1+\delta}\delta$	δ	$\delta\frac{1+\delta}{2}$
ID	$\frac{2\delta}{1+\delta}$	$\frac{2\delta}{1+\delta}\delta$	$\frac{2\delta}{1+\delta}$	$\left(\frac{2\delta}{1+\delta}\right)^2$	$\frac{2\delta}{1+\delta}$	$\frac{2\delta}{1+\delta}\frac{1+\delta}{2}$
ICD	$\frac{1+\delta}{2}$	$\frac{1+\delta}{2}\delta$	$\frac{1+\delta}{2}$	$\frac{1+\delta}{2}\frac{2\delta}{1+\delta}$	$\frac{1+\delta}{2}$	$\left(\frac{1+\delta}{2}\right)^2$

Although nine different topologies are realized in this analysis, only six different output voltage profiles are obtained, since the topologies I-ID/ID-I, I-ICD/ICD-I and ID-ICD/ICD-ID provide the same output voltage profile, while different intermediate voltage profiles are observed. Figure 7 shows the graphical representation of the output voltage profiles presented in Table 3. It is noticed that, due to the equations of the voltage profile shown in Figure 5, the highly nonlinear behavior of the quadratic buck converter is attenuated when the ID or ICD structures are used in one of the PoCs. The gain of the topologies, mathematically expressed in Table 3 and graphically in Figure 7, is less nonlinear if compared with the conventional quadratic converter, which is interesting for control purposes. These converters, however, are not suitable for applications that require high step-down capability, since the ID and ICD structures decrease the step-down capability of the structure, as shown in Figure 5 for application in a regular buck and Figure 7 in the quadratic version. Although the component part count increases for ID and ICD implementation, it also increases the flexibility to achieve multiple intermediate voltage levels to supply different loads.

On comparison of Table 2, related to region 2, and Table 3, related to region 3, it is noticed that the gain of the structures are the same. As mentioned in the previous subsection, this behavior occurs because the antiparallel diode of switch S_2 continue to conduct even if switch S_2 is in 'off'-state until switch S_1 commutates from 'close' to 'open'. This analysis concludes that operational regions 2 and 3 generate similar PWM modes and, consequently, the same intermediate and output voltage levels while region 1 is distinguished by the independence between the stages. Section 4 will further discuss the operational principle of the double switch quadratic buck with ID and ICD structures, for operation in Region 3.

4. Operational Principle of the Double Switch Quadratic Buck Converter in Region 3

Similar to Section 2, where the one-stage I, ID, and ICD topologies have been introduced, this section introduces the PWM modes of the two-stage I, ID, and ICD topologies, where the PWM signal remains the same. The phase shift between δ_2 and δ_1 is considered zero (in phase with each other) for the specific analysis but if differs from zero, the gain behavior shown in Tables 1–3 will differ, since the phase-shift will influence the PWM stages and, consequently, the gain of the structures. The equivalent circuit for the first and second stages, considering all the possibilities between the exchangeable circuits, are present in Figure 8a,b, respectively. In order to evaluate the main characteristics of the topologies, the equivalent circuits presented in Figure 8 are used to mathematically evaluate the voltage and current stresses in all power components. This information is crucial to further dimension the components for practical implementation.

The voltage stress across each power semiconductor are extracted from the PWM mode stages in Figure 8 and summarized in Table 4. The voltage stress across switch S_1 and diode D_1 is affected by the structure applied in PoC2, for instance, if the I structure is applied to PoC2, the voltage stress across switch S_1 is defined by $(1 + \delta)V_{IN}$, while if the ID structure is applied in PoC2, the voltage stress across switch S_1 is defined by equation $\frac{(1+3\delta)}{(1+\delta)}V_{IN}$. Similarly, the voltage stress across diodes $D_3/D_5/D_7$, connected to PoC1, are related to the structure connected in PoC1. For instance, maintaining PoC2

fixed with the ID structure, if the ID structure is connected to PoC1, the voltage across the diodes D_3/D_5 is expressed by $\frac{\delta^2}{(1+\delta)^2} V_{IN}$ and, if PoC1 is changed for an ICD structure, the voltage across diodes D_3/D_5 is expressed by $\frac{\delta}{(1+\delta)} V_{IN}$. Switch S_2 and diode D_2 stresses are independent on the structures and are equal to the input voltage V_{IN} . The voltage stress across diodes D_3 - D_4 - D_5 - D_6 - D_7 - D_8 , which are the diodes implemented in the ID and ICD structures, are related to the operational duty cycle, input voltage, and in which PoC the structures are implemented.

Similarly, the PWM modes also provide the RMS current stress in each power semiconductor. To evaluate the RMS current stress in all components, equation (3) is introduced, where i_{x1} is the current that the semiconductor conducts during the first PWM mode and i_{x2} is the current conducted during the second PWM mode. Applying (3), the current stress in each semiconductor is characterized and presented in Table 5. Different than the voltage stress, the current stress of switches S_2 and D_2 depend on the structure connected to PoC2 but are independent of the structure connected to PoC1. For instance, the RMS current stress across switch S_2 is expressed by $\frac{I_{IN}(1-\delta)}{\delta} \sqrt{\frac{1}{\delta}}$ if the I structure is connected to PoC2, and expressed by $\frac{I_{IN}(1-\delta)}{2\delta} \sqrt{\frac{1}{\delta}}$ if the ID structure is connected. It is also noticed that the current is independent on PoC1, in this case.

The analysis abovementioned is important in order to select the components for experimental validation, since the RMS current and voltage stress are the most important characteristics to select MOSFETs and diodes. The next section presents a numerical simulation for the proposed converter performed in PLECS (4.0.2, Plexim GmbH, Zurich, Switzerland).

$$i_{xRMS} = \sqrt{\frac{1}{T_S} \left(\int_0^{DT_S} i_{x1}^2 dt + \int_{DT_S}^{T_S} i_{x2}^2 dt \right)} \quad (3)$$

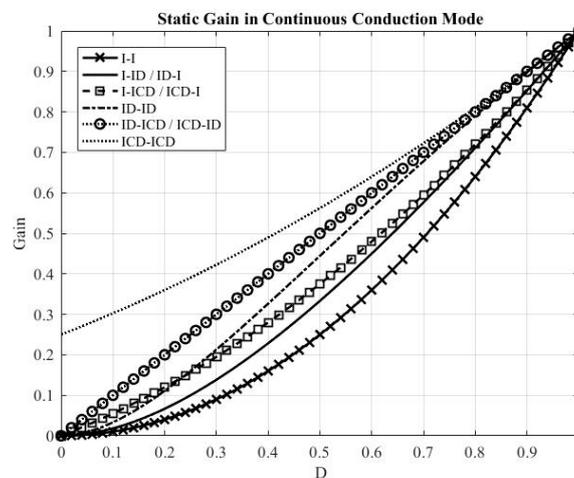


Figure 7. Continuous conduction mode graphical gain representation.

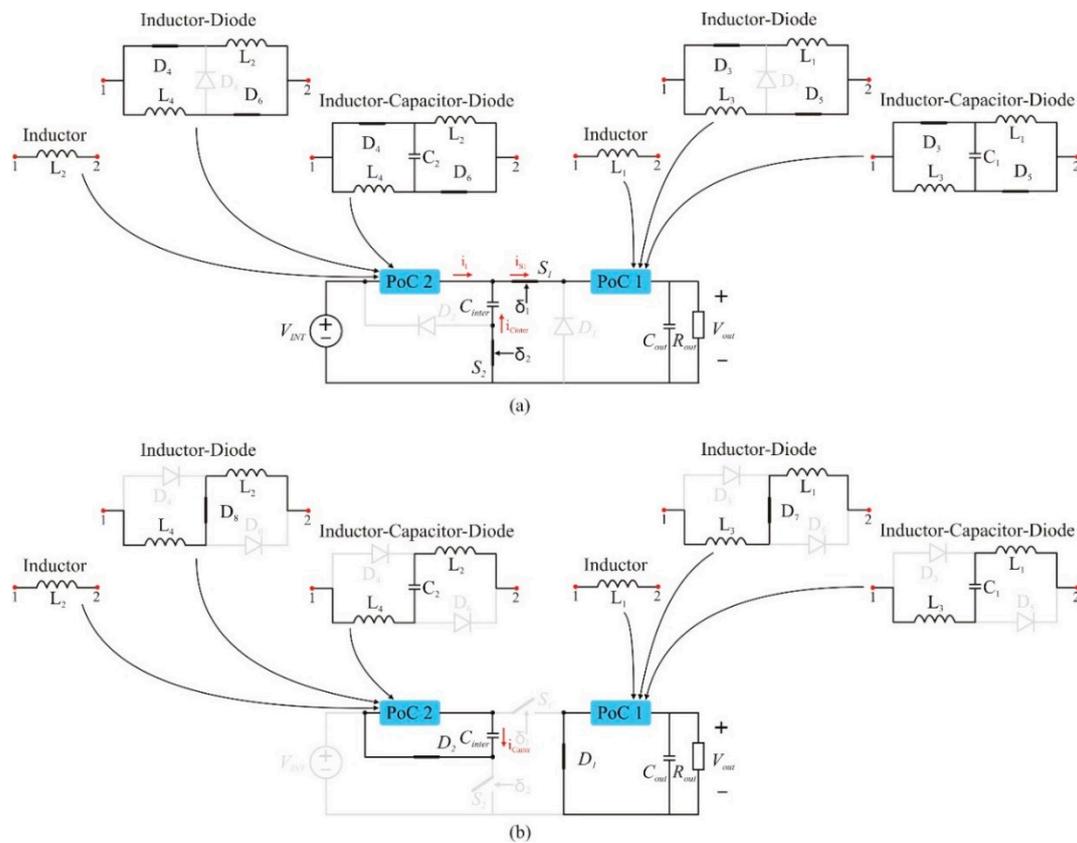


Figure 8. (a) Equivalent circuit for PoC 2 and PoC 1 applying I, ID, and ICD structures during the first PWM mode and (b) equivalent circuit for PoC 2 and PoC 1 applying I, ID, and ICD structures during the second PWM mode.

Table 4. Voltage stress sum up for all power semiconductors in the power stage. Equations are in function of the input voltage.

PoC2-PoC1	S ₁	S ₂	D ₁	D ₂	D ₃ /D ₅	D ₄ /D ₆	D ₇	D ₈
I-I					-		-	
I-ID	$(1 + \delta)V_{IN}$		δV_{IN}		$\frac{\delta^2}{(1 + \delta)} V_{IN}$	-	$\frac{(1 - \delta)\delta}{(1 + \delta)} V_{IN}$	-
I-ICD					$\frac{\delta V_{IN}}{2}$		-	
ID-I					-			
ID-ID	$\frac{(1 + 3\delta)}{(1 + \delta)} V_{IN}$	V_{IN}	$\frac{2\delta}{(1 + \delta)} V_{IN}$	V_{IN}	$\frac{\delta^2}{(1 + \delta)^2} V_{IN}$	$\frac{\delta}{(1 + \delta)} V_{IN}$	$\frac{2(1 - \delta)\delta}{(1 + \delta)^2} V_{IN}$	$\frac{(1 - \delta)}{(1 + \delta)} V_{IN}$
ID-ICD					$\frac{\delta}{(1 + \delta)} V_{IN}$		-	
ICD-I					-			
ICD-ID	$\frac{(3 + \delta)}{2} V_{IN}$		$\frac{(1 + \delta)}{2} V_{IN}$		$\frac{\delta V_{IN}}{2}$	$\frac{V_{IN}}{2}$	$\frac{(1 - \delta)}{2} V_{IN}$	-
ICD-ICD					$\frac{(1 + \delta)}{4} V_{IN}$		-	

Table 5. RMS Current stress sum up for all power semiconductors in the power stage. Equations are in function of the input current.

PoC2-PoC1	S ₁	S ₂	D ₁	D ₂	D ₃ /D ₃	D ₄ /D ₄	D ₇	D ₈
I-I			$\frac{I_{IN}}{\delta^2} \sqrt{(1-\delta)}$		-		-	
I-ID	$\frac{I_{IN}}{\delta} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1-\delta)}{\delta} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{2\delta^2} \sqrt{(1-\delta)}$	$\frac{I_{IN}}{\delta} \sqrt{(1-\delta)}$	$\frac{I_{IN}}{2\delta} \sqrt{\frac{1}{\delta}}$	-	$\frac{I_{IN}}{2\delta^2} \sqrt{(1-\delta)}$	-
I-ICD			$\frac{I_{IN}}{\delta(1+\delta)} \sqrt{(1-\delta)}$		$\frac{I_{IN}}{\delta(1+\delta)} \sqrt{\frac{1}{\delta}}$		-	
ID-I			$\frac{I_{IN}(1+\delta)}{2\delta^2} \sqrt{(1-\delta)}$		-			
ID-ID	$\frac{I_{IN}(1+\delta)}{2\delta} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1-\delta)}{2\delta} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1+\delta)}{4\delta^2} \sqrt{(1-\delta)}$	$\frac{I_{IN}}{2\delta} \sqrt{(1-\delta)}$	$\frac{I_{IN}(1+\delta)}{4\delta} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{2} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1+\delta)}{4\delta^2} \sqrt{(1-\delta)}$	$\frac{I_{IN}}{2\delta} \sqrt{(1-\delta)}$
ID-ICD			$\frac{I_{IN}}{2\delta} \sqrt{(1-\delta)}$		$\frac{I_{IN}}{2\delta} \sqrt{\frac{1}{\delta}}$		-	
ICD-I			$\frac{2I_{IN}}{\delta(1+\delta)} \sqrt{(1-\delta)}$		-			
ICD-ID	$\frac{2I_{IN}}{(1+\delta)} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}(1-\delta)}{(1+\delta)} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{\delta(1+\delta)} \sqrt{(1-\delta)}$	$\frac{I_{IN}}{(1+\delta)} \sqrt{(1-\delta)}$	$\frac{I_{IN}}{(1+\delta)} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{(1+\delta)} \sqrt{\frac{1}{\delta}}$	$\frac{I_{IN}}{\delta(1+\delta)} \sqrt{(1-\delta)}$	-
ICD-ICD			$\frac{2I_{IN}}{(1+\delta)^2} \sqrt{(1-\delta)}$		$\frac{2I_{IN}}{(1+\delta)^2} \sqrt{\frac{1}{\delta}}$		-	

5. Numerical Simulations

A numerical simulation was carried out to show the available intermediate voltage levels when an output voltage of 12 V is set as standard output voltage. The 12 V voltage level can supply low voltage/low power loads to, for instance, LEDs or to charge small batteries (unidirectional power flow to charge, since the topologies are unidirectional); this is one of the main reasons to fix the output voltage on this level. The simulation and experimental parameters are presented in Table 6.

Different intermediate voltage levels are generated, depending on the structure connected in PoC2 and the operational duty cycle of the converter, as shown in Table 3. The simulation model was developed in PLECS. The only configuration that is not able to be simulated and experimentally validated in this paper is the ICD-ICD structure, since the input/output voltage level is 48 V/12 V and the theoretical gain of this structure is $0.25 < \text{ICD-ICD} < 1$, making it impossible to provide the required output voltage.

A simulation is performed for each configuration and the results are shown in Figure 9. The conventional quadratic buck with I-I is shown in Figure 9a, generating an intermediate voltage level of 24 V. According to Table 3, the I-ID and ID-I configurations generate the same output voltage but different intermediate voltage levels for operation with the same duty cycle. This behavior is proved via simulation and presented in Figure 9b,d, where the voltage level of 20.25 V (I-ID) and 28.5 V (ID-I) are obtained for a duty cycle of 42.2%.

Similarly, the topologies I-ICD and ICD-I operate with the same duty cycle (36.6%) and input/output voltages, however the intermediate voltage level changes since is applied different structures in PoC2. Simulation results shown in Figure 9c,g confirm the analysis, since an intermediate voltage of 17.6 V (I-ICD) and 32.8 V (ICD-I) are obtained and available to supply loads in different voltage ranges in a flexible way. The structures ID-ICD and ICD-ID are also evaluated via simulation for similar input/output voltages. Intermediate voltages of 19.2 V (ID-ICD) and 30 V (ICD-ID) are obtained and shown in Figure 9f,h, respectively, validating the theoretical analysis presented in Table 3. Additionally, the last configurations present similar overall gain (δ) with the regular buck converter, however they present an additional voltage level that can be used to supply additional loads in different voltage levels. The drawback of the structure, compared with the conventional buck, is the component part count, since the number of inductors and diodes in the power stage increase.

Finally, the ID-ID structure is briefly discussed herein. Figure 9e shows the voltage levels obtained from simulation. Similarly with the conventional I-I quadratic buck, an intermediate voltage level

of 24 V is obtained, however an operational duty cycle of 33.3% is used to match the desired output voltage of 12 V.

The simulations were performed with a switching frequency of 300 kHz (switching period of 3.33 μ s), since this frequency was used to calculate the I, ID, and ICD inductances for further implementation of the structures. All the inductances were select to present a 20% ripple current limit across the inductors in nominal power. A summary of the theoretical inductor current expressions in each scenario is present in Table 7, in function of the input current I_{IN} . From the PWM mode stages discussed in the previous section and shown in Figure 8a,b, the inductors of the ID and ICD structures charge its terminals in parallel and discharge in series, which guarantees natural balance between the internal currents of the structure. This characteristic enable the non-use of current sensors to control the inductor current, since this control is guarantee directly by the ID and ICD structures, also known as switched-inductor structures. The drawback, as previously mentioned, is the increase in the number of components in the power stage.

With the objective of validating the equations shown in Table 7, a comparison between the theoretical analysis and numerical simulation results was performed and shown in Table 8. The input/output voltage of the circuit is 48 V/12 V and a rated input power of 100 W. The different configurations operate with their respective duty cycles to generate an output voltage of 12 V (check Figure 7 for duty cycle). The comparison shows that the theoretical equations match the simulation results, which proves the validity of the equations to select the correct inductances for experimental verification.

Table 6. Simulated and experimental parameters for validation.

Variable	Symbol	Value/Model
Input Voltage	V_{IN}	48 V
Output Voltage	V_{OUT}	12 V
Input Power	P_{IN}	100 W
Output Capacitance	C_{OUT}	20 μ F
Switching Frequency	f_s	300 kHz
Switch Technology	S_1/S_2	STMicroelectronics 100 V 0.0145 Ohm typ 30 A

Table 7. Theoretical expressions for current across the inductors of the structures.

PoC2-PoC1	I_{L2}	I_{L4}	I_{L1}	I_{L3}
I-I			$\frac{I_{IN}}{\delta^2}$	-
I-ID	$\frac{I_{IN}}{\delta}$	-	$\frac{I_{IN}}{2\delta^2}$	
I-ICD			$\frac{I_{IN}}{\delta(1+\delta)}$	
ID-I			$\frac{I_{IN}(1+\delta)}{2\delta^2}$	-
ID-ID	$\frac{I_{IN}}{2\delta}$		$\frac{I_{IN}(1+\delta)}{4\delta^2}$	
ID-ICD			$\frac{I_{IN}}{2\delta}$	
ICD-I			$\frac{2I_{IN}}{\delta(1+\delta)}$	-
ICD-ID	$\frac{I_{IN}}{(1+\delta)}$		$\frac{I_{IN}}{\delta(1+\delta)}$	

Table 8. Inductor current comparison: theoretical/simulation.

PoC2-PoC1	I_{L2}	I_{L4}	I_{L1}	I_{L3}
	theo./sim.	theo./sim.	theo./sim.	theo./sim.
I-I	4.16 A/4.164 A		8.32 A/8.324 A	-
I-ID	4.95 A/4.955 A	-	5.868 A/5.871 A	
I-ICD	5.628 A/5.662 A		4.12 A/4.12 A	
ID-I	2.464 A/2.465 A		8.304 A/8.306 A	-
ID-ID	3.093 A/3.098 A		6.191 A/6.201 A	
ID-ICD	4.1 A/4.096 A		4.1 A/4.096 A	
ICD-I	1.515 A/1.517 A		8.281 A/8.272 A	-
ICD-ID	1.65 A/1.643 A		6.601 A/6.567 A	

6. Experimental Verification and Test Bench

6.1. Region 2 ($\delta_2 < \delta_1$)/Region 3 ($\delta_2 = \delta_1 = \delta$)

This subsection will discuss the results obtained for operation in Region 3 ($\delta_2 = \delta_1 = \delta$). The topologies, discussed in Sections 3 and 4, were realized for further validation. A test bench was built for experimental verification of the configurations discussed herein. Figure 10 shows the test bench setup, together with a simplified bench schematic. It is shown in Figure 10 that a function generator (equipment (4)) is used to generate the PWM signals to drive S_1 and S_2 . The experimental results shown herein are in open-loop operation, without a control strategy to regulate the intermediate and output voltage levels. Figure 11 shows the converter realization (middle) surrounded by the PoCs (PoC2 and PoC1) developed for each configuration (the inductors were selected based on the 20% maximal current ripple for each structure).

The PoCs, developed to test the different configurations, were designed separately following the plug-n-play methodology. As shown in the converter realization in Figure 11, the PoC2 and PoC1 are actual points of connection, where different external boards are connected to test different inductor configurations (I, ID, and/or ICD). Points 1 and 2, for PoC2, and 3 and 4, for PoC1, are available to connect the external PoCs. Additionally, Table 6 present the parameters defined for the experimental setup, in which the switching frequency of 300 kHz was select to simulate and experimental validation.

When comparing the waveforms presented in Figure 9a–h (simulation) and in Figure 12a–h (experimental), it can be seen that the voltage levels in all topologies are similar in shape (DC shape) and in amplitude. Figures 9 and 12 present the input, intermediate, and output voltages of the converter for the following configurations (PoC2-PoC1); (a) I-I, (b) I-ID, (c) I-ICD, (d) ID-I, (e) ID-ID, (f) ID-ICD, (g) ICD-I, and (h) ICD-ID. Small deviations are observed between the amplitude values in simulation and in the experimental waveforms due to the nonidealities inherent in the components selected to build the prototype. We also noticed that spikes of voltage appears in all voltage levels. This behavior is common in circuits that operate in high frequency, since internal parasitics of the components and also the parasitic inductances related to tracks and soldering points start to become prominent. Additionally, the commutation between ‘on’- and ‘off’-stages of switches S_1 and S_2 also generate internal oscillations in the circuit.

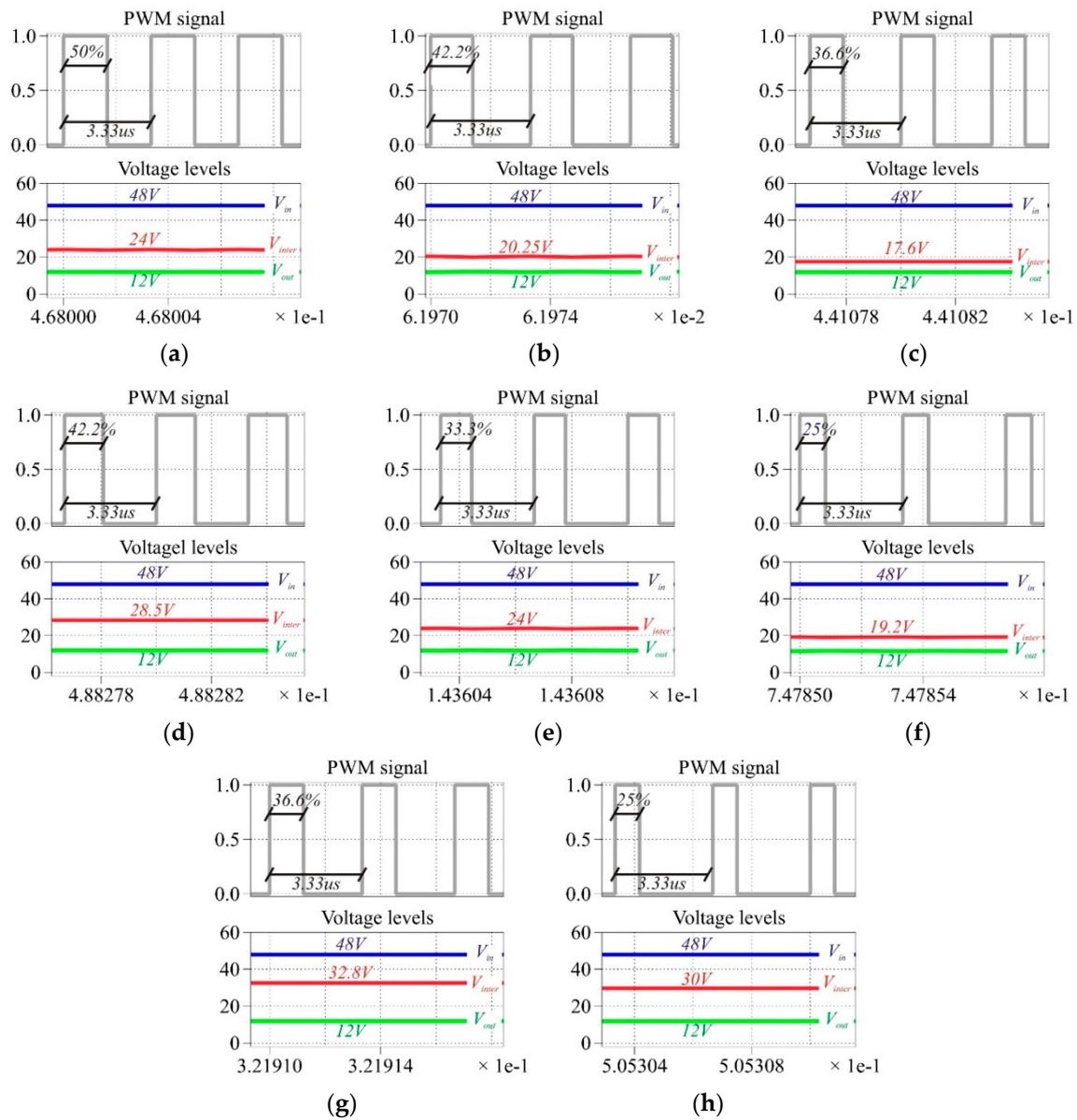


Figure 9. Simulation results showing the different intermediate voltage levels obtained by exchanging the structures for an input/output voltage of 48 V/12 V. PoC2-PoC1: (a) I-I; (b) I-ID; (c) I-ICD; (d) ID-I; (e) ID-ID; (f) ID-ICD; (g) ICD-I; and (h) ICD-ID, respectively.

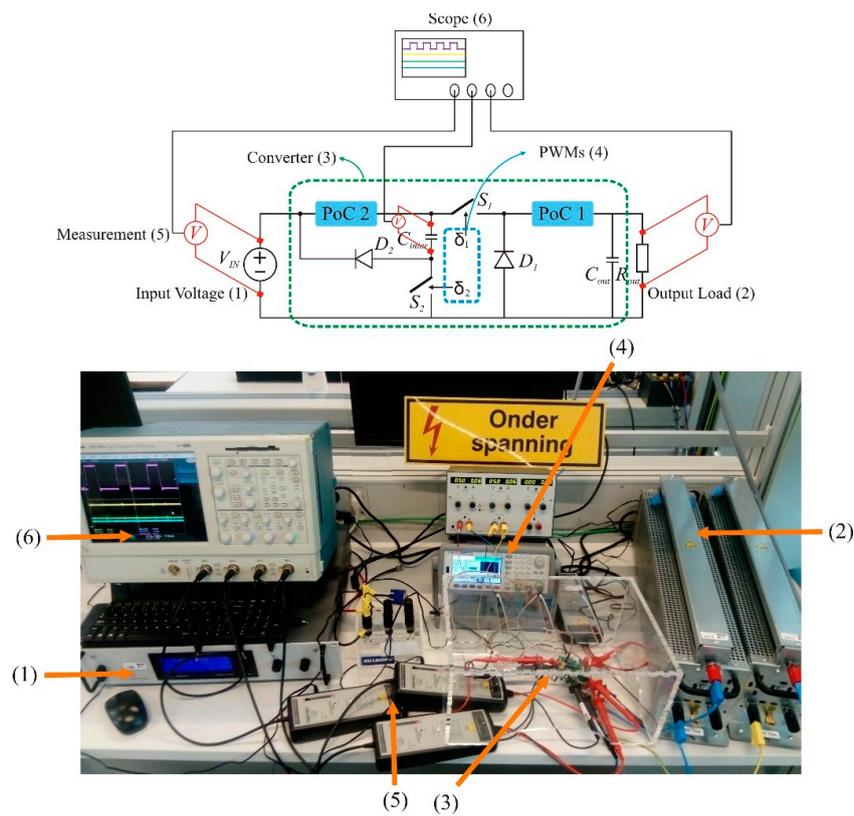


Figure 10. Test bench for experimental realization with (1) input source, (2) output load, (3) quadratic PoC converter, (4) PWM generator, (5) voltage measurements, and (6) scope.

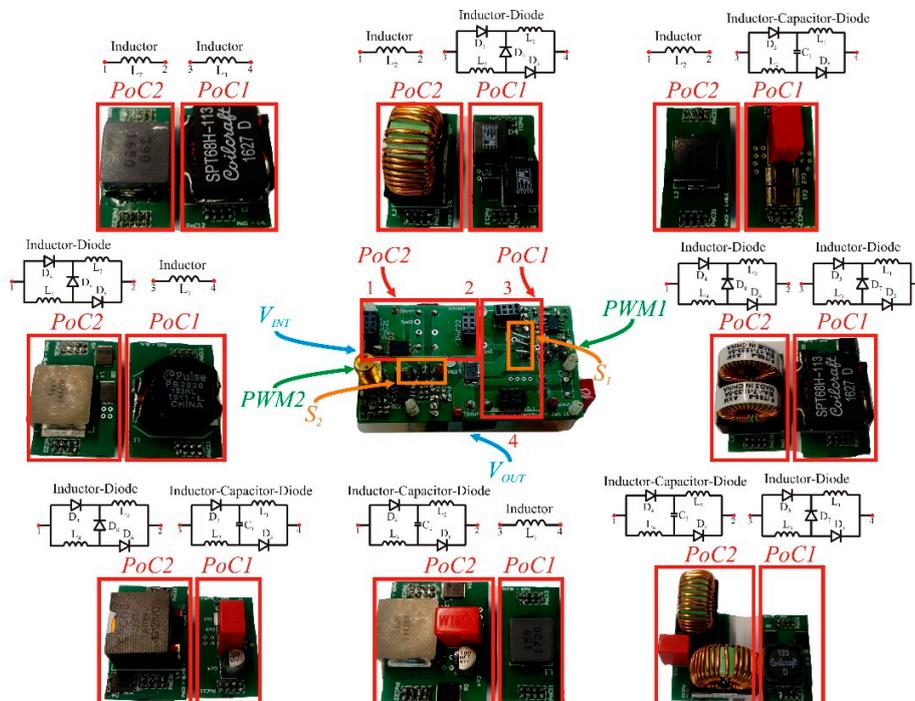


Figure 11. Converter realization (middle) surrounded by PoCs (PoC2 and PoC1) developed to experimental validation of the proposed topologies.

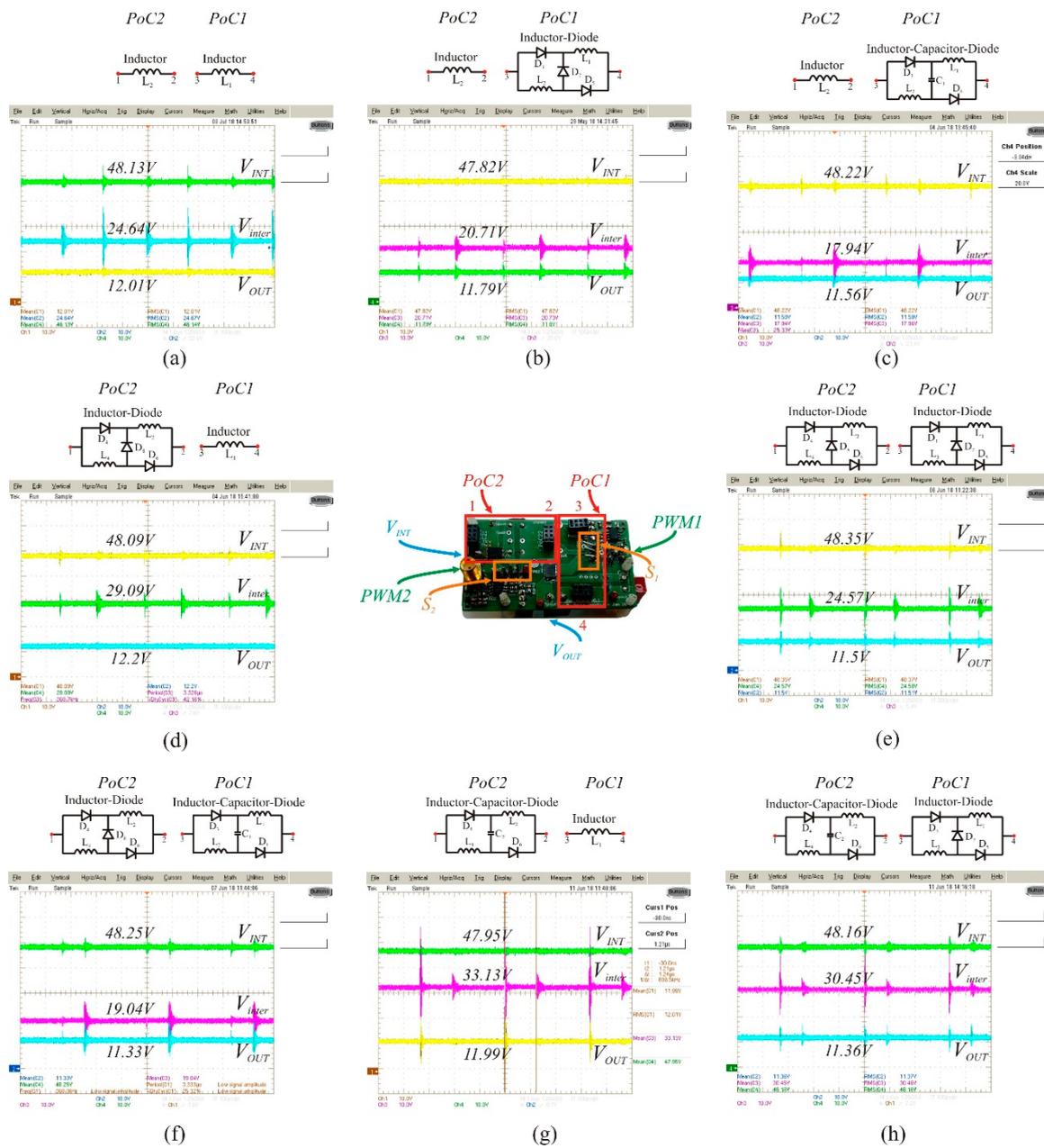


Figure 12. Voltage levels for different structures configurations. From top to bottom and left to right: (a) I-I with $\delta = 0.5$; (b) I-ID with $\delta = 0.422$; (c) I-ICD with $\delta = 0.366$; (d) ID-I with $\delta = 0.422$; (e) ID-ID with $\delta = 0.333$; (f) ID-ICD with $\delta = 0.25$; (g) ICD-I with $\delta = 0.366$ and; and (h) ICD-ID with $\delta = 0.25$.

As mentioned in Section 3, the gain analysis performed for the operation in region 2 and 3 results in the same gain expressions. The experimental results shown herein are for operation in region 3, but can be extended for the case when region 2 is in operation.

As discussed previously, it was shown that for different operating points and configurations connected in PoC2 and PoC1, different intermediate voltage levels are obtained for an input/output voltage of 48 V/12 V. This voltage, which varies from 33 V to 18 V depending the configuration, is available in the intermediate stage and can be used to supply loads in a broad range. Depending the required intermediate voltage, the best suited configuration can be selected to connect in PoC2 and PoC1. The ICD structure, as shown in Figure 5, limits the gain in the region between $[0.5 ; 1]$, and can be used for a small voltage regulations with a certain accuracy. The ID structure, on the other hand, presents a nonlinear gain behavior in the range between $[0 ; 1]$. For the same duty cycle, this

structure can be used to achieve gains in between the regular buck with I structure and the buck with ICD structure, with the disadvantage of a nonlinear gain.

6.2. Region 1 ($\delta_2 > \delta_1$)

For operation in region 1, an extra PWM mode is performed between the normal PWM modes 1 and 2, during the switching period. This extra PWM mode guarantee the independence between stages 1 and 2, leading to the gain presented in Table 1 for all possible PoC configurations. We noticed that the intermediate gain depends only on the duty cycle δ_2 , while the output gain is relate to duty cycles of both stages, since the converters are cascade connected.

Figure 13 shows the PWM modes for operation in region 1 for the I-ICD configuration. Nevertheless, this analysis can be extended for all configurations. As previously mentioned, an extra PWM mode arises during the switching period (PWM mode 2 in this analysis). Switch S_1 —the component which is subject to the greatest voltage stress among the power components—as highlighted in Table 4, blocks only the intermediate voltage level during the switch transient between ‘on’ and ‘off’ while when operates in regions 2 and 3, the switch blocks the sum between the intermediate voltage and the input voltage. This phenomenon enables the reduction of switching losses in this component once the voltage that the component blocks during the switching transient has a lower value compared with the normal operation, although the maximum voltage that the switch needs to block remains in the same level as shown in Table 4.

Figure 14 presents an experimental verification of the stages discussed previously and shown in Figure 13. Figure 14a presents a waveform with the significant voltage levels of the circuit. As expected, an intermediate voltage of 19.5 V is achieved for a duty cycle of 40% applying the I structure in PoC2. Additionally, Figure 14a also presents the second voltage regulation stage made by the ICD structure connected in PoC1, operating with a duty cycle of 25%, in which a voltage of 11.2 V is achieved at the output of the converter. Figure 14b presents the PWMs applied to the circuit and its switching period, together with the input/output voltage of the circuit. As expected, input and output voltages are in accordance with the theoretical analysis above presented.

Finally, Figure 14c shows the experimental results of the voltage stress across the active semiconductors S_1 and S_2 . For the same duty cycle abovementioned, the voltage stress across switch S_2 is independent of the operational duty cycle and equal to the input voltage, as shown in Figure 14c. Additionally, the stress across switch S_1 was also evaluated and presented in Figure 14c. It is verified that, as theoretically explained, the voltage that the switch blocks during transition between ‘on’ and ‘off’ stages is the intermediate voltage across C_{inter} , although the maximum voltage stress is related to the sum of input and intermediate voltages (verify PWM mode 3 between points 2–3 in Figure 13). Moreover, the switching losses generated by the overlap between current and voltage during the transition time decrease due to the lower blocking voltage during this transition. For operation in region 1, the addition of switch S_2 with independent duty cycle improves the flexibility of the system and decreases the switching losses across switch S_1 .

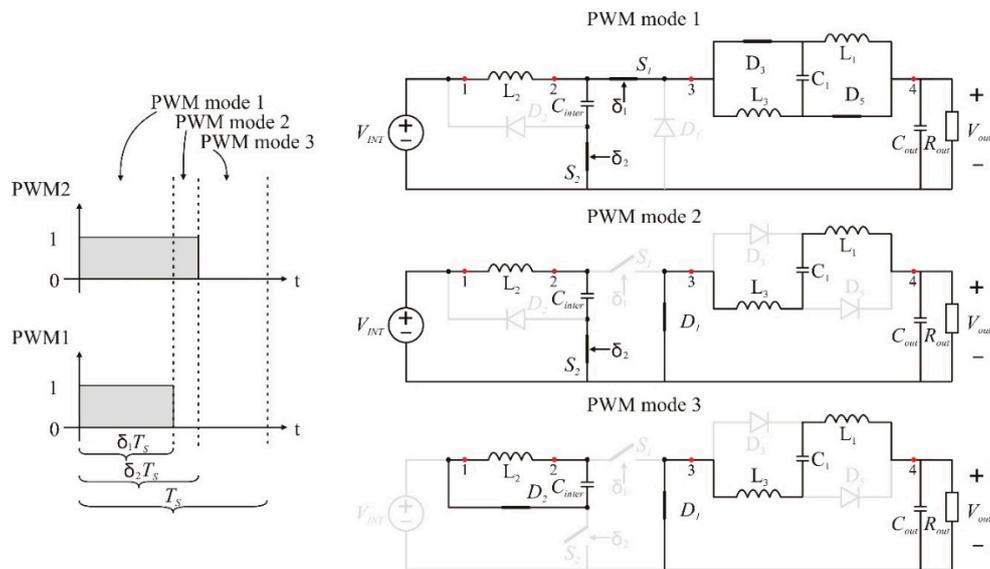


Figure 13. PWM modes with the equivalent circuits during one switching period when $\delta_2 > \delta_1$.

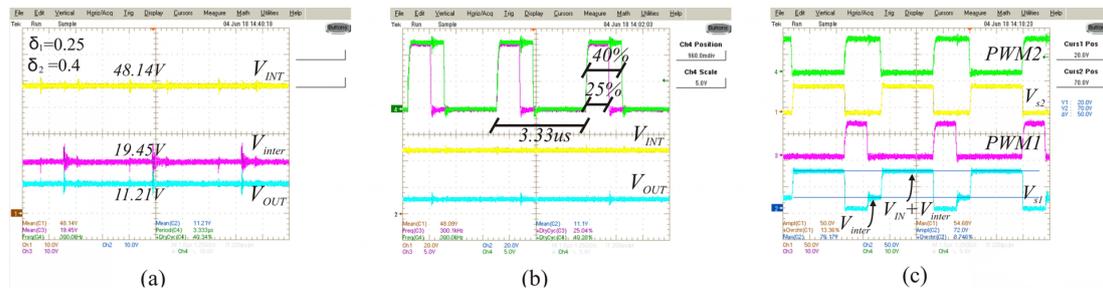


Figure 14. Experimental results for operation in region 1 for operation with $\delta_2 = 0.4$ and $\delta_1 = 0.25$ and switching frequency of 300 kHz: (a) input, intermediate and output voltages; (b) input and output voltages together with the respective duty cycles; and (c) PWMs and voltage stress across switches S_1 and S_2 .

As discussed previously, the introduction of the ID and ICD structures in a step-down configuration (one-stage buck or quadratic buck) enable the possibility to change the voltage level of these structures. When applied in a one-stage buck converter, the ICD structure present similar voltage gain $\left(\frac{1+D}{2}\right)$ as the converter proposed in [50]. The structures, however, present different functionalities, since the abovementioned structure is a switched capacitor based converter with one switch, three diodes, one inductor, and three capacitors in the power stage while the structure, herein presented, is a switched inductor based topology with one switch, three diodes, two inductors, and one capacitor in the power stage. In terms of component part count number, the one-stage ICD structure present lower amount of components compared with the switched capacitor version that present similar gain [50]. The ID structure, on the other hand, presents a nonlinear step-down behavior with one extra diode and one less capacitor in the power stage (compared with the above-mentioned converters).

The ID structure is also explored in step-up configurations [39] and, when applied in a step-down structure, it changes the structure to a one composed by two inductors and two diodes, which leads to a gain of $\frac{D}{1+D}$, performing a higher step-down ratio than the ID structure. A topology with different switched capacitor/inductor structure is proposed for similar voltage gains [44] Comparing these topologies with the quadratic-buck configuration applying the ID and I structures (see Table 3), the gain of these structures is $\frac{2D*D}{1+D}$. The proposed structures, although implement more components in

the power stage, present a higher step-down ratio for duty cycles lower than 0.5. For duty cycles above 0.5, the proposed converter present lower step-down capability with higher component part count.

The one-stage buck converter present similar gain (D) compared with the quadratic buck applying ID and ICD structures in PoC1 or PoC2 (see Table 3). For a component part count point of view, the conventional buck converter present more benefits compared to the structures above-mentioned, since the conventional buck converter present the lowest part count structure for a DC–DC step-down configuration. On the other hand, the converters proposed herein present multiple output ports, e.g., intermediate and output voltages, and, according to the analysis presented herein, if a second switch S_2 is implemented, these voltage levels can be independently regulated (operation in Region 1), which is beneficial for an application point of view.

The major advantage that the topologies proposed herein have is the flexibility to adjust the intermediate voltage level according with the project specifications. The experimental results presented in Figures 12 and 14 show that, for the same input/output voltage, different intermediate voltage levels can be obtained depending on the operational regions (Region 1, 2, or 3) and the structure applied to PoC1 and PoC2. The main disadvantage, however, is the number of components in the power stage. When applied in a quadratic buck converters, the ID and ICD structures increase the number of semiconductor and magnetics in the power stage. This feature is undesired in some applications that power density is required, since extra space is required to place all the components. As previously mentioned, the ID and ICD structures are suited for lower voltage regulations and are not applicable if high step-down conversion ratios are required.

7. Conclusions

The analysis in this paper shows the influence of the ID and ICD structures, previously applied in step-up topologies, in a step-down configuration from 48 V to 12 V input-to-output voltage. To achieve the required voltage levels, a quadratic buck structure was implemented since the first analysis showed that the ID and ICD structures have a lower voltage regulation capability compared with the conventional I structure and, if a single stage buck converter is considered for application, the ICD structure cannot achieve the required output voltage level.

A complete theoretical analysis with PWM stages for all possible regions of operation, voltage gain, voltage/current profiles, and simulation is shown for all possible configurations generated by the substitution of the structures in PoC2 and PoC1. Voltage and current stress were evaluated for dimensioning and component selection to subsequently build the prototype for experimental validation. The analysis showed that the ID and ICD structures change the voltage and current profile depending on which PoC is connected. It is proven that the addition of a second switch S_2 , together with the operation in Region 1, decreases the voltage stress during turn-off of switch S_1 . The main advantage of the proposed approach is that the intermediate voltage level can be selected according to the application, since switch S_2 is implemented and the ID and ICD structures provide different voltage profiles that can be desired for specific operational duty cycles.

The main advantages of the proposed topologies compared to the conventional buck and quadratic buck converters are as follows.

- (1) The addition of the second switch S_2 and the possibility to choose between I, ID, and ICD structures to connect in PoC2 and PoC1, increase the flexibility of the circuit, resulting in a broad range of intermediate and output voltage levels.
- (2) The circuits with ID and/or ICD feature diode and inductor redundancy, which leads to lower current stress and a fail-safe structure, after all, if one diode/inductor fails in open-circuit, the system can still maintain its functionality but with limited power.
- (3) The implementation of S_2 also increase the number of regions of operation, since region 1 is now a possible region of operation. In this region, the blocking voltage of switch S_1 decreases from $V_{IN} + V_{inter}$ to only V_{inter} , as shown in Section 6.

A test bench was assembled and experimental results showing that the ID and ICD structures can be used for small voltage adjustments in a step-down application were presented. Simulation and experimental waveforms were presented to validate the theoretical analysis in Section 4. The ID and ICD proved to be effective structures for applications where small voltage adjustments are required, but did not prove being useful solutions when a high step-down voltage level is required due to its gain characteristics.

8. Patent

A patent related to this work was filled in on the 15th of May 2018, with application number GB1807795.8 at the UKIPO (reference [47]).

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