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Experimental Investigation on the Performances of a Multilevel Inverter Using a Field Programmable Gate Array-Based Control System

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Abstract: The Field Programmable Gate Array (FPGA) represents a valid solution for the design of control systems for inverters adopted in many industry applications, because of both its high flexibility of use and its high-performance with respect to other types of digital controllers. In this context, this paper presents an experimental investigation on the harmonic content of the voltages produced by a three-phase, five level cascaded H-Bridge Multilevel inverter with an FPGA-based control board, aiming also to evaluate the performance of the FPGA through the implementation of the main common modulation techniques and the comparison between simulation and experimental results. The control algorithms are implemented by means of the VHDL programming language. The output voltage waveforms, which have been obtained by applying to the inverter the main PWM techniques, are compared in terms of THD%. Simulation and experimental results are analyzed, compared and finally discussed.

Keywords: multilevel converters; FPGA; renewable energies

1. Introduction

Over the last decades, the technological advances of software for the implementation of digital systems, which are generally finalized to the control of specific applications, has significantly contributed to the simplification of the design processes of digital controllers dedicated for the electrical energy conversion [1]. The Digital Signal Processor (DSP) is a very wide-spread digital controller that allows the implementation of control algorithms through a purely software programming (C or C++). The related hardware, even if composed by several peripherals (e.g., the RAM or the ROM), presents an already designed structure and, therefore, the flexibility of use of the microcontroller is significantly reduced.

The Field Programmable Gate Array (FPGA) is another example of digital controller composed by a matrix of Configurable Logic Blocks (CLBs) with completely reprogrammable connections. Thus, if compared with a DSP, the FPGA ensures a higher flexibility, even if the complexity of the system in the low-level programming is challenging. Moreover, the previously mentioned feature allows the realization of a system of logic operations developed in parallel, reducing the computing time and leading to the achievement of high-performance control systems, which can be even compared with equivalent controllers composed by analogical components [2–5]. Nevertheless, it has to be highlighted that the adoption of a DSP could generally provide a much faster software development with respect to a FPGA. However, according to [1,2,6], the latter can overcome to some of the major

disadvantages of the conventional microprocessor or DSP controls. In fact, as aforementioned, one of the main advantages is the independence between the architecture of the device and the written code. Furthermore, the hardware can be reconfigured in a very easy manner [2].

Moreover, in comparison with Complex Programmable Logic Devices (CPLDs), the adoption of an FPGA allows the design of very complex digital systems, providing higher flexibility with a lower design security and allowing the adoption of Computer-Aided Design (CAD) [1,5].

Several papers in the literature have focused their attention in the field of multilevel converters controlled by FPGA, especially for high-speed control systems [7–18]. For instance, Islam et al. [8], as well as Zhou et al. [9], proposed the modeling and experimental evaluation of multilevel inverters control, focusing their interest towards the implementation through FPGA and not on the harmonic content of the voltage waveform for the different modulation techniques. Similar analysis and experimental results are given in [10–12], but for different cases of applications. In addition, Aime et al. [13] proposed the use of a FPGA for the Peak Current Control (PCC) in a multilevel inverter: the main tasks of the FPGA architecture, such as ramp generation, dead time creation, switching orders generation, voltage regulation, are well described. Gateau et al. [14] highlight the role of FPGA in the implementation of a digital sliding-mode observer of the flying capacitors in stacked multicell converters (SMCs). Nevertheless, the potential benefits in terms of THD improvement are not extensively proven.

In [15], Coppola et al. presented an FPGA-based control strategy for Cascade Half Bridge (CHB) inverters: despite a wide exploitation of the FPGA tasks (e.g., Maximum Power Point Tracking, MPPT, and sorting algorithm implementation, dead time generation, measurement stage) the FPGA system is not responsible for the PWM control, which is implemented by a DSP. Moreover, the work described in [16] takes into account only three modulation techniques, also referring several DSP disadvantages such as the increased processing time or a reduced accuracy due to the limited available resources. Mentions of the flexibility of the FPGA system in terms of industry applications can be found in [17–22]. In particular recent papers [17,18,20] address the control of modular multilevel converters, and others face the growing application on electrical mobility from battery management systems [19] and traction [21–23]. All proposed recent papers report FPGA as the best answer for implementing in real time the control techniques, due to its adaptive parallel processing hardware structure, which permits implementing diverse algorithms with reducing the serial and consecutive operations compared to traditional CPU implementation.

In this context, this paper aims to present a detailed investigation and experimental validation on the performances in terms of harmonic distortion of the voltages produced by a cascade h-bridge multilevel inverter, defined in Section 2, controlled by an FPGA and for several modulation techniques. The harmonic content is evaluated by means of the approximate total harmonic distortion parameter, which is defined in Section 5.

Moreover, in the field of the DC-AC conversion systems, multilevel converters, with respect to the traditional ones, provide great advantages such as lower Total Harmonic Distortion (THD) of the waveforms, lower strains to both load and switches and reduction of the issues related to the electromagnetic compatibility. However, the main drawbacks for these converters can be identified in a higher overall cost of the device and a higher complexity for the design of control and command circuits.

Multilevel converters are commonly used for medium voltage/high power applications, as reported in [24]. Furthermore, the use of components with high switching frequencies and low losses (i.e., power MOSFET) allows the multilevel converters to be applied also for low-power and low voltage applications, as reported in [25,26].

In comparison with multilevel converters of the traditional type, higher number of levels can be obtained through particular structures reported in [27–29].

Generally, due to the complex structure of the multilevel inverters, several studies have been carried out in order to reduce the number of components. For instance, Jamaludin et al. [30] proposed

the use of bidirectional switches with an auxiliary circuit in order to reduce the complexity of a three-phase full-bridge inverter. A hybrid circuital structure was proposed by Gautam et al. [31], in which the number of controlled switches, diodes and DC sources is considerably reduced. Another innovative topology for medium/high voltage is presented in [32], consisting of a series-connected symmetric module and a three-phase inverter. However, the reduction of the number of components leads to a reduction on its flexibility of use and, therefore, innovative control techniques must be developed [33].

In this context, the aim of this paper is to present an experimental investigation of the main Multicarrier Pulse Width Modulation (MC PWM) techniques for a three-phase, five level cascaded H-bridge inverter by means of a FPGA controller-based board, which represents a favorable solution for the design of control systems for inverters, mainly due to its high flexibility of use.

In the first step, the analysis is carried out in order to compare the simulation and experimental results of the proposed techniques. For this purpose, the Total Harmonic Distortion (THD%) is used as a parameter for comparison. Then, the analysis is focused on two cases of study, in order to experimentally investigate on the harmonic content of the voltage waveforms, deeply describing the steps of the low-level programming with FPGA implementation. Finally, this extensive analysis is also validated by means of the Approximate Total Harmonic Distortion (ATHD) parameter, described in detail in Section 4. This paper is structured as follows: the Cascaded H-Bridge structures and the multicarrier modulation techniques are described in Sections 2 and 3, respectively. The steps for the design of the control software for FPGA control board are reported in Section 4. Finally, by means of a test bench specifically equipped for this purpose, the experimental validation and discussions of the results of the modulation techniques are reported in Section 5.

2. Cascaded H-Bridge Multilevel Inverter

Among the classic structures of multilevel inverters presented in the literature, this work considers the three-phase, five-level Cascaded H-Bridge Multilevel Inverter (CHBMI) topology, which is depicted in Figure 1.

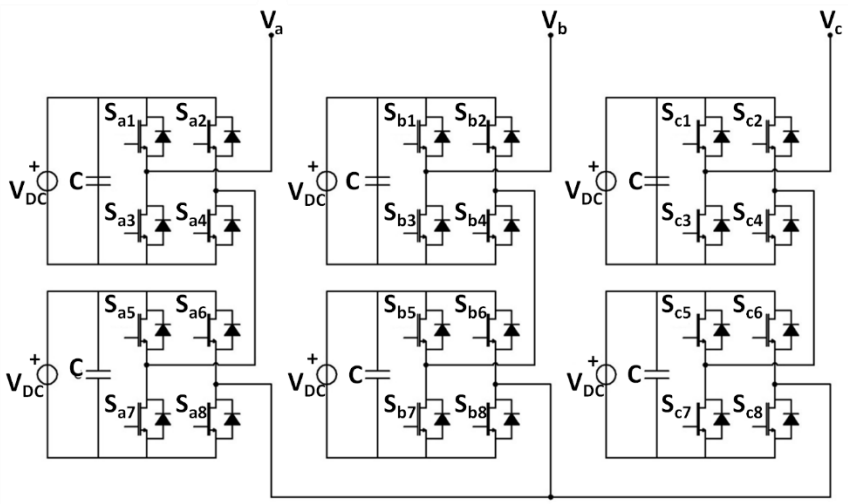


Figure 1. Three-phase, five-level structure of a CHBMI.

This structure is composed by two cascaded-connected H-bridges per phase, each of them requiring its DC source. The latter represents an advantage with respect to the other multilevel structures (i.e., the Diode Clamped Multilevel Inverter or the Capacitor Clamped Multilevel Inverter) for specified fields of applications, such as photovoltaic generation and automotive. Another advantage is represented by the modulability of the structure, providing a high simplicity in case of substituting damaged modules. Moreover, the CHBMI is intrinsically fault-tolerant, as reported in [34]. Generally,

the number of levels n_L can be expressed as a function of the number of the H-bridges, here named n_{HB}:

$$n_L = 2n_{HB} + 1 \tag{1}$$

The output converter voltage (e.g., for phase a) is given by the sum of the voltages generated by the n series-connected modules of each phase:

$$V_a = \sum_{i=1}^{n} V_{AN,i} \tag{2}$$

Therefore, the CHBMI is capable of generating a five-level phase voltage and a nine-level line-to-line voltage.

3. Overview of Multicarrier Modulation Techniques

The PWM techniques adopted for multilevel converters, namely MC PWM [35–40], are usually the same as those applied for traditional converters. The common techniques for Multilevel Power Inverter (MPI) use several triangular carrier signals and one modulating signal per phase. By taking into account the CHBMI topology, the command signals delivered to the components of the same leg of the bridge are obtained through the comparison between each carrier signal and the modulating signal. For a MPI with a number of levels equal to n_L, the number of carrier signals N_c is given by the following equation:

$$N_c = n_L - 1 \tag{3}$$

The modulation index m can be expressed as function of n_L:

$$m = \frac{A_M}{A_C(n_L - 1)} \tag{4}$$

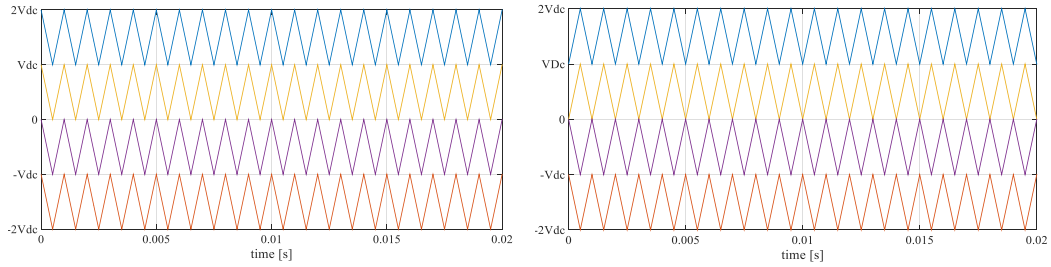
where A_M is the amplitude of the modulating signal, whereas A_C is the amplitude of the carrier signal.

Moreover, the frequency modulation index, namely m_f, is given by the ratio between the frequency of the carrier signal f_C and the frequency of the output fundamental signal f_1:

$$m_f = \frac{f_C}{f_1} \tag{5}$$

In the literature, several MC PWM modulation techniques for multilevel inverters are provided. In particular, depending on the phase shift among the carrier signals, the following dispositions can be obtained:

- Phase Disposition PWM–PD PWM (Figure 2a);
- Phase Opposition Disposition PWM–POD PWM (Figure 2b);
- Alternative Phase Opposition Disposition PWM APOD PWM (Figure 2c);
- Phase Shifted - PS PWM (Figure 2d).



(**a**) (**b**)

Figure 2. *Cont.*

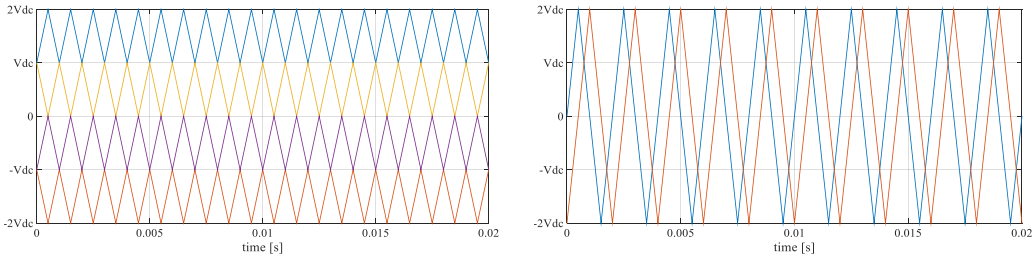


Figure 2. Multicarrier modulation techniques for five-level inverter. (**a**) Sinusoidal Phase Disposition (SPD). (**b**) Sinusoidal Phase Opposition Disposition (SPOD). (**c**) Sinusoidal Alternative Phase Opposition Disposition (APOD). (**d**) Sinusoidal Phase-Shifted (SPS).

Depending on the modulating signal waveform, the following techniques can be obtained:

- Sinusoidal PWM–S (Figure 3);
- Third Harmonic Injection–THI (Figure 4);
- Switching Frequency Optimal–SFO (Figure 5);

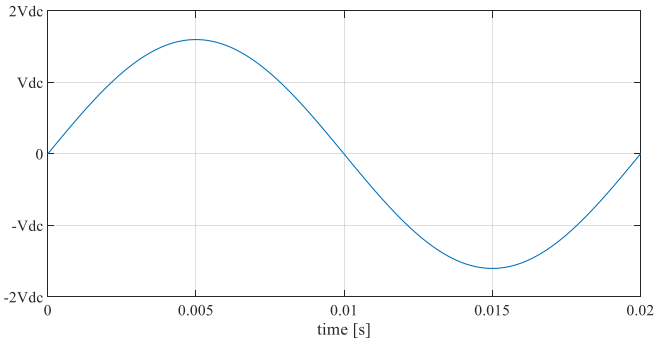


Figure 3. Sinusoidal modulating signal.

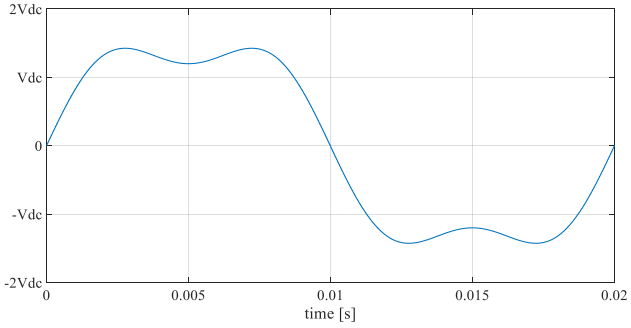


Figure 4. Third Harmonic Injection (THI) modulating signal.

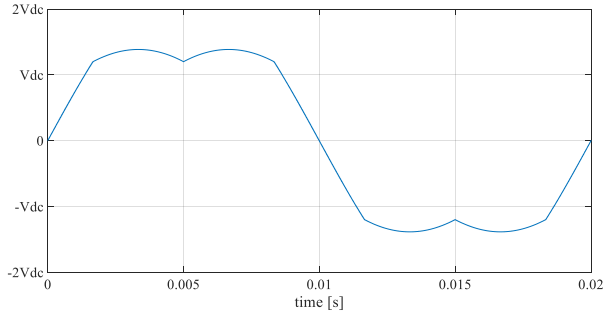


Figure 5. SFO (Switching Frequency Optimal) modulating signal.

4. FPGA Design of the Control Software

The FPGA is commonly used in order to implement complex functions, such as Arithmetic Logic Unit (ALU), memories, communication units and so on [2]. It can be stated that this digital device, due to both its flexibility and high number of configurable digital outputs, is suitable for the implementation of the modulation techniques by using the traditional formula for the evaluation of the duty cycle, providing also higher accuracy in terms of design of the related algorithm, due to the possibility of choice of the frequencies for the clock signals. This section describes the main technical aspects related to the design, implementation and simulation of the control software.

4.1. Features of the Control Software

In order to design a digital system capable of generating the carrier and modulating signals and compare them in an adequate manner, the operations must be synchronized with respect to the chosen operating frequency.

The converter has been controlled with a modulating frequency equal to 10 kHz. The number of samples of the modulating signal is chosen based on the type of modulation. With the purpose of obtaining a synchronous modulation, the number of samples n_s, which are required in the construction of the 50 Hz modulating signal, is given by:

$$n_s = \frac{f_{PWM}}{50}. \tag{6}$$

From Equation (6), the number of obtained samples for the modulating wave is equal to 200. The updating of the modulating samples is managed with a $CLK_{reference}$ clock signal with a frequency equal to f_{PWM}.

The number of samples of the carrier waves $N_{carrier}$ has been chosen equal to 1000 in order to obtain a good resolution. Based on this value, the frequency of the clock signal for the updating of the carrier samples can be determined as follows:

$$CLK_{carrier} = f_{PWM} \cdot N_{carrier} \tag{7}$$

Thus, the frequency of the $CLK_{carrier}$ clock signal obtained from Equation (7) is equal to 10 MHz.

4.2. Digital System Design

The implemented digital system has been designed with the aim of obtaining a synchronous sequential system, so that the data flow can be managed from adequately synchronized timing signals, namely $CLK_{reference}$ and $CLK_{carrier}$, allowing the updating of the modulating and carrier signals, respectively. These signals are generated from the use of a digital Phase Locked Loop (PLL) circuit, whose input source is an external clock signal available in the control board, as reported in [41].

In order to increase the speed of computation of the entire digital system, the reference signals are generated from the use of a Look-Up Table (LUT) with dimensions and resolutions equal to 200×1 and 13 bit, respectively. The carrier signals are generated by adopting up-down binary counters with a resolution of 13 bit and the comparison between reference and carrier signals is realized by a 13-bit digital comparator. This circuit adopts the $CLK_{reference}$ as temporizing signal. Therefore, the comparison is achieved 1000 times for each PWM period equal to 100 µs. The output signals from the comparators represent the command signals for the upper components of the H-Bridges legs.

The generation of the command signals of the components of the lower H-Bridge legs, as well as the obtainment of the dead-time for the protection of the series-connected components, is achieved through the logic circuit shown in Figure 6. The delayed signal is obtained by using several cascaded-connected D flip-flops, whose number is dependent on the adopted clock signal. In order to obtain a 400 ns of delay, four D flip-flops have been connected and managed with the 10 MHz $CLK_{carrier}$ clock signal.

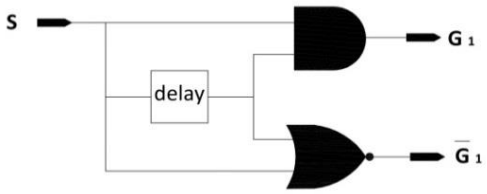


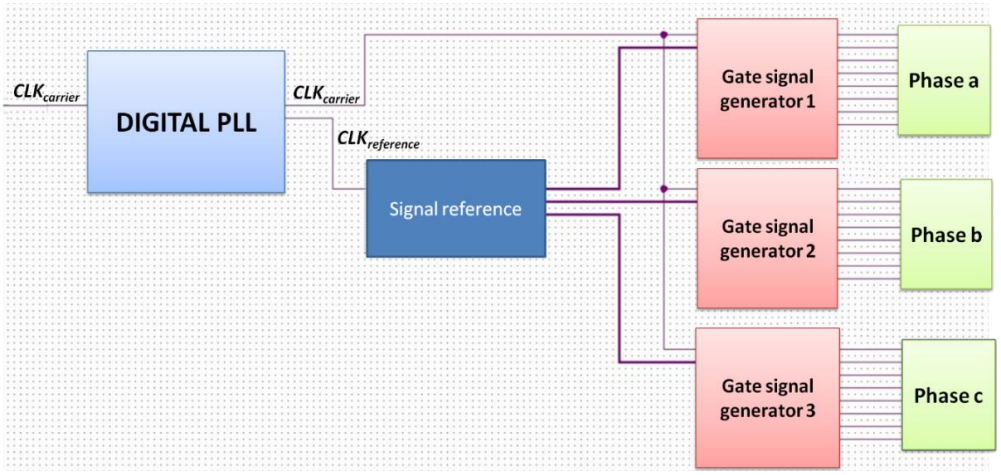
Figure 6. Logic circuit for the dead-time generation.

4.3. FPGA and Software Environment

The digital signal above described has been implemented in a Cyclone III EP3C40Q FPGA (ALTERA®, San Jose, CA, USA). The software environment is Quartus II, produced by ALTERA®; VHDL has been adopted as programming language [42]. The block scheme of the implemented software is depicted in Figure 7a,b.

The digital PLL circuit (see Figure 7a) generates two synchronized clock signals, namely $CLK_{reference}$ and $CLK_{carrier}$, from an external clock signal. For each rising edge of the $CLK_{reference}$ clock, the signal generator block produces the modulating signals for each phase of the converter.

Inside the Gate signal generator block (see Figure 7b), the samples of triangular waves are available for each rising edge of the $CLK_{carrier}$ clock signal. The carrier and modulating samples are compared during the falling edge. For each phase, the command signals are generated at the same instant of time, since the comparisons are realized in parallel.



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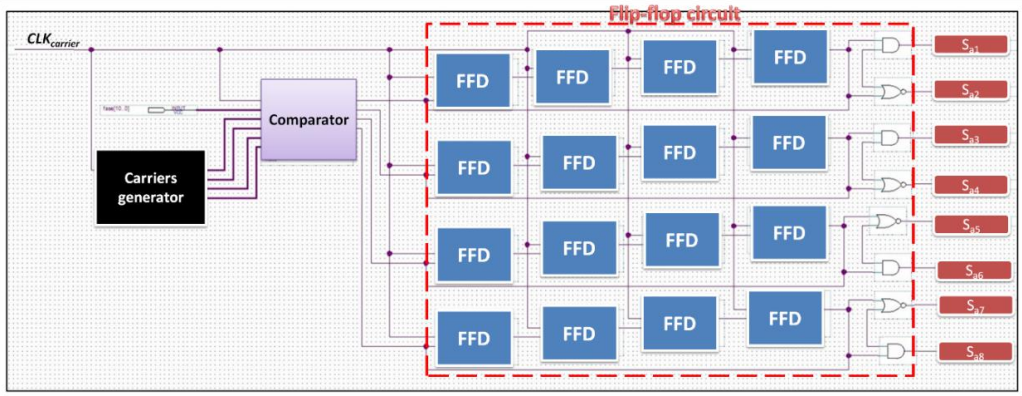
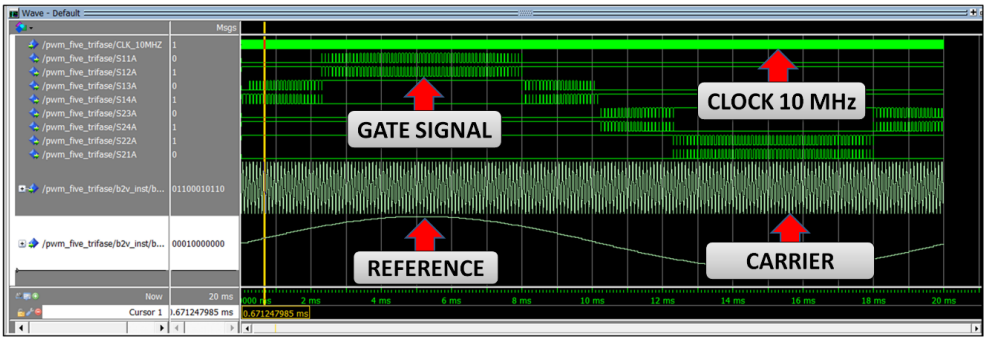


(**b**)

Figure 7. Block scheme of the control software: (**a**) Main schematic, (**b**) Gate signal generator for one phase. PLL: Phase Locked Loop; FFD: Flip-Flop Device.

4.4. Gate Level Simulation

The correct working operation of the implemented control software has been simulated by means of the *ModelSim* environment produced by ALTERA®. Figure 8a shows the results of the simulation, which include the command signals of the components of one phase, the carrier signals and the sinusoidal modulating waveform. A photograph of the test bench is depicted in Figure 8b.



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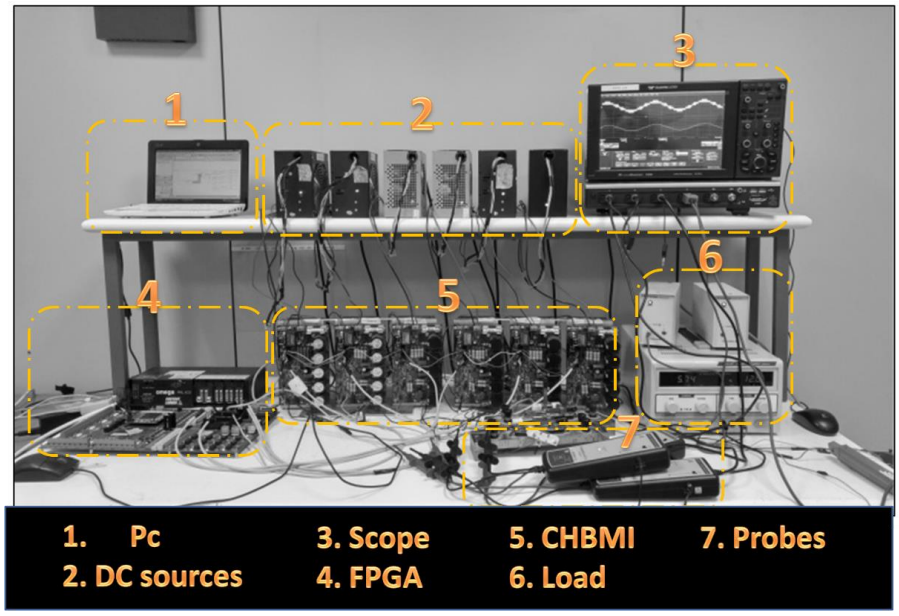

(**b**)

Figure 8. Experimental implementation: (**a**) Gate level simulation results and (**b**) a photograph of the test bench.

5. Comparison between Simulation and Experimental Results

In order to determine the harmonic content of the voltage waveforms produced by a CHBMI controlled by FPGA, the sinusoidal modulation techniques briefly reported in Section 3 have been taken into account due to their greater use in the field of industry applications. Moreover, as previously reported, this analysis is performed by considering the THD%, which can be evaluated as follows [39]:

$$THD\% = \sqrt{\frac{V_{rms}^2 - V_{rms,1}^2}{V_{rms,1}^2}} \cdot 100 \tag{8}$$

where V_{rms} is the root mean square value of the phase voltage and $V_{rms,1}$ is the root mean square value of its fundamental harmonic.

For this purpose, in a first phase (simulation phase), the trends of both the phase and line-to-line voltages have been simulated by means of the Matlab/Simulink environment, in which the model of a 5-level CHBMI was implemented. Several simulations have been carried out with different values of the modulation index, ranging from 0.4 to 1.2.

In a second phase (experimental verification), the prototype of a 5-level CHBMI has been assembled and the related test bench (see Figure 8b), is mainly composed by:

- A prototype of FPGA-based control board (Cyclone III–ALTERA®, DigiPowers.r.l);
- Six power MOSFET-based H-bridge prototypes (model IRFB4115PbF, DigiPowers.r.l, city, country), whose technical features are summarized in Table 1;
- A LeCroy WaveRunner 6Zi scope (Teledyne, city, state abbrev if USA, country) used for the real-time monitoring and acquisition of the related waveforms;
- Six DC sources with 12 V of rated voltage;
- A balanced RL three-phase electric load.

Table 1. Features of the IRFB4115PBF device [43].

Magnitude (unit)	Symbol	Value
Voltage (V)	V_{dss}	150
Resistance (mΩ)	$Rds_{(on)}$	9.3
Current (A)	$I_{d\ (siliconlimited)}$	104
Turn on delay (ns)	$T_{D(ON)}$	18
Rise time (ns)	t_R, rise time	73
Turn off delay (ns)	$T_{D(OFF)}$,	41
Fall time (ns)	t_F	39
Reversal recovery (ns)	t_{RR}	86

The voltage waveforms have been acquired by the Teledyne LeCroy WaveRunner 6Zi acquisition system with a number of samples equal to 1 Ms and in a time interval equal to 20 ms, corresponding to a sampling frequency of 50 MHz. The THD% values of the acquired waveforms have been, then, processed through means of the Matlab software.

Figure 9 shows the comparison between the simulation and experimental values of THD% as function of m of both the phase and line voltage for each of the modulation techniques taken into account.

From Figure 10 it can be noticed that the THD% values experimentally obtained are comparable with those derived through simulations. This is due to both the implementation of parallel computing and the relatively high speed of processing of the FPGA.

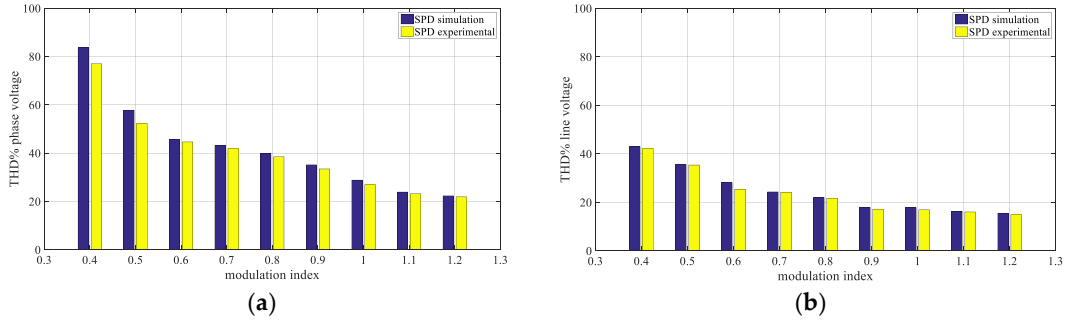

Figure 9. *Cont.*

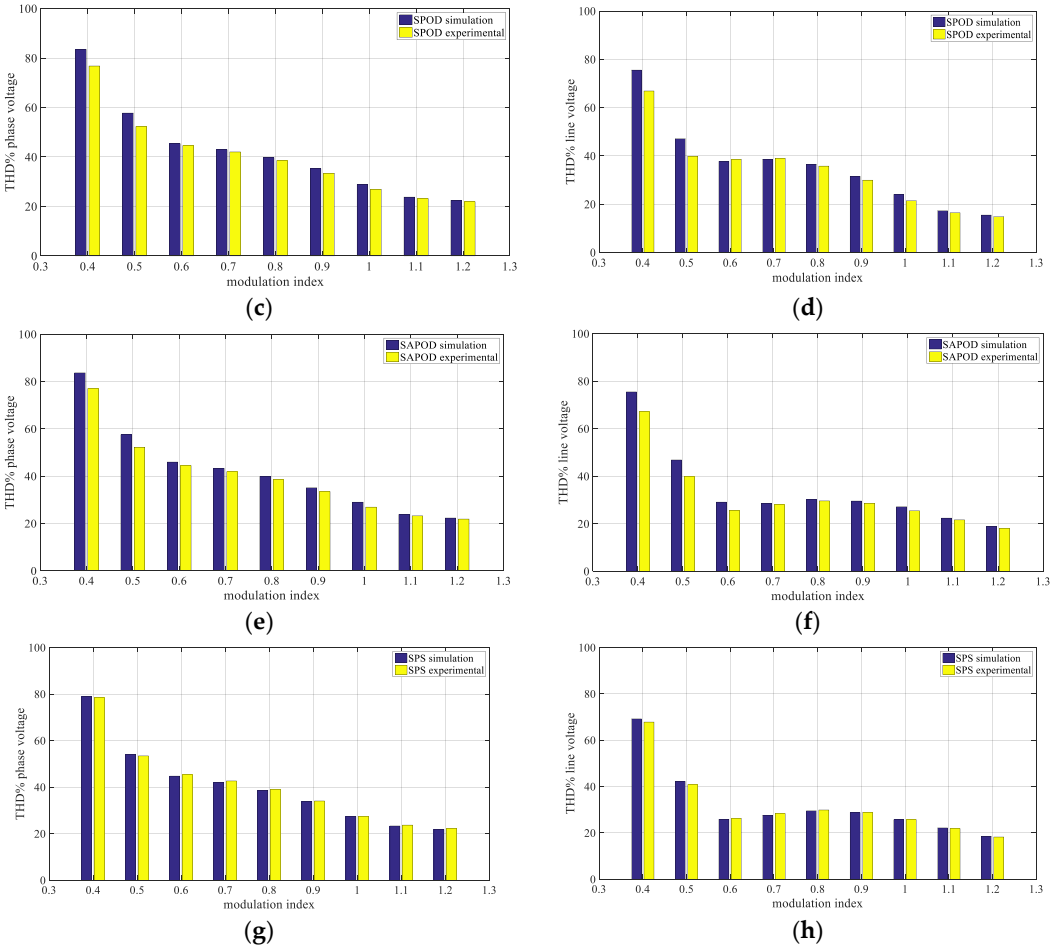

Figure 9. Comparison between the simulated (blue) and the experimental (yellow) THD% values. (**a**) Phase Voltage-SPD; (**b**) Line Voltage-SPD; (**c**) Phase Voltage-SPOD; (**d**) Line Voltage-SPOD; (**e**) Phase Voltage-SAPOD; (**f**) Line Voltage-SAPOD; (**g**) Phase Voltage-SPS; (**h**) Line Voltage-SPS.

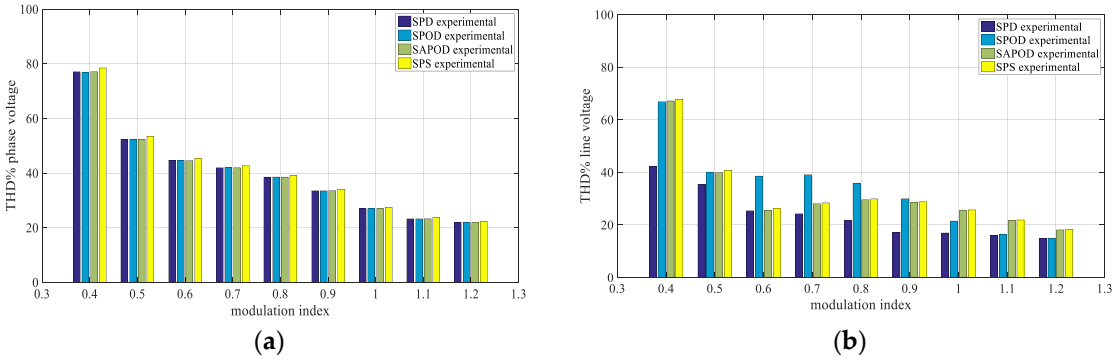

Figure 10. Comparison between the experimental THD% results for (**a**) phase voltage and (**b**) line voltage.

By referring to Figure 11, in which the experimental results are plotted all together for the phase voltage (Figure 11) and the line-to-line voltage (Figure 11), it is interesting to observe that the THD% values of the phase voltages for each modulation technique are almost close to each other. On the contrary, the THD% values for the line voltages significantly differ between the modulation techniques, with the lowest values corresponding to the SPD technique for any value of m. Moreover, the SAPOD technique presents the highest THD% values in the modulation range between 0.6 and 0.9.

The spectra of the SPD, SPOD and SAPOD modulation techniques present harmonics centered at a frequency f_h equal to:

$$f_h = k \cdot f_{PWM} \tag{9}$$

where f_{PWM} is the switching frequency and k is an integer number.

On the contrary, by considering the harmonic spectrum of the SPS technique, the harmonics are centered at a frequency f_h corresponding to:

$$f_h = 4k \cdot f_{PWM} \tag{10}$$

In order to deeply investigate the performance of the converter controlled by the previously described techniques, the harmonic spectra of the measured line voltages have been analyzed for two specific values of m, equal to 0.5 and 0.9. The first value corresponds to the condition of comparable THD% between the proposed modulation techniques, whereas the second value corresponds to the condition of minimum values of THD% within the linear region.

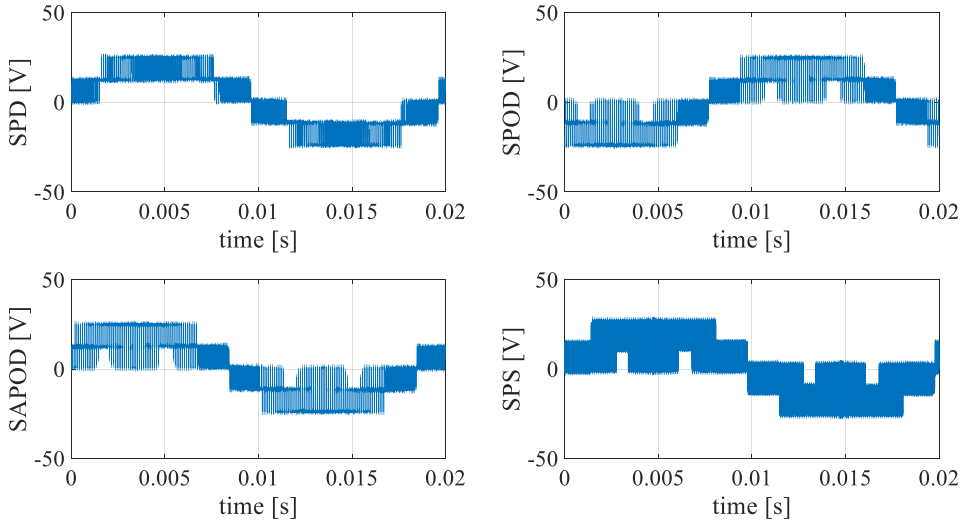

Figure 11. Line voltage waveforms acquired with a modulation index equal to 0.5.

Table 2 summarizes the values obtained from this analysis and the corresponding trends of the line voltages for the eight conditions of Table 2 are all plotted in Figure 11 (m = 0.5) and Figure 12 (m = 0.9).

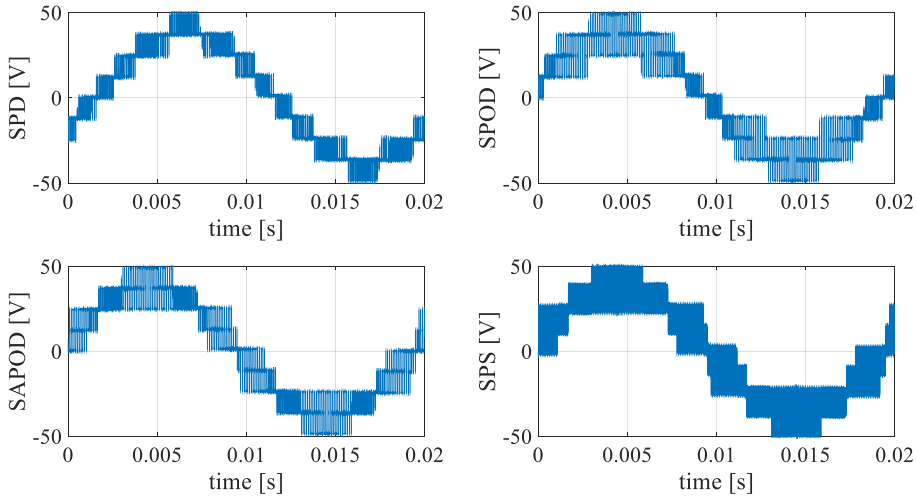

Figure 12. Line voltage waveforms acquired with a modulation index equal to 0.9.

Table 2. THD% for modulation indexes equal to 0.5 and 0.9.

Modulation Technique	THD% m = 0.5	THD% m = 0.9
SPD	35.38%	17.19%
SPOD	39.88%	29.95%
SAPOD	39.87%	28.64%
SPS	40.77%	28.83%

It can be noticed that these trends present differences in terms of voltage waveforms, at the same value of m. Figure 13 shows the comparison between the harmonic spectra centered around the switching frequency of 10 kHz (see Figure 14a) and their multiples from 20 kHz to 80 kHz (see Figure 14b–h) in the case of study of m=0.5 (the harmonic amplitudes are expressed as percentage of the fundamental harmonic).

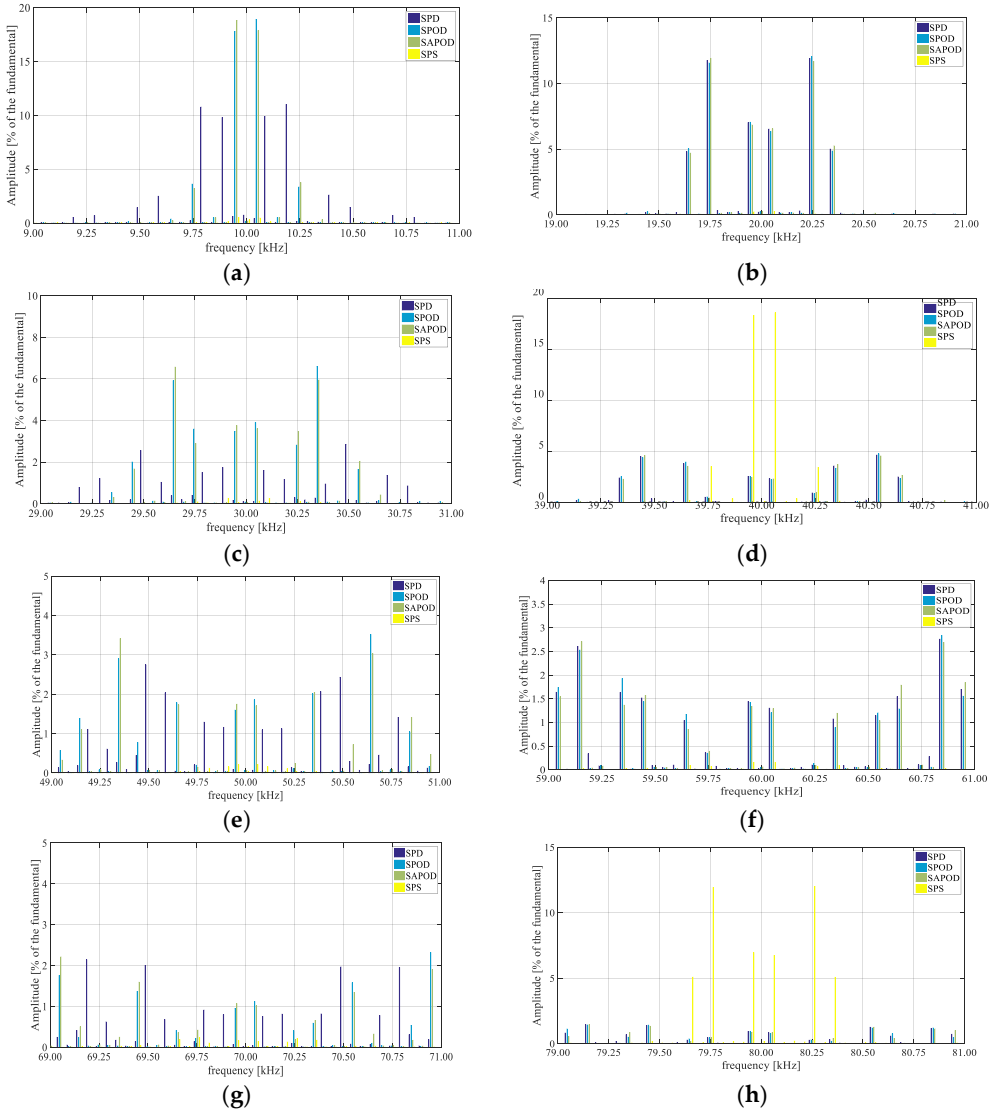

Figure 13. Comparison between the harmonic spectra around the center of multiples of the switching frequency for m equal to 0.5: SPD (blue bar), SPOD (light-blue bar), SAPOD (green bar) and SPS (yellow bar). (**a**) harmonic spectrum centered at 10 kHz; (**b**) harmonic spectrum centered at 20 kHz; (**c**) harmonic spectrum centered at 30 kHz; (**d**) harmonic spectrum centered at 40 kHz; (**e**) harmonic spectrum centered at 50 kHz; (**f**) harmonic spectrum centered at 60 kHz; (**g**) harmonic spectrum centered at 70 kHz; (**h**) harmonic spectrum centered at 80 kHz.

For each frequency, only lateral bands are detected. Moreover, at the 10 kHz frequency and for odd values of k, the major contribution in terms of amplitude is given by the SPOD and SAPOD techniques, whereas the SPD presents a lower contribution, even with the presence of a higher number of harmonics.

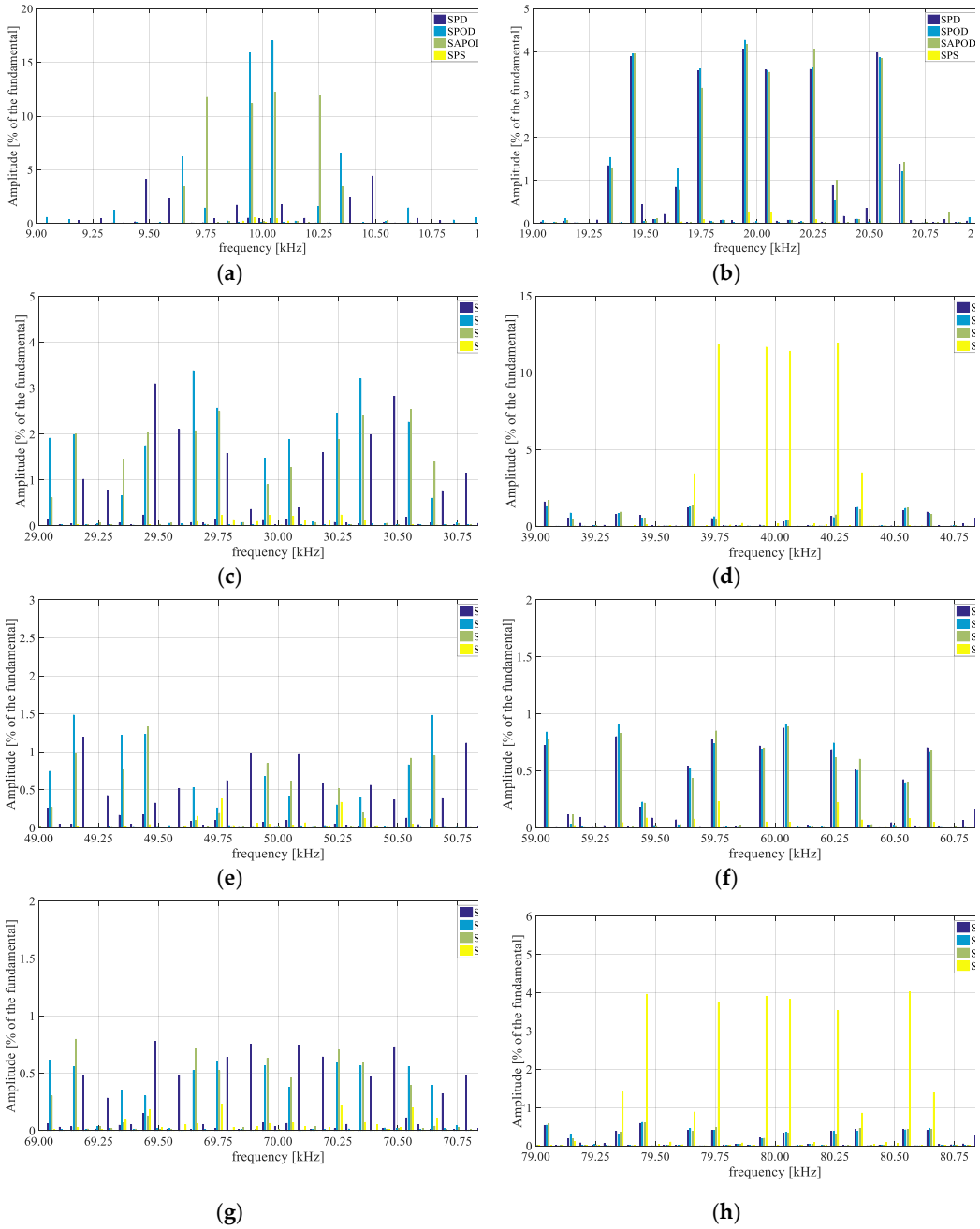

Figure 14. Comparison between the harmonic spectra around the center of multiples of the switching frequency for m equal to 0.9: SPD (blue bar), SPOD (light-blue bar), SAPOD (green bar) and SPS (yellow bar). (**a**) harmonic spectrum centered at 10 kHz; (**b**) harmonic spectrum centered at 20 kHz; (**c**) harmonic spectrum centered at 30 kHz; (**d**) harmonic spectrum centered at 40 kHz; (**e**) harmonic spectrum centered at 50 kHz; (**f**) harmonic spectrum centered at 60 kHz; (**g**) harmonic spectrum centered at 70 kHz; (**h**) harmonic spectrum centered at 80 kHz.

Instead, for even values of k, the SPD, SPOD and SAPOD techniques present the same harmonic contribution both in terms of amplitude and spectra distribution. Moreover, the SPS technique presents

harmonic content only for 2k multiples. The case of study of m = 0.9 is investigated in Figure 14, which shows the comparison between the harmonic spectra of the proposed techniques centered around the switching frequency of 10 kHz (see Figure 14a) and their multiples from 20 kHz to 80 kHz (see Figure 14b–h).

As in the previous case, only lateral bands are detected. In addition, in case of even values of k, the SPD, SPOD and SAPOD techniques present almost the same harmonic content and the SPS harmonics appear for frequencies equal to 4k. For odd values of k, the major harmonic contributions are given by the SPOD and SAPOD techniques, while the SPD presents the lowest contribution, except for the frequency equal to 70 kHz, in which the harmonic content is comparable in terms of amplitude. Therefore, from this analysis it can be stated that the different values of THD% depend on the harmonic components with frequencies corresponding to odd values of k.

The well-known equation for the determination of the *THD* is given by:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \tag{11}$$

In order to evaluate the contribution produced by each modulation technique for each of the considered frequency f_h, the following Approximate Total Harmonic Distortion formula, namely *ATHD*, is considered:

$$ATHD^2 = \frac{\sum_{h=9}^{11} V_h^2}{V_1^2} + \frac{\sum_{h=19}^{21} V_h^2}{V_1^2} + \frac{\sum_{h=(kf_{PWM}-1)}^{(kf_{PWM}+1)} V_h^2}{V_1^2} \tag{12}$$

The *ATHD* is based on distributing Equation (11) only for the frequencies of interest, as shown by Equation (12). Thus, the sum is extended only within the range of the analyzed frequencies and, therefore, each sum defines a partial *THD* (*PTHD*). Consequentially, the *ATHD* can be also expressed as function of the *PTHD*:

$$ATHD^2 = PTHD_{10kHz} + PTHD_{20kHz} + \ldots + PTHD_{kf_{PWM}} \tag{13}$$

$$ATHD = \sqrt{\sum_{h=f_{PWM}}^{kf_{PWM}} PTHD_h} \tag{14}$$

Furthermore, the *PTHD* values allow the evaluation of the contribution to the *ATHD* for each modulation technique.

Figures 15 and 16 show the PTHD values computed for the two cases. From this graphical view, it can be noticed that the SPD technique provides the lowest harmonic contribution (the highest difference can be detected for f = 10 kHz and m = 0.5), whereas the SPS technique gives the major contribution at the frequencies of 40 kHz and 80 kHz.

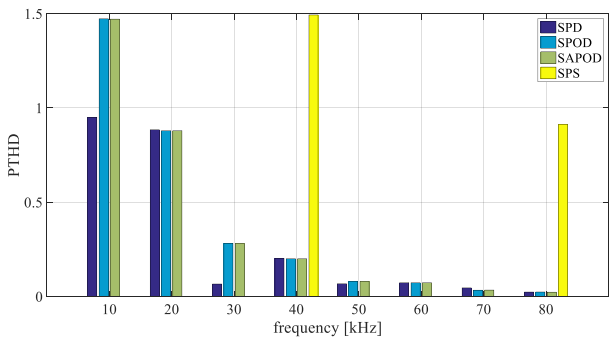

Figure 15. Comparison of PTHD values for modulation index equal to 0.5.

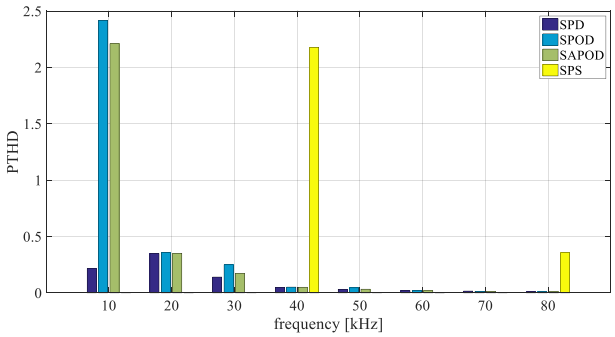

Figure 16. Comparison of PTHD values for modulation index equal to 0.9.

6. Conclusions

This paper has presented the performance of a CHBMI five-level three phase with an FGPA-based controller. The first step of this analysis has provided a comparison between the simulation and experimental results obtained from the multicarrier modulation techniques with sinusoidal waveform as reference signal. Both for the phase and line voltages, the THD% values computed from the simulations and from the experimental data are almost comparable to each other, for any of the considered modulation techniques and independently from the value of the modulation index, demonstrating the high-performance of the FPGA control system.

Even though the obtained THD% values for the phase voltage are comparable between the proposed modulation techniques independently from the value of modulation index, the THD% related to the line-to-line voltage differ among the techniques, with the lowest contribution provided by the SPD technique.

Finally, the line voltage harmonic spectra for two specific cases of study (m = 0.5 and m = 0.9) have been taken into account by evaluating the THD% in the frequency range of interest for each of the proposed described modulation technique. From this comparison, it can be stated that the SPD technique provides the lowest contribution for each of the considered frequency range.

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