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Development of an SDBC-MMCC-Based DSTATCOM for Real-Time Single-Phase Load Compensation in Three-Phase Power Distribution Systems

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Abstract: This paper proposes a newly developed single-delta bridge-cell, modular multilevel cascade converter (SDBC-MMCC)-based distribution-level static synchronous compensator (DSTATCOM) for single-phase load compensation in three-phase, three-wire electric power distribution systems. Each main circuit arm of the DSTATCOM uses a modular multilevel cascade converter based on full-H-bridge (FHB) cells. The three main DSTATCOM arms are delta-connected to allow phase-independent operations for phase balancing and unity power factor correction of the single-phase load in three-phase, three-wire electric power distribution systems. By using the symmetrical components method, a feedforward compensation algorithm was employed for the DSTATCOM. A simulation of the DSTATCOM was performed for functioning verification. Finally, a hardware test system was built by using a multi-DSP-based control system. The test results verified the effectiveness of the proposed SDBC-MMCC-based DSTATCOM in single-phase load compensation.

Keywords: DSTATCOM; full-H-bridge converter; phase balancing; power factor correction; SDBC-MMCC; single-phase load compensation

1. Introduction

In a three-phase electric power distribution system, a large power capacity of single-phase load (e.g., an electrical railway traction system) absorbs unbalanced (negative-sequence) load current and reactive power. The unbalanced load current produces an unbalanced voltage drop on the electric power distribution line. The resulting unbalanced voltage affects other sensitive loads connected to the distribution system. For example, AC rotary machines will induce extra losses, and rectifier loads will generate ripples in their DC links. Moreover, the unbalanced current will disturb the normal operation of an electric power generator. To keep good power quality, the unbalanced current from the single-phase load should be improved [1,2].

Traditionally, the delta connection of passive inductive/capacitive reactances, also known as a "Steinmetz compensator", was employed for single-phase load compensations in three-phase power systems [3–5]. The operation principle of the Steinmetz compensator has been used in many applications of unbalanced load compensations [6]. Presently, static var compensators (SVC) are widely used in the load compensations of high-power, single-phase traction systems [7–9]. The thyristor-controlled reactor with fixed capacitor (TCR–FC) type of SVC is applied in these traction systems. A drawback of the TCR–FC type of SVC is that it demands large space for installation. Two-level converters can also

be used for single-phase load compensations in three-phase power systems [10–12]. However, the power ratings of two-level converters are limited.

Recently, static synchronous compensators (STATCOMs) have been introduced as the next-generation shunt compensators [13–16]. Compared to traditional SVCs, STATCOMs have quicker response times, more compact structures, wider compensation ranges, and smaller installation space demand. Therefore, distribution-level static synchronous compensators (DSTATCOMs) are highly suitable for unbalanced load compensations in modern three-phase electric power distribution systems. Various types of converters can be employed to construct the main circuit of a DSTATCOM. Due to lower voltage stress and modular structure, single-delta bridge-cell, modular multilevel cascade converters (SDBC-MMCCs) are very suitable for the main circuits of DSTATCOMs in high-voltage and high-power applications [17–20]. Hence, the SDBC-MMCC-based DSTATCOMs can replace the SVCs in single-phase load compensations.

In this paper, a new concept of applying an SDBC-MMCC-based DSTATCOM for real-time single-phase load compensation in a three-phase, three-wire power distribution system is proposed. Applications of multilevel full-H-bridge (FHB) converters and staircase modulation in the DSTATCOM main circuit can achieve high-efficiency operation in practical applications. A feedforward compensation algorithm derived from the symmetrical components method was designed for the DSTATCOM, which was constructed using the MATLAB/SimuLink program for preliminary verification. Finally, a hardware prototype test system was built using a multi-TMS320F2812 digital signal processor (DSP)-based control system. Experimental results show that the proposed SDBC-MMCC-based DSTATCOM has a rapid response and a satisfactory compensation effect. This paper is a further development of the SDBC-MMCC-based DSTATCOM for three-phase unbalanced load compensation that we previously described [21]. In single-phase load compensation, the control algorithm of the DSTACOM is more compact, and the sizing of the DSTATCOM is more precisely defined.

2. DSTATCOM Load Compensation Algorithm

Figure 1 illustrates the study system for deriving the DSTATCOM compensation algorithm. A shunt type of DSTATCOM is installed for the on-site single-phase load compensation. The feedforward compensation algorithm detects the load power parameters, P^L_{ab} and Q^L_{ab}, and sends three reactive power compensation commands, $Q^{ST*}_{ab,bc,ca}$, to the DSTATCOM's main circuit arms. The three DSTATCOM arms independently regulate their reactive power inputs, then the synthesized DSTATCOM line current compensates the unbalanced single-phase load current. Consequently, the source currents are balanced with a unity power factor. Using the symmetrical components method, we derived the feedforward compensation algorithm. Figure 2 shows the phase-sequence circuits of Figure 1.

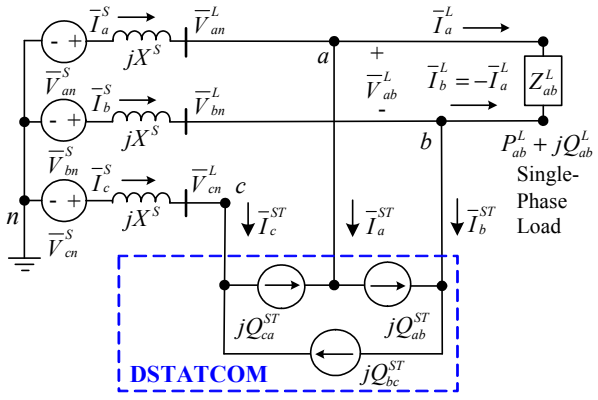

Figure 1. Three-phase, three-wire power distribution system with single-phase load and distribution-level static synchronous compensator (DSTATCOM).

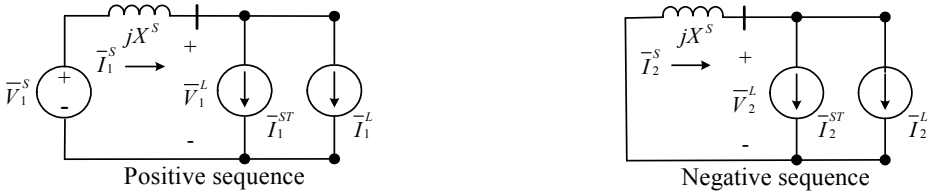

Figure 2. Phase-sequence circuits of Figure 1.

Equation (1) expresses the line voltage of the load bus illustrated in Figure 1, where V^{ll} represents the line voltage. The phase-*a* load current is shown in Equation (2), in which the relationship of $(\overline{V}_{ab}^{L})^{*}\cdot\overline{I}_{a}^{L} = P_{ab}^{L} - jQ_{ab}^{L}$ is used. The symmetrical components of the load current are then calculated using Equation (3).

$$\overline{V}_{ab}^{L} = \overline{V}_{an}^{L} - \overline{V}_{bn}^{L} = V^{ll}\angle 30^{o} \tag{1}$$

$$\overline{I}_{a}^{L} = \frac{1}{V^{ll}\angle -30^{o}}(P_{ab}^{L} - jQ_{ab}^{L}) \tag{2}$$

$$\begin{bmatrix} \overline{I}_{0}^{L} \\ \overline{I}_{1}^{L} \\ \overline{I}_{2}^{L} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ & 1aa^{2} & \\ & 1a^{2}a & \end{bmatrix}\begin{bmatrix} \overline{I}_{a}^{L} \\ -\overline{I}_{a}^{L} \\ 0 \end{bmatrix} \tag{3}$$

Equation (3) can be rewritten as rectangular forms, as indicated in Equations (4) and (5). The zero-sequence component of the load current is zero. Equation (6) gives the three arm currents of the DSTATCOM, where the relationship of $\overline{V}^{*}\cdot\overline{I} = P - jQ$ is used. Equation (7) shows the DSTATCOM line currents. Using the symmetrical components transformation in Equation (8), Equation (9) shows the symmetrical components of the DSTATCOM line current in terms of the reactive power flows of the three DSTATCOM arms. For a DSTATCOM with a delta-connected main circuit, the zero-sequence current, $\overline{I}_{0}^{ST}$, in Equation (8) is zero.

$$\begin{aligned} \overline{I}_{1}^{L} &= \tfrac{1}{\sqrt{3}V^{ll}}[P_{ab}^{L} - jQ_{ab}^{L}] = \tfrac{P_{ab}^{L}}{\sqrt{3}V^{ll}} - j\tfrac{Q_{ab}^{L}}{\sqrt{3}V^{ll}} \\ &= \mathrm{Re}\left\{\overline{I}_{1}^{L}\right\} + j\mathrm{Im}\left\{\overline{I}_{1}^{L}\right\} \end{aligned} \tag{4}$$

$$\begin{aligned} \overline{I}_{2}^{L} &= \tfrac{1}{\sqrt{3}V^{ll}}(\tfrac{1}{2}P_{ab}^{L} + \tfrac{\sqrt{3}}{2}Q_{ab}^{L}) + j\tfrac{1}{\sqrt{3}V^{ll}}(\tfrac{\sqrt{3}}{2}P_{ab}^{L} - \tfrac{1}{2}Q_{ab}^{L}) \\ &= \mathrm{Re}\left\{\overline{I}_{2}^{L}\right\} + j\mathrm{Im}\left\{\overline{I}_{2}^{L}\right\} \end{aligned} \tag{5}$$

$$\begin{aligned} \overline{I}_{ab}^{ST} &= \left(-jQ_{ab}^{ST}\right)/(V^{ll}\angle -30^{\circ}) \\ \overline{I}_{bc}^{ST} &= \left(-jQ_{bc}^{ST}\right)/(V^{ll}\angle 90^{\circ}) \\ \overline{I}_{ca}^{ST} &= \left(-jQ_{ca}^{ST}\right)/(V^{ll}\angle -150^{\circ}) \end{aligned} \tag{6}$$

$$\begin{bmatrix} \overline{I}_{a}^{ST} \\ \overline{I}_{b}^{ST} \\ \overline{I}_{c}^{ST} \end{bmatrix} = \begin{bmatrix} \overline{I}_{ab}^{ST} - \overline{I}_{ca}^{ST} \\ \overline{I}_{bc}^{ST} - \overline{I}_{ab}^{ST} \\ \overline{I}_{ca}^{ST} - \overline{I}_{bc}^{ST} \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} \overline{I}_{0}^{ST} \\ \overline{I}_{1}^{ST} \\ \overline{I}_{2}^{ST} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^{2} \\ 1 & a^{2} & a \end{bmatrix}\begin{bmatrix} \overline{I}_{a}^{ST} \\ \overline{I}_{b}^{ST} \\ \overline{I}_{c}^{ST} \end{bmatrix},\ a = 1\angle 120^{\circ} \tag{8}$$

$$\begin{aligned} \overline{I}_{1}^{ST} &= \tfrac{-j}{3V^{ll}}(Q_{ab}^{ST} + Q_{bc}^{ST} + Q_{ca}^{ST}) \\ \overline{I}_{2}^{ST} &= \tfrac{1}{\sqrt{3}V^{ll}}(\tfrac{\sqrt{3}}{2}Q_{ab}^{ST} - \tfrac{\sqrt{3}}{2}Q_{ca}^{ST}) + j\tfrac{1}{\sqrt{3}V^{ll}}(\tfrac{-1}{2}Q_{ab}^{ST} + Q_{bc}^{ST} - \tfrac{1}{2}Q_{ca}^{ST}) \end{aligned} \tag{9}$$

As shown in Figure 2, for the single-phase load compensation, the DSTATCOM should compensate the entire negative-sequence component and imaginary part of the positive-sequence component currents generated by the single-phase load, as revealed in Equation (10) [21,22]. The source current only supplies the real part of the positive-sequence load current. As a result, with the assistance of the DSTATCOM compensation, the source current is balanced with a unity power factor.

$$\bar{I}_1^{ST} + \mathrm{Im}\left\{\bar{I}_1^{L}\right\} = 0, \bar{I}_2^{ST} + \bar{I}_2^{L} = 0 \tag{10}$$

Finally, combining Equations (4), (5) and (9), (10), we obtained the required load compensation algorithm of each DSTATCOM arm for real-time single-phase load compensation, as indicated by Equation (11). Equation (11) is very compact and suitable for the SDBC-MMCC-based DSTATCOM. The sizing of the DSTATCOM can easily be calculated using Equation (11). The DSTATCOM is treated as a reactive power load in the compensation. The reactive power flow of each DSTATCOM arm, which can be inductive or capacitive, is independently controlled by the compensation algorithm in Equation (11). By using power calculation definitions, $P = (\int_T i{\cdot}v\,dt)/T$ and $Q = (-\int_T i{\cdot}v(\pi/2)dt)/T$, in the time domain, Equation (12) shows another version of Equation (11) for the DSATCOM, where T is the period of the fundamental frequency. Equation (12) can easily be digitized and implemented in a digital controller. Finally, Equation (13) shows the three-phase source current with DSTATCOM compensation.

$$\begin{array}{l} Q_{ab}^{ST*} = -Q_{ab}^{L} \\ Q_{bc}^{ST*} = -P_{ab}^{L}/\sqrt{3} \\ Q_{ca}^{ST*} = P_{ab}^{L}/\sqrt{3} \end{array} \tag{11}$$

$$\begin{array}{l} Q_{ab}^{ST*} = \frac{1}{\sqrt{3}T} \times \int_T [i_a^L{\cdot}(v_{ca}^L - v_{bc}^L)]dt \\ Q_{bc}^{ST*} = \frac{-1}{\sqrt{3}T} \times \int_T (i_a^L{\cdot}v_{ab}^L)\,dt \\ Q_{ca}^{ST*} = \frac{1}{\sqrt{3}T} \times \int_T (i_a^L{\cdot}v_{ab}^L)\,dt \end{array} \tag{12}$$

$$\begin{bmatrix} \bar{I}_a^S \\ \bar{I}_b^S \\ \bar{I}_c^S \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} \bar{I}_0^S \\ \bar{I}_1^S \\ \bar{I}_2^S \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} 0 \\ P_{ab}^L/(\sqrt{3}V^{ll}) \\ 0 \end{bmatrix} = \begin{bmatrix} P_{ab}^L/(\sqrt{3}V^{ll})\angle 0^\circ \\ P_{ab}^L/(\sqrt{3}V^{ll})\angle -120^\circ \\ P_{ab}^L/(\sqrt{3}V^{ll})\angle 120^\circ \end{bmatrix} \tag{13}$$

3. DSTATCOM Main Circuit

Figure 3 shows a three-phase power distribution system, a single-phase load, and the proposed seven-level, SDBC-MMCC-based DSTATCOM as the test system in the paper. Each STATCOM arm consists of an internal voltage source, V^{ST}, modulated by a seven-level, cascade full-H-bridge converter and a commutation reactor, X^{ST}. In this study, each DSTATCOM arm is equivalent to a purely reactive power load.

The reactive power flows of these three DSTATCOM arms are regulated independently for the single-phase load compensation. The power inputs of each DSTATCOM arm in Figure 3 are expressed in Equations (14) and (15), respectively. An indirect phasor-domain power angle regulation method is used for the reactive power control in the DSTATCOM. For a reactive power demand, the DSTATCOM controller regulates the power angle, δ^{ST}, to absorb or release the active power from the power source according to Equation (14). The active power flow charges or discharges the DC-link capacitors and then regulates the DC-link voltages. Finally, the cascaded DC-link voltages synthesize the internal voltage, V^{ST}, then the DSTATCOM absorbs capacitive or inductive reactive power according to Equation (15). When the reactive power response is completed, the power angle returns to near-zero values. With the delta-connected main circuit, the three DSTATCOM arms achieve phase-independent operation. Hence, much like a traditional SVC, the DSTATCOM can easily compensate the unbalanced load current and correct the power factor caused by a single-phase load.

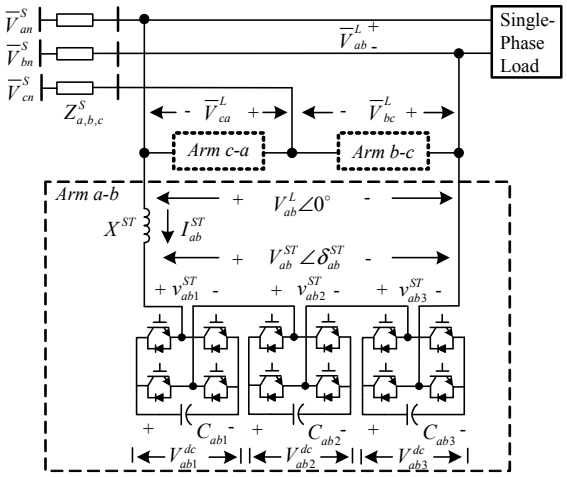

Figure 3. The test system with a single-phase load and the proposed seven-level, single-delta, bridge-cell, modular multilevel cascade converter (SDBC-MMCC)-based DSTATCOM.

A typical staircase modulation scheme, depicted in Figure 4, enables the DSTATCOM main circuit to operate with high efficiency. Each level and internal voltage waveform of the DSTATCOM arm *a-b* in Figure 3 are also shown [21]. The internal voltage v^{ST} shows a staircase waveform. The three switching angles, θ_1–θ_3, should be determined to minimize the harmonics generated. The internal voltage v^{ST} in Figure 4 can be represented as a Fourier series, as detailed in Equation (16), where n is the harmonic order ($n = 1, 3, 5, 7, \ldots$). Ideally, the harmonic order contains only odd-order components. Equation (17) shows the harmonic components in Equation (16).

$$P^{ST} = -\frac{V^{ST}V^{L}}{X^{ST}}\sin\delta^{ST} \tag{14}$$

$$Q^{ST} = \frac{V^{L}(V^{L} - V^{ST}\cos\delta^{ST})}{X^{ST}} \tag{15}$$

$$v^{ST}(\omega t) = \frac{4V^{dc}}{\pi}\sum_{n}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)]\cdot\frac{\sin(n\omega t)}{n}, 0^{\circ} < \theta_1 < \theta_2 < \theta_3 < 90^{\circ},\ n = 1, 3, 5, 7, \ldots \tag{16}$$

$$H(n) = \frac{4V^{dc}}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)] \tag{17}$$

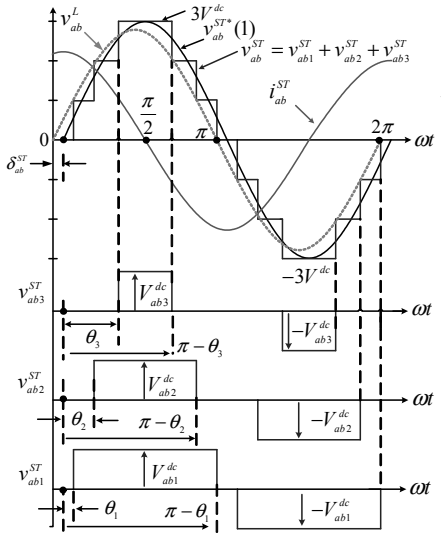

Figure 4. Voltage waveforms of the DSTATCOM arm *a-b* using staircase modulation.

In Equation (17), setting $n = 1$ produces the fundamental component $H(1)$, which consists of the DC-link voltage V^{dc} and three switching angles, θ_1–θ_3. The fundamental component $H(1)$ is used for the reactive power regulation. To eliminate the specified harmonic orders, a harmonic-minimizing method is used [23]. Assigning $H(1) = 3V^{dc}$ for the fundamental-component modulation and setting $H(5) = H(7) = 0$ for the 5th and 7th orders' harmonic cancellation produces Equation (18). Subsequently, solving Equation (18) results in the required switching angles, namely, $\theta_1 = 11.68^\circ$, $\theta_2 = 31.18^\circ$, $\theta_3 = 58.58^\circ$.

$$\begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= 3\pi/4 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) &= 0 \end{aligned} \tag{18}$$

Figure 5 depicts the functional block diagram of the DSTATCOM controller proposed in this paper. As noted, the control algorithm using Equation (11) calculates the required reactive power values of the three DSTATCOM arms in real time. Three well-tuned proportional integral derivative (PID) feedback controllers in the inner loops regulate the reactive power inputs of the three DSTATCOM arms independently, as shown in Equation (19). The three output commands of the PID controllers, $\delta^{ST*}_{ab,bc,ca}$, generate the gating signals, as shown in Figure 4 for these switching elements in the three DSTATCOM arms. With the proposed controller shown in Figure 5, the DSTATCOM completes the single-phase load compensation in real time. The DSTATCOM controller in Figure 5 requires a fast power detection method. Figure 6 schematizes the fast calculation method of active and reactive powers that applies the single-phase $\alpha - \beta$ reference axis method. Applying this fast calculation results in the load power values for Equation (11) and the reactive power inputs of the three DSTATCOM arms in real time.

$$\begin{aligned} \delta^{ST*}_{ab,bc,ca} &= K_P \Delta Q^{ST}_{ab,bc,ca} + K_I \int \Delta Q^{ST}_{ab,bc,ca} dt + K_D \tfrac{d}{dt} \Delta Q^{ST}_{ab,bc,ca} \\ \text{where,} \quad \Delta Q^{ST}_{ab,bc,ca} &= Q^{ST*}_{ab,bc,ca} - Q^{ST}_{ab,bc,ca} \end{aligned} \tag{19}$$

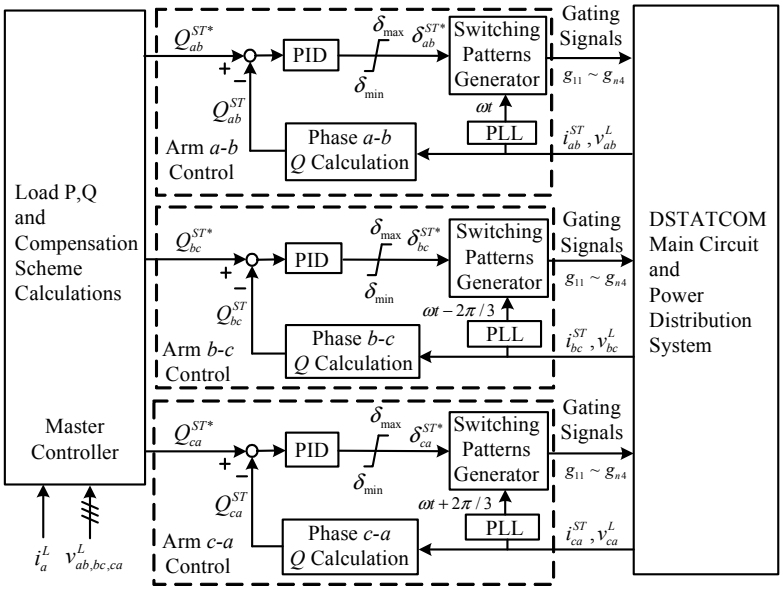

Figure 5. The proposed DSTATCOM controller.

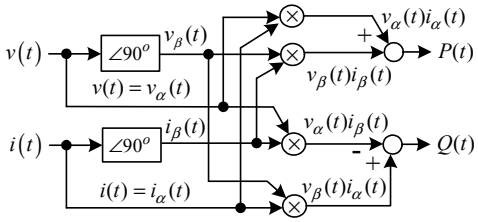

Figure 6. Fast power calculation method.

4. Simulation Verification

Figure 7 shows the simulation system, which was developed in the MATLAB/SimuLink program for a preliminary verification of the proposed DSTATCOM. A single-phase inductive load was used in the testing. First, the DSTATCOM main circuit was built according to Figure 3. In the simulation, the switch (SW) in Figure 7 was closed at t = 0.605 s to make a step response caused by the single-phase load. With the setting, the transient and steady-state performances of the DSTATCOM compensation were observed from the simulation results. Appendix A lists the system parameters.

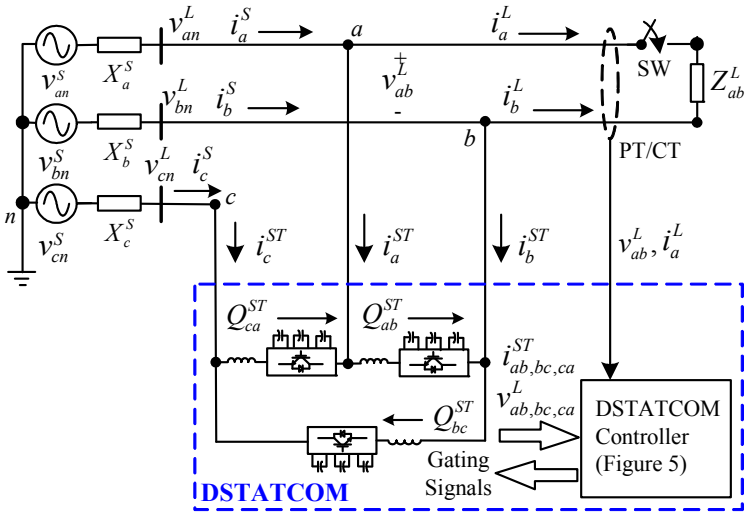

Figure 7. DSTATCOM simulation system setup.

Figures 8 and 9 are the simulation results. Figure 8a shows the transient load current response. With the assistance of the DSTATCOM, the three-phase source current was corrected to be balanced with a unity power factor, as shown in Figure 8b. Figure 8c depicts the synthesized line current of the DSTATCOM. Figure 8d,e show the power flows from the power source to the load, which reveal that the DSTATCOM very rapidly compensated the reactive power demand of the load. Figure 9 shows the compensation response in the DSTATCOM. Figure 9a is a recording of the internal voltage responses in the three DSTATCOM arms. When the single-phase load was switched in, the three DSTATCOM arms changed to phase-independent operation, as shown in Figure 9a,b. Figure 9c–e reveal other DSTATCOM responses in the single-phase load compensation for reference.

The simulation results in Figures 8 and 9 clearly indicate that the proposed DSTATCOM discussed in this paper is suitable for single-phase load compensation. It is also observed that the unbalanced operation of the three DSTATCOM arms produce high-order harmonic currents. The harmonic currents tend to flow into the system and aggravate the electric power quality. An adequate front-end filter can be installed to lessen the harmonic current pollution. Increasing the cascade numbers of the FHB cells in the DSTATCOM main circuit can markedly reduce the high-order harmonic currents.

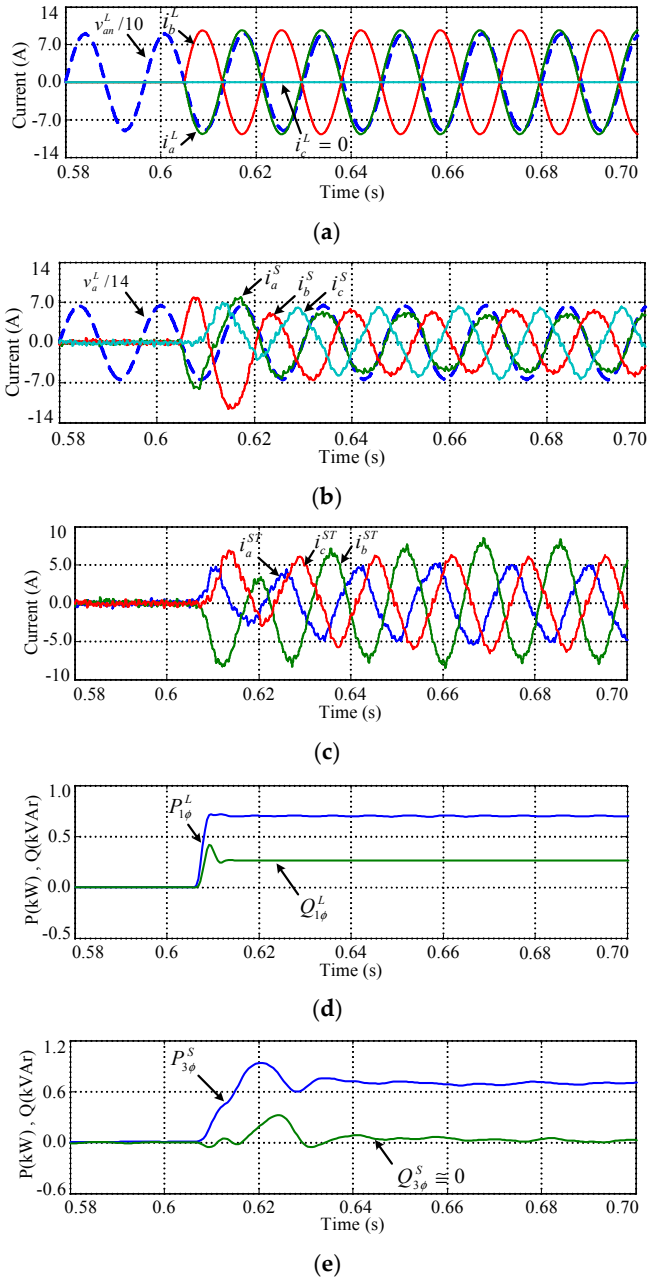

Figure 8. DSTATCOM compensation response. (**a**) Three-phase load current ($i_{a,b,c}^{L}$); (**b**) Three-phase source current ($i_{a,b,c}^{S}$); (**c**) Line current of DSTATCOM ($i_{a,b,c}^{ST}$); (**d**) Power ($P_{1\phi}^{L}$, $Q_{1\phi}^{L}$) to the single-phase load; (**e**) Power ($P_{3\phi}^{S}$, $Q_{3\phi}^{S}$) from the source.

Figure 10 shows the steady-state power flow with the DSTATCOM compensation. It can be observed that the DSTATCOM offers a path to rearrange the power flow for single-phase load compensation.

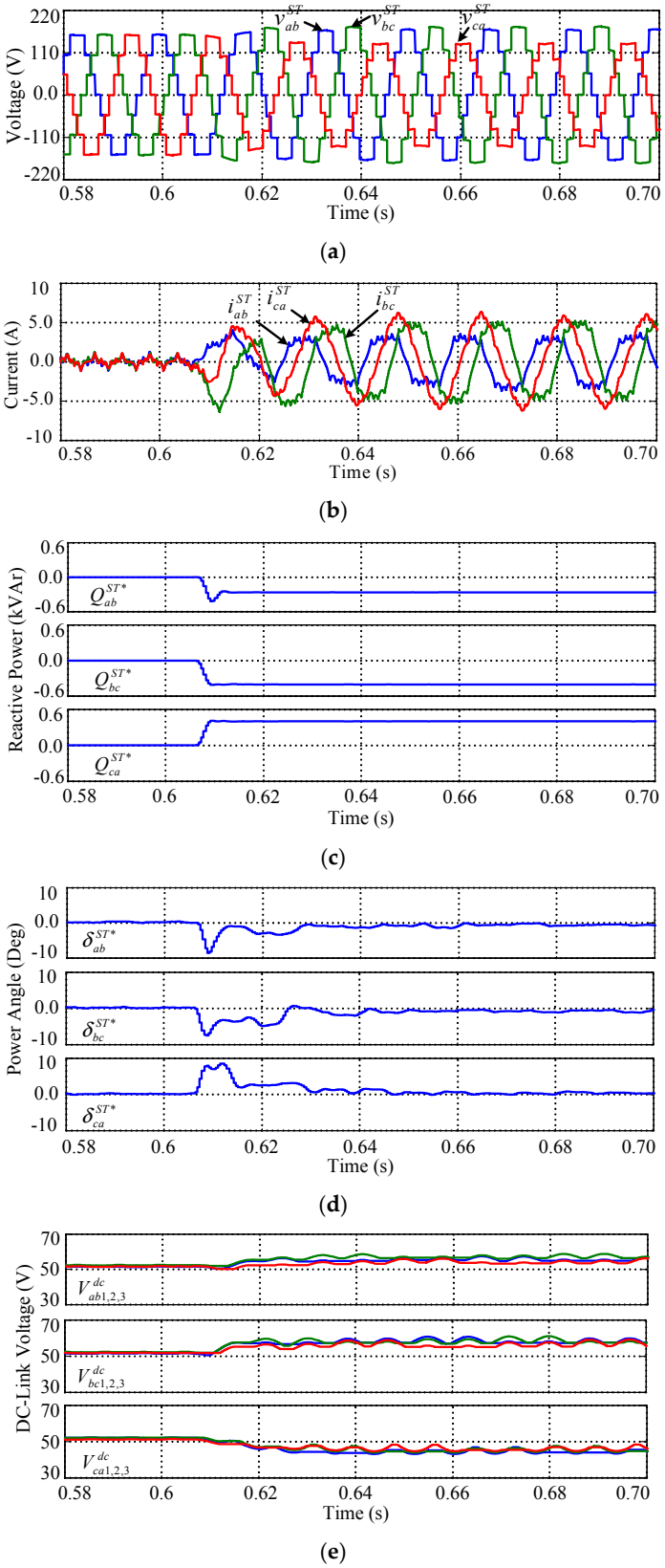

Figure 9. DSTATCOM compensation response. (**a**) Internal voltage ($v^{ST}_{ab,bc,ca}$); (**b**) Current ($i^{ST}_{ab,bc,ca}$); (**c**) Compensation command ($Q^{ST*}_{ab,bc,ca}$); (**d**) Power angle command ($\delta^{ST*}_{ab,bc,ca}$); (**e**) DC-link voltages of full-H-bridge (FHB) cells.

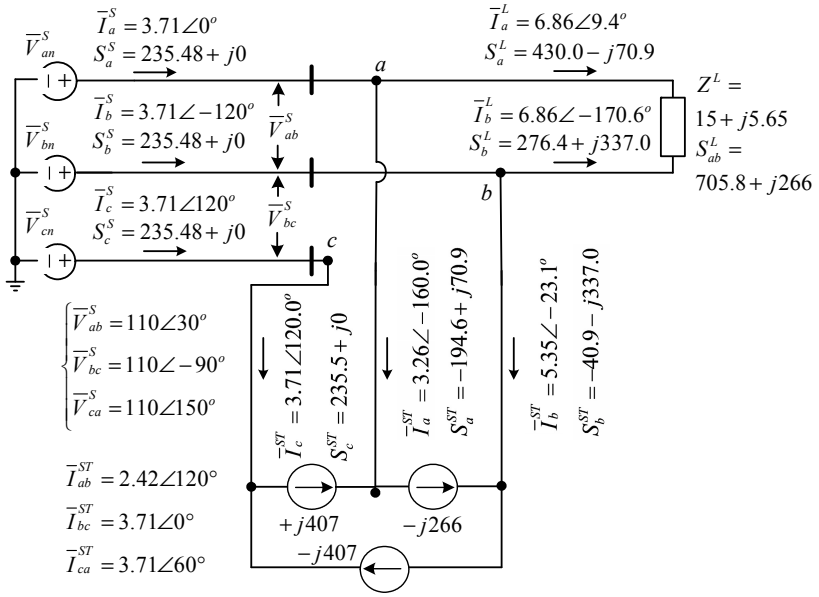

Figure 10. Steady-state power flow with DSTATCOM compensation.

5. Hardware Experimental Results

Figure 11 shows the hardware prototype test system constructed in the laboratory, and Appendix B lists the system parameters used. A single-phase load was used for verification testing in the physical experiment. The SDBC-MMCC-based DSTATCOM main circuit had a seven-level, transformerless configuration with a delta connection. In the hardware implementation of the DSTATCOM main circuit, insulated-gate bipolar transistors (IGBTs) were used. The DSTATCOM controller was a multi-TMS320F2812 DSP-based system with a sampling time of 0.52 ms to digitize the three PID controllers in Figure 5. The control program in the multi-DSP-based controller was first developed in C language on a host PC. The execution file was downloaded to the multi-DSP-based controller through Joint Test Action Group (JTAG) data links. Two multi-channel digital scopes were employed to record the transient responses of the DSTATCOM. During the DSTATCOM operation, some selected on-line calculation results in the controller were sent to the host PC for further evaluation.

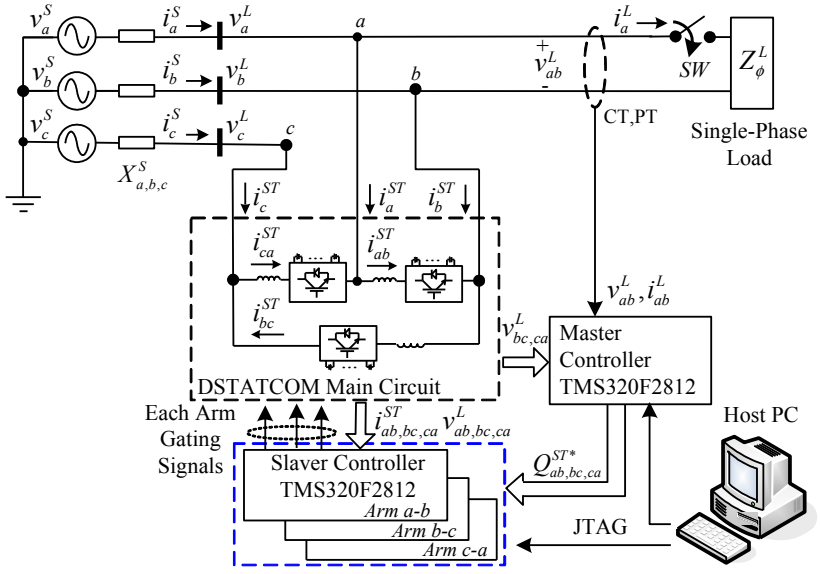

Figure 11. Functional block diagram of the DSTATCOM hardware prototype test system.

Figures 12 and 13 reveal the hardware experimental results. Figure 12 shows the current responses with DSTATCOM compensation. In Figure 12a, the switching-in of the single-phase load created an unbalanced operation. The single-phase load operation requires active power with a lagging power factor. Figure 12b illustrates the source current response; the phase-*a*-to-ground voltage waveform was recorded at the same time for reference. With the real-time compensation of the DSTATCOM, the source current was corrected very quickly to be balanced with a unity power factor. Figure 12c shows the transient response of the synthesized DSTATCOM line current in the compensation. Table 1 records the steady-state DSTATCOM compensation result in Figure 12. The current unbalanced ratio $I_{UR}(\%)$, expressed in Equation (20) indicates the effect of current balancing in the power source. The unbalanced ratio of the load current, $I^{L}_{UR}(\%)$, was 100%. With DSTATCOM compensation, the unbalanced ratio of the source current, $I^{S}_{UR}(\%)$, was substantially improved to a nearly perfect value of 3.26%.

$$I_{UR}(\%) = Max(\left|I_a - I_{avg}\right|, \left|I_b - I_{avg}\right|, \left|I_c - I_{avg}\right|)/I_{avg} \times 100\% \quad (20)$$

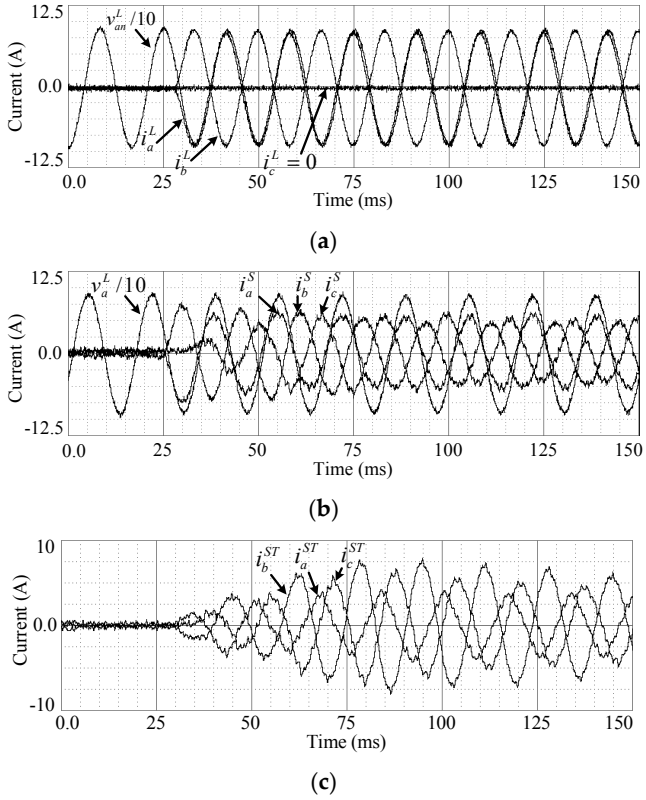

Figure 12. Transient responses with DSTATCOM compensation. (**a**) Single-phase load current ($i^{L}_{a,b,c}$); (**b**) Source current ($i^{S}_{a,b,c}$); (**c**) DSTATCOM line current ($i^{ST}_{a,b,c}$).

Table 1. DSTATCOM compensation result in the hardware test.

Load	I^{L}_{a}	I^{L}_{b}	I^{L}_{c}	$I^{L}_{UR}(\%)$
	6.46	6.43	0	100%
Source	I^{S}_{a}	I^{S}_{b}	I^{S}_{c}	$I^{S}_{UR}(\%)$
	4.1	3.85	4.0	3.26%

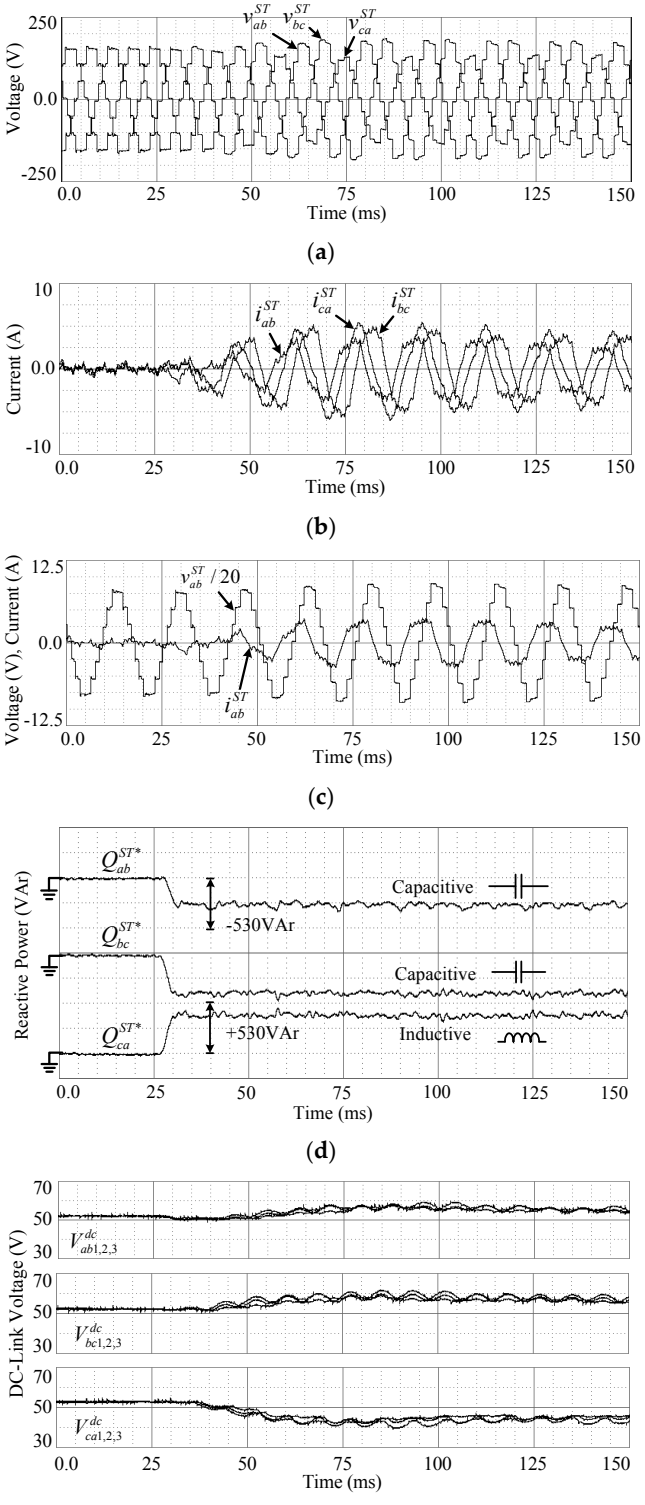

Figure 13. Transient responses of the DSTATCOM. (**a**) Internal voltage ($v^{ST}_{ab,bc,ca}$); (**b**) Arm current ($i^{ST}_{ab,bc,ca}$); (**c**) Arm *a-b* voltage and current (v^{ST}_{ab}, i^{ST}_{ab}); (**d**) Compensation command ($Q^{ST*}_{ab,bc,ca}$); (**e**) DC-link voltages ($V^{dc}_{ab1,2,3}$, $V^{dc}_{bc1,2,3}$, $V^{dc}_{ca1,2,3}$).

Figure 13 shows other responses in the DSTATCOM main circuit. The three DSTATCOM arms changed to phase-independent operation when the single-phase load was switched in. The physical test results agreed with the simulation results presented in Figure 9. The transient compensation

response of the DSTATCOM was quite fast. The delta-connected DSTATCOM main circuit and the harmonics-minimizing method eliminated the specified harmonic components in the synthesized DSTATCOM line currents, as shown in Figure 13b,c. However, high-order harmonic currents were unavoidably generated in the three DSTATCOM arms.

The hardware experimental results verified that the proposed SDBC-MMCC-based DSTATCOM is suitable for real-time phase balancing and power factor correction of single-phase loads in three-phase, three-wire power distribution systems.

6. Conclusion

In a three-phase, three-wire electric power distribution system, a newly designed SDBC-MMCC-based DSTATCOM employing staircase modulation and an indirect phasor-domain power angle regulation method for real-time single-phase load compensation was studied. An effective feedforward compensation algorithm was proposed for the DSTATCOM. The computer simulation results showed that the function of the proposed DSTATCOM was quite satisfactory. Finally, a hardware test system was built for functional verification. The proposed DSTATCOM showed a fast transient response and a satisfactory steady-state compensation effect. However, the simulation and experimental results also revealed that unbalanced operation of the DSTATCOM induced unbalanced harmonic currents in the three DSTATCOM arms. Thus, in practical applications, harmonic filters should be installed to enhance the electric power quality. Increasing the cascade numbers of the FHB cells in each DSTATCOM main circuit arm can also reduce undesired harmonic currents.

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Nomenclature

General:	
P	active power
Q	reactive power
v	instantaneous voltage
i	instantaneous current
δ	power angle
V	voltage phasor
I	current phasor
C	dc-link capacitor
X	reactance
Re	real part
Im	imaginary part
Superscripts:	
S	power source
L	load
ll	line to line
ST	DSTATCOM
$ST*$	DSTATCOM command
dc	dc link
$*$	complex conjugate
Subscripts:	
3ϕ	three-phase
1ϕ	single-phase
$0, 1, 2$	Zero, positive, negative sequences

Appendix A. Simulation System Parameters

System side:

$V_{ll}^{S} = 110V$, $f_S = 60Hz$, $X_{a,b,c}^{S} = 0.1\Omega$, $Z_{ab}^{L} = 15 + j5.655\Omega$

DSTATCOM side:

$C_{ab1,2,3} = C_{bc1,2,3} = C_{ca1,2,3} = 3,300\mu F$, $X_{ab,bc,ca}^{ST} = 3.77\Omega$, $\theta_1 = 11.68^{\circ}$, $\theta_2 = 31.18^{\circ}$, $\theta_3 = 58.58^{\circ}$, $K_P = 1.0$, $K_I = 0.65$, $K_D = 0.0007$

Appendix B. Experimental System Parameters

System side:

$V_{ll}^{S} = 110V$, $f_S = 60Hz$, $X_{a,b,c}^{S} = 0.1\Omega$, $Z_{ab}^{L} = 15 + j5.655\Omega$

DSTATCOM side:

$C_{ab1,2,3} = C_{bc1,2,3} = C_{ca1,2,3} = 3,300\mu F$, $X_{ab,bc,ca}^{ST} = 3.77\Omega$, $\theta_1 = 11.68^{\circ}$, $\theta_2 = 31.18^{\circ}$, $\theta_3 = 58.58^{\circ}$, $K_P = 0.8$, $K_I = 0.65$, $K_D = 0.0007$

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