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10 kV Silicon Carbide PiN Diodes—From Design to Packaged Component Characterization

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Abstract: This paper presents the design, fabrication and characterization results obtained on the last generation (third run) of SiC 10 kV PiN diodes from SuperGrid Institute. In forward bias, the 59 mm^2 diodes were tested up to 100 A. These devices withstand voltages up to 12 kV on wafer (before dicing, packaging) and show a low forward voltage drop at 80 A. The influence of the temperature from 25 °C to 125 °C has been assessed and shows that resistivity modulation occurs in the whole temperature range. Leakage current at 3 kV increases with temperature, while being three orders of magnitude lower than those of equivalent Si diodes. Double-pulse switching tests reveal the 10 kV SiC PiN diode's outstanding performance. Turn-on *dV/dt* and *di/dt* are −32 V/ns and 311 A/µs, respectively, whereas turn-off *dV/dt* and *di/dt* are 474 V/ns and −4.2 A/ns.

Keywords: SiC 10 kV PiN diode; device processing; electrical characterization; high-voltage device packaging; double-pulse test; smartgrid; MVDC; HVDC

1. Introduction

Marketing of SiC devices has expanded during the past decade; transistors and diodes are now available at lower cost. Although some high-voltage devices have been produced [1–7], the ones industrially available are mostly metal-oxide semiconductor field-effect transistors (MOSFET) and junction-barrier Schottky (JBS) diodes up to 1700 V [8]. Despite the fact that reliability studies have yet to be carried out, unipolar devices seem to be suitable for this voltage range and show state-of-the-art characteristics both at conduction and switching. For medium-voltage direct current (MVDC) and high-voltage direct current (HVDC) grid applications, it is interesting to work with bipolar devices [9] of higher breakdown voltages [10], such as 10 kV or more. At these voltages, most of the device's resistivity is due to their epitaxial layer, which is the thick and lightly-doped zone that withstands the electrical field. As a consequence, unipolar devices can be resistive. Plus, when operating at high temperature, the charge carrier mobility is reduced, which is even more detrimental to the on-state resistance of unipolar devices that make use of the field-effect conduction. For bipolar devices this effect is of lesser importance as they can benefit from resistivity modulation due to the possible high-level injection of carriers [11]. If the carrier lifetimes are high enough, the on-state resistance can be greatly reduced in high-injection operation mode. When the lifetime is extremely low, dynamic characteristics are similar to those of unipolar devices. The field-assisted current conduction mechanism is reinforced by the diffusion mechanism, which is less sensitive to temperature and produces a lower increase of the on-state resistance with temperature in bipolar devices. For all these reasons, SuperGrid Institute decided to design and fabricate SiC 10 kV PiN diodes. This paper reports on the design, fabrication, packaging and characterization of the SiC 10 kV–50 A PiN diodes.

2. High-Voltage PiN Diode Design

Finite-element simulations using Sentaurus^{TM} TCAD commercial software (vO-2018.06-SP2, Synopsys, Mountain View, CA, USA) [12] have been performed to determine the drift region parameters for capability to withstand 10 kV. A trade-off between breakdown voltage and on-state forward voltage has to be chosen. A 4 in commercial epitaxial wafer from Cree has been chosen, which consists of a stack of P^{++} ($5{\cdot}10^{19}$ cm^{-3}, 0.5 µm)/P^{+} ($2{\cdot}10^{17}$ cm^{-3}, 1 µm)/N^{-} ($7{\cdot}10^{14}$ cm^{-3}, 110 µm) epilayers grown from top to bottom on a heavily-doped N^{+}-type buffer layer and substrate. The theoretical breakdown voltage of an infinite plane-parallel junction of this wafer would be 13.2 kV, according to ionization coefficients given in [13].

The TCAD tool used in this paper is "sdevice" from Synopsys^{TM} (Mountain View, CA, USA) [12]. This finite-element software (vO-2018.06-SP2, Synopsys, Mountain View, CA, USA) solves Poisson's equation coupled with both continuity equations for electrons and holes. The discretization of the structure is performed through a triangular mesh. Semi-automatic directives allow for controlling the length of the mesh. P–N junctions and interfaces have small length while the non-critical zone have longer length of the mesh. The main parameters concerning 4H–SiC material used for the simulation were already described [14,15], and for the ionization coefficients [13].

In order to sustain the high voltage, the junction termination has to be designed to spread the electric field that naturally occurs at the edge of the termination. A plethora of papers present in the literature report on techniques that fulfill this task with a relatively high efficiency (>80%) [16–35]. Another study on high-voltage bipolar diodes from SuperGrid has shown that an efficient peripheral protection is achieved by a mesa structure with a combination of junction termination extension (JTE) with JTE rings. In order to implement such a solution, the first step is to determine the JTE length. The efficiency of the peripheral protection has been evaluated through two dimensional (2D) TCAD simulations. As shown in Figure 1a, the edge termination efficiency has a strong dependence on the JTE dose. The efficiency is defined as the ratio between the breakdown voltage and the theoretical blocking voltage (13.2 kV). Increasing the JTE length above 400 µm does not improve further the breakdown voltage. For the sake of spatial optimization of the device (lowest material consumption), the optimal JTE length has been fixed to 400 µm and the computed JTE dose has been kept at 8.5 10^{12} cm^{-2}. A smaller JTE length would result in a very small radius of curvature and produces a field crouding at the edges of the rectangular devices. Two-dimensional simulations do not take into account the radius of curvature and give a wrong impression on the JTE efficiency [28,36].

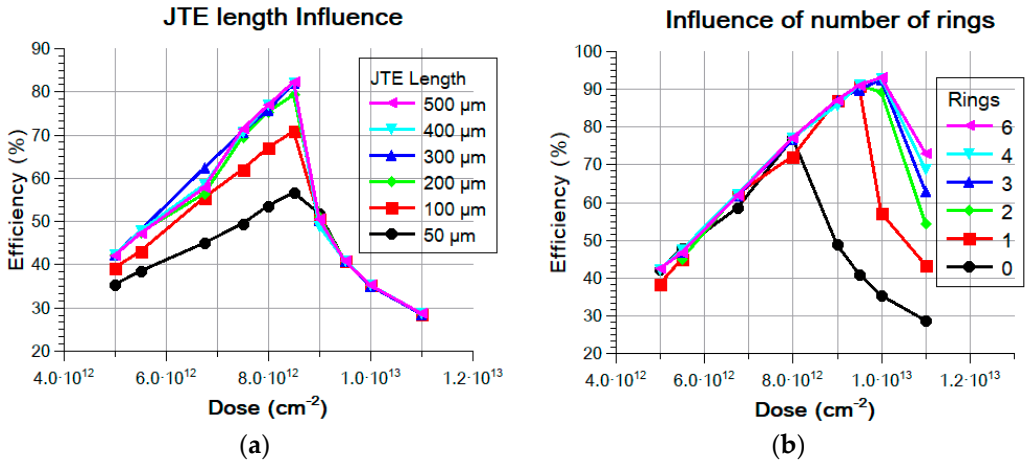


Figure 1. Simulated results showing the efficiency of the JTE dose for different JTE length (**a**) and the efficiency of the JTE dose for a different number of rings with a 400 µm JTE length (**b**). The mesa depth is 2.5 µm for both cases.

The next step is to compute the number of useful JTE rings. As shown in Figure 1b, the simulation of a JTE length of 400 µm with an increasing number of rings increases the efficiency of the peripheral protection. As a consequence, the JTE dose can be pushed further while the peripheral efficiency keeps increasing above 80%. Since the higher number of rings increases the dose tolerance, six rings were chosen with optimized width and increasing distance between them. Three-dimensional simulations could have been carried out to show the necessity of 400 µm JTE and six rings, but would require a long computing time [28].

3. Device Processing

Seven-level set masks have been designed to fabricate 10 kV–50 A silicon carbide bipolar diodes. Two sizes of diodes were fabricated. The active area was 59 mm^2 for the bigger diodes and 9 mm^2 for the smaller ones. The large diodes were optimized for the nominal current (50 A). This study focused on the large-size devices only.

A cross-section of the device is shown in Figure 2. As described in the previous section, the edge termination of the PiN diodes is made of a mesa and 400 µm long junction termination extension (JTE) assisted by six JTE-rings with varying spacing between them (D_i). The diode is square shaped with rounded edges. Each side has a length of 7.7 mm (0.6 cm^2) and the radius of curvature of the corners fixed to 600 µm. The processed wafer, the breakdown voltage mapping and the packaging of the device are shown in Figures 3–5, respectively.

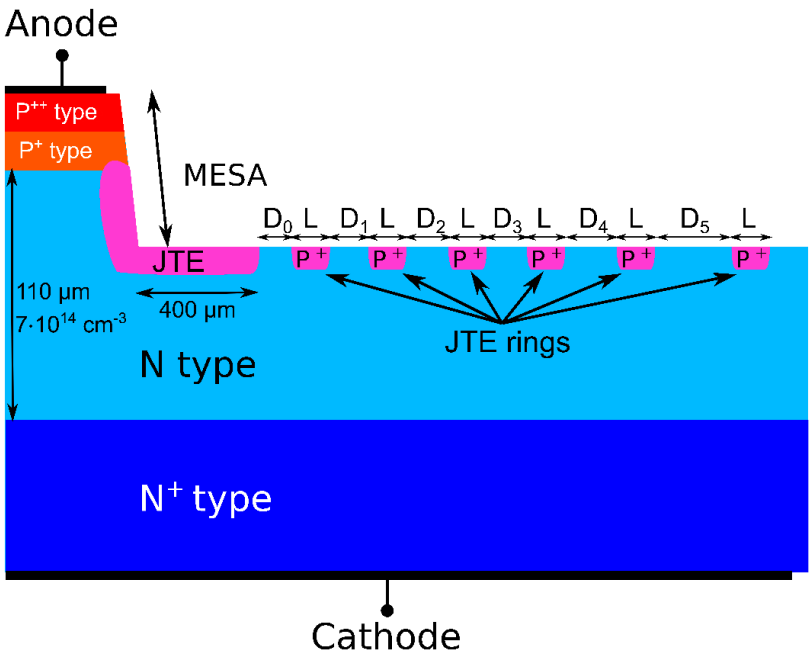


Figure 2. Schematic cross-section of the fabricated PiN diode with its high-voltage peripheral protection. D_i is the spacing between rings and L is the length of the ring.

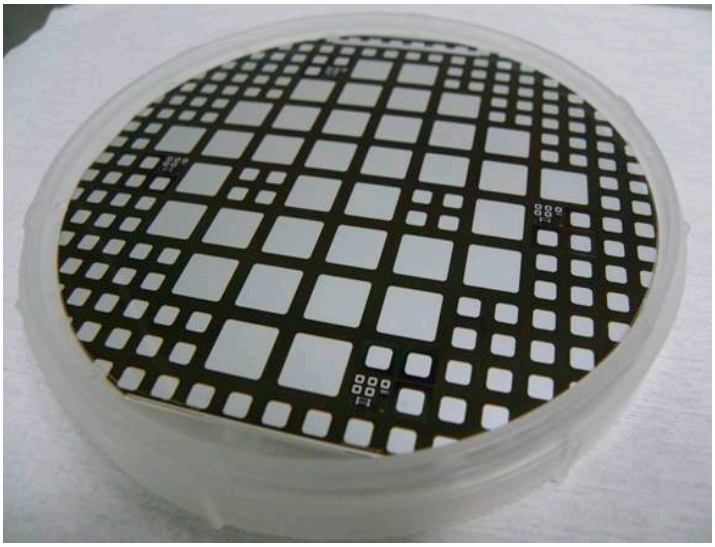


Figure 3. Example of realized PiN diodes on a 4″ SiC wafer with 50 A–10 kV bipolar diodes.

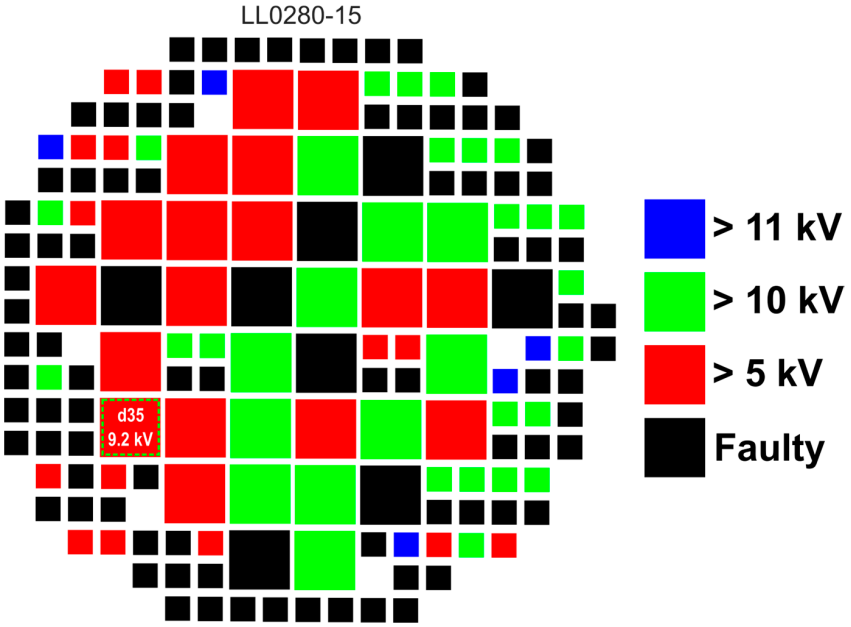
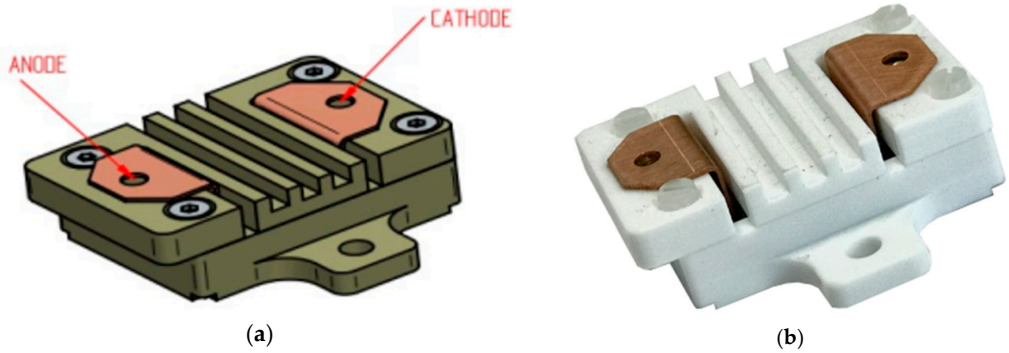


Figure 4. Breakdown voltage mapping of the wafer LL0280-15. Some devices withstand more than 11 kV and more than 60% (>5 kV) of the wafer surface yields exploitable devices. Device d35 is shown in dashed square.



(**a**) (**b**)

Figure 5. 3D rendering (**a**) and the packaged device (**b**) after processing and wafer dicing.

4. Static and Dynamic Characterizations

Some devices have been packaged for high current and switching characterizations. Figure 6 shows the reverse-bias-static characterization results of large diodes. Static electrical characterizations were performed at SuperGrid Institute with a Keysight B1505A power device (B1505A, Keysight, Santa Rosa, CA, USA) analyzer equipped with a 10 kV module for high-voltage measurements and a Keysight B1506 (B1506, Keysight, Santa Rosa, CA, USA) (another power device analyzer) for repetitive measurements on components. Twelve large diode dies were packaged and measured as shown in Table 1. The packaged diodes were fixed on a hot plate and the specified temperature is the case temperature. To avoid any self-heating or temperature variation, pulsed-mode characterization was performed with 50 µs pulse duration. As can be seen in Table 1, forward voltage at 50 A (V_F (50 A)) and 80 A (V_F (80 A)), reverse leakage current at 1 kV (I_R (1 kV)) and 3 kV (I_R (3 kV)), the junction capacitance at 0 V (C_J (0 V)), 60 V (C_J (60 V)) and 3 kV (C_J (3 kV)) are in a tight distribution. This reveals the maturity of the fabrication process of the 10 kV SiC PiN diodes.

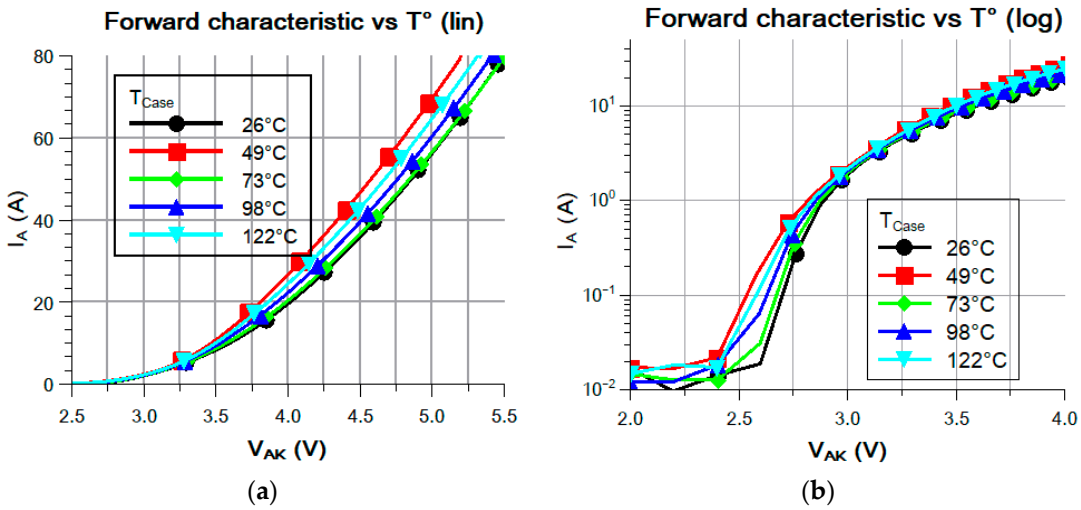


Figure 6. Forward characteristics of a packaged diode (d35) for different ambient temperatures: (**a**) linear scale and (**b**) semi-logarithmic scale.

Table 1. Statistics on twelve characterized devices.

Device Feature	V_F (50 A)	V_F (80 A)	I_R (1 kV)	I_R (3 kV)	C_J (0 V)	C_J (60 V)	C_J (3 kV)
unit	V	V	nA	nA	pF	pF	pF
average	4.98	5.68	15.2	193.2	2557	594	82.2
min	4.59	5.19	1.99	4.57	2480	567	79.1
max	5.36	6.22	32.7	359	2640	622	85.1
σ	0.20	0.29	9.79	137.12	50.30	17.07	2.44

4.1. Forward Characteristics

Figure 6 shows the forward static characteristic for different temperatures. Standard behavior for a bipolar diode is observed with a voltage drop reduction (Figure 6a). The logarithmic scale clearly shows the reduction of the building potential at low current values (Figure 6b). At 10 A, a typical V_F = 3.5 V and on-state resistance lower than 25 mΩ is obtained through a metallization process enhancement. The measured resistance is lower than the unipolar limit, proving that the device performs in high-injection operation mode and benefits from resistivity modulation.

Particularly, Figure 7 shows the decrease of the drop voltage at 80 A with increasing temperature. This is a well-known characteristic of bipolar devices. For low temperature, probably the serial resistance that increases with the temperature compensates the phenomenon.

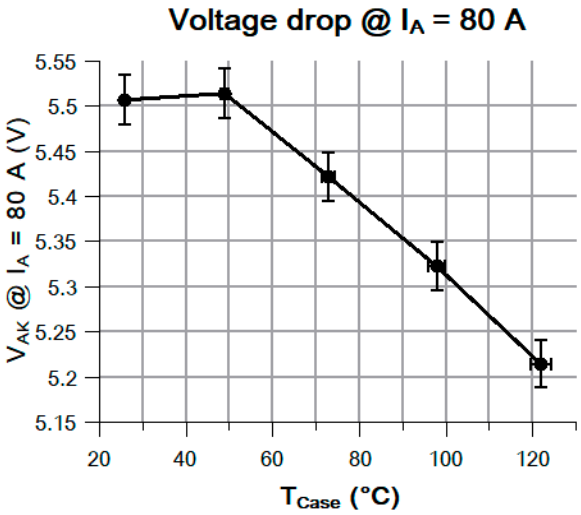


Figure 7. Voltage drop at 80 A versus the temperature (Device d35).

4.2. Reverse Blocking Characteristics

As shown in Figure 5, the breakdown voltage of the wafer LL0280-15 is very good with 38 diodes (big and small included) withstanding more than 10 kV and more than 60% of the wafer surface withstanding 5 kV. All the breakdown voltage curves are shown in Figure 8. The reason behind the breakdown voltage failure is related to the material quality, which is guaranteed at <5 defects/cm^{-2}.

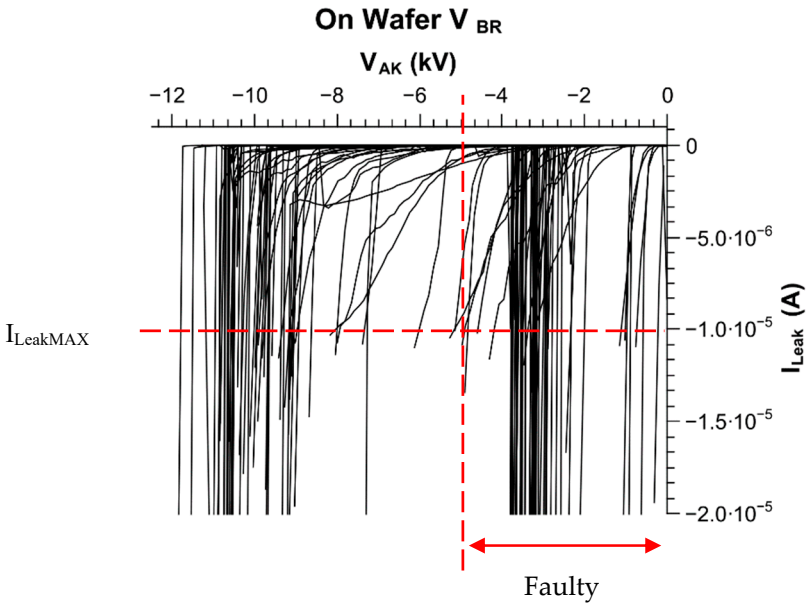


Figure 8. Leakage current vs. the applied voltage for all the devices on wafer LL0280-15. The dashed line defines the breakdown voltage.

Concerning the reverse characteristic, Figure 9 shows the classical increase of the leakage current with the applied reverse voltage and the temperature.

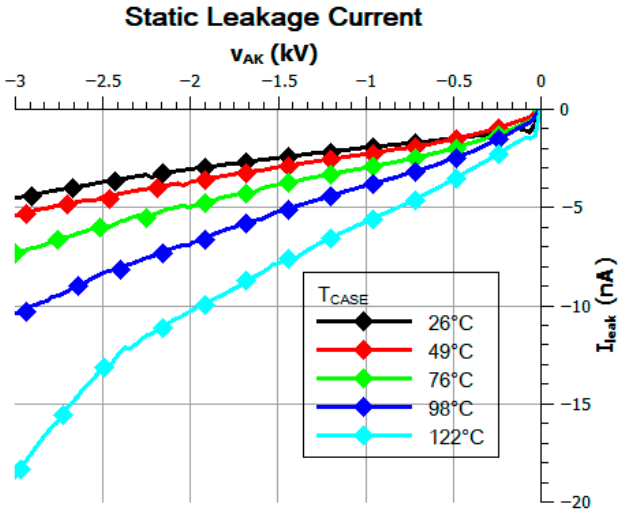


Figure 9. Leakage current vs. the applied voltage for different temperatures (Device d35).

Particularly, Figure 10 shows the increase of the leakage current vs. the temperature at 3 kV. It shows a very small leakage current density, about one thousand times lower than equivalent silicon diodes or even SiC JBS diodes [37].

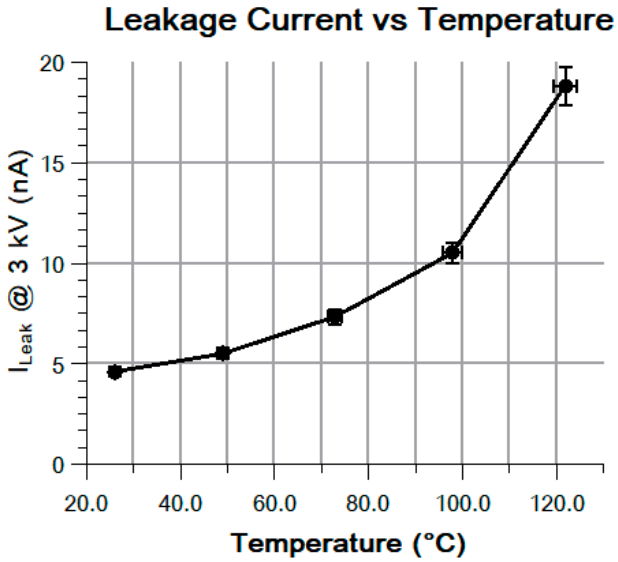


Figure 10. Leakage current vs. the temperature at 3 kV (Device d35).

4.3. Junction Capacitance

Figure 11a shows the junction capacitance with a very standard behavior for a bipolar junction. Moreover, Figure 11b shows the same curve in a log-log scale with an approximately constant slope of 0.52. The theoretical slope is 0.5 because the capacitance of a plane junction decreases with the square root of reverse voltage [38] (p. 87).

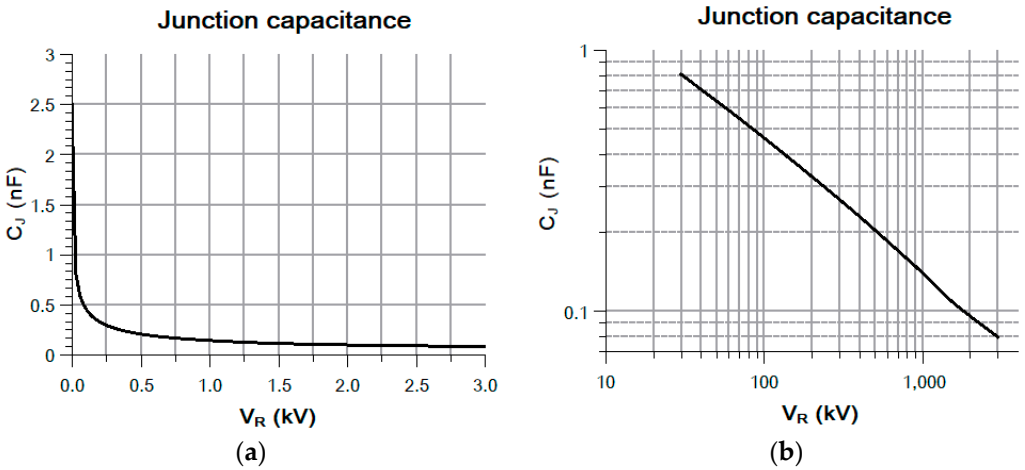


Figure 11. Junction capacitance vs. the reverse applied voltage at 26 °C (Device d35). Linear scale and log-log scale are shown on (**a**) and on (**b**) respectively.

5. Switching Characteristics

The switching performance of the manufactured devices was tested by means of clamped load inductive switching, commonly referred to as a double pulse test. The test circuit schematics are illustrated in Figure 12. All the parasitic elements were omitted even though they greatly degrade the operation of the device under test (DUT). The high-side MOSFET switch is made of a series association of six C2M0045170P 1.7 kV SiC MOSFETs. The unipolar nature of the switch renders it fast enough not to affect the switching performance of the freewheeling diode. No further details will be given on the switch as this paper focuses on the behavior of the 10 kV PiN diode only.

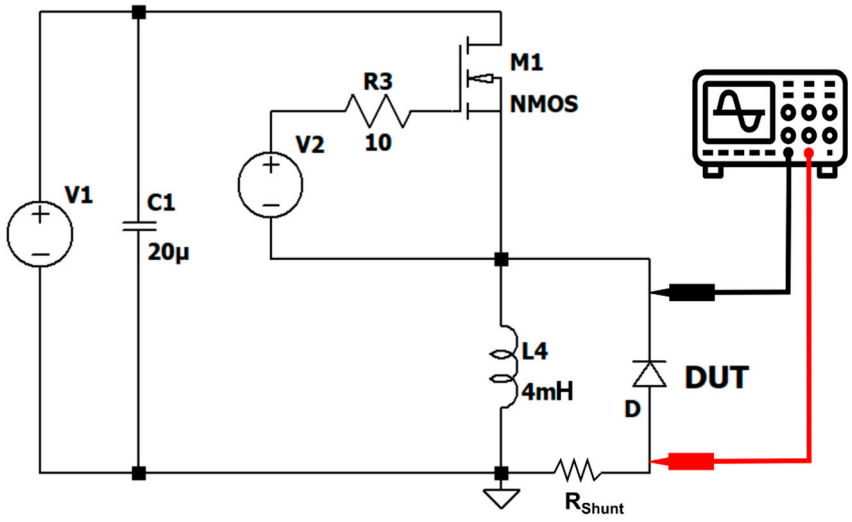


Figure 12. Clamped load inductive switching circuit schematic without the parasitic elements.

Measurements were carried out at room temperature on a DPO 5054B oscilloscope from Tektronix. A 25 mΩ current viewer resistor from T&M Research was placed in series with the PiN diode in order to accurately measure the current flowing through it. The signal was fed into the scope using a 50 Ω coaxial cable. The V_{KA} voltage was measured with a high-voltage P6015A probe.

The recorded waveforms of the turn-on and turn-off behavior are shown in Figures 13 and 14, respectively. The outstanding performance of the SiC PiN diode is plagued by the parasitic elements of the test circuit. Nevertheless, hard turn-on waveforms for a bus voltage of 2750 V and a current of 18.5

A show a very fast switching with low losses. The SiC PiN diode turns on in less than 100 ns for a di/dt = 311 A/µs and a dV/dt = −32 V/ns. The resulting turn-on energy is very low (E_{ON} = 0.53 mJ).

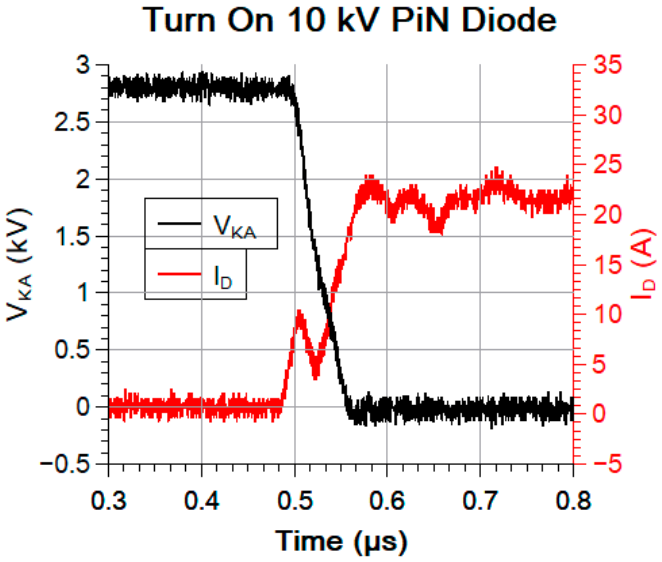


Figure 13. Room temperature turn-on of the PiN diode happens faster than 100 ns with very low energy loss. Turn-on energy is only 0.53 mJ for a bus voltage of 2750 V at 18.5 A (Device d35).

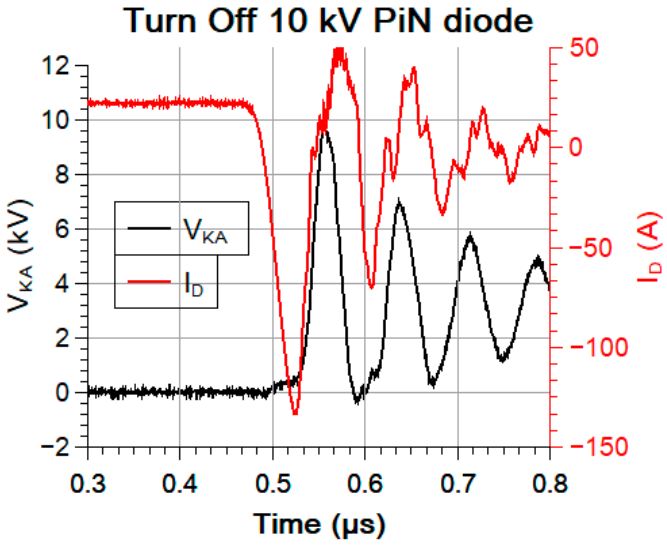


Figure 14. Room temperature turn-off of the PiN diode happens faster than 200 ns with low energy loss. Turn-on energy is only 6.1 mJ for a bus voltage of 2750 V at 21 A (Device d35).

It is true that for turn-on operation there is room left for the bus voltage to be increased, but that would be too much risk to take since the most demanding conditions are met at a turn-off. As a matter of fact, due to parasitic inductances, an important overvoltage appears at a turn-off. As can be seen in Figure 14, the actual overvoltage is very important and almost undamped oscillations are observed. This is certainly due to the non-optimized layout of the test circuit because of the targeted 10 kV applied voltage. During these oscillations, the current in the diode becomes positive several times, which indicates a great contribution of the capacitive current. This situation can be very dangerous for the switch, as the high dV/dt and di/dt may induce EMC issues in the gate driver or/and high overvoltage on the switch side and lead to catastrophic failure. Nevertheless, the 10 kV SiC PiN diode handles the high dV/dt = 474 V/ns and high di/dt = −4.2 A/ns without apparent impact. Turn-off time can be

estimated to less than 300 ns in these conditions. The turn-off energy is evaluated to E_{OFF} = 6.1 mJ whereas the reverse recovery charge is calculated to be Q_{RR} = 4.1 µC. The current devices outrun the previous generation devices, both in terms of static and switching characteristics [39].

6. Conclusions

To the knowledge of the authors, this is the first time that high voltage and high current switching of a 10 kV 50 A SiC PiN device is reported. The switching performance of the device is proven to be outstanding, both from the static- and the dynamic/switching point of view. The design has been optimized and the fabrication has been matured. Static performance shows that the device makes use of the resistivity modulation from room temperature to 125 °C. Switching during the high-injection mode operation is carried out so fast that the parasitic elements of the test circuit become a limiting factor.

In the future, improvements to test circuit layout may allow for higher bus voltage and higher current operation of the device. Stress tests have to be carried out both in and out of the safe operating area (SOA) to assess the robustness and the reliability of the 10 kV PiN SiC diodes. Bipolar degradation tests have to be carried out.

Author Contributions: Conceptualization, D.P., H.M. and B.A.; TCAD simulation, L.V.P.; static and dynamic characterization, H.M.; switching tests, B.A.; coordination, D.P.

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