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Comparative Design of Gate Drivers with Short-Circuit Protection Scheme for SiC MOSFET and Si IGBT

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Abstract: Short-circuit faults are the most critical failure mechanism in power converters. Among the various short-circuit protection schemes, desaturation protection is the most mature and widely used solution. Due to the lack of gate driver integrated circuit (IC) with desaturation protection for the silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET), the conventional insulated gate bipolar transistor (IGBT) driver IC is normally used as these two devices have similar gate structure and driving mechanism. In this work, a gate driver with desaturation protection is designed for the 1.2-kV/30-A SiC MOSFET and silicon (Si) IGBT with the off-the-shelf driver IC. To further limit voltage-overshoot at the rapid turn-off transient, the active clamping circuit is introduced. Based on the experiments of switching characterization and short-circuit test, the SiC MOSFET shows faster switching speed, more serious electromagnetic interference (EMI) issue, lower switching loss (half), and higher short-circuit current (1.6 times) than the Si IGBT, even with a slower gate driver. Thus, a rapid response speed is required for the desaturation protection circuit of SiC MOSFET. Due to the long delay time of the existing desaturation protection scheme, it is technically difficult to design a sub-μs protection circuit. In this work, an external current source is proposed to charge the blanking capacitor. A short-circuit time of 0.91 μs is achieved with a reliable protection. Additionally, the peak current is reduced by 22%.

Keywords: desaturation; gate driver; protection circuit design; pulse current; short-circuit; Si IGBT; SiC MOSFET

1. Introduction

The increasing demand in high power density requires power converters to be operated at high frequency and high efficiency, thus reducing the size of filters and heat sinks, respectively. Currently, the silicon (Si) insulated gate bipolar transistor (IGBT) is most widely used in medium- and high-power applications such as motor drives in vehicle and traction due to the advantages of being easy-to-drive and having low conduction loss [1,2]. However, the turn-off tail current leads to a high switching loss [3]. Thus, the switching frequency of Si IGBT is normally limited below 20 kHz for hard switching power converters [4].

The emerging silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) is an attractive replacement of Si IGBT for high power density applications [5–8]. Due to the similar MOS gate structure, it is normally regarded that the gate driver design of SiC MOSFET can directly inherit from that of Si IGBT with various off-the-shelf gate driver integrated circuits (ICs). However, the high switching speed with increasing dv/dt and di/dt ratios makes the gate driver design for SiC MOSFET a new challenge. It may lead to parasitic effects including phase-leg crosstalk and electromagnetic interference (EMI) issues due to the ringings, which are where the early works mainly focused on. To summarize, the gate driver design for SiC MOSFET should follow such rules [9–12]:

- Negative power supply to avoid crosstalk in half-brige configuration;
- A low impedance path for faster turn-off and suppression of crosstalk;
- A small gate loop inductance to reduce the gate-source voltage ringing, especially the common source inductance (the trace shared by gate driver and power loops) should be minimized to reduce the interference between the two loops;
- A small power loop inductance to reduce the ringings of drain-source voltage and drain current with the low-ESL (equivalent stray inductance) decoupling capacitance placed as close as possible.

Nevertheless, the short-circuit protection for SiC MOSFET has not been fully resolved yet, which is one of the factors hindering its wide usage. Short-circuit faults are the most critical failure mechanism in power converters, which may result from the controller fault, device breakdown, or load short-circuit. Due to the excessive power dissipation during the short-circuit transient, the device junction temperature may easily exceed the limit and lead to a permanent failure of thermal runaway or explosion.

Due to the popularity of Si IGBT in the modern power converters, its short-circuit protection has been extensively investigated. The device manufacturers normally specify a short-circuit withstand capability, which is the amount of time from the start of short-circuit fault until the device is completely damaged. For Si IGBT, the typical short-circuit withstand capability is around several μs, which is long enough for the action of protection circuit. Compared with Si IGBT, the short-circuit protection circuit design for SiC MOSFET is more challenging. Firstly, from the thermal aspect, the short circuit withstand capability of SiC MOSFET is smaller due to the smaller chip size and higher current density [13]. Besides, SiC MOSFET shows a higher surge current due to the short channel effect [14]. Last but never least, the less mature SiC device processing technology results in a gate oxide reliability issue. As a consequence, a faster speed is required for the short-circuit protection of SiC MOSFET.

Generally, the fault conditions can be classified into two types: hard switching fault (HSF) and fault under load (FUL). HSF and FUL are defined by the short-circuit conditions while the switch is turned on or in on-state, respectively [15]. The conventional short-circuit protection schemes include detection of current [15], V_{CE} or V_{DS} (desaturation) [13,16–18], di/dt [13,19,20], gate voltage [21–23], and gate charge [24–26]. Among these methodologies, the desaturation technique is the most mature and widely used solution, with lots of off-the-shelf IGBT gate driver ICs. However, a driver IC especially designed for short-circuit protection of SiC MOSFET is still lacking. Thus, the early works on the desaturation protection mainly used discrete devices and logic gates. Although a short-circuit time less than 1 μs was reported in [17], the circuit structure is too complex to be implemented and not preferred by the circuit designers. Thus, the device vendors still provide the protection solution based on the IGBT gate driver IC with desaturation detection. For example, Wolfspeed has released two- and six-channel gate drivers [27,28] for the 1.2-kV SiC power modules using the Infineon gate driver IC [29]. To ensure a fast desaturation detection and avoid false triggering, a good layout is mandatory [30]. However, the short-circuit protection time is normally not given by these application notes.

Another issue under the short-circuit fault is the high di/dt at the rapid turn-off transient, which may lead to a large voltage overshoot considering the effect of stray inductance. Conventionally, snubbers such as RC or RCD can be used to suppress the over-voltage issue. However, a bulky snubber circuit tends to increase the system cost, size, and losses [31]. Thus, the 2-level turn-off and soft shutdown methods were proposed to lower the di/dt and implemented in the off-the-shelf gate driver

ICs and boards [32–34]. However, it slows down the turn-off speed even when the device operated at normal conditions. Considering the tail current of IGBT, the additional loss is not important and can be ignored in practice [2], but it may lead to a significant increase in the turn-off loss of SiC MOSFET.

Although the existing works have demonstrated the advanced protection circuits with sub-μs short-circuit time, the potential or physical limits of desaturation protection has not been fully investigated, especially for the emerging SiC MOSFET. This work aims to design a gate driver with protection circuit for SiC MOSFET based on the traditional Si IGBT gate driver IC. The comparison and design considerations are also recommended for the design engineers to fully utilize the performances of SiC MOSFET.

The rest of the paper is organized as follows. In Section 2, the design details of gate driver and protection circuits are demonstrated. In Section 3, the devices used in this work are compared. In Section 4, two experiments including double pulse test (DPT) and HSF are set up. Section 5 presents the experimental results and conducts the discussion. Finally, Section 6 summarizes the main conclusion of this work.

2. Circuit Design and Analysis

2.1. Gate Driver

A half-bridge gate driver with a short-circuit protection circuit is developed, as Figure 1a shows. The logic circuits consist of low pass filter (LPF) and level shifter. The isolated single gate driver IC is the 1ED020I12-B2 from Infineon, which provides a galvanic isolation up to 1.2 kV based on coreless transformer technology [29]. Since this driver IC can only provide a rail-to-rail output current of 2 A, a totem-pole driver with the co-packaged NPN and PNP transistors is used to improve the driving capability. A pair of Zener diodes is used to suppress the voltage spike across the gate oxide. The power supply of driver IC is provided by the isolated DC/DC converter module with 5.2-kV isolation voltage. Thus, the gate driver allows a 1.2-kV galvanic isolation. Considering the different recommended gate voltages for these two devices, the asymmetric output voltages of $15/-9$ V and $20/-5$ V are used for Si IGBT and SiC MOSFET, respectively. The gate driver is implemented in a four-layer PCB with the area of 50 mm $\times$ 46 mm, as Figure 1b shows. In addition, a clearance between the primary and secondary sides of gate driver is required to ensure small coupling capacitance and safe electrical isolation during the layout design. The maximum operating frequency of a gate driver can be estimated by the equation:

$$P_{GD} = Q_G(V_{CC} - V_{EE})f_{sw} \tag{1}$$

where Q_G is the gate charge, V_{CC} and V_{EE} are the positive and negative power supply voltages of gate driver respectively, and f_{sw} is the switching frequency.

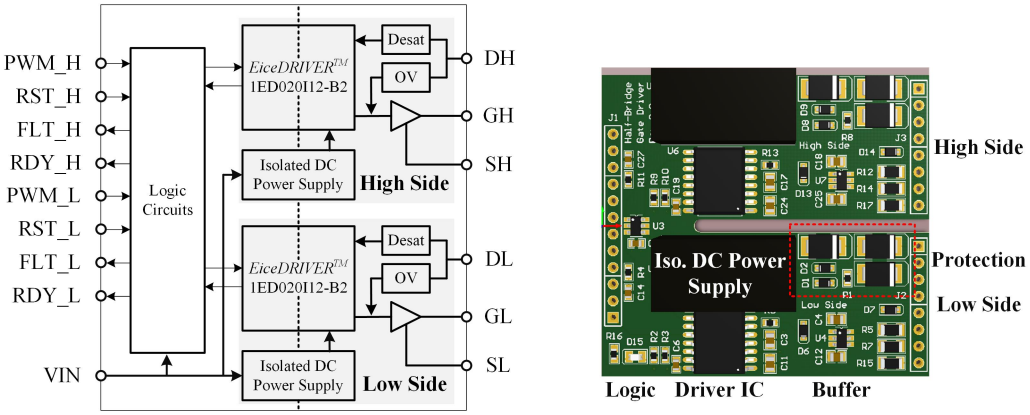


Figure 1. Half-bridge gate driver: (**a**) block diagram and (**b**) prototype.

2.2. Desaturation Protection Circuit

The detailed circuit diagram of desaturation protection circuit is further shown in Figure 2. The operation principles at both normal and short-circuit conditions are discussed with the switching waveforms shown in Figure 3.

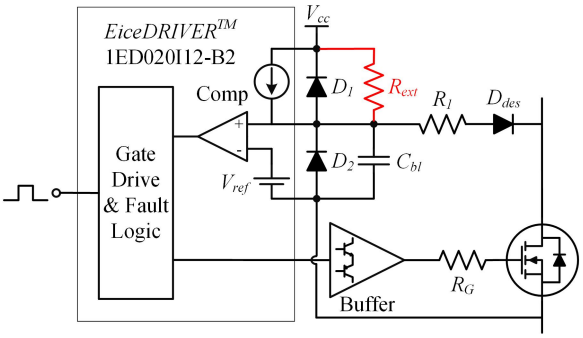


Figure 2. Circuit diagram of desaturation protection.

The classical switching waveforms of the switch (e.g., MOSFET) at the normal condition with inductive load have been extensively discussed in the text book [1]. Hence, the turn-on transient between the time intervals $t_0 \sim t_4$ is not presented in this work. As the desaturation protection is based on detecting V_{DS}, there is a risk of fault triggering of the protection circuit before t_3. Thus, a delay circuit is introduced with a current source to charge the blanking capacitor C_{bl}. The blanking time needs to be larger enough than the turn-on time. After t_4 when the switch is completely on, the desaturation diode D_{des} is forward biased, then the voltage on the desaturation pin (V_{des}) is pulled down and below the reference value V_{ref}, as given by

$$V_{des} = V_F + V_{DS,on} \tag{2}$$

where V_F is the forward voltage drop of D_{des} and $V_{DS,on}$ is the on-state drain-source voltage drop of MOSFET. Thus, the normal operation is unaffected.

During the HSF condition, as the MOSFET is directly subjected to the DC-bus voltage, the Miller plateau disappears and V_{GS} directly rises to the positive supply voltage from $t_0' \sim t_2'$ [22]. Meanwhile, the current starts to rise after V_{GS} exceeds V_{th} at t_1', and finally saturate at a peak value I_{sc} due to the short-channel effect. D_{des} is reversely biased and the current source starts to charge C_{bl} at t_3'. As the internal current source of gate driver IC is fixed, an external source of V_{cc}/R_{ext} is proposed in this work. Thus, the blanking time is given by

$$t_{bl} = t_d + t_c \tag{3}$$

$$t_c = \frac{C_{bl} V_{ref}}{I_{cs} + \frac{V_{cc}}{R_{ext}}} \tag{4}$$

where t_d is the delay time of desaturation circuit, and t_c is the charging time of C_{bl}. The MOSFET will be switched off once the voltage on C_{bl} exceeds V_{ref} at t'_4. The short-circuit time t_{sc} is defined as below

$$t_{sc} = t_{bl} + t_{off} \tag{5}$$

where t_{off} is the turn-off time of short-circuit current. The diodes D_1 and D_2 are used to clamp the voltage on C_{bl} to prevent damaging driver IC. The resistor R_1 is used to limit the current.

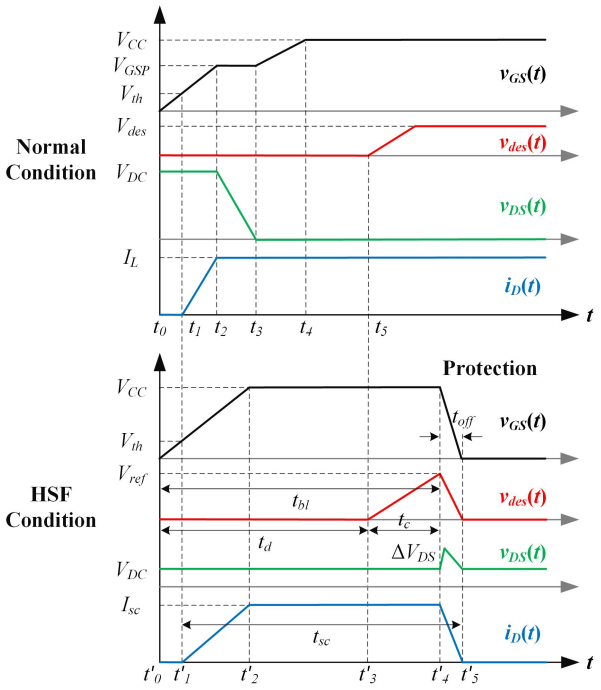


Figure 3. Switching waveforms at normal and hard switching fault (HSF) conditions of metal-oxide-semiconductor field-effect transistor (MOSFET).

2.3. Over-Voltage Protection Circuit

The circuit diagram of over-voltage protection circuit is shown in Figure 4. The active clamping connected between the gate-drain terminals of MOSFET can effectively suppress the over-voltage by a feedback loop with the transient voltage suppression (TVS) diode. Two TVS diodes are connected in series configuration for a clamped voltage of 500 V. The Schottky diodes D_1 and D_2 are to block the current flowing from gate to drain. When there is a voltage spike exceeding the clamped voltage between $t'_4 \sim t'_5$, the impedance of TVS will decease sharply within several ps and thus V_{DS} is clamped rapidly. The current flows into the gate capacitance of MOSFET via D_2, and into the lower switch of buffer via D_1. Hence, V_{GS} increases and the turn-off speed is slowed down, then the voltage spike is suppressed.

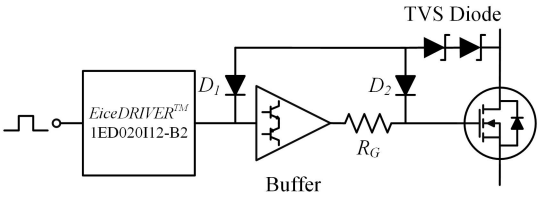


Figure 4. Circuit diagram of over-voltage protection.

3. Device Comparison

The two commercial power transistors used in this work are Infineon Si IGBT IHW15N120E1 (1.2 kV/30 A) and Wolfspeed SiC MOSFET C2M0080120D (1.2 kV/30 A). As Figure 5a shows, the Si IGBT adopts a trench gate structure to increase the channel density. As Figure 5b shows, the SiC MOSFET uses traditional planar gate. The body diode of SiC MOSFET shows excellent switching performance compared with the SiC Schottky diode [35]. For SiC IGBT, due to the lack of body diode, an n+ contact is introduced in the collector and a PiN diode (in red circle) is formed between emitter and collector.

The key electrical parameters are summarized in the Table 1. It can be found that although these two transistors have similar continuous current of 30 A at the room temperature, the pulse current of SiC MOSFET is around 2 times that of Si IGBT. This is because the SiC MOSFET tends to have a more serious short-channel effect, thus the drain current continues to increase with the increase of drain bias even in the saturation region [36]. Furthermore, the output capacitance of SiC MOSFET is significantly larger than that of Si IGBT due to the high doping concentration in the n-drift region. It results in a more serious *LC* oscillation during the switching transition. The gate charge of SiC MOSFET is around half of Si IGBT, thus leading to a smaller power loss in the gate driver. From Equation (1), the gate driver loss for both devices can be estimated. Considering the maximum power of DC/DC converter is 2 W, the maximum frequencies of the gate drivers for Si IGBT and SiC MOSFET can reach 500 kHz and 1 MHz, respectively, which are far beyond the recommended frequency and ensure enough design margin.

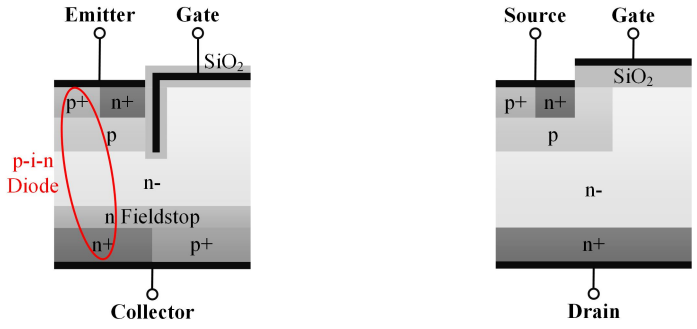


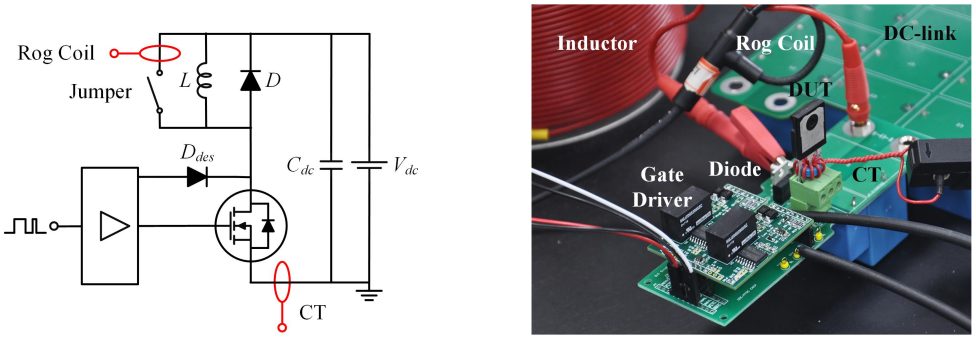
Figure 5. Device cross-sections: (**a**) silicon (Si) insulated gate bipolar transistor (IGBT) and (**b**) silicon carbide (SiC) MOSFET.

Table 1. Comparison of key electrical characteristics.

Parameter	Unit	Si IGBT	SiC MOSFET	Test Conditions
V_{BR}	V	1200	1200	-
I_{dc}	A	30	31.6	-
I_{pulse}	A	45	80	-
V_{th}	V	5.8	2.2	Si IGBT: I_C = 0.5 mA, V_{CE} = V_{GE}. SiC MOSFET: I_D = 1 mA, V_{DS} = 10 V.
C_{ies} (C_{iss}) C_{oes} (C_{oss}) C_{res} (C_{rss})	pF	810 24 20	990 340 22	$V_{CE}(V_{DS})$ = 25 V
Q_G	nC	90	49.2	Si IGBT: V_{CE} = 960 V, I_C = 15 A. SiC MOSFET: V_{DS} = 800 V, I_D = 20 A.

4. Experimental Setup

In this section, to test and optimize the gate driver, a test bench is setup for both DPT and HSF experiments, the latter of which can be built by a short connect of the inductive load of the typical DPT circuit, as Figure 6 shows.



(**a**) (**b**)

Figure 6. (**a**) Test circuit diagram and (**b**) experimental setup.

4.1. Double Pulse Test Experiment

A DPT experiment is firstly conducted to evaluate the impact of a gate driver on the switching performance. The gate driver is controlled by a double pulse signal, which is generated by the Texas Instruments digital signal processor (DSP) TMS320F28335. An inductive load and a clamped diode are inserted into the power loop. The inductor load uses single-layer winding and an air core to reduce the stray capacitance. It has a total inductance of 318 μH. To facilitate the replacement of device under test (DUT), it is installed on the PCB by a socket instead of direct soldering. The diode uses the 1.2-kV/20-A Wolfspeed SiC Schottky diode C4D20120A. It provides the freewheeling path for the reactive energy during the current commutation period. The DC-link consists of multiple 800-V film capacitors in parallel connections to ensure a stable DC-bus voltage. A laminated layout of DC-link is adopted to reduce the stray inductance. Additionally, the area of power loop must be minimized with a carefully designed layout. To ensure an accurate and high-bandwidth measurement of current, a custom-made current transformer (CT) with 10:1 turns ratio is used, and then connected with Tektronix current probe TCP0030 (30 A, 120 MHz) [37]. The Tektronix oscilloscope DPO7354C (3.5 GHz, 40 GS/s) is used to monitor the voltage and current waveforms.

4.2. Hard Switching Fault Experiment

A HSF test bench is setup to evaluate the protection circuit. The single pulse control signal of the gate driver is also generated from the DSP. The testing procedure is demonstrated as follows: firstly, the DC-link is charged to a stable voltage by a high-voltage power supply, then the gate driver is triggered on and the waveforms are captured by the oscilloscope. Compared with the DPT experiment, the short-circuit current through the DUT is measured by the PEM Rogowski coil CWTMini HF6B (30 MHz, 1.2 kA) as it has the highest current capability among the various current probes. In addition, the long short-circuit jumper is also used to verify the voltage-overshoot issue at turn-off due to the large stray inductance.

5. Results and Discussion

5.1. Impact of Gate Resistance

As a rule of thumb, the gate resistance is a tradeoff between switching loss and EMI. Thus, it is optimized by comparing the switching characteristics of Si IGBT and SiC MOSFET at four different values of 2 Ω, 4.7 Ω, 10 Ω, and 20 Ω, as Figures 7 and 8 show, respectively. Both devices are tested with a DC-bus voltage of 400 V and a load current of 30 A. It can be found that SiC MOSFET shows a faster switching speed, and Si IGBT shows a remarkable tail current at turn-off. Additionally, the voltage and current ringings of SiC MOSFET are more serious than those of Si IGBT.

The voltage spectrum of Si IGBT and SiC MOSFET are obtained by applying Fast Fourier Transform (FFT) to the V_{CE} and V_{DS} waveforms respectively, as Figure 9a–d shows. The SiC MOSFET shows an apparent resonant point at the frequency of 64.5 MHz, and the magnitude at this point decreases with the increase of gate resistance. The total stray inductance of power loop can be calculated by

$$f_r = \frac{1}{2\pi\sqrt{L_s C_{oss}}} \tag{6}$$

The C_{oss} of SiC MOSFET C2M0080120D at 400 V bias is 90 pF from the datasheet. Thus, the stray inductance is 68 nH. As the Si IGBT IHW15N120E1 uses the same package and testing circuit, the stray inductance can be also regarded as the same. It can be concluded that keeping the stray inductance of power loop as small as possible is crucial for the SiC MOSFET.

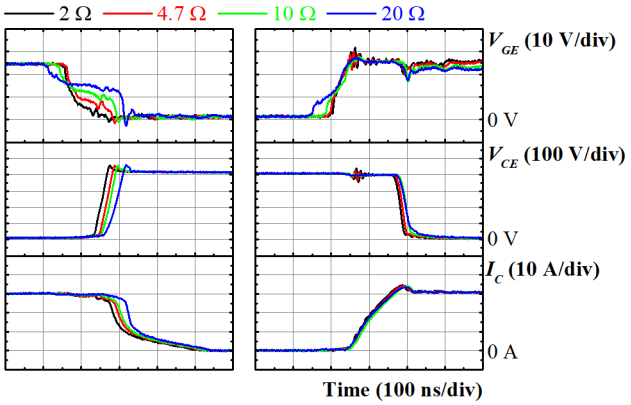


Figure 7. Switching waveforms Si IGBT at 400 V/30 A with different gate resistances.

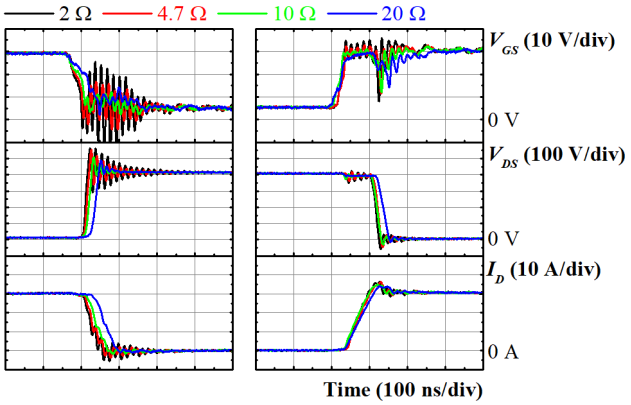


Figure 8. Switching waveforms SiC MOSFET at 400 V/30 A with different gate resistances.

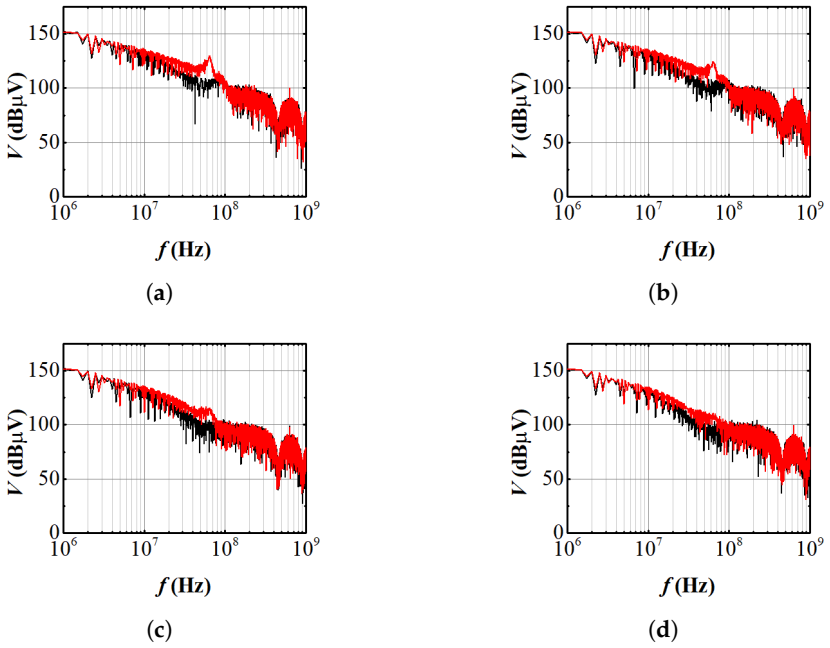


Figure 9. Comparison of voltage spectrum between Si IGBT (black lines) and SiC MOSFET (red lines) at different gate resistances: (**a**) 2 Ω, (**b**) 4.7 Ω, (**c**) 10 Ω, and (**d**) 20 Ω.

The switching energy with the variation of gate resistance is shown in Figure 10. It can be found that the switching energy of SiC MOSFET even at $R_G = 20\ \Omega$ is still much smaller than that of Si IGBT at $R_G = 2\ \Omega$. Thus, it is practical to use a large gate resistance for SiC MOSFET to reduce the EMI, and meanwhile the switching loss can still maintain smaller than Si IGBT. In this work, the optimal gate resistances are selected to be 4.7 Ω and 10 Ω for Si IGBT and SiC MOSFET, respectively. Figure 11 further shows the comparison of gate voltage waveforms at the optimal gate resistance. Although a slower gate driver with the higher time constant of *RC* is used for SiC MOSFET, the switching loss can still be reduced by half with the side-effect of increased EMI.

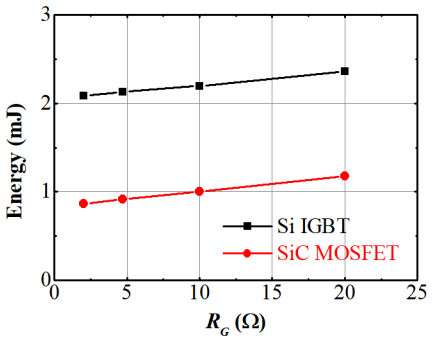


Figure 10. Comparison of switching energy between Si IGBT and SiC MOSFET at different gate resistances.

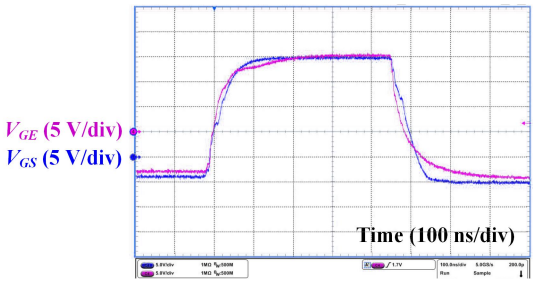


Figure 11. Comparison of gate voltage waveforms between Si IGBT and SiC MOSFET at the optimal gate resistance.

5.2. Short-Circuit Test

Based on the previous discussion, the surge current capabilities of Si IGBT and SiC MOSFET are directly evaluated at the optimal gate resistance, as Figure 12 shows. Both devices are subjected to HSF with a fixed DC-bus voltage of 400 V. Two duration times (2 µs and 5 µs) of gate signal are set. It can be found that the peak current of SiC MOSFET is 1.6 times of Si IGBT. The short-circuit current of SiC MOSFET shows a more significant decreasing tendency after the peak value, and finally becomes smaller than that of Si IGBT. Although the di/dt of Si IGBT at normal turn-off is smaller than that of SiC MOSFET, it is opposite at the short-circuit fault, and therefore its voltage-overshoot is slightly higher.

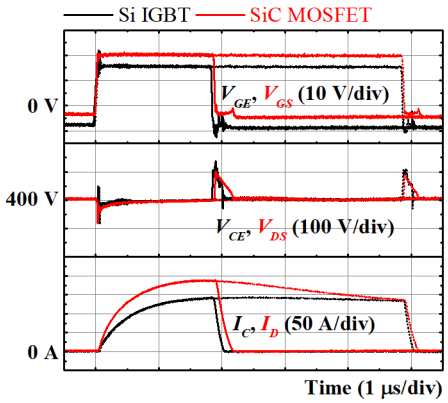


Figure 12. Comparison between Si IGBT and SiC MOSFET under short-circuit test with 2 µs (solid lines) and 5 µs pulses (dashed lines).

5.3. Protection Circuit Test

Due to the fast switching speed and high surge current of SiC MOSFET, a rapid response speed is required for the desaturation protection circuit. Based on Equation (4), smaller blanking capacitance or larger current source can be used to reduce the blanking time. Firstly, three different values of

C_{bl} (10 pF, 47 pF, and 100 pF) are investigated, and R_1 is 1 kΩ. Similar to the previous discussion, the DC-bus voltage is 400 V. A 5-µs triggering pulse is used to ensure the action of protection circuit. Figure 13a,b shows the test waveforms of HSF condition with desaturation protection for Si IGBT and SiC MOSFET, respectively. The duration times of short-circuit fault are summarized by the Table 2. It can be found that t_{sc} decreases with smaller C_{bl}. Although using the same protection circuit, Si IGBT shows a slightly smaller t_{sc} than SiC MOSFET. The voltage-overshoot is successfully limited below 500 V with the active clamping circuit.

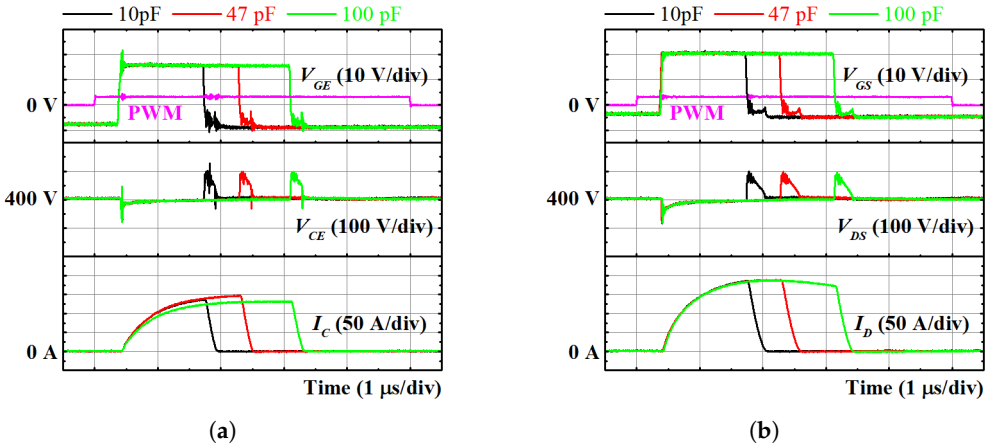


Figure 13. Desaturation protection test waveforms at different values of C_{bl}: (**a**) Si IGBT and (**b**) SiC MOSFET.

Table 2. Short-circuit times at different values of blanking capacitor.

C_{bl}	t_{sc} Si IGBT	t_{sc} SiC MOSFET
10 pF	1.5 µs	1.6 µs
47 pF	2 µs	2.1 µs
100 pF	2.9 µs	3 µs

Figure 14 shows the voltage drop across the desaturation pin for SiC MOSFET when C_{bl} = 47 pF to investigate the blanking time. It can be found that V_{des} increases gradually with a constant slope of 3.15 V/µs after a delay time t_d = 400 ns from the beginning of the short-circuit. The gate driver is switched off once V_{des} exceeds the reference voltage 9 V with a turn-off time of 260 ns. The effective charging current of C_{bl} is calculated to be $C_{bl}dv/dt$ = 150 µA. The fractions of t_{sc} can be shown by the histogram in Figure 15, and it can be found that t_c dominates the total t_{sc} in this situation. Although t_{sc} can be significantly reduced with smaller C_{bl}, a capacitance smaller than 10 pF is not recommended. The anti-parallel low-voltage Schottky diode D_2 used in this work is BAT165AX (40 V, 0.75 A), which has a junction capacitance around 5∼10 pF when reverse-biased. Thus, if C_{bl} is as small as 1 pF, the junction capacitance of D_2 may become the dominant factor for the blanking time. Considering it is a voltage-dependent capacitor, it will make the blanking time difficult to control. Even for the situation without anti-parallel diode, a capacitance that is too small will become very sensitive to the noise. As both t_d and t_{off} are fixed for a given gate driver, it is technically difficult to design a sub-µs protection circuit with the existing dasaturation protection scheme.

In this work, an external current source is introduced to reduce t_{sc} for SiC MOSFET. Figure 16 shows the test waveforms at three different values of R_{ext} (10 kΩ, 47 kΩ, and 100 kΩ) and two different values of C_{bl} (10 and 47 pF). The test results of short-circuit times are summarized in Table 3. It can be found that t_{sc} decreases with smaller R_{ext}. It is effective to use this external current source to increase the desaturation protection speed of off-the-shelf gate driver IC, although a too small R_{ext} will increase

the power loss of gate driver. A smallest short-circuit time of 0.91 µs is achieved with R_{ext} = 10 kΩ and C_{bl} = 10 pF. Compared with the situation without R_{ext}, it shows a reduction by 43%. In addition, the peak current is reduced by 22%. Thus, this modified protection circuit promises a fast sub-µs short-circuit protection response.

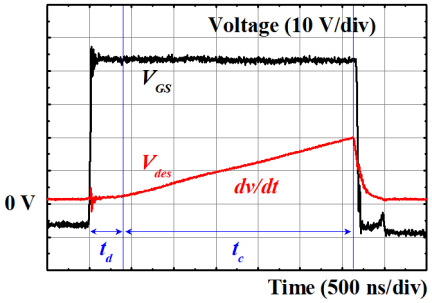


Figure 14. Voltage drop across desaturation pin.

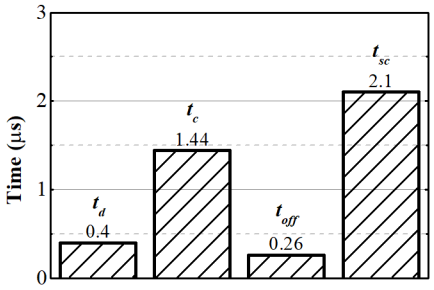
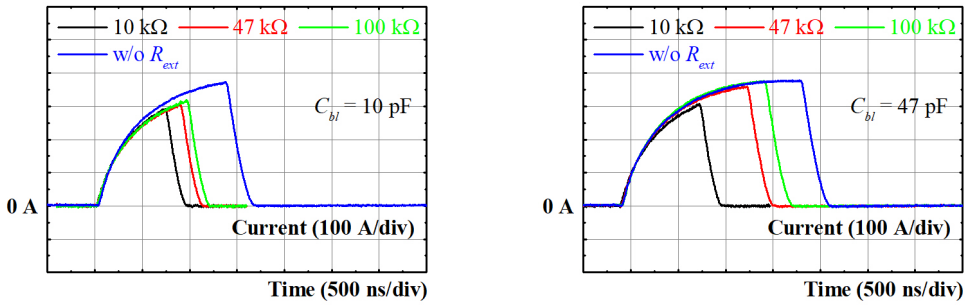


Figure 15. Histogram of short-circuit time fractions.



(**a**) (**b**)

Figure 16. Current waveforms of SiC MOSFET at different values of R_{ext}: (**a**) C_{bl} = 10 pF and (**b**) $C_{bl}F$ = 47 pF.

Table 3. Short-circuit times of SiC MOSFET at different values of blanking capacitor and external resistor.

R_{ext}	t_{sc}	
	C_{bl} = 10 pF	C_{bl} = 47 pF
w/o R_{ext}	1.6 µs	2.1 µs
10 kΩ	0.91 µs	1.02 µs
47 kΩ	1.07 µs	1.55 µs
100 kΩ	1.14 µs	1.74 µs

6. Conclusions

Although the existing works have proposed several advanced protection circuits with sub-μs short-circuit time, the complicated circuit topology makes it difficult to be implemented by the design engineers. The potential of traditional desaturation protection has not been fully investigated for the emerging SiC MOSFET. In this work, a gate driver with desaturation protection circuit based on the off-the-shelf driver IC is presented. It provides a fast driving capability and a reliable protection for both Si IGBT and SiC MOSFET. Additionally, it is easy to be implemented with an external resistance to increase the shut-down speed for a short-circuit fault.

Based on the experimental results, it is found that the SiC MOSFET shows faster switching speed, more serious EMI issue, and lower switching loss (half), even with a slower gate driver. At the HSF condition, the peak current and di/dt of SiC MOSFET are 1.6 times of Si IGBT, whereas its voltage overshoot at turn-off is slightly smaller. Generally, the fast switching speed and high surge current of SiC MOSFET require a desaturation protection circuit with rapid response speed. However, due to the limit of long delay time of existing desaturation scheme, a sub-μs protection circuit is technically difficult using the traditional circuit. Thus, with the external current source proposed in this work, the short-circuit time can be reduced to be 0.91 μs. The peak current also shows a reduction by 22%.

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