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A Modified DSC-Based Grid Synchronization Method for a High Renewable Penetrated Power System Under Distorted Voltage Conditions

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Received: 30 September 2019; Accepted: 18 October 2019; Published: 23 October 2019



Abstract: With the increasing penetration of renewable energy, a weak grid with declining inertia and distorted voltage conditions becomes a significant problem for wind and solar energy integration. Grid frequency is prone to deviate from its nominal value. Grid voltages become more easily polluted by unbalanced and harmonic components. Grid synchronization technique, as a significant method used in wind and solar energy grid-connected converters, can easily become ineffective. As probably the most widespread grid synchronization technique, phase-locked loop (PLL) is required to detect the grid frequency and phase rapidly and precisely even under such undesired conditions. While the amount of filtering techniques can remove disturbances, they also deteriorate the dynamic performance of PLL, which may not meet the standard requirements of grid codes. The objective of this paper is to propose an effective PLL to tackle this challenge. The proposed PLL is based on quasi-type-1 PLL (QT1-PLL), which provides a good filtering capability by using a moving average filter (MAF). To accelerate the transient behavior when disturbance occurs, a modified delay signal cancellation (DSC) operator is proposed and incorporated into the filtering stage of QT1-PLL. By using modified DSCs and MAFs in a cascaded way, the settling time of the proposed method is reduced to around one cycle of grid fundamental frequency without degrading any disturbance rejection capability. To verify the performance, several test cases, which usually happen in high renewable penetrated power systems, are carried out to demonstrate the effectiveness of the proposed PLL.

Keywords: phase-locked loop (PLL); synchronization; hybrid filter

1. Introduction

In modern power systems, more and more renewable energies such as solar and wind energy are integrated with the power grid through grid-connected power converters. To use this energy in more efficient ways, several advanced techniques, such as high voltage direct current transmission (HVDC) [1], flexible AC transmission systems (FACTS) [2] and energy storage systems (ESSs) [3], are developed. Some power electronic converter-based applications on the customer side, such as constant power load (CPL) and micro-grids with ESSs, are also widely used for some purposes, like peak load shaving. All the above yields a more complicated power system with a large amount of power converters. A typical power system integrating high penetrated renewable energy sources is depicted in Figure 1. The irregular phenomenon and uncertainty of wind and solar energy may cause undesired grid conditions [4]. Sub- and super-synchronous oscillations may emerge in wind farms if the controller is not well-designed [5]. In recent years, these issues happened several times in Oklahoma, USA [6]

and Hebei and Xinjiang, China [7,8], and caused many wind turbines to be tripped off. This highly impacted the operation of power distribution and renewable energy utilization. The grid frequency is prone to deviate from its nominal value since the inertia of the grid decreases. Grid voltages contain an amount of undesired components, such as fundamental frequency negative sequences (FFNSs) and harmonic components, which results in unbalanced and distorted grid conditions. It is an essential requirement for a renewable energy power converter to maintain stable operation with high performance under such conditions. To achieve this goal, a proper grid synchronization method is needed for all grid-connected applications. It is a big challenge for a grid synchronization method to extract grid frequency and phase information under such adverse conditions.

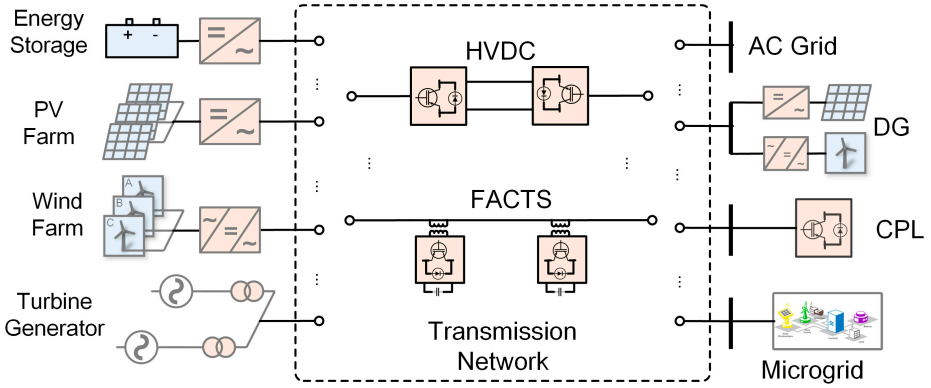


Figure 1. Block schematic of a typical power system with high penetration of renewable energy.

Among various grid synchronization techniques, phase-locked loop (PLL) is the most widely used method in grid phase and frequency detection area for its robust performance and simple implementation [9–12]. Figure 2 shows the most common employment of PLLs in practical applications. After extracting grid voltage information at the common coupling point (PCC), PLL sends estimated grid phases to the controller of the grid power converter (GPC). For a three phase power system, synchronous reference frame PLL (SRF-PLL) is an effective and typical method under ideal conditions [13,14]. However, with more utilization of renewable energy sources, a power system turns "weak" [15–18]. The grid voltages usually contain fundamental frequency negative sequence components (FFNSs) and other harmonic components. Furthermore, grid frequency does not always stay at its nominal value. To maintain the phase tracking accuracy under distorted grid voltages conditions, various filtering technique were used to remove disturbances at the cost of slowing down the transient response, which may violate the requirement on settling time in common grid codes [19–23].

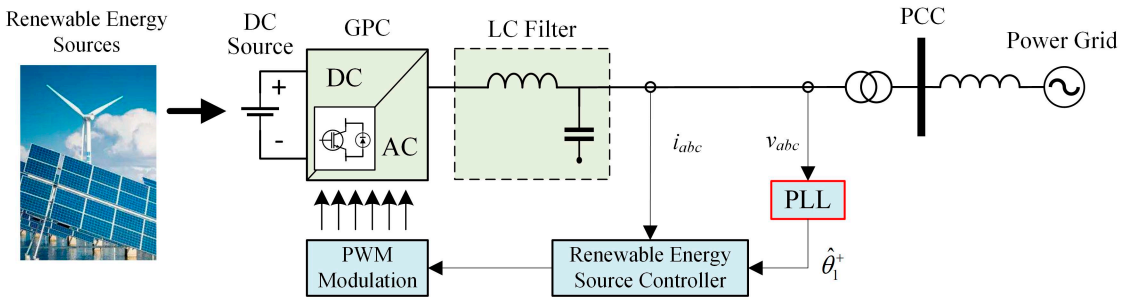


Figure 2. Block schematic of a typical grid-connected power converter system.

The block diagram of SRF-PLL is depicted in Figure 3. Park transformation is utilized as a phase detector (PD). An integrator is employed as a voltage controller oscillator (VCO). A proportional-integral controller (PI) is used to mitigate the phase-tracking error. To enhance the disturbance rejection capability and keep the phase tracking accuracy of SRF-PLL, a low pass filter (LPF) or moving average filter

(MAF) is employed in the inner loop. However, LPF-based PLL can only attenuate but not eliminate the disturbance component. To achieve good disturbance rejection, the bandwidth of LPF-based PLL must be significantly reduced, which results in a large settling time [23]. Compared with LPF, MAF can totally remove a specific set of disturbances, which depends on its window length (T_ω). However, T_ω deteriorates the dynamic response since T_ω has to be 0.01 s (half grid period) to eliminate all disturbance [24].

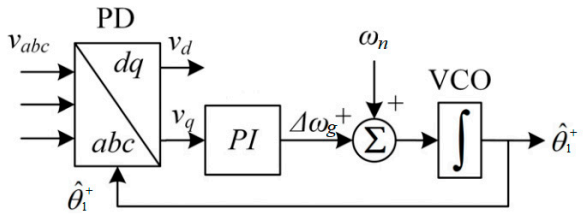


Figure 3. Block diagram of SRF-phase-locked loop (PLL).

To tackle the problem mentioned above, many advanced methods were proposed in recent years. According to their various filtering methods, these advanced PLLs can be classified into two categories: LPF-based PLLs and MAF-based PLLs. To improve the performance of LPF-based PLLs, dual second-order generalized integrators (DSOGIs) [25], multiple complex-coefficient filters (MCCFs) [26], multiple reference frame-based filter structures (MRFs) [27] and decoupled double synchronous reference frame-based filter structures (DDSRFs) [28] were arranged before applying Park transformation. The basic idea of these PLLs is to make the filtering stage act as a hybrid filter that consists of notch filters and LPFs. Notch filters are responsible for eliminating FFNS components and other important harmonics. LPFs are used to attenuate other disturbances. These methods are not suitable when grid voltages contain several significant components. Only the disturbance components coincident with the specific frequency in a notch filter can be totally removed. Compared with LPF-based PLLs, MAF-based PLLs can provide ideal filtering capabilities at the cost of increasing time delay. With a T_ω time delay, MAF can eliminate all n/T_ω (n = 1, 2, 3, ...) frequency components. The delay signal cancellation (DSC) operator is another effective filter, the behavior of which is similar to MAFs. However, single DSCs cannot eliminate all desired disturbances. To overcome this weakness, several DSCs with different T_ω are usually employed to build an entire filtering stage in cascaded [29–31]. Consequently, the time delay of the filtering stage is the sum of delay introduced by all DSCs. Too many DSCs also increases the computational burden and implementation complexity.

Besides using an advanced filter, another way to improve PLLs' performance is to change the control structure. In [32,33], a secondary control path is built to accelerate the transient behavior. However, an inappropriate design of a secondary control path may give rise to the stability problem. It also increases the order of open loop transfer functions and the implementation complexity of a system [34]. Recently, a PLL with a new structure named quasi-type-1 PLL (QT1-PLL) was proposed in [35]. Compared with the traditional type-2 SRF-PLL, QT1-PLL provides a feed-forward control path to the output. This makes QT1-PLL able to track phase precisely without using integral operations in the controller. One more open-loop pole is provided at the origin point, which accelerate the dynamic response. Since the filtering stage of QT1-PLL is built by MAFs, QT1-PLL can also offer a satisfied filtering capability. It is a good idea to do some further performance improvement of PLL based on the QT1-PLL structure.

To improve the dynamic performance without degrading PLLs' filtering capability, this paper propose a new PLL based on the QT1-PLL structure. In order to provide a fast transient response, a hybrid filtering stage is designed and arranged at the inner loop of the proposed PLL. The proposed hybrid filtering stage consists of a modified DSC (MDSC) and MAFs with narrowed T_ω. Our basic idea is to eliminate two sets of disturbance components by using MDSCs and MAFs, separately. Different from the conventional DSC-based PLL, there is only one MDSC unit in our method, which is easy for

digital implementation. To demonstrate the effectiveness, an experimental case study is carried out when grid voltage conditions are under phase jump, frequency jump, frequency ramp change and harmonic polluted voltage conditions, which usually happens to high renewable energy-penetrated power system.

This paper is organized as follows. In Section 2, the modified DSC is presented based on the analysis of DSCs. The hybrid filtering stage and new PLLs are proposed in Section 3. In Section 4, the mathematics model is established. Based on this model, the parameters are designed based on analysis of the system. In Section 5, the performance of the proposed method is validated by a comprehensive case study.

2. Modified Delay Signal Cancellation Operator

The DSC operator has been widely studied in much literature [36]. In the Laplace domain, most of the existing DSC operators can be written as:

$$\mathrm{DSC}_n(s) = \frac{1 + e^{\frac{j2\pi}{n}} e^{-\frac{T}{n}s}}{2} \tag{1}$$

To achieve a desired performance, several DSCs have to be connected in cascaded. For instance, five DSCs with different value of n (n = 2, 4, 8, 16, 32) were arranged at the pre-filtering stage in [37]. The typical block diagram of the control strategy is shown in Figure 4. Too many DSCs used in PLLs results in complicated implementation. It is a normal idea to simplify the system by reducing the number of DSCs.

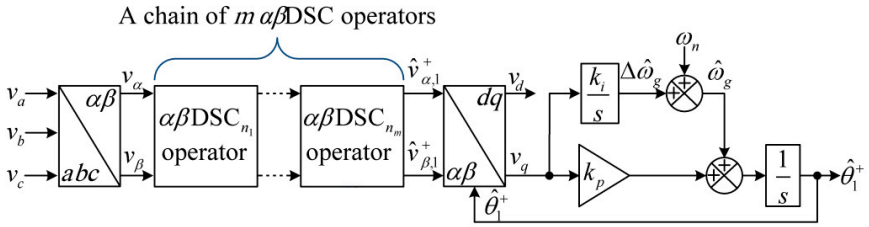


Figure 4. The common block diagram of using delay signal cancellation (DSC)s in PLL.

Observing Equation (1), it can be found that there is only one parameter n which can decide the characteristics of DSC_n. To make its property more flexible, DSC_n is modified to the following form with two parameters.

$$\mathrm{MDSC}_{m,n}(s) = \frac{1 + e^{\frac{j2\pi}{m}} e^{-\frac{T}{n}s}}{2} \tag{2}$$

In Equation (2), T is the grid period (0.02 s for 50 Hz power system). m is used to shift the original DSC_n frequency characteristics along the frequency axis. n is a parameter that can decide the time delay inside the DSC_n. After using Euler transformation, the implementation of $\mathrm{MDSC}_{m,n}$ is shown in Figure 5. It should be noted that the input of $\mathrm{MDSC}_{m,n}$ is a vector with two dimensions. The output of $\mathrm{MDSC}_{m,n}$ is also a 2D vector. The effect of m can be considered as a rotating operation to the input vector.

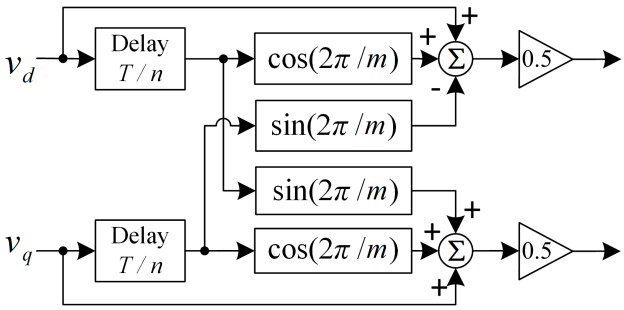


Figure 5. Time-domain implementation of a modified delay signal cancellation (MDSC) operator.

To examine the effect of two parameters (m, n), two bode diagrams are depicted in Figures 6 and 7. In Figure 6, n is set to 4. The solid lines, dashed lines and dotted lines correspond to different $\text{MDSC}_{m,n=4}$ with $m = 4, 2, 4/3$, respectively. The frequency characteristic of $\text{MDSC}_{m=4,n=4}$ can be considered as that of $\text{MDSC}_{m=1,n=4}$ shifted $\frac{n}{Tm} = 50$ Hz along the positive frequency direction. $\text{MDSC}_{m=2,n=4}$, $\text{MDSC}_{m=4/3,n=4}$ corresponds to $\frac{n}{Tm} = 100$ Hz and $\frac{n}{Tm} = 150$ Hz, respectively. This nice property can be used to arrange the notch frequency of MDSCs by setting an appropriate m.

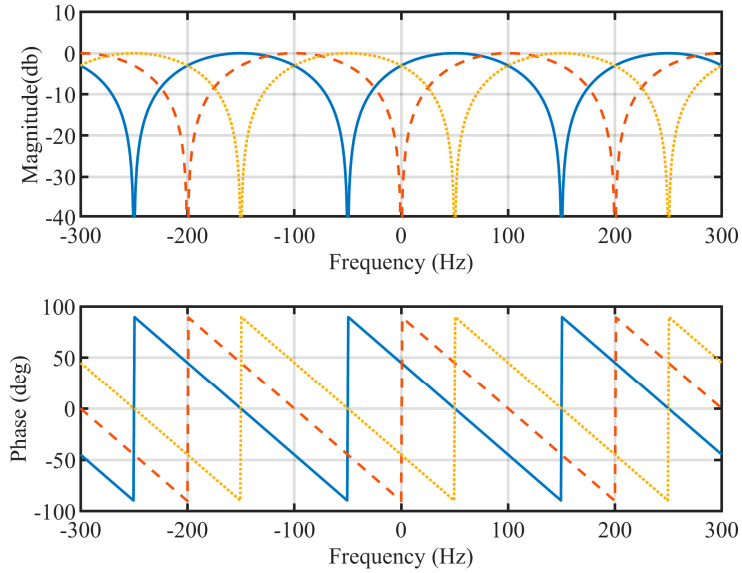


Figure 6. The frequency characteristic of MDSCs with different m ($n = 4$).

In Figure 7, m is 2. The solid lines, dashed lines and dotted lines are the bode diagrams of $\text{MDSC}_{m=2,n}$ with $n = 2, 4, 8$, respectively. With different value of n, the interval of the notch frequency of an MDSC can be changed. This property can be used to eliminate a set of specific harmonic frequency components. In the next section, the design procedure of the proposed hybrid filtering stage is presented based on the analysis of MDSCs above.

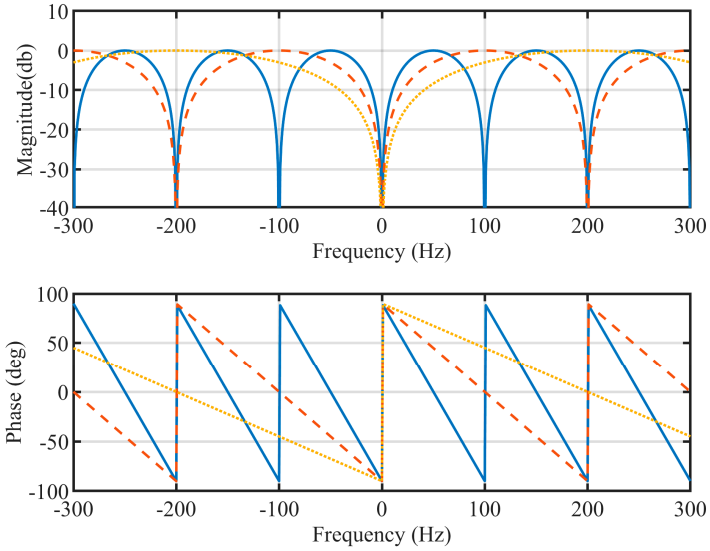


Figure 7. The frequency characteristic of MDSCs with different n (m = 2).

3. The Proposed PLL Structure

In this section, the voltage sequence component of non-ideal grid voltages is analyzed at first to provide the basis for the design procedure of the proposed PLL. To achieve our objective, a hybrid filtering stage based on MAFs and MDSCs is suggested and analyzed in this section. Then, it is incorporated into a QT1-PLL structure.

3.1. The Component Analysis of Distorted Grid Voltages

Under distorted grid voltage conditions, three-phase grid voltages contain fundamental frequency positive sequence (FFPS), fundamental frequency negative sequences (FFNS) and other harmonic sequence components. FFPS components can be written as follows:

$$\begin{aligned} v_{a,1}(t) &= V_1^+ \sin(\omega t) \\ v_{b,1}(t) &= V_1^+ \sin(\omega t - \tfrac{2\pi}{3}) \\ v_{c,1}(t) &= V_1^+ \sin(\omega t + \tfrac{2\pi}{3}) \end{aligned} \tag{3}$$

where V_1^+ represents the amplitude of FFPS and ω is the grid frequency. Then, n order harmonic sequence components can be written as:

$$\begin{aligned} v_{a,n}(t) &= V_n \sin(n\omega t + \varphi_n) \\ v_{b,n}(t) &= V_n \sin(n\omega t + \varphi_n - \tfrac{2\pi}{3}) \\ v_{c,n}(t) &= V_n \sin(n\omega t + \varphi_n + \tfrac{2\pi}{3}) \end{aligned} \tag{4}$$

By using the symmetrical component method, all voltage components can be considered as the sum of positive sequences, negative sequences and zero sequences. Applying Clark transformation to three phase voltages yields:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_0(t) \end{bmatrix} = \left[T_{\alpha\beta}\right] \begin{bmatrix} V^+_{1,4,7,\ldots} \sin(n\omega t + \phi_n) & +V^-_{2,5,8,\ldots} \sin(n\omega t + \phi_n) & +V^0_{3,6,9,\ldots} \sin(n\omega t + \phi_n) \\ V^+_{1,4,7,\ldots} \sin(n\omega t + \phi_n - \frac{2\pi}{3}) & +V^-_{2,5,8,\ldots} \sin(n\omega t + \phi_n + \frac{2\pi}{3}) & +V^0_{3,6,9,\ldots} \sin(n\omega t + \phi_n) \\ V^+_{1,4,7,\ldots} \sin(n\omega t + \phi_n + \frac{2\pi}{3}) & +V^-_{2,5,8,\ldots} \sin(n\omega t + \phi_n - \frac{2\pi}{3}) & +V^0_{3,6,9,\ldots} \sin(n\omega t + \phi_n) \end{bmatrix} \tag{5}$$

In Equation (5), $T_{\alpha\beta}$ is the transfer matrix of Clark transformation. After applying Clark transformation, Equation (5) is as follows:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_0(t) \end{bmatrix} = \begin{bmatrix} v^+_{\alpha,1,7,13,\ldots}(t) \\ v^+_{\beta,1,7,13,\ldots}(t) \\ 0 \end{bmatrix} + \begin{bmatrix} v^-_{\alpha,5,11,\ldots}(t) \\ v^-_{\beta,5,11,\ldots}(t) \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ v^0_{3,6,9,\ldots}(t) \end{bmatrix} \tag{6}$$

Observing Equation (6), it can be found that there is no triple odd harmonic in v_α and v_β. In the $\alpha\beta$-frame, only n= +1, −5, +7, −11, +13, ... order sequence components exist. By using Park transformation, the components in the $\alpha\beta$-frame turn out to be n = −2, ±6, ±12, ... order and DC components. The voltage sequence components can be summarized in Table 1. It should be noticed that the sign of frequency represents the rotating direction of the voltage sequence vector. A negative frequency means the voltage vector rotates in a counterclockwise direction.

Table 1. Voltage sequence components in grid voltages.

Harmonic Order	...	**+1**	**−1**	**−5**	**+7**	**−11**	**+13**	...
$\alpha\beta$-frame (Hz)	...	50	−50	−250	350	−550	650	...
Harmonic order	...	0	−2	−6	+6	−12	+12	...
dq-frame (Hz)	...	0	−100	−300	300	−600	600	...

3.2. The Hybrid Filtering Stage

According to the analysis of components in distorted grid voltages, a hybrid filter is well designed to eliminate the undesired components listed in Table 1. The hybrid filtering stage consists of an MDSC operator and two MAFs, which are arranged after Park transformation at the inner loop of the proposed PLL. MDSC is responsible for rejecting the FFNS component. Other dominant components are eliminated by two MAFs.

To achieve this goal, m and n, which are the parameters in MDSC, are chosen to be $m = 4$ and $n = 8$, respectively. The window length of MAF is set to be 1/300 s. The gain and phase of MDSC$_{m=4,n=8}$ can be calculated by following equations.

$$\left| \mathrm{MDSC}(j\omega)_{\substack{m=4 \\ n=8}} \right| = \left| \frac{1}{2} + j\frac{1}{2}\left(\cos\frac{0.02}{8}\omega - j\sin\frac{0.02}{8}\omega \right) \right| \tag{7}$$

$$\angle\mathrm{MDSC}(j\omega)_{\substack{m=4 \\ n=8}} = \tan^{-1}\left(\frac{\cos 0.0025\omega}{1+\sin 0.0025\omega} \right) \tag{8}$$

The bode diagram of MAF and MDSC$_{m=4,n=8}$ are depicted in Figure 8. The frequency characteristic reveals that MDSC$_{m=4,n=8}$ (solid lines) can eliminate the FFNS component. Furthermore, MAF in Figure 8 can remove ±300 Hz, ±600 Hz, ... sequence components. One thing should be noticed. Since the MDSC is implemented in a dq-frame, the FFPS component turns to be a DC component (0 Hz). According to Equations (7) and (8), the gain of MDSC$_{m=4,n=8}$ at 0 Hz is 0.707. the phase of FFPS at 0 hz is +45°. The impact on amplitude and phase of input vector will be discussed and compensated below. The bode plot of the entire hybrid filtering stage is depicted in Figure 9. The components list in Table 1 is totally removed. A +45° phase deviation exists at 0 Hz owing to MDSC$_{m=4,n=8}$.

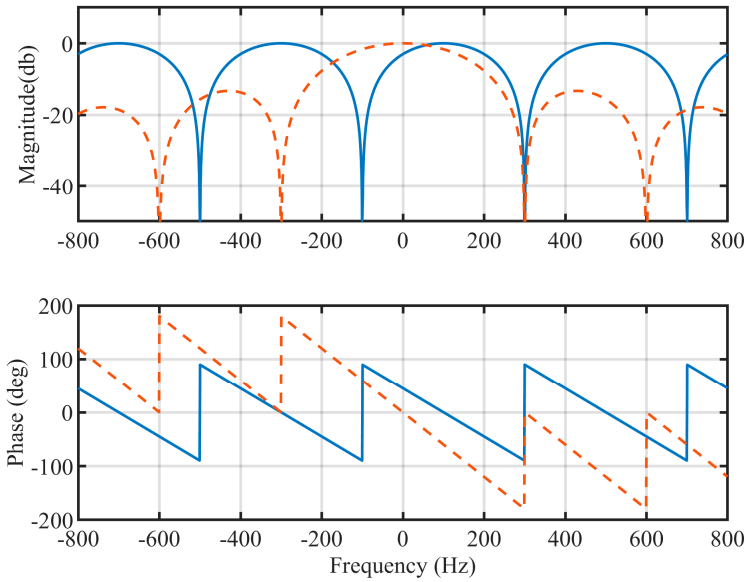


Figure 8. Bode diagram of MDSC$_{m=4,n=8}$ and moving average filter (MAF).

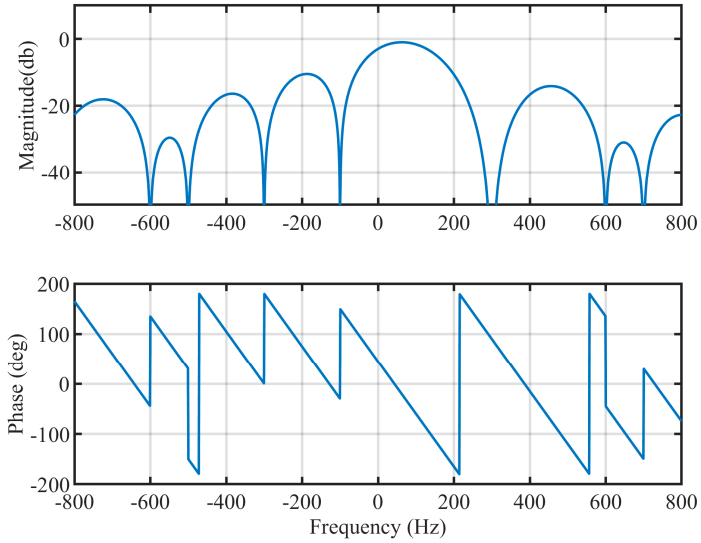


Figure 9. Bode diagram of MDSC$_{m=4,n=8}$ and MAF.

3.3. The Proposed PLL Structure

The proposed PLL structure is based on the QT1-PLL structure which is depicted in Figure 10. ω_n is the nominal frequency of the grid. $\hat{\omega}_g$ is the estimated grid frequency. $\hat{\theta}_1^+$ is the estimated phase of FFPS. The arc tangent function can remove the impact of amplitude variation of the input voltage vector. k is the only control parameter of QT1-PLL.

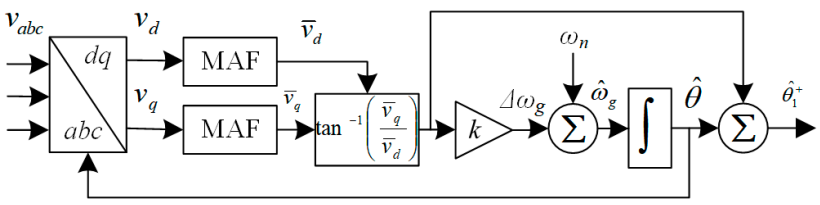


Figure 10. Block diagram of quasi-type-1 (QT1)-PLL.

Replacing the MAFs in QT1-PLL by the proposed hybrid filtering stage yields the proposed PLL structure as shown in Figure 11. While arc tangent function can remove the impact of amplitude variation, phase deviation still exists. Hence, to compensate a $\pi/4$ phase deviation introduced by $\text{MDSC}_{m=4,\, n=8}$, which is mentioned above, $-\pi/4$ is added at the output of proposed PLL. k is the only one control parameter to be designed.

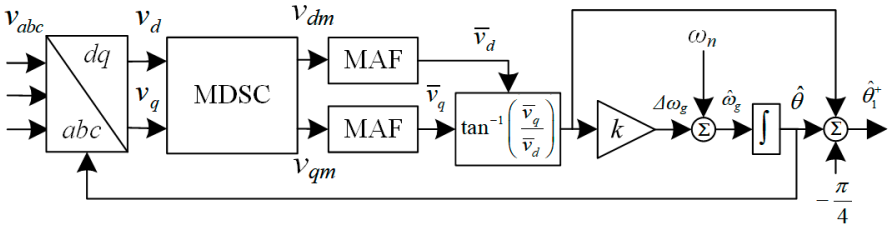


Figure 11. Block diagram of the proposed PLL.

4. Mathematics Model and Parameters Design Procedure

According to Figure 11, the mathematics model is derived in this section. To achieve a desired dynamic response, the parameter design procedure is also given. After providing the mathematics model, the stability of the system is also examined.

4.1. Mathematics Model

After Clark transformation, the FFPS component in $\alpha\beta$-frame can be written as:

$$\begin{aligned} v_\alpha(t) &= V_1^+ \cos(\theta_1^+) \\ v_\beta(t) &= V_1^+ \sin(\theta_1^+) \end{aligned} \tag{9}$$

By using Park transformation, the FFPS component in the dq-frame becomes:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = V_1^+ \begin{bmatrix} \cos(\theta_1^+ - \hat{\theta}) \\ \sin(\theta_1^+ - \hat{\theta}) \end{bmatrix} \tag{10}$$

According to Figure 5, after $\text{MDSC}_{m=4,n=8}$, the FFPS component turns out to be:

$$\begin{bmatrix} v_{dm}(t) \\ v_{qm}(t) \end{bmatrix} = 0.5 \begin{bmatrix} 1 & -e^{-\frac{T}{8}s} \\ e^{-\frac{T}{8}s} & 1 \end{bmatrix} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = 0.5 \begin{bmatrix} v_d(t) - v_q(t - \frac{T}{8}) \\ v_q(t) + v_d(t - \frac{T}{8}) \end{bmatrix} \tag{11}$$

Since two MAFs are arrange at each control path, the arc tangent function can be considered as arranged after $\text{MDSC}_{m=4,n=8}$. Then, the arc tangent operation can be expressed as:

$$\arctan\left(\frac{v_{qm}(t)}{v_{dm}(t)}\right) = \arctan\left(\frac{\cos(\theta_1^+ - \hat{\theta} - \frac{\pi}{2}) + \cos(\theta_1^+(t - \frac{T}{8}) - \hat{\theta}(t - \frac{T}{8}))}{-\sin(\theta_1^+ - \hat{\theta} - \frac{\pi}{2}) - \sin(\theta_1^+(t - \frac{T}{8}) - \hat{\theta}(t - \frac{T}{8}))}\right) \tag{12}$$

By applying trigonometric operation, Equation (12) turns out to be:

$$\arctan\left(\frac{v_{qm}(t)}{v_{dm}(t)}\right) = \arctan\left(\tan\left(\frac{\theta_1^+ - \hat{\theta} - \frac{\pi}{2} + \theta_1^+(t - \frac{T}{8}) - \hat{\theta}(t - \frac{T}{8})}{2} - \frac{\pi}{2}\right)\right) \tag{13}$$

Therefore, Equation (13) can be written as:

$$\arctan\left(\frac{v_{qm}(t)}{v_{dm}(t)}\right) = \frac{\theta_1^+ + \theta_1^+(t - \frac{T}{8}) - \hat{\theta} - \hat{\theta}(t - \frac{T}{8})}{2} + \frac{\pi}{4} \tag{14}$$

According to the derivation of Equations (9)–(14), the mathematics model of the proposed PLL is depicted in Figure 12. D'(s) is the disturbance components injected into the input voltages. $R(s)$ is defined as follows:

$$R(s) = \frac{1}{2} + \frac{1}{2}e^{-\frac{T}{8}s} \tag{15}$$

Compared with the model of other existing PLLs, our mathematics model is not a small-signal model since the arc tangent function extracts phase information directly without any linearization procedure.

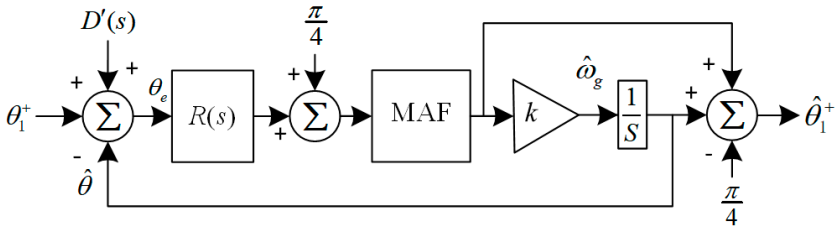


Figure 12. Mathematics model of the proposed PLL.

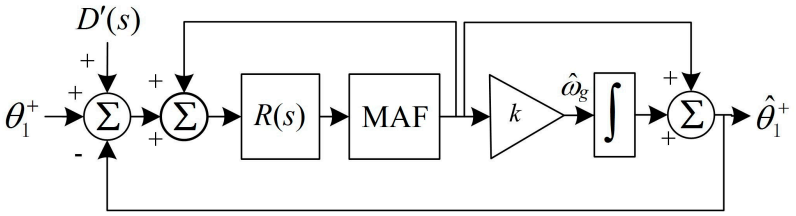


Figure 13. Simplified model of the proposed PLL.

4.2. Parameter Design Guidelines and Stability Analysis

To transform the proposed PLL into a traditional form of a closed-loop feedback system, block diagram algebra is utilized. The block diagram in Figure 12 is transformed to a simplified schematic shown in Figure 13. Hence, the open-loop transfer function can be written as:

$$G_{ols}(s) = \frac{\hat{\theta}_1^+(s)}{\theta_1^+(s) - \hat{\theta}_1^+(s)} = \left(\frac{R(s)\mathrm{MAF}(s)}{1 - R(s)\mathrm{MAF}(s)}\right)\left(\frac{s+k}{s}\right) \tag{16}$$

Then, the transfer function of phase-error can be expressed as:

$$G_e(s) = \frac{\theta_e}{\theta_1^+} = \frac{1}{1 + G_{ols}(s)} \tag{17}$$

In this paper, a parameter is chosen by its impact on the settling time of the phase-error transfer function. With different values of k, the settling time of $G_e(s)$ is examined. The phase-error transfer function under these two conditions is expressed by:

$$\Theta_e^{\Delta\theta}(s) = \frac{\Delta\theta}{s} G_e(s) \tag{18}$$

$$\Theta_e^{\Delta\omega}(s) = \frac{\Delta\omega}{s^2} G_e(s) \tag{19}$$

To calculate the settling time, inverse Laplace transformation is applied to Equations (18) and (19). Two curves of settling time as a function of k are depicted in Figure 14. When phase error is less than 2% of step change, transient response is considered to be over. To make a trade-off under both

conditions, k is selected to be 148 to achieve an optimal dynamic performance for both conditions. The settling time is around one grid period.

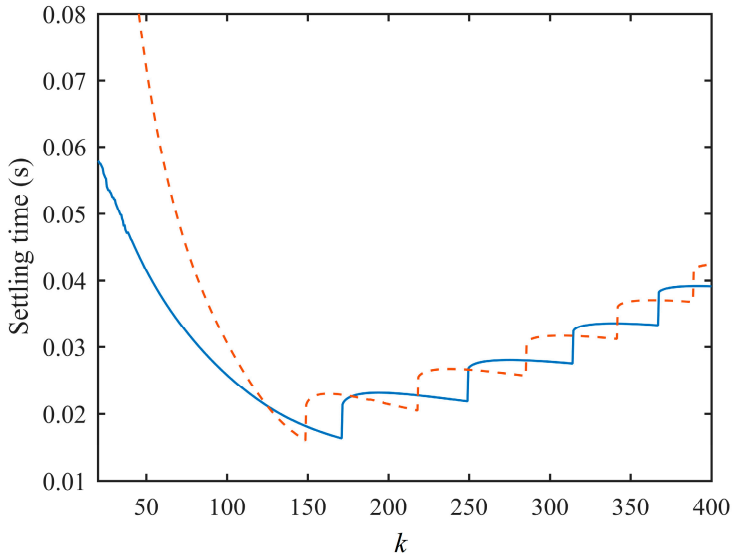


Figure 14. The settling time of the proposed PLL with different values of k under. phase jump (solid line) and frequency step-change (dashed line) conditions.

Since the model of the proposed PLL contains a time delay unit, the system turns out to be a non-minimum phase system. To examine the stability, nyquist stabilization criterion is employed in this paper instead of using a bode diagram. The nyquist diagram of $G_{ols}(s)$ is depicted in Figure 15. The nyquist curve does not surround the (−1, j0) point, which means the closed-loop feedback system of $G_{ols}(s)$ is stable. The gain stability margin (GM) is 16.5 dB at 162 Hz. The phase stability margin (PM) is 45° at 56.6 Hz.

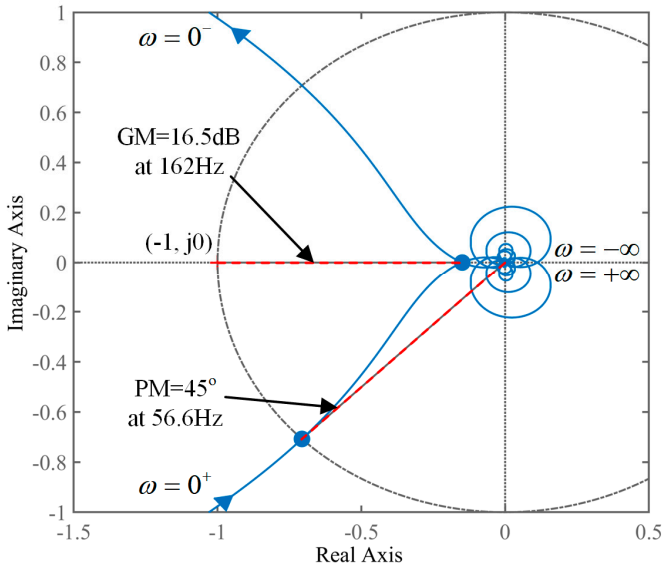


Figure 15. The Nyquist diagram of $G_{ols}(s)$.

The bode diagram of the proposed PLL and QT1-PLL is depicted in Figure 16. It can be seen that the crossover frequency of the proposed PLL is larger than that in the QT1-PLL. This yields faster transient behavior for the proposed method. It is noted that the 100 Hz component is only attenuated in the bode diagram. This does not reveal the filtering capability at 100 Hz, since the diagram is based on

the model whose input is grid phase, not grid voltages. The filtering performance is already analyzed in Section 3. Experiments are also carried out to verify the filtering capability in the next section.

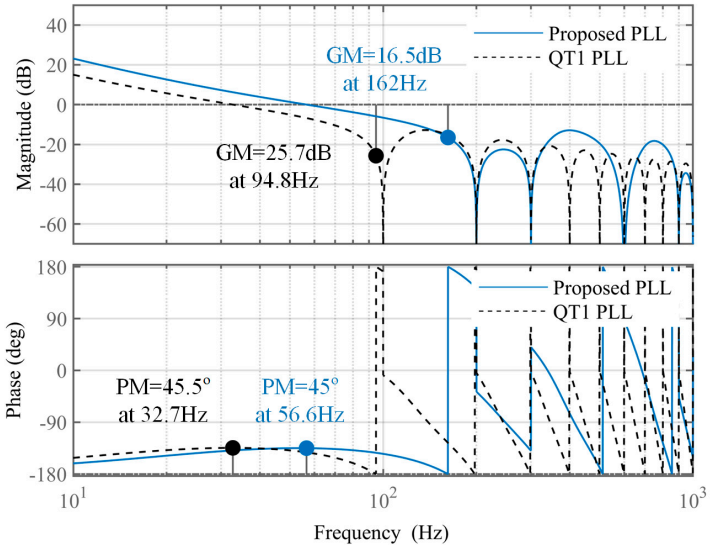


Figure 16. Bode diagram of open-loop system: Proposed PLL (solid lines), QT1-PLL (dashed lines).

4.3. Assessment of Model Accuracy

To validate the analysis above, a simulation is implemented under two conditions. The transient behaviors of phase-errors are depicted in Figure 17. This figure shows that the phase-errors of proposed PLL and its mathematics model are equal to each other during two step change in phase and frequency. The design procedure based on the mathematics model is reasonable.

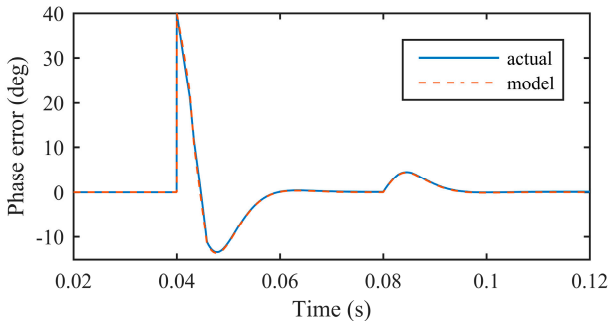


Figure 17. The transient response of the proposed PLL (solid line) and its mathematics model (dashed line) under +40° phase jump (at 0.04 s) and +5 Hz frequency jump (at 0.08 s).

5. Experimental Results

In this section, experiments are carried out under several distorted grid conditions. Different from a traditional grid, when a grid is dominated by renewable energy sources, called a "weak grid", phase jump is inevitable during the process of grid faults, sudden large load tripping and other transient behavior. Wind power fluctuation is an important issue with the increasing penetration of wind power plants, which usually cause grid frequency deviation. Thus, the proposed method is also evaluated under frequency step change and frequency ramp change conditions. Owing to the existence of a large amount of power electronics elements, harmonic disturbances are injected by power converter-based equipment such as HVDC, MMC, etc. Sub/super-synchronous oscillations arising from inappropriate system configuration can also pollute grid voltages. Hence, the proposed PLL is also examined under unbalanced and harmonic distorted voltage conditions.

In this section, experiments are implemented on a real-time experimental platform to examine the performance of the proposed PLL. Three phase voltage signals are generated by a personal computer with a data acquisition board. Through the Digital-Analogy output ports, the voltages signals are exported. PLL is implemented on a digital signal processor (DSP TMS320F28335) board. After receiving voltage signals, the estimated phase and frequency are exported through DA ports on a DSP board. Oscilloscope is used to capture all waveforms.

The grid nominal frequency is 50 Hz. The sampling frequency of a digital system is 10 kHz. The zero-order hold method is used for discretization. Besides this, the proposed PLL, EGDSC-PLL [37] is also implemented as a traditional DSC-based PLL for comparative study. QT1-PLL [36] and MAF-PLL [38] are also compared to assess the performance. Figure 18 shows the setup of the experimental platform.

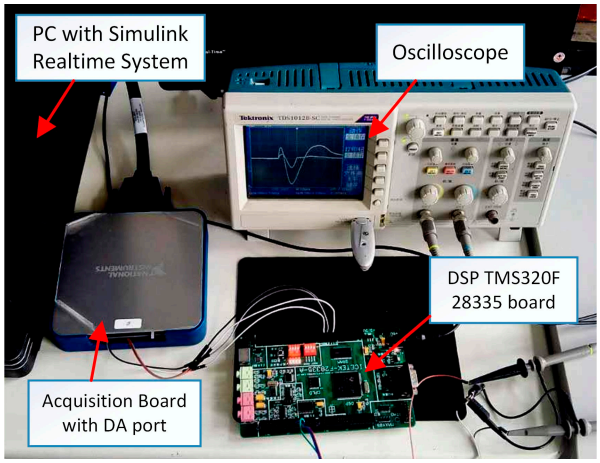


Figure 18. The experimental setup.

5.1. Test Case 1: Phase Jump

The performance is evaluated when phase jump occurs in grid voltages. Figure 19 shows the waveform of three phase voltages. A +40° phase jump came up during the experiments. Figure 20 shows the transient behavior after a phase jump. It is observed that the proposed PLL provides the fastest transient response. The settling times of phase-error and estimated frequency are around one grid period. The dynamic behavior of QT1-PLL takes over 30 ms to converge. The dynamic performance of EGDSC-PLL and MAF-PLL are even more unacceptable, owing to their more than two grid period settling time. According to the requirement of a transient response in some grid codes [21,22], an accurate estimation of grid voltage information should be extracted after undesired injection of disturbance within 25 ms. EGDSC-PLL and MAF-PLL can definitely not fulfill this requirement.

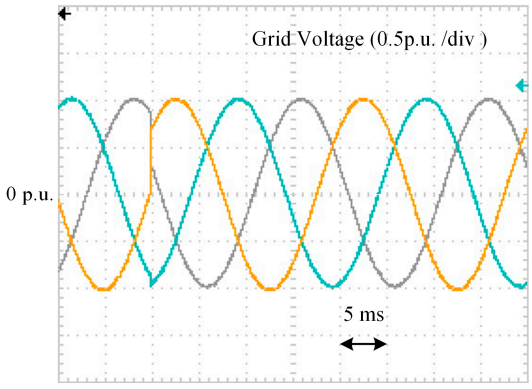


Figure 19. Grid voltages under +40° phase jump condition.

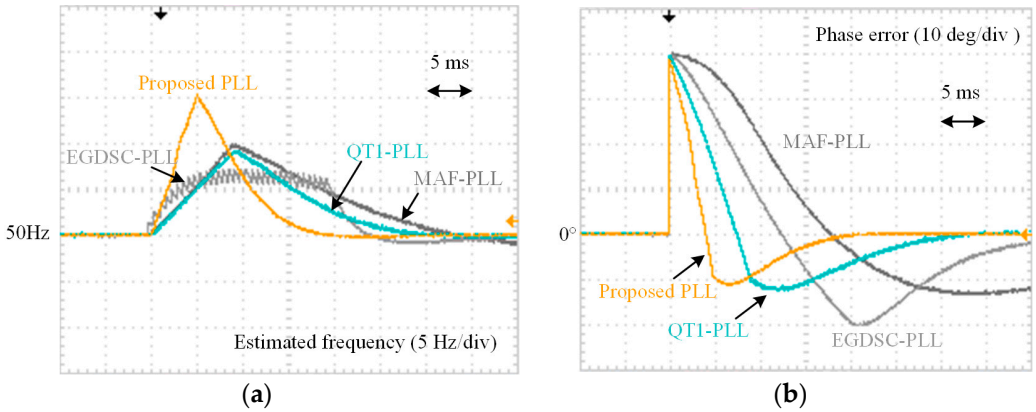


Figure 20. The experimental results of test case 1. (**a**) Estimated frequency and (**b**) phase error.

5.2. Test Case 2: Frequency Step Change

Test case 2 is carried out when grid voltages are under +5 Hz frequency step change. Figure 21 depicts the waveform of three phase voltages. The waveform of estimated frequency and phase error are shown in Figure 22. It is observed that the proposed PLL can accurately estimate grid frequency in less than one period. The phase error of the proposed PLL can converge to zero within only 15 ms. The settling time of QT1-PLL is around one period in both estimated frequency and phase error, which is acceptable for most practical application. While EGDSC-PLL can track grid frequency as fast as QT1-PLL, the phase error takes over 30 ms to converge.

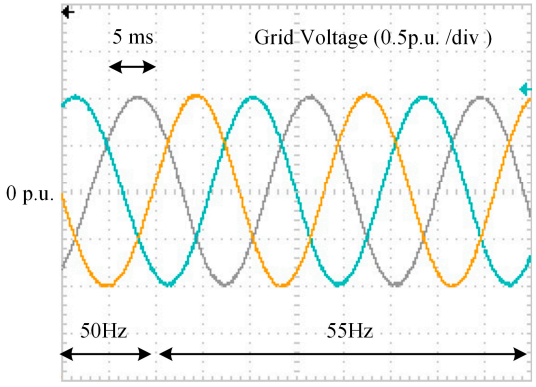


Figure 21. Grid voltages under +5 Hz frequency step change condition.

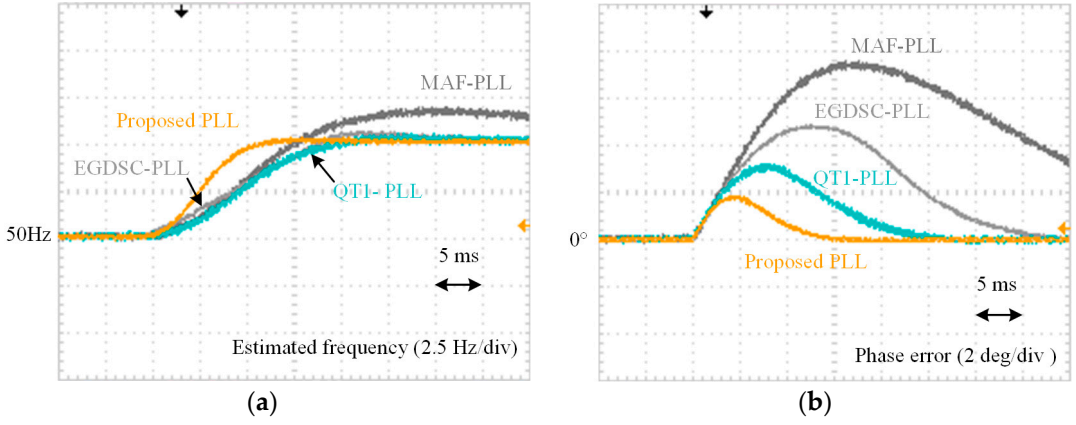


Figure 22. The experimental results of test case 2. (**a**) Estimated frequency and (**b**) phase error.

5.3. Test Case 3: Frequency Ramp Change

In practical conditions, grid frequency can hardly have a step change. Most of time, grid frequency varies bit by bit continuously. Consequently, a ramp change is implemented to the grid frequency to examine PLLs' performance. The grid frequency rises from 50 Hz to 55 Hz with a +100 Hz/s ramp rising rate. The whole behavior last for 50 ms. Figure 23 shows the waveform of grid voltages during this rising procedure. Figure 24 shows the transient behavior of four advanced PLLs. It can be seen that the proposed PLL provides 0.5° phase error during the frequency rising procedure. The phase error of QT1-PLL is less than 2°, which is also acceptable. By contrast, the phase errors of EGDSC-PLL and MAF-PLL are too big, which means PLL cannot provide acceptable phase information during the frequency changing procedure.

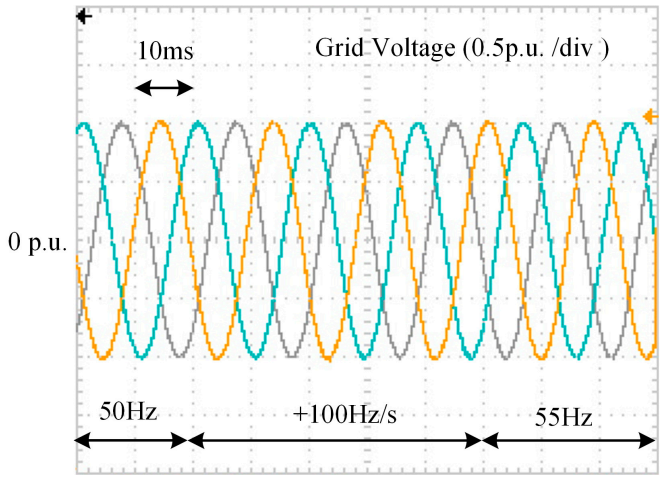


Figure 23. Grid voltages under +5 Hz frequency step change conditions.

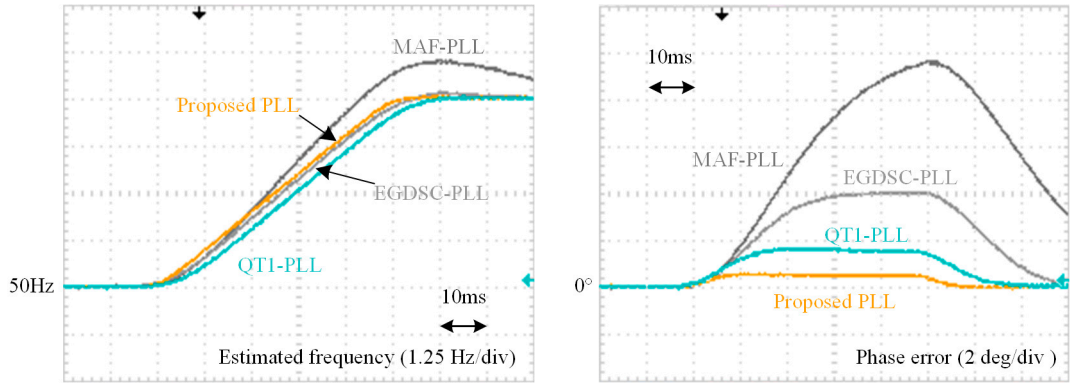


Figure 24. The experimental results of test case 3. (**a**) Estimated frequency and (**b**) phase error.

5.4. Test Case 4: Unbalanced and Distorted Grid Voltages

To examine the filtering capability, the proposed PLL is evaluated under unbalanced and distorted grid voltages condition. A frequency step change occurs during the experimental procedure. The parameters of voltage components in the polluted grid voltages are listed in Table 2. To achieve a satisfactory performance, the delay and MAF units in the proposed PLL, QT1-PLL and MAF-PLL are frequency adaptive. The corresponding implementation of a frequency adaptive structure can be found in [36] and [38]. While EGDSC-PLL can also improve its performance by making DSCs adaptive, too many DSCs used in its filtering stage increases its computational burden dramatically. Hence, EGDSC-PLL with non-adaptive DSCs is more practical for the comparison.

Table 2. Parameters of grid voltages.

Voltage Component (in $\alpha\beta$-frame)	Amplitude (p.u.)
Fundamental positive sequence (+1st order)	1
Fundamental negative sequence (−1st order)	0.1
5^{th} harmonic negative sequence (−5th order)	0.1
7^{th} harmonic positive sequence (+7th order)	0.05
11^{th} harmonic negative sequence (−11th order)	0.05
13^{th} harmonic positive sequence (+13th order)	0.05

The polluted grid voltages are depicted in Figure 25. The transient responses of four PLLs are depicted in Figure 26. It can be observed that all PLLs can eliminate disturbances completely when grid frequency is at its nominal value. When grid frequency jumps from 50 Hz to 55 Hz, transient behavior occurs for every PLL. Thanks to frequency adaptive implementation, the proposed PLL, QT1-PLL and MAF-PLL can still provide a satisfactory filtering capability after frequency change. However, oscillation of phase error occurs in the transient behavior of EGDSC-PLLs for its non-adaptive DSCs. While this problem can be solved by applying adaptive DSCs, a huge computational burden is still a big problem for designers to solve.

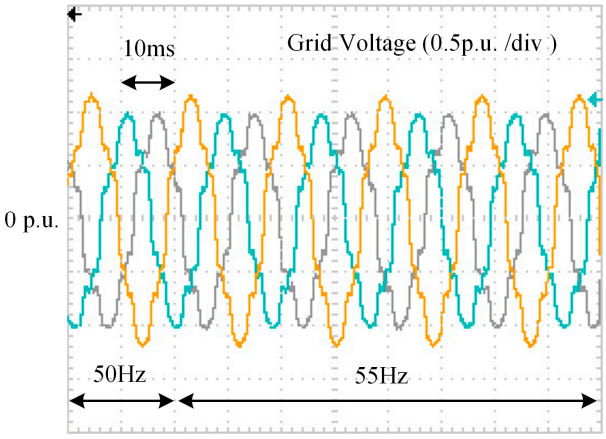


Figure 25. Grid voltages under +5 Hz frequency step change conditions.

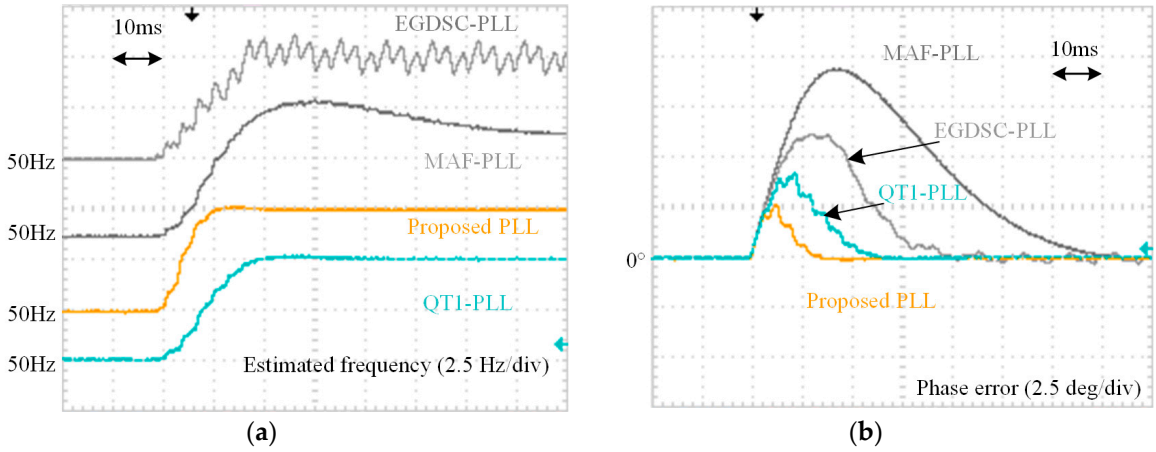


Figure 26. The experimental results of test case 3. (**a**) Estimated frequency and (**b**) phase error.

6. Conclusions

With more and more wind and solar energy plants connected to power systems, grid voltages are prone to be distorted. To keep grid frequency and phase tracking accuracy during distorted

and even faulty conditions without degrading dynamic performance, a hybrid filter-based PLL is proposed. By using well designed MDSCs and MAFs with narrowed window length, time delay introduced by filtering stage is reduced. The hybrid filtering stage is incorporated with a QT1-PLL structure. A comprehensive experimental study is implemented to examine the effectiveness. Test cases concerning several conditions, which are easily triggered in high renewable penetration power systems, are carried out. Experimental results illustrate that the proposed PLL can provide a more satisfactory dynamic response than other traditional methods. The filtering capability and implementation complexity are also better than the conventional DSC-based PLLs.

Author Contributions: T.L. and J.Y. proposed the original idea and analyzed the experimental results. Y.L. built the experimental setup and performed the experiments. T.L. wrote the full manuscript. W.G. and B.H. supervised the experiments.

Funding: This work was supported by scientific research fund from Liaoning Electric Power Co., Ltd., State Grid Co. of China.

Acknowledgments: This work was with technical assistance from Liaoning Electric Power Co., Ltd., State Grid Co. of China.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

The following nomenclatures are used in this manuscript:

v_{abc}	Three-phase grid voltage
v_d, v_q	The d-q-axis voltage components after Park transformation
v_α, v_β	The α-β-axis components of grid voltage after Clarke transformation
$\hat{v}^+_{\alpha,1}$, $\hat{v}^+_{\beta,1}$	The α-β-axis components after prefiltering stage
$\overline{v}_d$, $\overline{v}_q$	The d-q-axis voltage components after filtering processing
v_{dm}, v_{qm}	The d-q-axis voltage components after MDSC
ω_n	The fundamental nominal angular frequency of grid voltage
$\Delta\omega_g$	The error of estimated angular frequency of grid voltage
$\hat{\omega}_g$	The estimated angular frequency of grid voltage
θ^+_1	The angular phase of input grid voltage
$\hat{\theta}^+_1$	The estimated phase of grid voltage
θ_e	The phase-tracking error
T_ω	The window length of MAF
$\Delta\theta^+_1$	The value of phase jump
k	The only control parameter in the proposed PLL

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