



# Article A Hybrid Predictive Control for a Current Source Converter in an Aircraft DC Microgrid

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Received: 24 September 2019; Accepted: 20 October 2019; Published: 23 October 2019



**Abstract:** A current source converter (CSC) is a promising topology for interfacing aircraft generators with the onboard DC microgrid. In this paper, a hybrid predictive control is proposed for the CSC with an output LC filter in such application. Deadbeat predictive control with larger sampling time is applied to the output circuit, generating reference source currents. Finite-set model predictive control with smaller sampling time is applied to the input circuit to achieve sinusoidal source currents, which is simplified by saving the source current predictions. The proposed scheme eliminates both the proportional-integral control complexity. A SiC-MOSFET-based prototype is used to verify the validity of the proposed scheme. Experimental results under 150 V/350–800 Hz AC input and 270 V DC output demonstrate the superior control performance.

**Keywords:** more electric aircraft; DC microgrid; current source converter; deadbeat predictive control; finite-set model predictive control

# 1. Introduction

There has been an increasing trend of more electric aircraft (MEA) in the aerospace industry [1], towards better performance in efficiency, reliability and safety. The onboard power system is a typical microgrid (MG) system with distributed supplies and loads [2]. The DC MG has been widely considered as a preferable solution for the future onboard MG and has garnered great attention [3–5]. A typical paradigm of the DC MG is shown in Figure 1. In such a system, most of the power supplies and loads, including the main generators, auxiliary power units, energy storage units and low-voltage (LV) DC loads, are connected to the high-voltage (HV) DC bus (typically 270 V) through power electronic converters.



Figure 1. Typical architecture of the aircraft DC microgrid.

This paper focuses on the AC–DC converters that interface variable-frequency generators with the MG. Currently, multi-pulse diode rectifiers with phase-shift transformers dominate in such applications [2], because of their very high reliability. Yet, the bulky filter components and unidirectional power flow could not satisfy requirements of future MEAs. There are some studies that adopt voltage source converter (VSC) to replace diode rectifiers [6,7], which could achieve good power quality and smaller filter components. However, both the diode rectifiers and VSC do not have the capability to isolate DC bus faults, and have to work under low and narrow range of input voltages. A promising alternative to diode rectifiers and VSC is the current source converter (CSC), which is also known as buck rectifier or AC–DC matrix converter. Like VSC, CSC can also achieve high-quality input and output currents with small filter components. Moreover, CSC has the intrinsic capability to limit overcurrent and can work under a higher and wider range of input voltages. Therefore, it could achieve more efficient and compact design of the whole system. Many researchers have studied the usage of CSC in aircraft applications [8–11].

Modulation and control are important research topics of CSC, which have great achievements in civil applications. In [12], the optimal modulation scheme is proposed, which could achieve the minimum switching loss and ripples, and thus has been widely adopted in later studies. Some new modulation and control techniques have also been developed for CSC regarding new topologies and applications [13–16].

Benefiting from the fast development of microcontrollers, predictive control has been suggested as an emerging control technique for power converters [17,18]. The basic principle of a predictive control scheme is to predict the system behavior using the discrete prediction models. There are typically two kinds of predictive control schemes: deadbeat predictive control (DBPC) and finite-set model predictive control (FS-MPC). DBPC generates the reference signals based on the prediction models, and a linear modulation scheme is usually used in the inner loop to operate the converter [19,20]. On the contrary, FS-MPC relies on the minimization of the defined cost function to select the optimal switching state for the converter, and eliminates the modulator. In addition to the simple concept and easy implementation, FS-MPC features fast dynamic response and multi-objective optimization. As the most popular predictive control scheme in recent years, FS-MPC has been applied to various power converters [21–26], including those used in naval MGs, which are similar to the aircraft MGs [27,28].

MPC has also attracted attentions in the area of CSC control. In [29], FS-MPC is applied to control the input reactive power and output current of CSC. Yet, this scheme is unable to mitigate some input harmonics especially those around the filter resonant frequency [30], resulting in the need of a very large filter. The input reactive power control can be replaced by direct source current control to achieve sinusoidal source currents [31], which has been well acknowledged in recent studies [32,33]. However, reference source currents need to be appropriately generated, otherwise the output control performance could be degraded. In [31–33], reference source currents are calculated according to the load model, but this kind of reference generation is only applicable to the situations with a known load model (e.g., passive R–L load).

For CSC used in the aircraft DC MG, an LC filter should be installed at the output circuit so as to smooth the load voltage. In this case, the load model is usually unknown and thus the above reference generation is not applicable. Besides, for optimal tradeoff between the input and output control performance, weighting factor in the cost function of the above FS-MPC scheme needs to be tuned properly, which is usually based on empirical knowledge and thus increases the implementation complexity. In [34,35], the proportional integral (PI) controller is used to generate the reference source currents and eliminate the weighting factor. Although this method could address the above two issues, it violates the fundamental principle of the predictive control and also increases the control complexity.

The contribution of this paper lies in the following: A novel hybrid predictive control scheme is proposed for the CSC with an output LC filter used in the aircraft DC MG. The proposed scheme has a hybrid and cascaded structure, which successfully eliminates both the PI controller and weighting factor, reducing the control complexity. DBPC is applied to control load voltage and output current,

while FS-MPC is applied to control source currents. Reference source currents are generated from the output DBPC. In addition, the output DBPC has larger sampling time and the input FS-MPC is simplified by eliminating source current predictions, which reduces the computational burden.

This paper is organized as follows. Section 2 presents the mathematical model of the CSC system for aircraft DC MG. Section 3 elaborates the principle of the proposed hybrid predictive control scheme. Section 4 shows the simulation and experimental verification. Section 5 draws the conclusion.

#### 2. Mathematical Model of the CSC System

Schematic of the CSC system for the aircraft DC MG is shown in Figure 2. Power source connected to the input side of CSC could be the variable frequency main generators or the auxiliary power units. The input LC filter constituted by the inductor  $L_{fi}$  and the capacitor  $C_{fi}$  attenuates high-frequency harmonics in input currents of CSC. In practice, part or all of the filter inductance can be provided by the armature inductance of generators. CSC consists of six switches with reverse blocking capability. If bidirectional power flow is required, each switch can be composed of two transistors in common-source connection. Otherwise, one transistor and one diode in series could serve as each switch if unidirectional power flow is sufficient. One freewheeling diode can be installed at the output side of CSC to reduce the conduction loss, yet negative output voltage will be unavailable. An LC filter composed of the inductor  $L_{fo}$  and capacitor  $C_{fo}$  is installed at the output of CSC to provide smooth load voltage.



**Figure 2.** Schematic of the current source converter (CSC) system as the interface in aircraft DC microgrid (MG).

According to Figure 2, continuous model of the input circuit of CSC can be expressed in the state-space form:

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \mathbf{i}_{\mathrm{s}} \\ \mathbf{u}_{\mathrm{i}} \end{bmatrix} = A_{\mathrm{i}} \begin{bmatrix} \mathbf{i}_{\mathrm{s}} \\ \mathbf{u}_{\mathrm{i}} \end{bmatrix} + B_{\mathrm{i}} \begin{bmatrix} \mathbf{u}_{\mathrm{s}} \\ \mathbf{i}_{\mathrm{i}} \end{bmatrix}, \tag{1}$$

where  $u_s$  and  $i_s$  are the vectors representing source voltages and currents respectively;  $u_i$  and  $i_i$  are the vectors representing input voltages and currents of CSC respectively and matrices  $A_i$  and  $B_i$  are expressed as:

$$A_{i} = \begin{bmatrix} -R_{fi}/L_{fi} & -1/L_{fi} \\ 1/C_{fi} & 0 \end{bmatrix}, B_{i} = \begin{bmatrix} 1/L_{fi} & 0 \\ 0 & -1/C_{fi} \end{bmatrix},$$
(2)

where  $R_{\rm fi}$  is the parasitic resistance of the filter inductor  $L_{\rm fi}$ .

For simplifying the derivation of prediction models for the output DBPC, differential equations rather than the state-space equation are adopted to model the output circuit:

$$\frac{di_{o}}{dt} = -\frac{R_{fo}}{L_{fo}}i_{o} + \frac{1}{L_{fo}}(u_{o} - u_{L}),$$
(3)

$$\frac{\mathrm{d}u_{\mathrm{L}}}{\mathrm{d}t} = \frac{1}{C_{\mathrm{fo}}}(i_{\mathrm{o}} - i_{\mathrm{L}}),\tag{4}$$

where  $u_0$  and  $i_0$  are the output voltage and current of CSC respectively;  $u_L$  and  $i_L$  are the load voltage and current respectively and  $R_{fo}$  is the parasitic resistance of the inductor  $L_{fo}$ .

By controlling switches of CSC, appropriate input current vector  $i_i$  and output voltage  $u_o$  can be generated to obtain desired source current vector  $i_s$ , output current  $i_o$  and load voltage  $u_L$ . According to the principle of CSC, there are nine valid switching states in total, as listed in Table 1. The first six states generate active  $i_i$  and non-zero  $u_o$ . In Table 1,  $u_{xy}$  denotes the input line–line voltage between phase x and phase y, where  $x, y \in \{A, B, C\}$ . The last three states generate zero  $i_i$  and  $u_o$ . If a freewheeling diode is adopted, these zero states can be replaced by the on-state of the freewheeling diode.

N	S <sub>AP</sub>	S <sub>BP</sub>	S <sub>CP</sub>	S <sub>AN</sub>	S <sub>BN</sub>	S <sub>CN</sub>	i <sub>i</sub>	u <sub>o</sub>
1	1	0	0	0	0	1	$(1 + 1j/\sqrt{3}) \cdot i_0$	$-u_{\rm CA}$
2	0	1	0	0	0	1	$2j/\sqrt{3}\cdot i_{o}$	$u_{\rm BC}$
3	0	1	0	1	0	0	$(-1 + 1j/\sqrt{3}) \cdot i_0$	$-u_{AB}$
4	0	0	1	1	0	0	$-(1 + 1j/\sqrt{3}) \cdot i_0$	$u_{\rm CA}$
5	0	0	1	0	1	0	$-2j/\sqrt{3}\cdot i_{\rm o}$	$-u_{\rm BC}$
6	1	0	0	0	1	0	$(1 - 1j/\sqrt{3}) \cdot i_0$	$u_{AB}$
7	1	0	0	1	0	0	0	0
8	0	1	0	0	1	0	0	0
9	0	0	1	0	0	1	0	0

Table 1. Valid switching states of CSC.

## 3. Proposed Hybrid Predictive Control Scheme

### 3.1. Control Block Diagram

Block diagram of the proposed hybrid predictive control scheme is shown in Figure 3. It can be seen that the proposed scheme consists of two parts: (1) DBPC for the output circuit and (2) FS-MPC for the input circuit. Besides, it is clear that the proposed scheme has a cascaded structure. DBPC of the load voltage generates the reference output current  $i_0^*$ , while DBPC of the output current generates the reference output voltage  $u_0^*$ . Product of  $i_0^*$  and  $u_0^*$  is the reference source active power  $p_s^*$ . FS-MPC of source currents finally generates the optimal switching state for CSC.



Figure 3. Block diagram of the proposed hybrid control scheme (Different colors indicate different sampling times).

The following parts of this section will present the principle of the output DBPC, input FS-MPC and the generation of reference source currents separately. It should be noted that sampling time for the input and output control are different in the proposed scheme, which are highlighted by different colors in Figure 3. Setting different sampling time is necessary for the proposed scheme, for which the reason is discussed in Part 3.4.

#### 3.2. DBPC for the Output Circuit

According to the continuous model of the load voltage shown in Equation (4), the discrete model for predicting  $u_L$  is obtained with the forward Euler method:

$$u_{\rm L}[n+1] = u_{\rm L}[n] + \frac{T_{\rm so}}{C_{\rm fo}}(i_{\rm o}[n] - i_{\rm L}[n]),$$
(5)

where x[n] denotes the value of variable x at the beginning of the nth sampling period. Note that the sampling time is  $T_{so}$  for Equation (5). For the load voltage model, the only controllable variable is the output current  $i_o$ . Therefore, if the load voltage  $u_L$  reaches the desired value at the beginning of the (n + 1)th sampling period, the reference value of  $i_o$  can thus be obtained from Equation (5):

$$i_{\rm o}^*[n] = \frac{C_{\rm fo}}{T_{\rm so}} \left( u_{\rm L}^*[n+1] - u_{\rm L}[n] \right) + i_{\rm L}[n],$$
 (6)

where the reference load voltage  $u_{L}*[n + 1]$  is a constant DC value. A constraint can be added at this step to limit the maximum output current.

Similarly, the discrete prediction model for the output current is obtained from Equation (3) with a forward Euler method:

$$i_{\rm o}[n+1] = \left(1 - \frac{R_{\rm fo}T_{\rm so}}{L_{\rm fo}}\right)i_{\rm o}[n] + \frac{T_{\rm so}}{L_{\rm fo}}(u_{\rm o}[n] - u_{\rm L}[n]).$$
(7)

Note the sampling time for the output current control is also  $T_{so}$ . For the prediction model of the output current, the only controllable variable is the output voltage  $u_0$ . Therefore, the reference output voltage can be obtained based on Equation (7):

$$u_{\rm o}^*[n] = \frac{L_{\rm fo}}{T_{\rm so}} \bigg[ i_{\rm o}^*[n+1] - \left( 1 - \frac{R_{\rm fo} T_{\rm so}}{L_{\rm fo}} \right) i_{\rm o}[n] \bigg] + u_{\rm b}[n].$$
(8)

It can be seen that, to obtain the reference output voltage  $u_o^*[n]$ , the reference output current  $i_o^*[n + 1]$  at the beginning of the (n + 1)th sampling period should be obtained first. However, according to Equation (6), only  $i_o^*[n]$  is generated in the *n*th sampling period, while  $i_o^*[n + 1]$  is not available. Therefore, the following approximation needs to be applied:

$$i_{0}^{*}[n+1] \approx i_{0}^{*}[n].$$
 (9)

Such approximation is reasonable because the output current is DC current and can be considered constant within one sampling period if the output filter inductor is big enough. With the substitution of Equation (9) into Equation (8), the reference output voltage is thus rewritten as:

$$u_{\rm o}^*[n] \approx \frac{L_{\rm fo}}{T_{\rm so}} \bigg[ i_{\rm o}^*[n] - \bigg( 1 - \frac{R_{\rm fo} T_{\rm so}}{L_{\rm fo}} \bigg) i_{\rm o}[n] \bigg] + u_{\rm L}[n].$$
(10)

#### 3.3. FS-MPC for the Input Circuit

The discrete prediction model for the input circuit is obtained from Equation (1):

$$\begin{bmatrix} \mathbf{i}_{\mathrm{s}}[k+1] \\ \mathbf{u}_{\mathrm{i}}[k+1] \end{bmatrix} = \Phi_{\mathrm{i}} \begin{bmatrix} \mathbf{i}_{\mathrm{s}}[k] \\ \mathbf{u}_{\mathrm{i}}[k] \end{bmatrix} + \Gamma_{\mathrm{i}} \begin{bmatrix} \mathbf{u}_{\mathrm{s}}[k] \\ \mathbf{i}_{\mathrm{i}}[k] \end{bmatrix},$$
(11)

where y[k] denotes the value of variable *y* at the beginning of the *k*th sampling period. Note that the sampling time is  $T_{si}$  for the input control. Matrices in Equation (11) are expressed as:

$$\Phi_{\rm i} = e^{A_{\rm i} \cdot T_{\rm s}} = \begin{bmatrix} \Phi_{\rm i11} & \Phi_{\rm i12} \\ \Phi_{\rm i21} & \Phi_{\rm i22} \end{bmatrix},\tag{12}$$

and

$$\Gamma_{i} = A_{i}^{-1} (\Phi_{i} - I) B_{i} = \begin{bmatrix} \Gamma_{i11} & \Gamma_{i12} \\ \Gamma_{i21} & \Gamma_{i22} \end{bmatrix}.$$
(13)

The basic idea of FS-MPC is to find the optimal switching state by minimizing the defined cost function. For the digital control in practice, the switching state determined in the *k*th sampling period has to be applied to the CSC in the (k + 1)th sampling period, resulting in one sampling period delay. Performance of FS-MPC is sensitive to the control delay and thus delay compensation must be implemented. At the beginning of the *k*th sampling period, the digital controller measures source voltage  $u_s[k]$ , source current  $i_s[k]$  and input voltage  $u_i[k]$ . Besides, the input current  $i_i[k]$  can be looked-up from Table 1 using the switching state S[k], which is determined in the previous sampling period. Therefore, source current  $i_s[k + 1]$  and input voltage  $u_i[k + 1]$  can thus be calculated based on Equation (11).

For determining the switching state S[k + 1] in the next sampling period, the prediction model for the source current vector and input voltage vector is obtained from Equation (11):

$$\begin{bmatrix} \mathbf{i}_{\mathrm{s}}[k+2] \\ \mathbf{u}_{\mathrm{i}}[k+2] \end{bmatrix} = \Phi_{\mathrm{i}} \begin{bmatrix} \mathbf{i}_{\mathrm{s}}[k+1] \\ \mathbf{u}_{\mathrm{i}}[k+1] \end{bmatrix} + \Gamma_{\mathrm{i}} \begin{bmatrix} \mathbf{u}_{\mathrm{s}}[k+1] \\ \mathbf{i}_{\mathrm{i}}[k+1] \end{bmatrix}.$$
(14)

In FS-MPC, cost function is the only criterion to determine which switching state is the optimal one that should be applied to the converter. It should include prediction errors of all the desired control objectives. In this paper, to achieve sinusoidal source currents, prediction errors of source currents are included in the cost function:

$$g = \|\mathbf{i}_{s}^{*}[k+2] - \mathbf{i}_{s}[k+2]\|^{2},$$
(15)

where generation of the reference source current  $i_s * [k + 2]$  is presented in the next part. Note that there is no weighting factor adopted in the cost function, which saves the empirical adjustment and thus reduces the control complexity.

According to Table 1, Equations (14) and (15), each valid switching state corresponds to a value of  $i_i[k + 1]$ . Therefore, there are seven possible values of the source current  $i_s[k + 2]$  in total, which generate seven values of g. Zero g means perfect tracking performance of source currents. Therefore, the switching state that generates the minimum value of g should be applied to the CSC in the (k + 1)th sampling period.

However, if the cost function shown in Equation (15) is directly evaluated to select the optimal switching state, the computational burden is relatively high. This is because every calculation of *g* requires the prediction of source currents using Equation (14), resulting in many multiplication operations. To reduce the computational burden, the FS-MPC can be simplified as presented below.

According to (14), the reference input current vector  $i_i^*$  is defined as:

$$\dot{i}_{i}^{*}[k+1] = \frac{\dot{i}_{s}^{*}[k+2] - \Phi_{i11}\dot{i}_{s}[k+1] - \Phi_{i12}u_{i}[k+1] - \Gamma_{i11}u_{s}[k+1]}{\Gamma_{i12}}.$$
(16)

With the substitution of Equations (14) and (16), (15) can be rewritten as:

$$g = \Gamma_{i12}^2 \| \boldsymbol{i}_i^* - \boldsymbol{i}_i[k+2] \|^2.$$
(17)

According to the deduction, Equation (17) is completely equivalent to Equation (15). Therefore, if applied to the FS-MPC, Equation (17) could achieve exactly the same control performance with Equation (15). However, for each valid switching state, Equation (17) can be directly calculated with  $i_i$  looked up from Table 1, which saves the source current predictions, the computational burden is thus reduced significantly. In practice, the constant coefficient  ${}_{i12}{}^2$  in Equation (17) can also be eliminated, since it does not affect the minimization of the cost function.

#### 3.4. Generation of Reference Source Currents

Ideally, the active power generated by the power source should be equal to those absorbed by the load. Since the reference output voltage and current are obtained using Equations (6) and (10), the reference source active power at the beginning of the (k + 2)th sampling period can be calculated as:

$$p_{\rm s}^*[k+2] = u_{\rm o}^*[n]i_{\rm o}^*[n]/\eta, \tag{18}$$

where is the conversion efficiency from the supply to the load. The reference source current vector is further calculated based on the instantaneous power theory:

$$\dot{\mathbf{i}}_{s}^{*}[k+2] = \frac{(p_{s}^{*}[k+2] + jq_{s}^{*}[k+2])\mathbf{u}_{s}[k+2]}{1.5||\mathbf{u}_{s}[k+2]||^{2}} \approx \frac{(p_{s}^{*}[k+2] + jq_{s}^{*}[k+2])\mathbf{u}_{s}[k]}{1.5||\mathbf{u}_{s}[k]||^{2}},$$
(19)

where  $q_s^*$  is the reference source reactive power, which can be set as zero for unity power factor operation, or other values for reactive power compensation. Theoretically, the source voltage  $u_s$  at the beginning of (k + 2)th sampling period should be used to calculate  $i_s^*[k + 2]$ , but it is unavailable at the *k*th sampling period. Therefore,  $u_s[k + 2]$  is approximated by  $u_s[k]$  and can also be estimated using an interpolation algorithm in order to achieve higher control accuracy.

Note that, in Equation (18), the sampling time for variables at the left and right sides of the equal sign are different, which is necessary for the proposed control scheme. Although the predictive control has theoretically very fast dynamic response, it still takes some sampling periods for the actual source currents to reach the references, because of the practical voltage and current limit of the converter. If the input and output control have the same sampling time, the actual active power cannot respond to the load demand promptly, leading to the unstable operation of the control. In addition, as it can be deduced from Equations (6), (10) and (18), the smaller the sampling time of the output control is, the more high-frequency ripples of the reference source active power will contain, which deteriorate the input power quality. Therefore, to achieve sinusoidal source currents, the sampling time of the output control should be larger than that of the input control. In this study, the input sampling time  $T_{si}$  is 6.67 s, while the output sampling time  $T_{so}$  is 333 s or 667 s, which is 50 or 100 times of  $T_{si}$ . As a result, the reference source active power obtained from Equation (18) remains invariable within every 50 or 100 input sampling periods, which helps to reduce the low-frequency harmonics in source currents. Although  $T_{so}$  is much larger than  $T_{si}$ , it is still small enough to obtain fast dynamic response of the output control.

#### 4. Simulation and Experimental Verification

#### 4.1. Experimental Setup

Effectiveness of the proposed control scheme was verified on an experimental prototype shown in Figure 4. Parameters of the prototype are summarized in Table 2. A simulation model was built in the MATLAB/Simulink (R2018) software, of which the parameters were the same with those listed in Table 2. The source voltage was 150 V (phase, RMS) and source frequency varied from 350 Hz to 800 Hz. The normal source frequency was 400 Hz. The normal load resistor was 30, but changed to 45 during the dynamic process. The reference load voltage was 270 V. Power switches used were SiC-MOSFETsproduced by Rohm, which have a very small rising and falling time. The digital controller

was composed of a digital signal processor (DSP) operating at the system frequency of 300 MHz, and a field-programmable gate array (FPGA), which assists the signal sampling, switching commutation and gate driving. The digital controller has a very strong computational capability, which guarantees the completion of all the calculations within one input sampling period  $T_{si}$ . The converter efficiency was measured in experiments, which was about 95.8% and compensated in Equation (18). Yet, in the simulation model, was assumed unity since ideal switches are used.



Figure 4. Picture of the experimental setup.

Table 2. Parameters of the SiC-MOSFET-based ex	perimental prototype.
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Variables	Description	Values	
Source			
$U_{ m s}$	Source Voltage (phase, RMS)	150 V	
$f_{s}$	Source Frequency	350-800 Hz	
Input Filter			
$L_{\mathrm{fi}}$	Input Filter Inductor	1 mH	
$C_{\mathrm{fi}}$	Input Filter Capacitor	5 F	
$R_{\mathrm{fi}}$	Resistance of $L_{\rm fi}$	0.01	
CSC Power Setup			
MOSFET	Power Switches	SCH2080KE	
DSP	Digital Signal Processor	TMS320C28346	
FPGA	Field Programmable Gate Array	EP3C40F324	
ADC	Analog-to-Digital Converter	ADS8568	
DAC	Digital-to-Analog Converter	AD5754	
$T_{si}$	Input Sampling Time	6.67 s	
$T_{so}$	Output Sampling Time	333/667 s	
	Converter efficiency	≈95.8%	
Output Filter			
$L_{fo}$	Output Filter Inductor	10 mH	
$C_{\rm fo}$	Output Filter Capacitor	200 F	
$R_{\rm fo}$	Resistance of $L_{fo}$	0.1	
Load			
$R_{ m L}$	Load Resistor	30/45	
$u_{\rm L}$ *	Reference load voltage	270 V	

If both the output DBPC and the input FS-MPC were implemented in an input sampling period, the execution time for the whole calculations in the DSP was only about 5.83 s. For the existing methods, which apply FS-MPC to both the input and output circuits, comparable execution time could be achieved if the simplification technique presented in Part 3.3 was adopted. However, as the output DBPC in the proposed scheme was only implemented in every 50 or 100 output sampling periods, the average execution time was lower than 5.83 s. In addition, the proposed scheme did not need any weighting factor. Therefore, the proposed scheme had very low control complexity.

To demonstrate the necessity of a larger output sampling period  $T_{so}$ , two values of  $T_{so}$  were used in both simulation and experiments, which were 333 s (50 times of  $T_{si}$ ) and 667 s (100 times of  $T_{si}$ ) respectively. Although the input FS-MPC operates at the sampling frequency of 150 kHz, the measured average switching frequency of CSC was only about 20 kHz, which is far less than the sampling frequency.

#### 4.2. Simulation Results

The simulation results were obtained and shown in Figure 5. Figure 5a shows the results when the output sampling time  $T_{so}$  was 50 times of  $T_{si}$ , while Figure 5b shows the results when  $T_{so}$  was 100 times of  $T_{si}$ . It is clear that when  $T_{so}$  was small, large ripples were contained in the output current and load voltage, and significant low-order frequency harmonics were contained in source currents, indicating poor power quality. On the contrary, when the output sampling time was increased, the current and voltage ripples were suppressed effectively and highly sinusoidal source currents were obtained. The simulation results demonstrated the necessity for using much larger output sampling time than input sampling time.



**Figure 5.** Simulation results of CSC with the proposed control scheme at the nominal conditions: (**a**) the output sampling time  $T_{so}$  was 333 s and (**b**)  $T_{so}$  was 667 s.

#### 4.3. Experimental Results

The steady-state experimental results are shown in Figure 6. Figure 6a shows the results when the output sampling time  $T_{so}$  was 50 times of  $T_{si}$ , while Figure 6b shows the results when  $T_{so}$  was 100 times of  $T_{si}$ . It can be seen that in both cases, the source current  $i_{sA}$  approaches sinusoidal, and ripples of the load voltage and output current were relatively small. This indicates that the proposed hybrid predictive control scheme worked properly to achieve the desired control objectives. Yet, there were still differences between the waveform quality in the two cases, which was clearer from the waveforms of reference values. When  $T_{so}$  was 333 s, significant low-frequency ripples in  $u_0^*$ ,  $i_0^*$  and  $p_s^*$  were observed, leading to the distorted waveform of reference source current  $i_{sA}^*$ . On the contrary,  $u_0^*$ ,  $i_0^*$  and  $p_s^*$  were almost constant values and  $i_{sA}^*$  was purely sinusoidal when  $T_{so}$  was 667 s, which were the reasons for the higher waveform quality in this case. Figure 6 indicates that the output sampling time should be large enough to achieve satisfactory power quality.



**Figure 6.** Steady-state experimental waveforms of source voltage  $u_{sA}$ , source current  $i_{sA}$ , load voltage  $u_L$ , output current  $i_o$ , reference output voltage  $u_o^*$ , reference output current  $i_o^*$ , reference source active power  $p_s^*$  and reference source current  $i_{sA}^*$ : (**a**) the output sampling time  $T_{so}$  was 333 s; and (**b**)  $T_{so}$  was 667 s.

The spectral analysis results of the source current  $i_{sA}$  and output current  $i_o$  at the steady-state are shown in Figure 7. It is found that in both cases the total harmonic distortions (THDs) of  $i_{sA}$  and  $i_o$  were very small with no harmonic content higher than 1.0% observed. Yet, more low-frequency harmonics were contained in  $i_{sA}$  and  $i_o$  when  $T_{so}$  was 333 s, with THDs up to 3.49% and 3.33% separately. With the increased output sampling time, the low-frequency harmonics were suppressed, with THDs reduced to 2.42% and 2.72% separately. This is another evidence for the necessity of higher output sampling time for the proposed control scheme.



**Figure 7.** Spectral analysis results of source current  $i_{sA}$  and output current  $i_0$ : (**a**) the output sampling time  $T_{so}$  was 333 s and (**b**)  $T_{so}$  was 667 s.

When the source frequency varied between 350 Hz and 800 Hz, THD analysis results of source current  $i_{sA}$  and output current  $i_o$  are shown in Figure 8a,b respectively. It can be seen that the proposed scheme could always obtain satisfactory power quality with THDs lower than 5.0%, even when the source frequency varied in a very wide range. In addition, with output sampling time  $T_{so}$  set as 667 s, the input and output power quality were better with THDs less than 3.0%. These results demonstrated the superior steady-state performance obtained by the proposed control scheme.



**Figure 8.** Total harmonic distortions (THDs) of source current  $i_{sA}$  and output current  $i_o$  when the source frequency varies between 350 Hz and 800 Hz: (a) THD of  $i_{sA}$  and (b) THD of  $i_o$ .

The dynamic results with the proposed scheme are shown in Figure 9, when the load resistor changed from 30 to 45. It could be found that the load voltage  $u_L$  was rarely disturbed by the variable load whether the output sampling time  $T_{so\neg}$  was 333 s or 667 s, which proved that the proposed scheme could suppress the effect of load variation on the load voltage. Yet, the performance of the source and output currents are quite different in the two cases. It is clear that with smaller  $T_{so}$ , more oscillations were observed in the currents during the dynamic process. This was because the input control could not respond to the demand of active power promptly. On the contrary, with larger  $T_{so}$ , the dynamic oscillations were suppressed effectively, and the source and output currents reached the steady-state quickly and smoothly.



**Figure 9.** Dynamic response of the proposed scheme when the load resistor changes from 30 to 45: (a) the output sampling time  $T_{so}$  was 333 s and (b)  $T_{so}$  was 667 s.

# 5. Conclusions

For the current source converter used in the aircraft DC MG, an output LC filter was necessary. In such an application, the proposed hybrid predictive control scheme fully utilized the technique of predictive control to operate the converter. By adopting the output deadbeat predictive control and input finite-set model predictive control, the usage of the PI controller and weighting factor was eliminated. The input control was also simplified by eliminating the source current predictions. Overall, the proposed scheme exhibited very low control complexity, which created a capability to work under high sampling frequency (up to 150 kHz). The steady-state and dynamic experimental results obtained on a SiC-MOSFET-based prototype demonstrated the superior performance of the proposed control scheme, even under very high and variable source frequency (360–800 Hz).

Realization of the power sharing in multi-supplies mode should be one of future work. For example, the typical droop control can be incorporated in the predictive control scheme. In this case, the steady-state error and low-frequency ripple could be important issues since they may cause the failure of droop control.

Author Contributions: Conceptualization, J.L. and H.Y.; Methodology, J.L. and K.W.; Software, C.W.; Validation, C.W. and K.W.; Formal analysis, R.T.; Investigation, K.W.; Resources, J.L. and S.F.; Data curation, W.W.; Writing—original draft preparation, R.T.; Writing—review and editing, S.F.; Visualization, C.W.; Supervision, H.Y., J.L., S.F.; Project administration, W.W. and S.F.; Funding acquisition, S.F., J.L. and H.Y.

**Funding:** This work was supported in part by the National Natural Science Foundation of China under Grant 51807025 and in part by the Natural Science Foundation of Jiangsu Province of China under Grant BK20180396 and BK20170674.

Conflicts of Interest: The authors declare no conflict of interest.

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