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Voltage Balance Switching Scheme for Series-Connected SiC MOSFET LLC Resonant Converter

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Abstract: To achieve high efficiency and power density, silicon carbide (SiC)-based Inductor-Inductor-Capacitor (LLC) resonant converters are applied to the DC/DC converter stage of a solid-state transformer (SST). However, because the input voltage of an SST is higher than the rated voltage of a commercial SiC device, it is essential to connect SiC devices in series. This structure is advantageous in terms of voltage rating, but a parasitic capacitance tolerance between series-connected SiC devices causes voltage imbalance. Such imbalance greatly reduces system stability as it causes overvoltage breakdown of SiC device. Therefore, this paper proposes a switching scheme to solve the voltage imbalance between SiC metal-oxide-semiconductor field-effect transistors (MOSFETs). The proposed scheme sequentially turns off series-connected SiC MOSFETs to compensate for the turn-off delays caused by parasitic capacitor tolerances. In addition, dead-time selection methods to achieve voltage balance and zero voltage switching simultaneously are provided in detail. To verify the effectiveness of the proposed scheme, experiments were conducted on a 2 kW series-connected SiC MOSFET LLC resonant converter prototype.

Keywords: series-connected SiC MOSFETs; voltage balancing; solid-state transformer; LLC resonant converter

1. Introduction

Due to the recent interest in smart grid, distributed power system, and renewable energy, researches have been actively conducted to replace large and heavy line-frequency transformers. A solid-state transformer (SST) proposed as a solution is a power converter that converts the magnitude or type of voltage using a power semiconductor and a high-frequency transformer [1–4]. As shown in Figure 1, an SST consists of an AC/DC rectifier stage, a DC/DC converter stage, and a DC/AC inverter stage. In particular, the DC/DC converter stage enables DC voltage conversion, high power density, and galvanic isolation by using a high-frequency transformer. The most commonly used topology for the DC/DC converter stage is a dual active bridge (DAB) [5–8], which exhibits characteristics of galvanic isolation and high power density, and can achieve zero-voltage switching (ZVS) without additional circuit. However, due to a high turn-off current, the turn-off loss is large and it is difficult to guarantee ZVS under light load conditions. In addition, it is difficult to achieve high efficiency over a wide load range because of the large conduction losses caused by circulating current. At the same time, an Inductor-Inductor-Capacitor (LLC) resonant converter has very low switching losses because it guarantees ZVS of the switches and zero-current switching (ZCS) of the rectifier diodes from no load to full load. As a result, operating at high switching frequencies, the size of passive elements and transformers can be reduced, which allows for high power density. Therefore, research has been conducted to replace DAB converters with LLC resonant converters to

improve the efficiency and power density of DC/DC converter stage [3,9–12]. However, silicon (Si)-based LLC resonant converters still exhibit high conduction and turn-off losses, making it difficult to design for high frequencies and power [3,9,10].

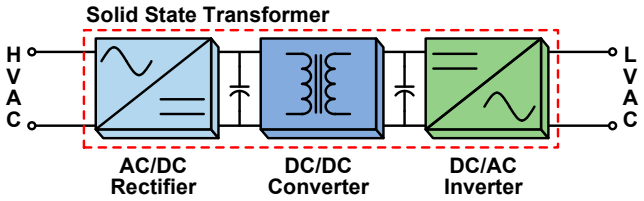


Figure 1. The block diagram of solid-state transformer.

To overcome the physical limitations of Si materials, researches are being conducted actively on wide-bandgap (WBG) materials such as silicon-carbide (SiC) and gallium-nitride (GaN). WBG materials have a very thin drift layer because they have a higher dielectric breakdown field than Si materials. As a result, WBG devices have a low on-resistance and reverse recovery loss [13–16]. Therefore, much effort is being put in to apply WBG devices to LLC resonant converters to achieve high efficiency and power density [17–21].

Among WBG devices, GaN devices typically have low voltage ratings of less than 600 V and hence SiC devices, which have relatively higher voltage ratings, are suitable for high-voltage applications. Although technological advances in SiC devices have greatly improved their voltage rating, they are still not a perfect replacement for Si devices. Thus, in the case of an SST where very high voltage ratings are required, it is essential to connect SiC devices in series [22–25]. However, connecting SiC devices in series may cause voltage imbalance due to a parasitic capacitor tolerance between them, which causes overvoltage breakdown of the device. In particular, SiC devices have a very small parasitic capacitor as their drift layers are thinner than those of Si devices [26], which causes a large voltage imbalance even with small parameter tolerances.

To solve voltage imbalance problems caused by the series connection, a number of methods have been proposed. Snubber circuits are the simplest way to resolve voltage imbalance [22–25,27]. These circuits can reduce voltage and current stress and switching losses, as well as voltage imbalances [23,24,27]. However, snubber circuits not only decrease the switching speed and power density but also reduce power conversion efficiency due to additional losses. In [22,25], a parameter optimization design was proposed to minimize snubber losses, but the optimal design of parameters is complicated.

In the active voltage control (AVC) method, the drain-source voltage of the switch is directly controlled [28–36]. In [28–30], a temporary clamp technique is proposed to eliminate the voltage imbalance. In [31–36], voltage imbalance was eliminated by adjusting the gate signal timing of series-connected switches. However, the gate driver circuit is enlarged by the AVC circuit, and these methods do not solve voltage imbalance during the transient [28–30]. In addition, it takes several milliseconds to solve voltage imbalance. Therefore, it is difficult to apply the methods to WBG devices operating at high frequency [31–36].

Quasi-active gate control (QAGC) [37,38] is a combination of snubber circuits and the AVC method. This method has the advantage that the number of additional devices is small and the circuit is simple. However, as the number of series-connected switches increase, the voltage balancing performance is greatly reduced and the parameter design is complicated.

Gate current control [39–43] eliminates voltage imbalance by controlling the gate charge or discharge current. This method, however, complicates the gate driver circuit due to additional components [39,40] and reduces the switching speed by limiting the gate current. In addition, very high current control bandwidth is required for fast response speed [41–43].

To overcome these problems, a gate signal delay control has been proposed in [44]. The advantage of this method is that no voltage balancing circuit is required, which implies no additional losses or power density reduction. In addition, this method enables voltage balancing through simple

gate signal adjustment even when the operating point changes. However, analysis of several series-connected switches is insufficient, and the analysis of problems that occur during turn-on when applying this method is not provided.

This paper proposes a switching scheme to solve the voltage imbalance in series-connected SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) LLC resonant converter without any additional circuitry. The proposed scheme sequentially turns off series-connected SiC MOSFETs to compensate for the turn-off delay caused by parasitic capacitor tolerances. A detailed analysis of the effect of input and output parasitic capacitance differences on voltage imbalance is presented. In addition, a dead-time analysis considering the junction capacitors of the rectifier diode is provided to achieve both voltage balance and ZVS. The effectiveness of the proposed scheme is verified experimentally using a 2 kW series-connected SiC MOSFETs LLC resonant converter prototype.

2. Series-Connected SiC-MOSFET LLC Resonant Converter

2.1. System Description

Figure 2 shows a series-connected SiC-MOSFET LLC resonant converter circuit. The circuit consists of a half-bridge converter with a split-capacitor, resonant tank, and center tap rectifier. V_{in} represents the input voltage of the bridge, C_{ds1} and C_{ds2} are split capacitors, respectively, Q_1–Q_8 are SiC-MOSFETs, and their output capacitances are expressed as C_{oss1}~C_{oss8}. Switches Q_1–Q_4 are connected in series with each other and they are turned on and off at the same time. The same is true for switches Q_5–Q_8. In addition, Q_1–Q_4 and Q_5–Q_8 operate complementary to each other. The resonant tank consists of the resonant capacitor C_r, leakage inductor of the transformer L_r, and magnetizing inductor of the transformer L_m. The center tap rectifier consists of rectifier diodes D_1 and D_2, an output capacitor C_o, and a load resistor R_L where C_{j1} and C_{j2} denote junction capacitances of the rectifier diodes.

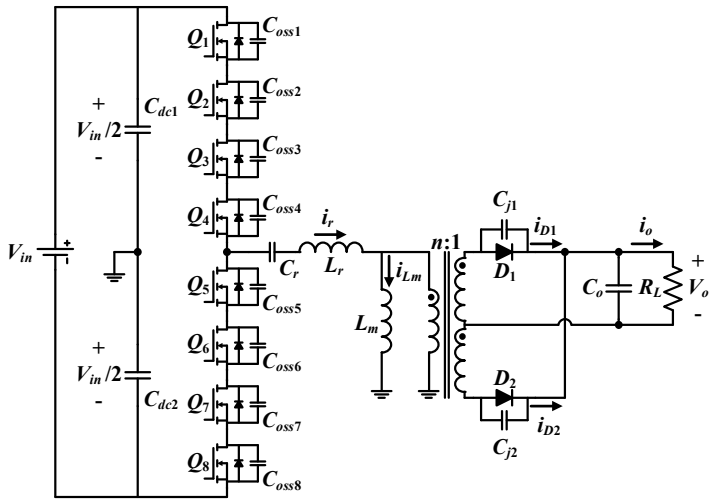


Figure 2. Circuit diagram of the series-connected silicone carbide (SiC)-MOSFETs LLC resonant converter.

2.2. Operating Principle

Figures 3 and 4 show the main waveforms of the series-connected SiC MOSFET LLC resonant converter and the equivalent circuit for each mode, respectively. To simplify analysis, it is assumed that the parasitic capacitances of the switches are the same and circuit operation is steady-state. The operation is divided into ten modes during the switching period.

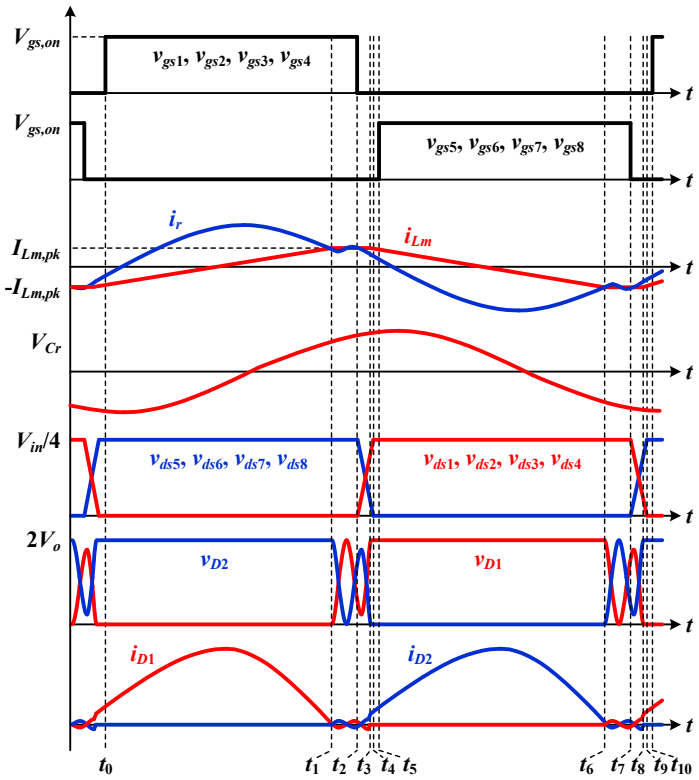
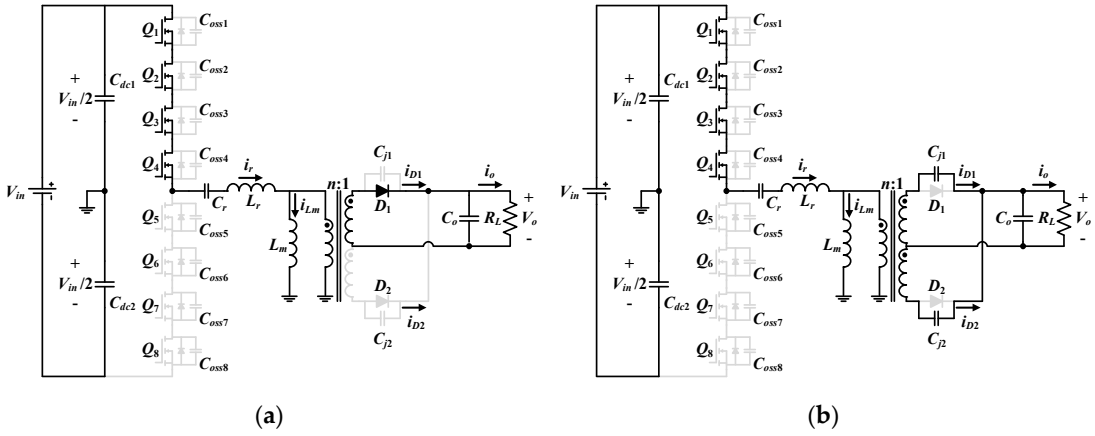
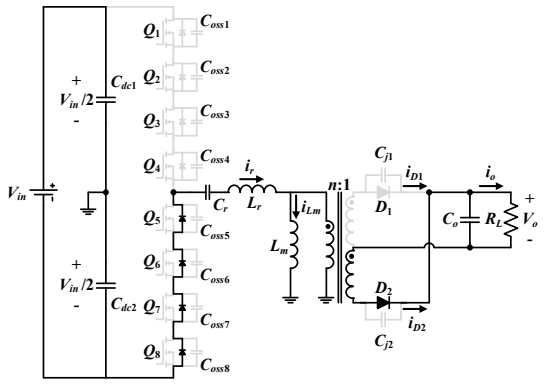


Figure 3. Operational waveforms of the LLC resonant converter.





(**e**)

Figure 4. Equivalent circuits for each mode: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5.

Mode 1 [$t_0 < t < t_1$]: At t_0, Q_1–Q_4 are turned on at the same time and Mode 1 is initiated. In this mode, L_r and C_r participate in resonance. L_m does not participate in resonance because it is clamped by the output voltage. A resonance current i_r flows through Q_1–Q_4. i_r is larger than the magnetizing inductance current i_{Lm} and energy is transferred to the load through the rectifier diode D_1. This mode ends when i_r equals i_{Lm}. During this mode, i_r, i_{Lm}, and the voltage of the resonant capacitor v_{Cr} can be expressed as follows

$$i_r(t) = i_r(t_0) \cdot \cos\omega_{r1}(t - t_0) + \frac{V_a}{Z_1}\sin\omega_{r1}(t - t_0) \tag{1}$$

$$i_{Lm}(t) = \frac{V_{op}}{L_m}t + i_{Lm}(t_0) \tag{2}$$

$$v_{Cr}(t) = Z_1 i_r(t_0) \cdot \sin\omega_{r1}(t - t_0) - V_a\cos\omega_{r1}(t - t_0) + \frac{V_{in}}{2} - V_{op} \tag{3}$$

where $\omega_{r1} = 1/\sqrt{(L_r C_r)}$ is the resonant angular frequency, $Z_1 = \sqrt{(L_r/C_r)}$ is the characteristic impedance, n is the turn ratio of transformer, $V_{op} = nV_o$ is the output voltage converted to the transformer primary side, and $V_a = V_{in}/2 - V_{op} - V_{cr}(t_0)$.

Mode 2 [$t_1 < t < t_2$]: This mode starts when the linearly increasing i_{Lm} becomes equal to i_r. At this time, the rectifier diodes D_1 and D_2 do not conduct, and junction capacitances C_{j1} and C_{j2} participate in resonance. L_m also participates in resonance as it is no longer clamped by the output voltage. Therefore, the resonant capacitor C_r, resonant inductor L_r, magnetizing inductor L_m, and junction capacitances of the rectifier diodes C_{j1} and C_{j2} form a resonant tank. Assuming that L_m is larger than L_r and that the interval of this mode is sufficiently short relative to the switching period, the magnitude of i_{Lm} is constant [45]. This mode ends when Q_1–Q_4 are turned off. During this mode, i_r, i_{Lm}, and v_{Cr} can be expressed as follows

$$i_r(t) = \left[i_r(t_1) - \frac{I_{Lm,pk}C_{eq1}}{C_{jp}}\right]\cos\omega_{r2}(t - t_1) + \frac{V_b}{Z_2}\sin\omega_{r2}(t - t_1) + \frac{I_{Lm,pk}C_{eq1}}{C_{jp}} \tag{4}$$

$$i_{Lm}(t) = I_{Lm,pk} = \frac{nV_o}{L_m}\frac{T_s}{4} \tag{5}$$

$$v_{Cr}(t)=\frac{1}{C_r\omega_{r2}}\left[i_r(t_1)-\frac{I_{Lm,\mathrm{pk}}C_{eq1}}{C_{jp}}\right]\sin\omega_{r2}(t-t_1)-\frac{V_b}{Z_2C_r\omega_{r2}}\cos\omega_{r2}(t-t_1)+\frac{I_{Lm,\mathrm{pk}}C_{eq1}}{C_{jp}C_r}t+\frac{V_a}{Z_1C_r\omega_{r2}}+v_{Cr}(t_2) \tag{6}$$

where T_s is the switching period, n is transformer turn ratio, $\omega_{r2}=1/\sqrt{(L_rC_{eq1})}$ is the resonant angular frequency, $Z_2=\sqrt{(L_r/C_{eq1})}$ is the characteristic impedance, $C_{jp}=2C_{j1}/n^2$ is the total junction capacitance of the rectifier diode converted to the transformer primary side, $C_{eq1}=C_r\|C_{jp}$, and $V_b=V_{in}/2-V_{op}-V_{cr}(t_1)$.

Mode 3 [$t_2<t<t_3$]: This mode starts when Q_1–Q_4 are turned off. In this mode, output capacitances C_{oss1}–C_{oss8} and junction capacitances, C_{j1} and C_{j2}, are charged or discharged by i_{Lm}. This mode ends when C_{j1} and C_{j2} are fully charged and discharged, respectively. During this mode, i_r, i_{Lm}, and v_{Cr} can be expressed as follows

$$i_r(t)=\left[i_r(t_2)-\frac{I_{Lm,pk}C_{eq2}}{C_{jp}}\right]\cos\omega_{r3}(t-t_2)+\frac{V_c}{Z_3}\sin\omega_{r3}(t-t_2)+\frac{I_{Lm,pk}C_{eq2}}{C_{jp}} \tag{7}$$

$$i_{Lm}(t)=I_{Lm,pk}=\frac{nV_o}{L_m}\frac{T_s}{4} \tag{8}$$

$$v_{Cr}(t)=\frac{1}{C_r\omega_{r3}}\left[i_r(t_2)-\frac{I_{Lm,\mathrm{pk}}C_{eq2}}{C_{jp}}\right]\sin\omega_{r3}(t-t_2)-\frac{V_c}{Z_3C_r\omega_{r3}}\cos\omega_{r3}(t-t_2)+\frac{I_{Lm,\mathrm{pk}}C_{eq2}}{C_{jp}C_r}t+\frac{V_c}{Z_3C_r\omega_{r3}}+v_{Cr}(t_2) \tag{9}$$

where $\omega_{r3}=1/\sqrt{(L_rC_{eq2})}$ is the resonant angular frequency, $Z_3=\sqrt{(L_r/C_{eq2})}$ is the characteristic impedance, $C_{oss,eq}=C_{oss1}/2$ is the total output capacitance of the switches, $C_{eq2}=C_{oss,eq}\|C_r\|C_{jp}$, and $V_c=V_{in}/2-V_{op}-V_{cr}(t_2)$.

Mode 4 [$t_3<t<t_4$]: At t_3, the rectifier diode D_1 is turned off and D_2 is turned on. Thus, the energy stored in the magnetizing inductor is not fully used to charge and discharge output capacitances; instead, a part of it is transferred to the load through D_2. This mode ends when C_{oss1}–C_{oss4} are fully charged and C_{oss5}–C_{oss8} are fully discharged. During this mode, i_r, i_{Lm}, and v_{Cr} can be expressed as follows

$$i_r(t)=i_r(t_3)\cos\omega_{r4}(t-t_3)+\frac{V_d}{Z_4}\sin\omega_{r4}(t-t_3) \tag{10}$$

$$i_{Lm}(t)=-\frac{V_{op}}{L_m}t+i_{Lm}(t_3) \tag{11}$$

$$v_{Cr}(t)=\frac{i(t_3)}{C_r\omega_{r4}}\sin\omega_{r4}(t-t_3)-\frac{V_d}{Z_4C_r\omega_{r4}}\cos\omega_{r3}(t-t_3)+\frac{V_d}{Z_4C_r\omega_{r4}}+v_{Cr}(t_3) \tag{12}$$

where $\omega_{r4}=1/\sqrt{(L_rC_{eq3})}$ is the resonant angular frequency, $Z_4=\sqrt{(L_r/C_{eq3})}$ is the characteristic impedance, $C_{eq3}=C_{oss,eq}\|C_r$, and $V_d=V_{in}/4+V_{op}-V_{cr}(t_3)$.

Mode 5 [$t_4<t<t_5$]: At t_4, the output capacitance is fully charged or discharged and this mode starts. In this mode, all the switches are off but the body diodes of Q_5–Q_8 start to conduct due to the continuity of the resonant current i_r. Therefore, the drain-source voltage of Q_5–Q_8 is equal to the forward voltage of its body diode; this ensures that ZVS conditions are achieved. This mode ends when Q_5–Q_8 are turned on. At this time, if resonant current i_r flows in the positive direction, Q_5–Q_8 are ZVS turned on. During this mode, i_r, i_{Lm}, and v_{Cr} can be expressed as follows

$$i_r(t) = i_r(t_4)\cos\omega_{r1}(t-t_4) + \frac{V_e}{Z_1}\sin\omega_{r1}(t-t_4) \tag{13}$$

$$i_{Lm}(t) = -\frac{V_{op}}{L_m}t + i_{Lm}(t_4) \tag{14}$$

$$v_{Cr}(t) = Z_1 i(t_3)\sin\omega_{r1}(t-t_4) - V_e\cos\omega_{r1}(t-t_4) + V_{op} - V_{in}/2 \tag{15}$$

where $V_e = V_{op} - V_{cr}(t_4) - V_{in}/2$.

Because the operation principle of Mode 6 to Mode 10 is similar to that of Mode 1 to Mode 5, a detailed description of these modes is omitted here.

3. Analysis of Voltage Imbalance in the Series-Connected SiC MOSFET LLC Resonant Converter

In this section, the effect of parasitic capacitance differences of series-connected switches on their turn-on and turn-off switching characteristics is discussed.

3.1. Turn-On Switching Characteristics

As shown in Figure 3, during Mode 3 and Mode 4, Q_5–Q_8 are off, and C_{oss5}–C_{oss8} are discharged by i_r. Because it is assumed that all parasitic capacitances of the switches are equal, the drain-source voltages V_{ds} of Q_5~Q_8 simultaneously decreases to zero. If C_{oss5}~C_{oss8} are different, their V_{ds} values decrease at different rates. These rates are inversely proportional to the output capacitance and can be calculated as follows

$$\Delta Q = C_{oss}\cdot\Delta V_{ds} \tag{16}$$

where ΔQ is the incremental change in the charge supplied by the resonant current, C_{oss} is the output capacitance of the switch, and ΔV_{ds} is the incremental change in the drain-source voltage of the switch.

Figure 5 shows the turn-on switching transient waveforms when C_{oss5}–C_{oss8} satisfy the following inequality:

$$C_{oss5} < C_{oss6} = C_{oss7} = C_{oss8}\,. \tag{17}$$

According to Equations (16) and (17), the drain-source voltage of switch Q_5, which has the smallest output capacitance, decreases most rapidly. Figure 6a shows the switch discharge situations during Interval 1. Because v_{ds5} is not fully discharged, the body diode of Q_5 does not conduct. Figure 6b shows the switch discharge situations during Interval 2. Once v_{ds5} is completely discharged, the body diode of Q_5 conducts due to continuity of the current. Those switches that are not yet fully discharged are discharged by the resonant current. v_{ds5} is clamped to the body diode forward voltage V_f until all the switches are fully discharged. Therefore, during turn-on transient, differences in the output capacitance do not cause voltage spikes.

As shown in Figure 6c, the body diodes of all switches are conducting when Q_5–Q_8 are fully discharged. Because v_{ds} of the switches is clamped to V_f, all the switches achieve ZVS conditions and differences in the input capacitance of the switches do not substantially affect v_{ds}. Thus, when ZVS turn-on is achieved, input and output capacitance differences between the series-connected switches do not cause problems during turn-on switching transients.

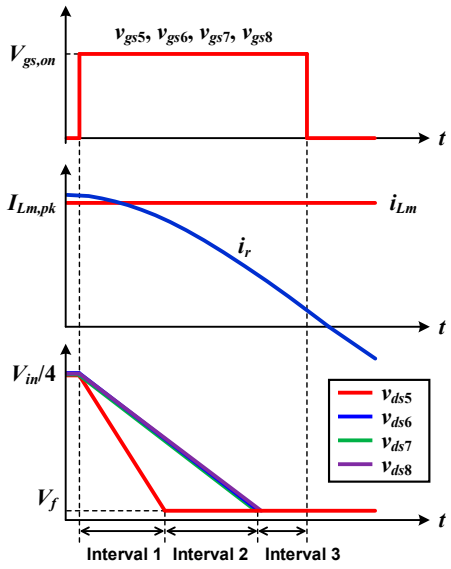


Figure 5. Turn-on switching transient waveforms.

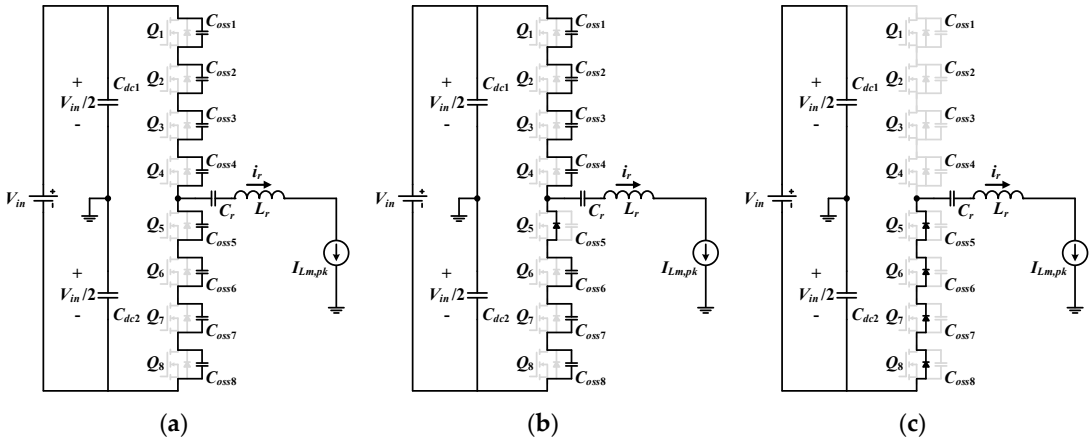


Figure 6. Equivalent circuits during turn-on switching transient: (**a**) Interval 1; (**b**) Interval 2; (**c**) Interval 3.

3.2. Turn-Off Switching Characteristics

The drain-source voltage imbalance caused by the parasitic capacitance difference in the series-connected switches during the turn-off switching transients is discussed in this section. Figure 7 shows the turn-off switching waveforms of the gate signal v_{sig}, gate-source voltage v_{gs}, and drain-source voltage v_{ds} of the switches with different input capacitance C_{iss} or output capacitance C_{oss} value. Figure 7a shows the turn-off switching waveforms when the input capacitance C_{iss1} of switch Q_1 is larger than the input capacitances C_{iss2}–C_{iss4} of switches Q_2–Q_4. Although turn-off signals are simultaneously applied at t_{a1}, v_{gs} decreases at different rates because the input capacitances are different. In other words, v_{gs1} of switch Q_1 decreases slowly and it takes longer to decrease from the gate-source turn-on voltage $V_{gs,on}$ to the threshold voltage V_{th}. In this case, the turn-off delay caused by the difference in input capacitance can be expressed as [44,46]

$$\Delta t_{d1} = R_g \left(C_{iss1} - C_{iss2} \right) \ln \left(\frac{V_{gs,on}}{V_{th}} \right) \tag{18}$$

where R_g denotes a gate resistor.

As can be seen in Figure 7a, even though the output capacitance C_{oss} of series-connected switches is equal, their v_{ds} rises at different time due to the time delay shown in Equation (18). Thus, a difference in input capacitance causes voltage imbalance. In this case, the steady-state voltage ratios of Q_1–Q_4 follow the relationship

$$v_{ds1} : v_{ds2} : v_{ds3} : v_{ds4} = \frac{\Delta t_{d2}}{C_{oss1}} : \frac{\Delta t_{d1} + \Delta t_{d2}}{C_{oss2}} : \frac{\Delta t_{d1} + \Delta t_{d2}}{C_{oss3}} : \frac{\Delta t_{d1} + \Delta t_{d2}}{C_{oss4}} \tag{19}$$

where Δt_{d2} is the time taken for v_{ds1} to reach steady-state from zero voltage under different input capacitance condition.

By assumption, the output capacitances are equal. Using Equation (19), the magnitude of voltage imbalance due to input capacitance tolerance is calculated as

$$\left| v_{ds2} - v_{ds1} \right| = \left| \frac{V_{in} \Delta t_{d1}}{3\Delta t_{d1} + 4\Delta t_{d2}} \right|. \tag{20}$$

Figure 7b shows the turn-off switching waveforms when the output capacitance C_{oss1} of switch Q_1 is larger than the output capacitances C_{oss2}–C_{oss4} of switches Q_2–Q_4. At t_{a1}, the turn-off signal is applied, and v_{gs} decreases at the same rate.

At t_{a2}, v_{gs} reaches V_{th} and v_{ds} increases. Because C_{oss1} is larger than C_{oss2}–C_{oss4}, v_{ds1} increases slowly, which causes a voltage imbalance. In this case, the steady-state voltage ratios of Q_1–Q_4 and the magnitude of voltage imbalance due to output capacitance tolerance are calculated as

$$v_{ds1} : v_{ds2} : v_{ds3} : v_{ds4} = \frac{\Delta t_{d3}}{C_{oss1}} : \frac{\Delta t_{d3}}{C_{oss2}} : \frac{\Delta t_{d3}}{C_{oss3}} : \frac{\Delta t_{d3}}{C_{oss4}} \tag{21}$$

$$\left| v_{ds2} - v_{ds1} \right| = \left| \frac{C_{oss1} - C_{oss2}}{3C_{oss1} + C_{oss2}} V_{in} \right| \tag{22}$$

where Δt_{d3} is the time taken for v_{ds1} to reach steady-state from zero voltage under different output capacitance condition.

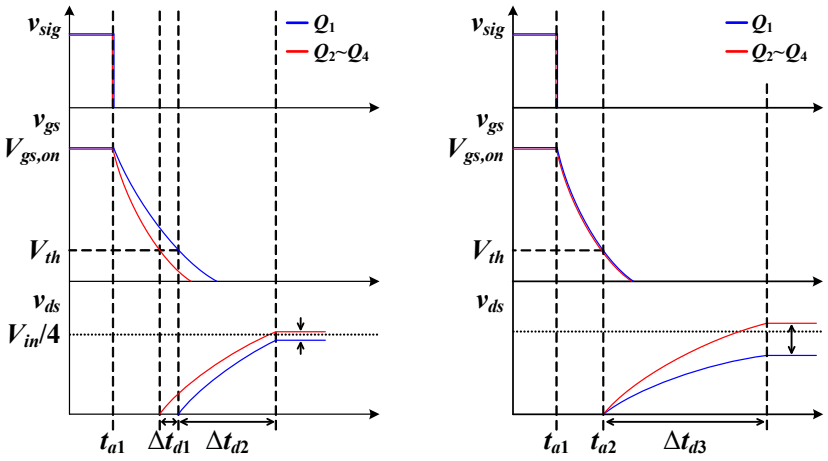


Figure 7. Turn-off switching waveforms: (**a**) with different input capacitances C_{iss}; (**b**) with different output capacitances C_{oss}.

4. Proposed Switching Scheme

In this section, a gate signal compensation method is proposed to overcome the voltage imbalance caused by discrepancies between the parasitic capacitances of series-connected switches.

To simplify analysis, it is assumed that the parasitic capacitances of all switches, except Q_1, are equal and the parasitic capacitances of Q_1 are larger than those of Q_2–Q_8.

Figure 8 shows the operation principle of the proposed switching scheme. As discussed in Section 3, when the proposed switching scheme is not applied, switch Q_1, which has a large parasitic capacitance, causes voltage imbalance. In this case, the steady-state voltage ratios of Q_1–Q_4 and the magnitude of voltage imbalance due to input and output capacitance tolerance are calculated as

$$v_{ds1} : v_{ds2} : v_{ds3} : v_{ds4} = \frac{\Delta t_{d4}}{C_{oss1}} : \frac{\Delta t_{d1} + \Delta t_{d4}}{C_{oss2}} : \frac{\Delta t_{d1} + \Delta t_{d4}}{C_{oss3}} : \frac{\Delta t_{d1} + \Delta t_{d4}}{C_{oss4}} \tag{23}$$

$$\left| v_{ds2} - v_{ds1} \right| = \left| \frac{\left(C_{oss1} - C_{oss2} \right) \Delta t_{d4} + C_{oss1} \Delta t_{d1}}{\left(3C_{oss1} + C_{oss2} \right) \Delta t_{d1} + 3C_{oss1} \Delta t_{d1}} V_{in} \right| \tag{24}$$

where Δt_{d4} is the time taken for v_{ds1} to reach from zero voltage to steady-state value under different input and output capacitance condition.

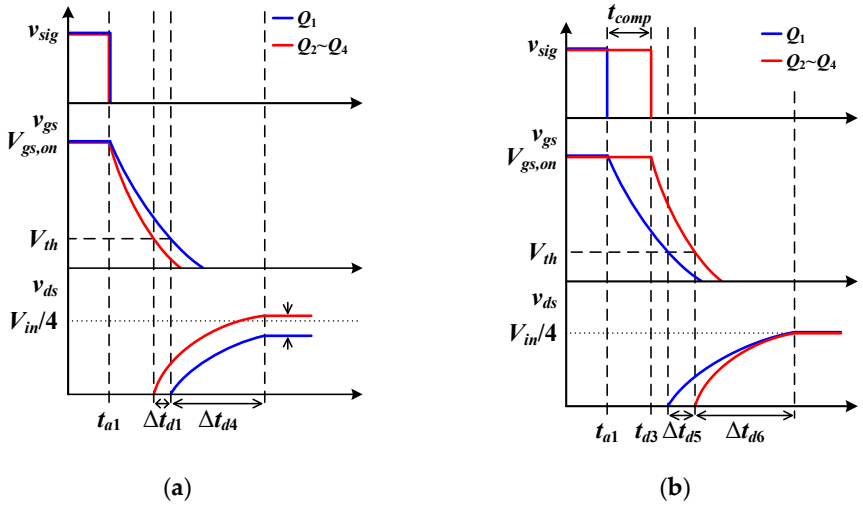


Figure 8. Turn-off switching waveforms: (**a**) without proposed switching scheme; (**b**) with proposed switching scheme.

Figure 8b shows the turn-off switching waveforms when the proposed scheme is applied. This scheme solves voltage imbalance by sequentially turning off switches with a large parasitic capacitance. This scheme ensures time for v_{ds} of the switch with a large parasitic capacitance to increase to $V_{in}/4$. As shown in Figure 8b, t_{comp} is required to compensate for the turn-off delay and it can be calculated as follows

$$t_{comp} = \Delta t_{d1} + \Delta t_{d5} \tag{25}$$

where Δt_{d1} and Δt_{d5} represent the time taken for v_{gs} to reach from $V_{gs,on}$ to V_{th} without and with the proposed switching scheme, respectively. Δt_{d1} is the time delay caused by input capacitance tolerance and it is constant in Equation (18), regardless of whether the proposed scheme is applied or not. Therefore, Δt_{d5} must be calculated to derive the gate signal compensation time. The magnetizing current is constant during turn-off switching transient by assumption. The best case is when the voltages of the series-connected switches are $V_{in}/4$ and this relationship is expressed as

$$\frac{V_{in}}{4} = \frac{\Delta t_{d6}}{C_{oss2}} I_{Lm,pk,H} = \frac{\Delta t_{d5} + \Delta t_{d6}}{C_{oss1}} I_{Lm,pk,H} \tag{26}$$

$$I_{Lm,pk,H} = \frac{C_{oss,H}}{C_{oss,H} + C_{oss,L}} I_{Lm,pk} \tag{27}$$

where $I_{Lm,pk,H}$ is the magnitude of current that charges the upper switches of the half-bridge during the dead-time and $C_{oss,H}$ and $C_{oss,L}$ are the total output capacitance of the upper and lower switches, respectively.

Using Equation (25), Δt_{d5} can be calculated as follows:

$$\Delta t_{d5} = \frac{C_{oss1} - C_{oss2}}{4I_{Lm,pk}} V_{in}. \tag{28}$$

5. Design Considerations for Achieving ZVS

In this section, the dead-time design process for achieving ZVS is analyzed. As discussed earlier, the LLC resonant converter achieves ZVS from no load to full load. However, some constraints must be met to achieve ZVS, one of which can be expressed as

$$I_{Lm,pk} \cdot t_{dead} \geq \sum_{i=1}^{8} \left(C_{oss1} \Delta V_{ds,i} \right) \tag{29}$$

where t_{dead} denotes dead-time [45,47].

Equation (29) indicates that charge supplied by the magnetizing current $I_{Lm,pk}$ should be larger than the charge necessary for fully charging and discharging the output capacitance of all switches in the dead-time. However, Equation (29) assumes that $I_{Lm,pk}$ is used only to charge or discharge the output capacitance to achieve ZVS during the dead-time, so it is not valid when considering the junction capacitance of the rectifier diode.

Figure 9 shows the equivalent circuit during dead-time. The magnetizing inductor is represented as a current source by assumption. During the dead-time, $I_{Lm,pk}$ charges or discharges the output capacitances of switches and junction capacitances of rectifier diodes. Therefore, if the dead-time is selected using Equation (29), ZVS cannot be achieved because v_{ds} is fully discharged. In this paper, a resonant current i_r is used instead of a magnetizing current for accurate dead-time design.

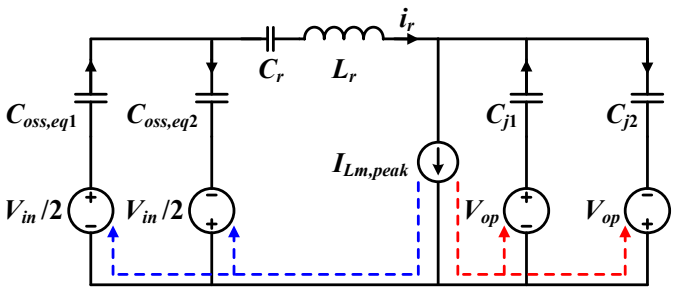


Figure 9. Equivalent circuit during dead-time.

Referring to Figure 3, the resonant current during dead-time can be approximated as

$$i_r(t) \approx f(t) = i_r'(t_2)(t - t_2) + i_r(t_2) \tag{30}$$

where

$$i_r'(t_2) = \frac{V_c \omega_{r3}}{Z_3} = \frac{V_c}{L_r} < 0 \tag{31}$$

$$i_r(t_2) = I_{Lm,pk}. \tag{32}$$

Because charge Q_{ir} supplied by the resonant current is equal to the area below $i_r(t)$ during the dead-time, it is obtained as

$$Q_{ir} = \frac{t_{dead}}{2}\left[I_{Lm,pk} + \left\{ \frac{V_c}{L_r} t_{dead} + I_{Lm,pk} \right\} \right] = t_{dead}\left(I_{Lm,pk} + \frac{V_c}{2L_r} t_{dead} \right) \tag{33}$$

Assuming that C_{oss1}–C_{oss8} are equal, using Equations (29) and (33), the dead-time constraint for achieving ZVS is derived as follows:

$$\frac{V_c}{2L_r}\left(t_{dead}\right)^2 + I_{Lm,pk} t_{dead} \geq \frac{C_{oss1} V_{in}}{2}. \tag{34}$$

Using Equation (31), the lower limit of t_{dead} is obtained as

$$t_{dead} \geq -\frac{L_r I_{Lm,pkc}}{V_c}\left\{ 1 + \sqrt{1 + \frac{V_c V_{in} C_{oss1}}{L_r \left(I_{Lm,pk} \right)^2}} \right\}. \tag{35}$$

Using Equation (35), it is possible to calculate the ZVS condition taking into account C_j. However, Equation (32) does not consider the parasitic capacitance tolerance at all. When the parasitic capacitances of individual switches are different, the lowest dead-time limit to achieve both ZVS and voltage balance is obtained as follows

$$t_{dead,i} \geq -\frac{L_r I_{Lm,pkc}}{V_c}\left\{ 1 + \sqrt{1 + \frac{2V_c V_{in} C_{oss,tot}}{L_r \left(I_{Lm,pk} \right)^2}} \right\} + t_{comp,i} \tag{36}$$

where $t_{dead,i}$ is the dead-time of switch Q_i, $C_{oss,tot}$ is the sum of C_{oss1}–C_{oss8}, and $t_{comp,i}$ is the gate signal compensation time of switch Q_i calculated using Equation (25).

The other constraint for achieving ZVS is related to turn-on switching. If the dead-time selected is too long and the direction of i_r is changed before the gate signal is applied, ZVS cannot be achieved. When i_r changes direction, the output capacitor being charged begins to discharge and vice versa. The ZVS constraint reflecting the above phenomenon is expressed as follows:

$$i_r\left(t_5\right) = i_r\left(t_4\right)\cos\omega_{r1}\left(t_{dead} + t_2 - t_4\right) + \frac{V_e}{Z_1}\sin\omega_{r1}\left(t_{dead} + t_2 - t_4\right) \geq 0. \tag{37}$$

Using Equation (37), the dead-time constraint is derived as follows

$$t_{dead} \leq \frac{\arctan\phi}{\omega_{r1}} + t_{low,lim} \tag{38}$$

where

$$\phi = -\frac{Z_1 i_r\left(t_4\right)}{V_e} \tag{39}$$

$$t_{low,lim} = -\frac{L_r I_{Lm,pk}}{V_c}\left\{ 1 + \sqrt{1 + \frac{2V_c V_{in} C_{oss,tot}}{L_r \left(I_{Lm,pk} \right)^2}} \right\}. \tag{40}$$

Using Equations (36) and (38), the dead-time range to achieve both ZVS and voltage balance is derived as follows:

$$t_{low,lim} + t_{comp,i} \leq t_{dead} \leq \frac{\arctan\phi}{\omega_{r1}} + t_{low,lim}. \tag{41}$$

6. Experimental Results

To verify the effectiveness of the proposed switching scheme, a series-connected SiC-MOSFET LLC resonant converter was implemented as shown in Figure 10. The equivalent circuit is shown in

Figure 2 and the design parameters are listed in Table 1. A Rohm 1.2 kV SiC MOSFET (SCH2080KE) was used for the series-connected switches and gate signals were generated by a Texas Instruments TMS320F28377D DSP board.

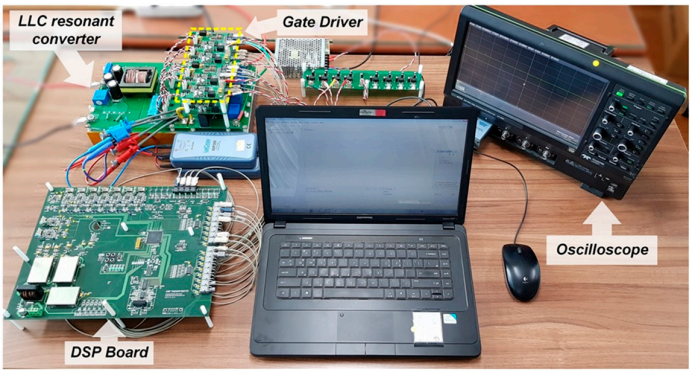


Figure 10. Test setup for series-connected SiC-MOSFETs LLC resonant converter.

Table 1. Component parameters of the test setup.

Symbol	Quantity	Value (Unit)
V_{in}	Input voltage	600–800 (V)
f_{r1}	Resonant frequency	100 (kHz)
f_s	Switching frequency	86.6 (kHz)
L_m	Magnetizing inductor	873 (μH)
L_r	Resonant inductor	135 (μH)
C_r	Resonant capacitor	11 (nF)
n_p:n_{s1}:n_{s2}	Transformer turns ratio	44:8:8

Figure 11 shows the drain-source voltage waveforms of the upper switches Q_1–Q_4 under different input voltage conditions. As discussed in Section 3, input and output capacitance tolerance causes a voltage imbalance between series-connected switches. Switch Q_4, which has the smallest parasitic capacitance, blocks higher voltage when compared to the other switches. V_{ds4} blocks 34.5%, 35%, and 37% of V_{in} at input voltages of 600 V, 700 V, and 800 V, respectively.

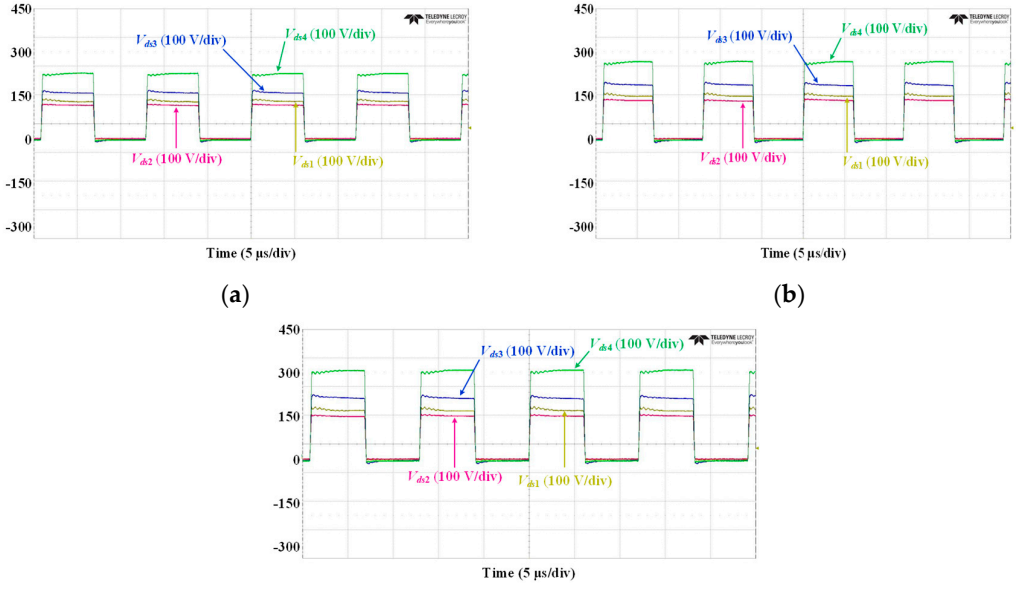


Figure 11. Experimental results with series-connected SiC MOSFETs without the proposed method: (**a**) V_{in} = 600 V; (**b**) V_{in} = 700 V; (**c**) V_{in} = 800 V.

Figure 12 shows the drain-source voltage waveforms of the upper switches when the proposed switching scheme is applied. Voltage imbalance is solved by turning off switches with a large parasitic capacitance in sequence. The gate signal compensation time is calculated using Equations (25) and (41).

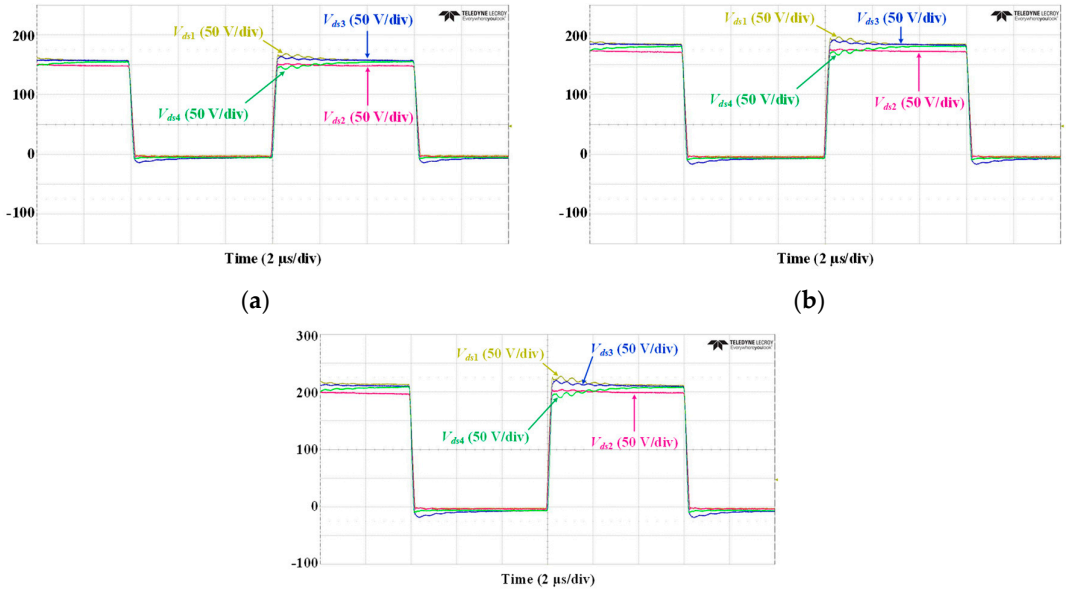


Figure 12. Experimental results with series-connected SiC MOSFETs with the proposed method: (**a**) V_{in} = 600 V; (**b**) V_{in} = 700 V; (**c**) V_{in} = 800 V.

Figure 13 compares the drain-source voltage of series-connected switches at different input voltages. Approximately 35% of the input voltage is applied to switch Q_4. Therefore, this switch has a risk of overvoltage breakdown. However, after using the proposed scheme, approximately 25 % of the input voltage is applied to switch Q_4. In addition, voltage imbalance between the series-connected switches is also significantly reduced.

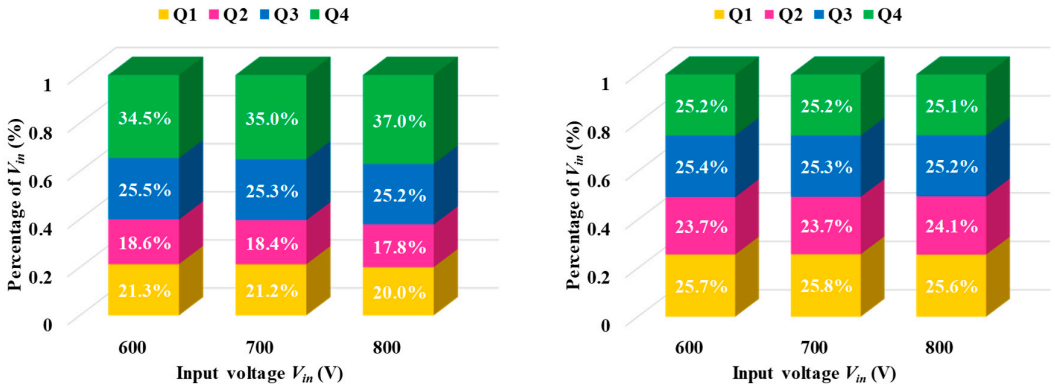


Figure 13. Comparison of the drain-source voltage of series-connected switches at different input voltages: (**a**) without the proposed scheme; (**b**) with the proposed scheme.

Figure 14 shows the maximum voltage imbalance between the series-connected switches. Parasitic capacitance tolerances cause a voltage imbalance of 101–158 V. However, after applying the proposed method, the maximum voltage imbalance reduced by 90% to 12–15 V.

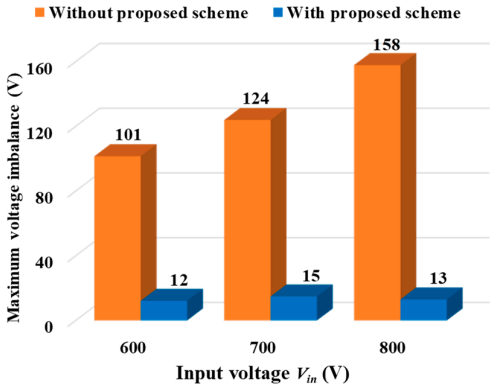


Figure 14. Comparison of the maximum voltage imbalance between the series-connected switches at different input voltages.

7. Conclusion

This paper proposes a switching scheme to overcome voltage imbalance in series-connected SiC MOSFET LLC resonant converter. The proposed method eliminates voltage imbalance by sequentially turning off switches with a large parasitic capacitance. Furthermore, we analyzed the effect of parasitic capacitance on voltage imbalance in detail. The procedure for calculating the gate signal compensation time was provided. In addition, to achieve both voltage balance and ZVS turn-on, dead-time design constraints were derived. In order to verify the effectiveness of the proposed method, experimental results were presented at various input voltages. Compared to series-connected switches in which the proposed method was not applied, voltage imbalance reduced by 91% at 800 V after applying the proposed method.

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