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A Novel Autonomous Current-Sharing Control Strategy for Multiple Paralleled DC–DC Converters in Islanded DC Microgrid

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Received: 2 September 2019; Accepted: 15 October 2019; Published: 17 October 2019

Abstract: Due to the existence of line impedances and low-bandwidth communication, the traditional peer-to-peer control method based on droop control has difficult meeting the requirements of current sharing and voltage stability in islanded DC microgrids at the same time. In this paper, a novel current-sharing control strategy based on injected small ac voltage with low frequency and low amplitude is proposed for multiple paralleled DC–DC converters. The small ac voltage is superimposed onto the output voltage of each converter. Then, the reactive circulating power is generated and used to regulate the output DC voltage of each converter. Under the droop characteristic between the injected frequency and output DC current, a feedback mechanism is generated to realize the accurate current sharing. On this basis, a reactive power-voltage limiter link and virtual negative impedance are added. Under the interaction of the two links, the bus voltage drop caused by line impedances can be almost completely eliminated. This method does not need any communication or to change the hardware structure. The controller design process is presented in detail along with a system stability analysis. Finally, the feasibility and effectiveness of the proposed control strategy are validated by the results obtained from simulations and experiments.

Keywords: DC microgrid; current sharing control; injected ac voltage; bus voltage regulation; virtual negative impedance

1. Introduction

As an effective means of application of distributed generation technology, microgrid has attracted more and more attention in recent years [1–3]. A microgrid generally consists of several renewable energy resources, storage systems, loads, and electronics devices. Due to the diversity and decentralization of distributed energy, power converters are usually used to connect them in order to realize energy conversion and management. How to achieve parallel operation, accurate load current sharing between power converters, and maintain stability has become a research hotspot in microgrids [4–22]. With the increasing demand of DC power at load side and the rapid development of distributed DC power sources such as photovoltaic cells, wind power, storage batteries, fuel cells, and supercapacitors, the research on DC microgrids has been gradually increasing in recent years [7–9]. Nowadays, DC microgrids have been preliminarily applied in independent power supply systems such as marine power systems, aerospace systems, and data centers [10–12].

In islanded DC microgrids, DC–DC converters are widely used for the distributed generations to connect the common bus. To study the parallel operation problem of distributed generations is essentially to study the current sharing control of multiple paralleled DC–DC converters. Accurate current sharing between paralleled converters and no deviation regulation for bus voltage

are two important control objectives in islanded DC microgrid [13–23]. At present, the current-sharing strategies that are most commonly used are master–slave control and peer-to-peer control.

In reference [13], a master–slave control method based on current-mode controlled dc-dc converters was proposed to maintain power balance of the parallel system. A power generation module is selected as the master module to stabilize bus voltage, and the other modules divide current equally according to the bus voltage and inject energy into the load in the form of current sources. The work in [14] proposed a master–slave control strategy based on adaptive multi-master power supply. When the load power changes, the distributed generations switch to the master control module in turn and adaptively adjust their own operation mode and output power. Reference [15] set up a central controller based on a multiagent system to adjust the output of each unit. By controlling the frequency oscillation of each agent, the controller minimizes the production cost of the whole interconnected system. The master–slave control methods are simple and easy to implement, but the whole system has a strong dependence on the master unit. Meanwhile, due to the existence of high-speed communication, the distance between generation units is limited. If the master unit or the communication failure occurs, the system may collapse.

When the peer-to-peer control is adopted, every unit in the system has the same status and can control itself through local information. High-speed communication is not required, so it is easy to implement the function of "plug and play". Now, the peer-to-peer control methods have become the research mainstream, among which, droop control is the most widely applied. The V-I droop method based on virtual impedance is usually adopted in DC microgrid. The introduction of virtual resistance can change the equivalent impedance of the power converter, and reduce the impedance difference caused by line impedance, so as to improve the load current sharing accuracy. This method does not need any communication, but its droop characteristics would cause serious voltage drop, and the uncertain line impedance would also affect the current sharing accuracy. Then, some optimization methods with variable droop coefficients were proposed [16–18]. According to the output current range, voltage deviation information, and the defined droop index of the converter, the optimal value of virtual impedance is calculated and then different droop coefficients are set to optimize the current sharing among the micro-sources. However, the above methods can not directly determine the droop coefficients, which are difficult to coordinate with each other if the number of micro-sources is large. So, these methods have no generality. The work in reference [19] changed the research idea. The droop curves are shifted by changing the reference voltages, not by changing the droop coefficients. This method can realize the current sharing among multi-converters and control the DC bus voltage within the allowable range. However, similar to the methods of variable droop coefficients, it is difficult to coordinate the variations of reference voltages when the number of converters in parallel is large. Based on this, hierarchical control methods based on low-bandwidth communication were proposed in references [20–24]. The primary control layer of converters follow the traditional virtual impedance droop control, and larger droop coefficients are selected to ensure the accuracy of power sharing. The secondary control layer is used to compensate the bus voltage drop by adjusting the droop curve. In the early stage of microgrid research, the related literatures usually adopted the centralized hierarchical control method. The information of each converter is transmitted to the central controller through low-speed communication, and then the compensation signal is sent to the primary layer of each converter through secondary control [20]. However, the centralized hierarchical control depends on the central controller. Once the central controller has problems, the whole system would fail or even collapse. In order to overcome the problem above, the concept of distributed hierarchical control was proposed. The secondary control layer is embedded in the bottom controller of each converter, so that every converter in the microgrid can be regarded as a relatively independent agent [21–24]. References [21,22] achieved the sharing of all local information through a global low-speed communication network, then the secondary control calculates the required control values based on the above information. References [23,24] combined the idea of autonomous decentralization. Each generation unit only needs to communicate with its neighboring units, after a certain number

of iterations, the target parameters converge to the average value. These methods greatly improved the contradiction between power sharing accuracy and bus voltage drop. However, the existence of a communication network would bring stability, redundancy, and cost problems to the microgrid, especially in the case of operating many sources along long feeders.

After that, some distributed control strategies, in which the units inject sinusoidal signals of specific frequency into the common bus, were proposed instead of the communication [25–30]. In references [25,26], the power line signaling (PLS) was used to transmit the frequency signals and realize the cooperation of multiple converters. The merit is prominent since the power network is the only communication medium. However, PLS is more complex to be implemented and it is not conducive to the expandability of the system. In references [27,28], a small ac signal, whose frequency is controlled by the harmonic power, was injected into the output voltage of each inverter as a control signal. Then, the active power produced by the injected signal was detected and utilized to adjust the virtual impedance at terminal of each distributed generation (DG) unit. Similar to AC microgrid, in references [29,30], the method with ac signal injection was used in a DC microgrid. The small frequency signal was superimposed onto the output voltage of each converter, and then the dc output voltage can be adjusted through the reactive power generated by the superimposed ac voltages. This method can improve the load current sharing accuracy, but it does not consider the bus voltage drop caused by line impedances. When the line impedance or the line impedance deviation is large, the bus voltage drop is still very serious. Besides, the principle of accurate power sharing under the injection method was not analyzed.

In order to overcome the bus voltage drop caused by line impedances, as well as to obtain the current sharing objectives, a novel current-sharing control strategy for multiple paralleled DC–DC converters is proposed. A small ac voltage, whose frequency is related to output current, is superimposed onto the output DC voltage of each converter. Then, the reactive circulating power would be generated in the parallel system and be used to regulate the output DC voltage of each converter. Under the feedback mechanism, the accurate current sharing can be realized. On this basis, an improved autonomous bus voltage regulation method is used to compensate bus voltage drop by adding limiter link and virtual negative impedance. In the proposed approach, every converter can locally carry out the load current sharing and the voltage regulation without utilizing communication network, which leads to reliable and flexible operation.

The rest of this paper is organized as follows: In Section 2, the proposed current sharing control strategy based on injected small ac voltage is discussed in detail. In Section 3, the autonomous bus voltage regulation strategy based on limiter link and virtual negative impedance is performed. The small signal modeling, as well as the stability analysis, is given in Section 4. Then, the simulation and experiment results under various working conditions are presented to verify the effectiveness of the proposed control strategy in Sections 5 and 6, respectively. Finally, the achievements are summarized in Section 7.

2. Current-Sharing Control Approach Based on Injected AC Voltage

2.1. Overall Description

A simplified dc microgrid structure in islanding mode, which is composed of distributed power sources, energy storage units, power converters, and various types of loads, is shown in Figure 1. In this paper, only the operation mode in which multiple converters are connected in parallel to maintain the bus voltage is considered. The PV source would be integrated into the bus by maximum power point tracking control, and it can be considered as a special constant power load whose output power is negative and stochastic because of its similar external characteristics with constant power load [31].

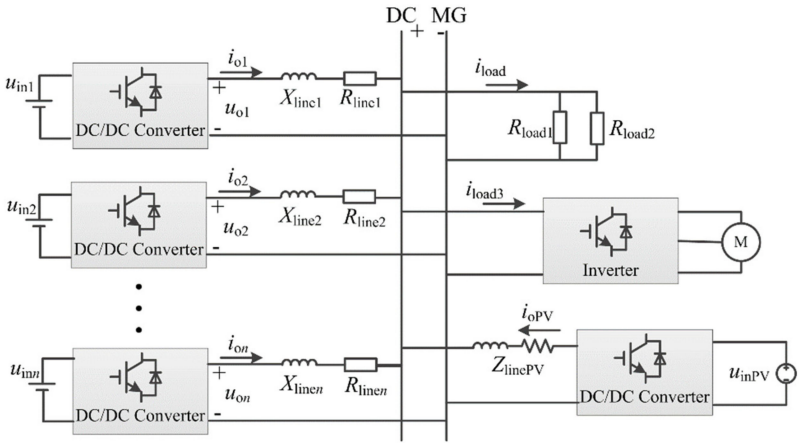


Figure 1. DC microgrid simplified structure with multiple distributed generations.

In traditional ac microgrids, power converter-based units are coordinated together with a frequency-droop controller as well [2,4,5]. There is a variable frequency, which can be controlled globally. By controlling the frequency droop, good current-sharing accuracy can be ensured. However, there is no global variable in dc microgrids. Voltage-based droop approaches rely on the dc link voltage, where the dc link voltage is a local variable and it does not have the same value through the microgrid to coordinate the different converters. So, the traditional droop methods usually have poor performance regarding the current-sharing accuracy. Based on this, in order to improve the current-sharing accuracy, a new control approach based on the frequency injection method is proposed. The proposed control structure for the *k*th converter is shown in Figure 2.

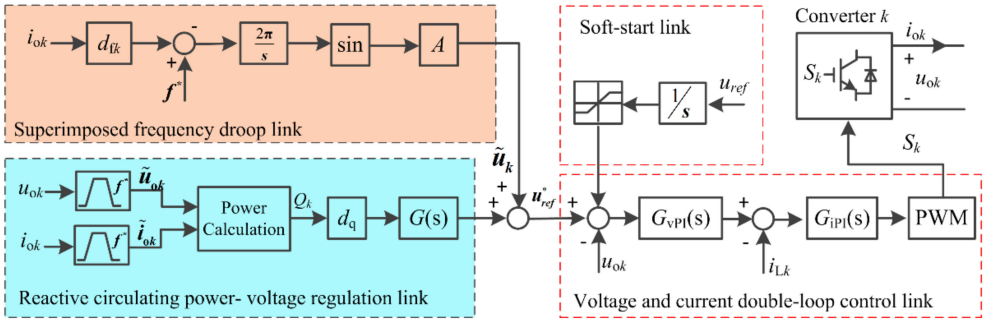


Figure 2. Proposed current sharing control structure based on injected small ac voltage.

The control structure of each converter has four parts: soft-start link, double-loop control link, superimposed frequency droop link, and reactive power-voltage regulation link. The soft-start link adopts ramp boost mode to realize a smooth start of the DC/DC converter. Double-loop control link is used for the nonerror control of the output voltage. In the last two links, the reactive circulating power generated by the injected ac voltage is used to regulate the dc output voltage of each converter, thus realizing the current sharing.

2.2. Injected ac Small Voltage Analysis

As shown in Figure 2, the injected small ac voltage for converter k (k = 1, 2, … N) can be represented as

$$\widetilde{u}_k = A\mathbf{sin}(2\pi f_k t) \tag{1}$$

where A is the ac voltage amplitude, and its value should be not too small or too large. If too small, it can't be detected without distortion by the measuring unit. If too large, the output voltage ripple would exceed the allowable range. In general, the value of A should not exceed 2.5% of the rated

DC output voltage, so the load voltage ripple would not exceed 5%. When the load voltage ripple requirement is high, the value of A should be as small as possible.

The frequency $f_{\ k}$ should be proportional to the output dc current I_{ok} of converter k, and satisfy the following droop characteristics:

$$f_k = f^* - d_{\mathbf{f}k} I_{\mathbf{o}k} \tag{2}$$

in which f^* is the rated frequency of ac voltage, d_{fk} is the frequency current droop coefficient of converter k, and its value meets the following restriction:

$$d_{\mathbf{f}k} \le \frac{f^* - f_{\mathbf{min}}}{I_{\mathbf{N}k}} \tag{3}$$

where $f_{\min}$ is the allowed minimum frequency, and here, $f_{\mathbf{min}}$=0.9f^*, $I_{\mathbf{N}k}$ is the output rated dc current of converter k.

For simplicity, a dc microgrid with two converters is considered. When in the steady state, the two converters should have the same frequency, so the following relationship can be derived from Equation (2).

$$\frac{d_{\mathbf{f2}}}{d_{\mathbf{f1}}} = \frac{I_{\mathbf{o1}}}{I_{\mathbf{o2}}} = \lambda = \frac{I_{\mathbf{N1}}}{I_{\mathbf{N2}}} \tag{4}$$

where λ represents the rated power ratio of two converters, $I_{\mathbf{N1}}$ and $I_{\mathbf{N2}}$ are the output rated dc currents of the two converters. For converters with different rated power, the relationship between d_{f} should meet the requirements of Equation (4).

According to Figure 2 and Equation (2), the ac component phase angles of the two converters can be obtained.

$$\varphi_1 = \frac{2\pi}{s}(f^* - d_{\mathbf{f1}} I_{\mathbf{o1}}) \tag{5}$$

$$\varphi_2 = \frac{2\pi}{s}(f^* - d_{\mathbf{f2}} I_{\mathbf{o2}}). \tag{6}$$

Then, the phase difference φ can be obtained as follow:

$$\varphi = \varphi_1 - \varphi_2 = \frac{2\pi}{s}(d_{\mathbf{f2}} I_{\mathbf{o2}} - d_{\mathrm{f1}} I_{\mathbf{o1}}). \tag{7}$$

As shown in Equation (7), the phase angles are related to the dc currents, if the output currents are not proportional to their rated power, the phase difference between the ac components would occur, and cause a reactive power flow. Considering the load impedance is much higher than the line impedances, the reactive power can be approximated as flowing only between converters. Meanwhile, the output dc currents can also be controlled by the dc voltages. Hence, the dc currents, the dc voltages, and the reactive circulating power can be connected together, and the reactive circulating power can be used to adjust the output dc voltage to realize accurate load current sharing. The detailed process analysis will be described in Section 2.3.

It must be noted that the DC/DC converter consisting of voltage and current double-loop controller is essentially equivalent to a low-pass filter. In order to ensure that the small ac voltage can be superimposed on dc output voltage without error, the influence of inductance, capacitance, and PI parameters should be considered comprehensively. Therefore, the injected frequency should be much less than the bandwidth of the double-loop controller. Meanwhile, if the injected frequency is too low, it obviously would affect the system dynamic performance. In this paper, like an AC microgrid, 50 Hz was selected as the rated frequency of the injected ac voltage. The reason for frequency selection is explained in the Appendix A.

2.3. Process Analysis of Reactive Power-Voltage Regulation

Figure 3a shows the ac simplified model of two parallel converters, where $Z_{line1} = R_{line1} + jX_{line1}$ and $Z_{line2} = R_{line2} + jX_{line2}$ represent the line impedance of the two converters, respectively. In a low-voltage DC microgrid, the inductance component X_{line} of line impedance is usually very small, so it is neglected here and only the resistive component R_{line} is considered.

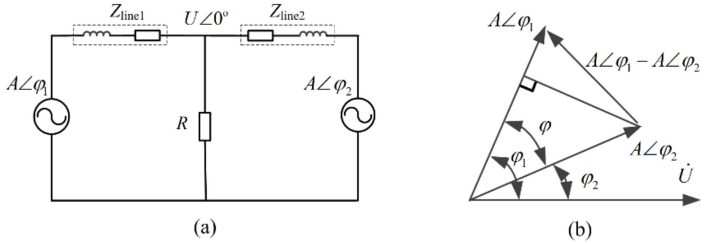


Figure 3. AC model and phasor diagram of two parallel converters: (**a**) AC model; (**b**) phasor diagram.

Assuming that the load resistance R is much larger than the line resistive component $R_{\mathbf{line}}$, the reactive circulating power can be calculated by the phasor diagram method, as shown in Figure 3b.

$$Q_1 = -\frac{A^2}{2(R_{\mathbf{line1}} + R_{\mathbf{line2}})}\mathbf{sin}\varphi \tag{8}$$

$$Q_2 = \frac{A^2}{2(R_{\mathbf{line1}} + R_{\mathbf{line2}})}\mathbf{sin}\varphi \tag{9}$$

where φ is the phase difference between the two converters.

As shown in Figure 2, the DC component of output voltage can be written as

$$U_{\mathbf{o}k} = U^*_{\mathbf{ref}} - d_{\mathbf{q}}Q_k G(\mathbf{s}) \tag{10}$$

where d_q is the reactive power compensation coefficient, $G(s)$ is a low-pass filter for eliminating high-frequency disturbances and improving stability, and $G(s) = \omega_c/(s + \omega_c)$.

Assuming that the two converters have the same power rating, and $R_{\mathbf{line1}} > R_{\mathbf{line2}}$. At the initial moment, because the output voltages of the converters are equal, the output current I_{o1} will be less than I_{o2}. Then, the control process of the parallel system is shown in Figure 4. According to Equation (2), the injected frequency $f_1 > f_2$, so the phase difference between the ac components would be generated. Then, combining the Equations (8) and (9), the reactive circuiting power would be generated, and $Q_1 < 0$, $Q_2 > 0$. Finally, the reactive power is used to compensate the output voltage of each converter, thus changing the output current, forming negative feedback, and realizing current sharing.

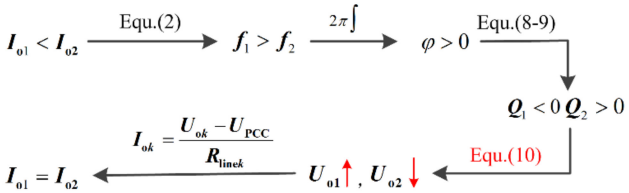


Figure 4. Reactive power-voltage feedback control process diagram.

2.4. Princile of Current Sharing

According to Figure 2 and Equation (10), the dc bus voltage can be obtained as

$$\begin{aligned} U_{\mathbf{PCC}} &= U^*_{\mathbf{ref}} - d_{\mathbf{q}} Q_k G(\mathbf{s}) - I_{\mathbf{o}k} R_{\mathbf{line}k} \\ &= U^*_{\mathbf{ref}} - \left(\frac{d_{\mathbf{q}} Q_k G(\mathbf{s})}{I_{\mathbf{o}k}} + R_{\mathbf{line}k} \right) I_{\mathbf{o}k} \end{aligned} \tag{11}$$

So the total equivalent output impedance of the converter k can be expressed as

$$\hat{R}_k = \frac{d_{\mathbf{q}} Q_k G(\mathbf{s})}{I_{\mathbf{o}k}} + R_{\mathbf{line}k}. \tag{12}$$

When the parallel system with two converters is extended to N converters, the reactive circuiting power will satisfy the following equation, because the load impedance is much larger than the line impedance.

$$\sum_{k=1}^{N} Q_k = 0. \tag{13}$$

The control process of reactive power-voltage negative feedback regulation described in the preceding sections is essentially to adjust the equivalent output impedance of each converter. By compensating the line impedance with reactive circuiting power, the equivalent output impedance $\hat{R}_k$ of each converter satisfies the requirement of current sharing control.

Assuming that the converters have the same power rating, and according to the Equations (12) and (13), the sum of the equivalent output impedance of the converters will be equal to the sum of the total line impedances, just as:

$$\sum_{k=1}^{N} \hat{R}_k = \sum_{k=1}^{N} R_{\mathbf{line}k}. \tag{14}$$

Under the reactive power-voltage negative feedback regulation, the equivalent output impedance $\hat{R}_k$ of each converter will tend to be the same. When the system stabilizes, it will satisfy the following relationship:

$$\hat{R}_1 = \hat{R}_2 = \cdots = \hat{R}_N = \sum_{k=1}^{N} R_{\mathbf{line}k}/N \tag{15}$$

This method makes the equivalent output impedance of each converter equal to the average value of the line impedances. In theory, the accuracy current sharing can be achieved. The feedback mechanism is also applicable to parallel system with different capacity converters. Compared with the traditional voltage droop control, this method not only can improve the current sharing accuracy, but also avoid a secondary drop of bus voltage caused by control strategy. The bus voltage drop is only determined by the average value of all line impedances.

It should be noted here that the capacitance and inductive components in the load are not considered. If considered, a fixed reactive power component would be generated on the load, so that the Equation (13) would equal to a nonzero constant. Combined with the Equations (12)–(15), the equivalent output impedance of each converter would be changed, and its variation would be a constant. In practice, this value is usually small and would not affect the feedback mechanism and the effect of current sharing. However, if the reactive power component in the load is too large, the method would have the risk of failure.

3. Autonomous Bus Voltage Regulation Strategy

When the line impedance and load current are large, the bus voltage drop caused by line impedance can't be ignored. In this section, an improved bus voltage regulation method based on reactive

power-voltage regulation limiter link and virtual negative impedance is proposed, which further reduces the voltage drop caused by line impedances. The control structure is shown in Figure 5.

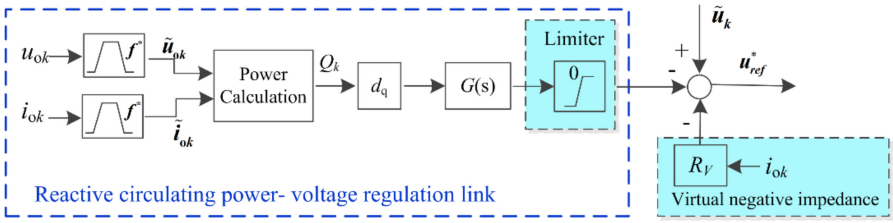


Figure 5. Improved bus voltage regulation method based on limiter link and virtual negative impedance.

3.1. Analysis of Limiter Link

For simplicity, the parallel system with two equal converters is also illustrated, and the control process of the parallel system with limiter link is shown in Figure 6.

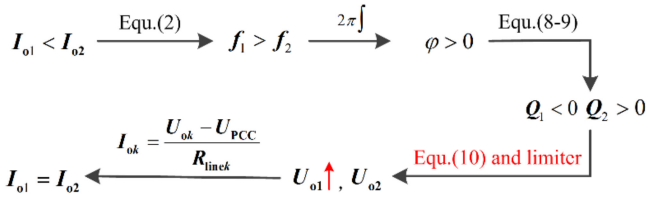


Figure 6. Reactive power-voltage feedback control process diagram with limiter.

Compared with the control method without limiter link, the difference is that if the reactive power is greater than zero, the compensation value will be forced to be zero due to the existence of the limiter link, and then U_{o1} will increase and U_{o2} will not change. Then, I_{o1} will increase with the increase of U_{o1}. The negative feedback can also be formed, and the feedback effect will not be affected by increasing the value of feedback coefficient d_q.

The feedback mechanism can also be extended to the parallel system with multiple converters. Next, the parallel system with three converters will be illustrated briefly. Assuming $R_{line1} > R_{line2} > R_{line3}$, and the sum of Q_1, Q_2, Q_3 is approximately zero. Then there will be two cases at the initial time:

1) $Q_1 < Q_2 < 0$, $Q_3 > 0$

In this case, according to the feedback mechanism with limiter link, U_{o1} and U_{o2} would increase, and $U_{o1} > U_{o2}$, U_{o3} would remain unchanged. Under the feedback mechanism, the system would gradually stabilize.

2) $Q_1 < 0$, $Q_3 > Q_2 > 0$:

In this case, according to the feedback mechanism with limiter link, U_{o1} would increase, and U_{o2} and U_{o3} would remain unchanged. The system is obviously unstable. At this moment, there would inevitably be a new reactive circulating power between converter #2 and #3 because of $R_{line2} \neq R_{line3}$. Under the further action of feedback mechanism, U_{o2} would increase and U_{o3} would remain unchanged. At this time, the reactive circulating between the three converters would form a new balance, and make $Q_1 < Q_2 < 0$, $Q_3 > 0$. Finally, the system would gradually stabilize.

From the above analysis, the line impedance of converter #3 is the smallest and its output voltage remains unchanged, so its equivalent impedance $\hat{R}_3$ is the line impedance R_{line3}. Under the feedback mechanism, the output currents of the three converters tend to be equal. Therefore, according to the requirement of current sharing, the conclusion can be obtained that $\hat{R}_1 = \hat{R}_2 = \hat{R}_3 = R_{\mathbf{line3}}$. In other words, the function of the reactive power-voltage regulation limiter link is essentially to make the equivalent output impedance of each converter tend to become the minimum line impedance.

This principle can obviously be extended to multiple converters with equal power rating. When the parallel system is finally stable, $\hat{R}_k$ would satisfy the following relationship:

$$\hat{R}_1 = \hat{R}_2 = \cdots = \hat{R}_N = R_{\mathbf{line-min}} \tag{16}$$

where $R_{\mathbf{line\text{-}min}}$ represents the minimum value of the line impedances among the parallel converters. The proposed control method with limiter link makes the final equivalent output impedance of the converter change from the average line impedance (Equation (15)) to the minimum value (Equation (16)). This method further restrains the bus voltage droop, especially when the line impedance deviation is large.

3.2. The Selection of Q-U Regulation Coefficient d_q

From the above analysis, it can be seen that the core of the injection method is to compensate the line impedance by reactive power. So the total equivalent output impedance $\hat{R}_k$ in Equation (12) must be able to meet the requirements of compensation. In order to ensure the validity of the injection method, the selection of d_{q} has some limitations. For simplicity, the parallel system with only two equal converters is illustrated.

According to Equations (8), (9), (12), and (16) and Figure 5, when the system is in steady, the relationship can be obtained as follows:

$$\frac{d_{\mathbf{q}} A^2 \mathbf{sin}\varphi}{2(R_{\mathbf{line1}} + R_{\mathbf{line2}}) I_{\mathbf{o}k}} + R_{\mathbf{line}k} = R_{\mathbf{line-min}} \tag{17}$$

where $R_{\mathbf{line}k} \neq R_{\mathbf{line-min}}$ and $\mathbf{sin}\varphi < 0$. Then, it can be derived as

$$d_{\mathbf{q}} A^2 \mathbf{sin}\varphi = -2(R_{\mathbf{line1}} + R_{\mathbf{line2}}) I_{\mathbf{o}k} |R_{\mathbf{line1}} - R_{\mathbf{line2}}|. \tag{18}$$

Therefore, in order to ensure that Equation (18) is always valid and maintains a certain margin, d_{q} should meet the following condition:

$$d_{\mathbf{q}} \geq \frac{2U^*_{\mathbf{ref}}(R_{\mathbf{line1}} + R_{\mathbf{line2}})|R_{\mathbf{line1}} - R_{\mathbf{line2}}|}{A^2 R_{\mathbf{min}}} \tag{19}$$

where $U^*_{\mathbf{ref}}$ is the rated output voltage of the converter, $R_{\mathbf{min}}$ is the minimum load resistance, $U^*_{\mathbf{ref}}/R_{\mathbf{min}} = I_{\mathbf{max}}$ represents the maximum load current.

3.3. Virtual Negative Impedance

From the analysis of Section 3.1, it can be seen that how much the control method with limiter link makes the bus voltage drop is entirely dependent on the minimum line impedance of each converter. If the minimum line impedance is large, the bus voltage drop is still serious. In order to further eliminate voltage drop caused by line impedance, the virtual negative impedance is added to the voltage control link. In order to simplify the analysis, next the parallel system with equal power rating is taken as an example in the following.

Combined with Figure 6 and Equation (16), the dc bus voltage can be deduced:

$$U_{\mathbf{PCC}} = U^*_{\mathbf{ref}} - I_{\mathbf{o}i} R_{\mathbf{line-min}} - I_{\mathbf{o}i} R_{\mathrm{v}} \tag{20}$$

in which i represents the converter with the smallest line impedance and R_{v} is the virtual negative impedance. At this time, as long as the value of $R_{\mathrm{v}} + R_{\text{line-min}}$ is zero, the bus voltage can be adjusted without error. It should be noted that the value of $R_{\mathrm{v}} + R_{\mathbf{line\text{-}min}}$ should not be too small, and only needs to satisfy the requirement of maximum allowable bus voltage drop. This is because if the equivalent output impedance is too small, very small voltage change between parallel converters would also lead

to serious current fluctuations. Therefore, the value of R_v should be determined according to the size of $R_{\mathbf{line\text{-}min}}$, and the basic rules are as follows:

$$R_V = \begin{cases} 0 & (R_{\mathbf{line-min}} < R_{\mathbf{limit}}) \\ R_{\mathbf{limit}} - R_{\mathbf{line-min}} & (R_{\mathbf{line-min}} > R_{\mathbf{limit}}) \end{cases} \tag{21}$$

where R_{limit} represents the maximum allowable equivalent output impedance of the converters, and

$$R_{\mathbf{limit}} = \frac{U^*_{\mathbf{ref}} - U_{\mathbf{PCC-min}}}{I_{\mathbf{o}i}}. \tag{22}$$

The key of this method is how to get the minimum line impedance of the converters. According to Figure 6 and the corresponding analysis, when the system is stable, the output voltage of the converter with the smallest line impedance is the reference given the voltage $U^*_{\mathbf{ref}}$. So the minimum line impedance can be obtained by measuring the bus voltage, that is, the virtual negative impedance can be calculated. Assuming that the measured bus voltage is $U^*_{\mathbf{PCC}}$, then

$$R_{\mathbf{line-min}} = \frac{U^*_{\mathbf{ref}} - U^*_{\mathbf{PCC}}}{I_{\mathbf{o}i}} \tag{23}$$

When the parallel system first runs or the state of power supplies changes, first the value of R_v needs to be set as zero and a certain load in the system needs to be connected, then, after the system is stable, the bus voltage can be measured. Then, the value of R_v can be obtained from the Equations (21)–(23). Due to the fact that the line impedance is usually a fixed value, even if there is parameter drift or estimation error, the influence on bus voltage deviation would not be great. Therefore, only when the parallel system first runs or the state of power supplies changes, does the virtual negative impedance need to be measured and calculated. So in normal operation, the virtual negative impedance is a fixed value.

4. Small Signal Modeling and Stability Analysis

In order to ensure the system stability as well as to design the control system parameters, a small signal model of the parallel system is established in this section. Taking the dc microgrid with two converters as an example, the relationship between the output voltages, output currents, and bus voltage of the converters can be obtained:

$$\begin{cases} U_{\mathbf{o1}} = U_{\mathbf{PCC}} + I_{\mathbf{o1}} R_{\mathbf{line1}} \\ U_{\mathbf{o2}} = U_{\mathbf{PCC}} + I_{\mathbf{o2}} R_{\mathbf{line2}} \\ U_{\mathbf{PCC}} = R(I_{\mathbf{o1}} + I_{\mathbf{o2}}) \end{cases} \tag{24}$$

in which R is the load resistor. The linear form of (24) can be obtained as

$$\begin{cases} \Delta U_{\mathbf{o1}} = \Delta U_{\mathbf{PCC}} + \Delta I_{\mathbf{o1}} R_{\mathbf{line1}} \\ \Delta U_{\mathbf{o2}} = \Delta U_{\mathbf{PCC}} + \Delta I_{\mathbf{o2}} R_{\mathbf{line2}} \\ \Delta U_{\mathbf{PCC}} = \Delta R(I_{10} + I_{\mathbf{20}}) + R_0(\Delta I_{\mathbf{o1}} + \Delta I_{\mathbf{o2}}) \end{cases} \tag{25}$$

where I_{10} and I_{20} are the DC output currents of the two converters at $R = R_0$, $\Delta(.)$ depicts the small variation of each variable.

For convenience of calculation, assume that $R_{\mathbf{line1}} < R_{\mathbf{line2}}$ and ignore the voltage gain caused by the voltage–current double-loop. According to the analysis of Section 3 and the Equations (10)–(12) and (20), the output voltage of each converter can be obtained as:

$$\begin{cases} U_{\mathbf{o1}} = U^*_{\mathbf{ref}} - I_{\mathbf{o1}} R_{\mathbf{V}} \\ U_{\mathbf{o2}} = U^*_{\mathbf{ref}} - d_q Q_2 G(\mathbf{s}) - I_{\mathbf{o2}} R_{\mathbf{V}} \end{cases}. \tag{26}$$

The linear form of Equation (26) can be written as

$$\begin{cases} \Delta U_{\mathbf{o1}} = -\Delta I_{\mathbf{o1}} R_{\mathbf{V}} \\ \Delta U_{\mathbf{o2}} = -d_q \Delta Q_2 G(\mathbf{s}) - \Delta I_{\mathbf{o2}} R_{\mathbf{V}} \end{cases}. \tag{27}$$

From the Equation (9), the small variation of Q_2 can be described as:

$$\Delta Q_2 = k_{\mathbf{q}} \Delta\varphi, k_{\mathbf{q}} = \frac{A^2}{2(R_{\mathbf{line1}} + R_{\mathbf{line2}})} \mathbf{cos}\varphi_{\mathbf{o}} \tag{28}$$

where φ_0 is the steady state value of phase angle difference. According to the Equation (7), the small variation of phase difference can be expressed as:

$$\Delta\varphi = \frac{2\boldsymbol{\pi}}{s}(d_{\mathbf{f2}} \Delta I_{\mathbf{o2}} - d_{\mathbf{f1}} \Delta I_{\mathbf{o1}}). \tag{29}$$

Combining the Equations (4), (25), and (27)–(29), and taking into considering $\Delta\varphi$ as a state variable and ΔR as a disturbance, the state space representation can be obtained as (30).

$$\frac{d^2\Delta\varphi}{d^2 t} + \omega_c \frac{d\Delta\varphi}{dt} + \alpha\Delta\varphi = \beta\omega_c \Delta R + \beta \frac{d\Delta R}{dt} \tag{30}$$

where

$\alpha = \frac{\pi d_{\mathrm{f1}} \omega_c A^2 d_{\mathrm{q}} \cos\varphi_0 [(1+\lambda)R_0 + \lambda(R_{\mathbf{line1}} + R_{\mathrm{V}})]}{\gamma(R_{\mathrm{line1}} + R_{\mathrm{line2}})}$

$\beta = \frac{2\boldsymbol{\pi} d_{\mathbf{f1}} (I_{10} + I_{20}) [R_{\mathbf{line2}} - \lambda R_{\mathbf{line1}} + (1-\lambda) R_{\mathbf{V}}]}{\gamma}$

$\gamma = (R_{\mathbf{line1}} + R_{\mathbf{V}})(R_{\mathbf{line2}} + R_{\mathbf{V}}) + R_0(R_{\mathbf{line1}} + R_{\mathbf{line2}} + 2R_{\mathbf{V}})$.

The characteristic equation for a closed loop system in Laplace domain can be obtained as:

$$s^2 + \omega_c s + \alpha = 0. \tag{31}$$

Then, the root locus of the system can be obtained by introducing the converter parameters into the characteristic equation. Since α is always greater than zero, the Equation (31) would have a pair of conjugate complex roots. Hence, the closed loop system is dynamically stable, and its dynamic performance is mainly affected by ω_c, A^2, d_q, d_{f1}, λ, and R. In order to facilitate analysis, the influence of $A2dqdf1$ on the closed loop system is considered together, because A^2, d_q, and d_{f1} have the same control effects. Figure 7 shows the root locus diagrams with the variation of ω_c, $A^2 d_q d_{f1}$, λ, and R, respectively.

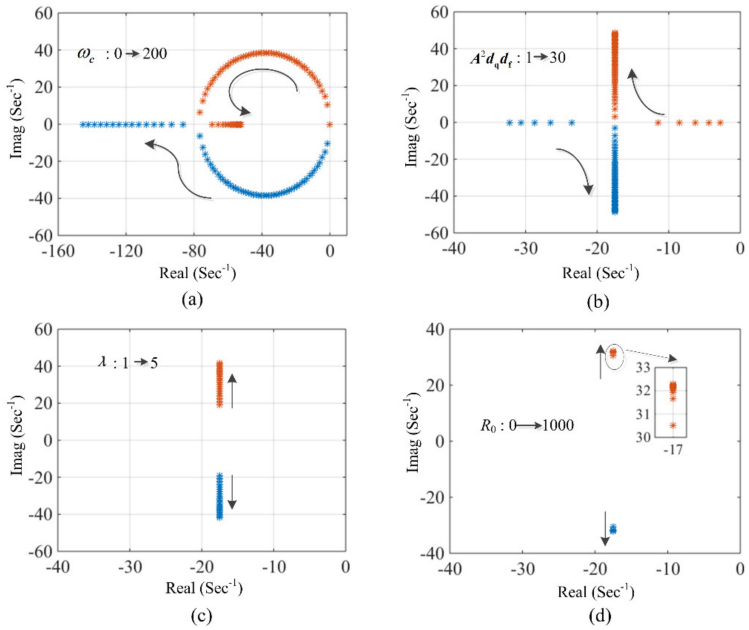


Figure 7. Root locus diagrams with the variation of ω_c, $A^2d_qd_{f1}$, λ, and R_0. (**a**) Effect of $A^2d_qd_f = 15$, $R_0 = 70$, and $\lambda = 1$; (**b**) effect of $R_0 = 70$, $\lambda = 1$, and $\omega_c = 35$ rad/s; (**c**) effect of $A^2d_qd_f = 15$, $R_0 = 70$, and $\omega_c = 35$ rad/s; (**d**) effect of $A^2d_qd_f = 15$, $\lambda = 1$, and $\omega_c = 35$ rad/s.

It can be seen from Figure 7a, the system is a typical second-order system. If ω_c is too small, the poles tend towards an imaginary axis, and the system would become oscillatory and even unstable. If ω_c is too large, the system damping would increase and the adjustment time would be too slow. Here $\omega_c = 35$ rad/s is selected, where the poles of the system would have a pair of conjugate complex roots and the performance would be good. The effort of $A^2d_qd_{f1}$ is demonstrated in Figure 7b. For small $A^2d_qd_{f1}$, one of the poles is near the origin and it affects the system damping performance. So, the selection of $A^2d_qd_{f1}$ in this system should be greater than 5. Of course, the selection of $A^2d_qd_{f1}$ should not to be too large, which would lead to system oscillation. Besides the root locus, the selection of A^2, d_q, and d_{f1} is also influenced by bus voltage ripple, sensor accuracy, converter rated capacity, and so on. The effort with the variation of the rated power ratio λ is shown in Figure 7c. Obviously, when the rated powers are unequal, the system dynamic performance would become worse. Finally, as it can be seen in Figure 7d, the system is not significantly affected by the load variation. Therefore, the performance of the control system at different load conditions is guaranteed.

5. Simulation Results

In order to verify the dynamic and static performance of the proposed control approach, the following three cases were simulated by Matlab/Simulink: 1) three paralleled converters with unequal power rating; 2) two paralleled converters with equal power rating considering the access of the PV converter; 3) two paralleled converters with unequal power rating under the motor-based constant power load. The corresponding circuit and control parameters are shown in Table 1.

Table 1. The parameters of the paralleled DC/DC converters.

Variables	Description	DC#1	DC#2	DC#3	Units
L	converter inductor	1	1	1	mH
C	converter capacitor	1000	1000	1000	μF
U_S	converter input voltage	450	450	450	V
$U^*_{\mathbf{ref}}$	rated output voltage	700	700	700	V
k_{ip}, k_{ii}	current controller PI parameters	0.05 + 1/s	0.05 + 1/s	0.05 + 1/s	
k_{vp}, k_{vi}	voltage controller PI parameters	1.5 + 20/s	1.5 + 20/s	1.5 + 20/s	
R_{line}	line resistance	1	1.5	1.2	Ω
d_q	Q-U regulation coefficient	8	8	8	V/Var
A	injected voltage amplitude	3.5	3.5	3.5	V
f *	rated injected frequency	50	50	50	Hz
ω_c	cut-off frequency	35	35	35	rad/s

5.1. Case I: Three Converters with 1:2:2 Power Rating

In this case, the current sharing performance between three converters with a 1:2:2 power rating was simulated. The initial load power was 7 kW. A 7 kW load was connected at t = 3 s and another 7 kW load was connected at t = 6 s. The frequency-current droop coefficients of the three converters were set as 0.2, 0.1, and 0.1 Hz/A, respectively. Then, the simulation results are shown in Figure 8.

As shown in Figure 8a, the bus voltage consisted of dc voltage and injected ac voltage, in which the amplitude of ac voltage was exactly 3.5 V. When the load changed, the bus voltage could recover independently within 0.3 s, and the steady-state value of dc voltage remained almost unchanged, which is equal to the rated voltage (700 V). Figure 8b,c show the load current and the output current of each converter, respectively. When the load changed, the system dynamic performance was acceptable, and the output currents could be stabilized within 0.4 s. As shown in Figure 8d, in steady state, taking 5 s < t < 6 s as example, the output currents of the three converters were about 4 ± 0.26 A, 8 ± 0.14 A, and 8 ± 0.12 A. The output dc current ratio of the three converters was 1:2:2, so the load was almost proportionately shared by the converters. Further, due to the ac voltage injection, a small ac ripple was superimposed onto the dc currents. The injected frequency of each converter is shown in Figure 8e, where the frequency was decreased by increasing the load. The decreasing frequency variation value was equal to the product of output current and d_{fk}, so the effectiveness of the proposed control strategy based on injection frequency method was verified.

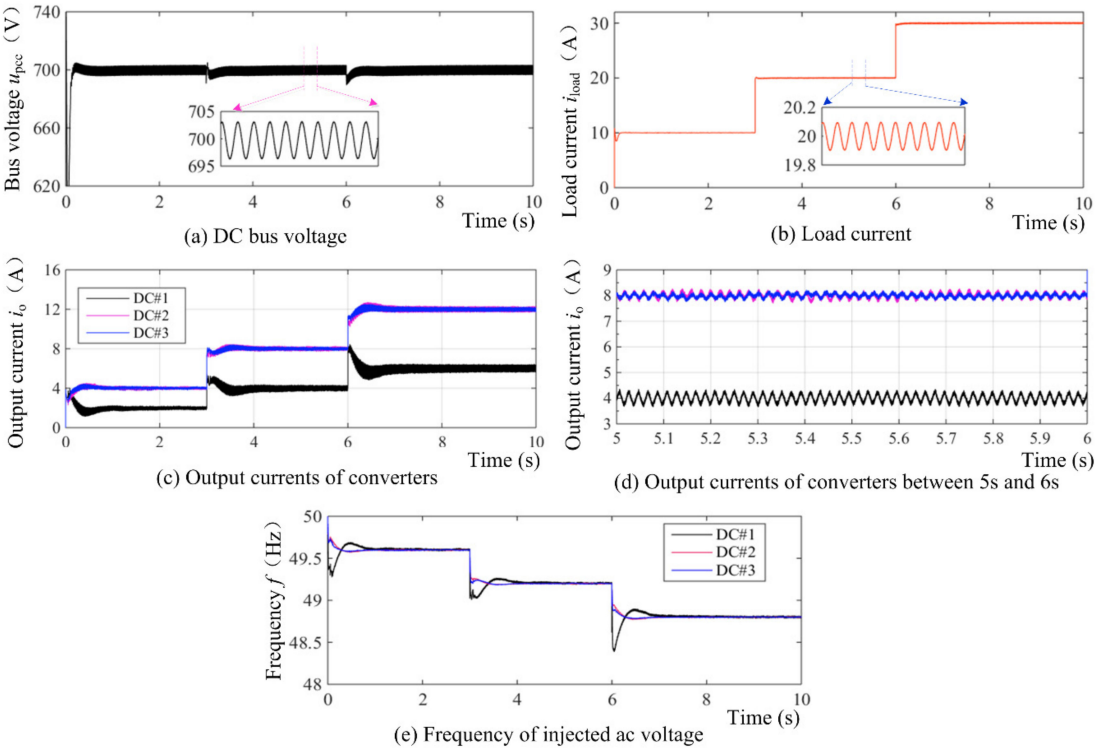


Figure 8. Simulation results of three paralleled converters with unequal power rating.

5.2. Case II: Two Equal Converters Considering the Access of PV Source

In order to further evaluate the proposed control system, the case with two parallel converters that consider the access of the PV source was simulated. The initial load power was 7 kW. The PV converter with a 2.1 kW input power was connected at t = 3 s and a 3.5 kW load was connected at t = 6 s. The frequency-current droop coefficients were both set as 0.1 Hz/A. In this case, two voltage-source-based converters with equal power rating and one current-source-based converter were connected in parallel. The PV converter operated in maximum power point tracking (MPPT) mode, and it was essentially equivalent to a current source. Then, the simulation results are shown in Figure 9.

As shown in Figure 9a, when the load or power supply changed, the bus voltage could recover within 0.2 s, and the steady-state value of DC voltage was almost equal to the rated voltage. From Figure 9b,c, it can be seen that the load current and the output current of each converter had very good dynamic performance when the PV converter was connected or the load changed. Moreover, the output currents of the two converters were nearly the same whether the PV unit was present or not. Figure 9d shows the detailed waveforms of the output currents of the two converters between 5 s and 5.6 s, it can be found that the two current waveforms were almost reversed, which is consistent with the previous theoretical analysis. In Figure 9e, the injected frequency of each converter converged to an equal value dictated by the droop characteristics. From the figure, it can be found that the parallel system had a better dynamic performance and power sharing accuracy, whether the output power on source side changed or the load power changed. Meanwhile, compared with Figure 8, it can be seen that the dynamic performance of two converters in parallel is better than that of three converters.

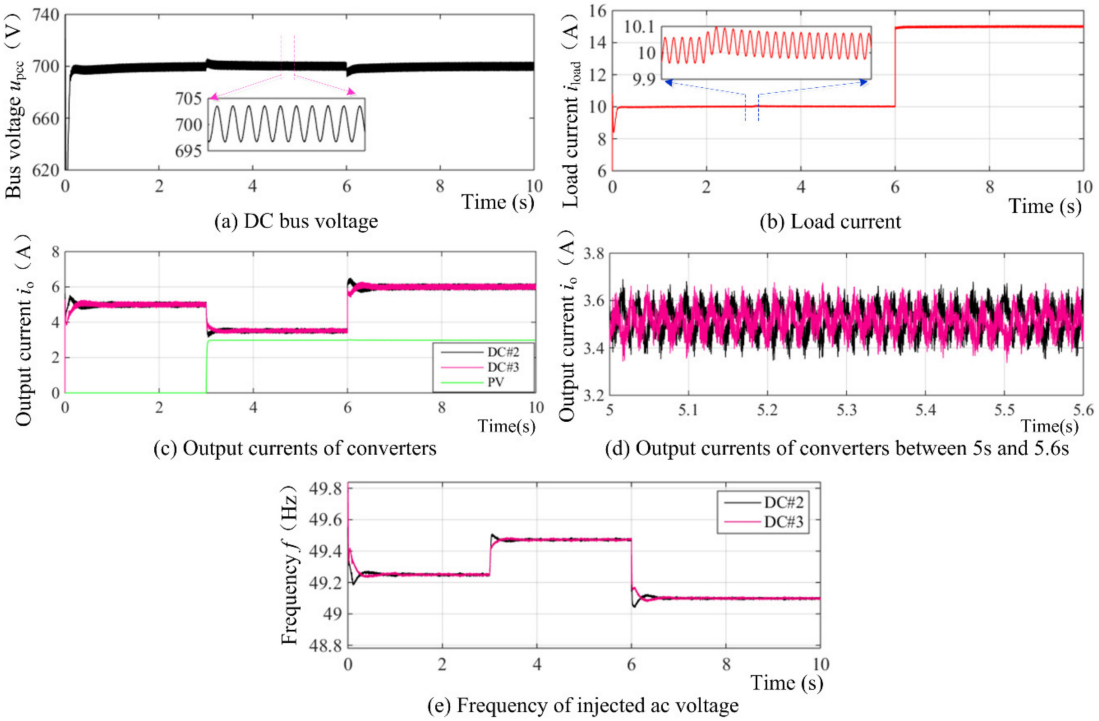


Figure 9. Simulation results of two equal converters considering the access of the PV converter.

5.3. Case III: Two Unequal Converters with CPL Load

In this case, a dc motor as a constant power load was connected to the parallel system through a dc/dc converter, shown in Figure 10. The parallel system mainly consisted of two converters with unequal power rating and some different loads. At first, the converters were supporting a 5 kW resistive load. At t = 5 s, the dc motor started at 1750 rpm without mechanical load. At t = 10 s, a 15 nm mechanical load was connected. The frequency-current droop coefficients of the two converters were set as 0.3 and 0.15 Hz/A, and the dc motor parameters are given in Table 2. Then, the simulation results are shown in Figure 11.

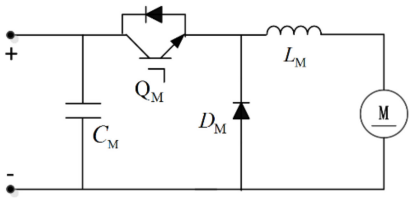


Figure 10. Block diagram of the simplified dc motor-based constant power load.

Table 2. The dc motor parameters.

Parameters	Value	Unit
Rated mechanical speed r_N	1750	rmp
Rated mechanical torque T_N	20	Nm
Rotor inertia J	0.05	Nms^2
Armature resistance R_a	0.78	Ω
Armature inductance L_a	0.016	H
Field resistance R_f	150	Ω
Field inductance L_f	0.11	H

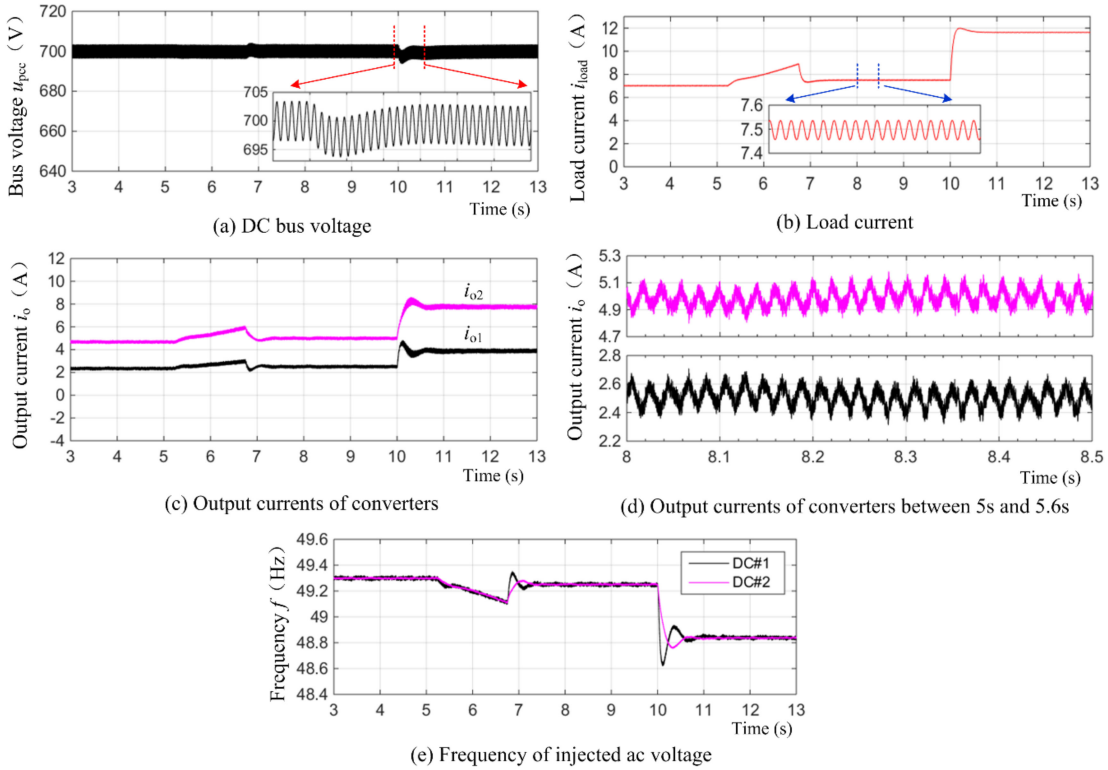


Figure 11. Simulation results of two unequal converters under the motor-based constant power load.

After starting the dc motor with no mechanical load at t = 5 s, the load current increased with the increase of the motor speed. About 1.8 s later, the starting process ended and the motor ran at rated speed without mechanical load. At this time, the load current decreased and kept constant. At t = 10 s, the load current increased rapidly with the increase of mechanical load. It can be seen from Figure 11 that when the motor load changed, it had less impact on the bus voltage, which fluctuated slightly in the whole process. Meanwhile, the dynamic recovery time of the voltage, current, and frequency were both less than 0.6 s. Compared with the resistive load, which is shown in Figures 8 and 9, the system dynamic performance was similar and could meet the dynamic requirements. As shown in Figure 11c,d, the load was almost proportionately shared by the two converters. At t = 8 s, their output currents were about 2.5 ± 0.1A and 5 ± 0.1 A. During the whole process, the output current rating of DC#1 and DC#2 was basically maintained at 1:2. At the same time, the output current ripple was basically the same as that of resistive load.

The simulation results indicate that the proposed control method can make the parallel system have better current sharing accuracy under both resistive load and constant power load. At the same time, this method can make the bus voltage have better dynamic performance and self-recovery characteristics without any communication.

6. Experimental Tests

In order to further validate the proposed control strategy, some experimental tests were performed, taking into account load variations, as well as equal and unequal converter ratings and different load types. The experiment setup, which consists of storage batteries, two boost converters, dc electronic load, dc/dc power converter load, and dSPCAE 1103 controller, is shown in Figure 12. The parameters are listed in Table 3 and the results are reported in the following.

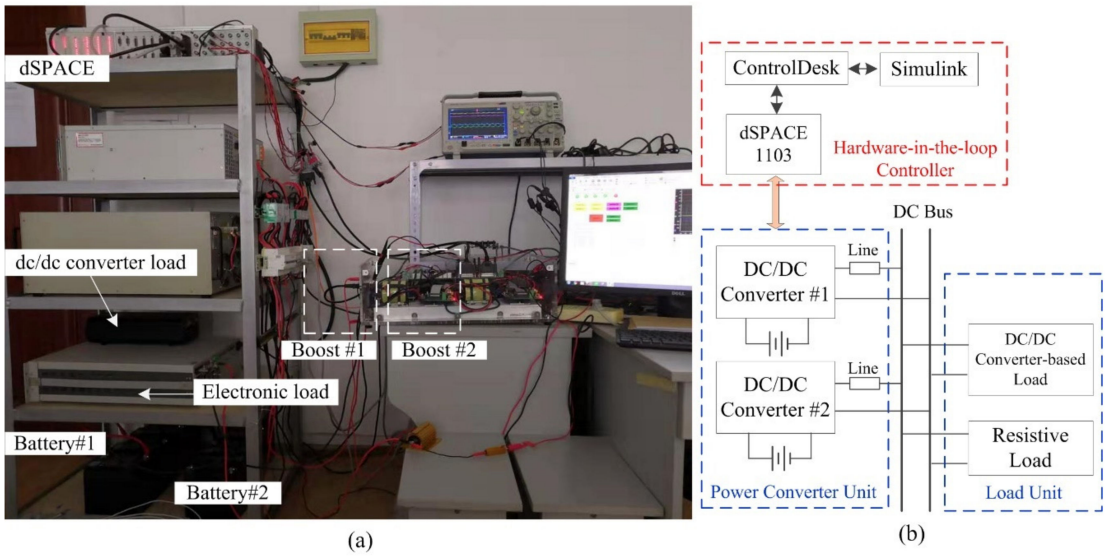


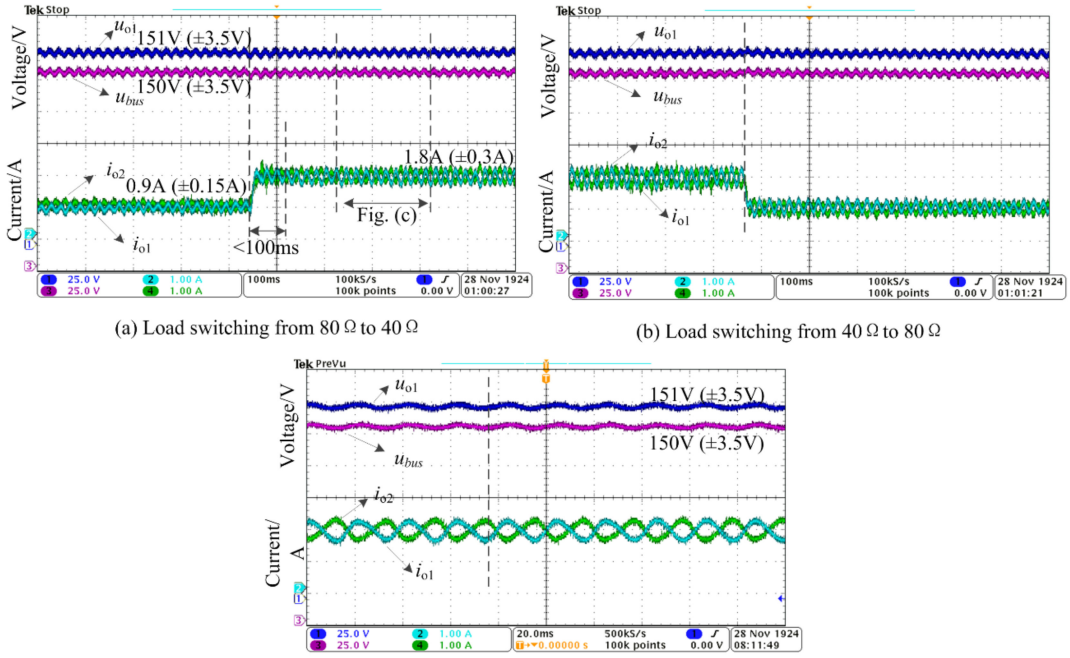
Figure 12. The experiment setup. (**a**) photograph; (**b**) configuration.

Table 3. The experiment setup parameters.

Variables	Descriptions	DC#1	DC#2	Unit
L	converter inductor	1	1	mH
C	converter capacitor	1000	1000	μF
U_S	converter input voltage	48	48	V
P_N	converter Rated power	1.5	1.5	kW
U_N	rated output voltage	150	150	V
k_{ip}, k_{ii}	current controller PI parameters	0.05 + 1/s	0.05 + 1/s	
k_{vp},k_{vi}	voltage controller PI parameters	0.47 + 10/s	0.47 + 10/s	
f_s	switching frequency	20	20	kHz
R_{line}	line resistance	1	0.5	Ω
d_q	*Q-U* regulation coefficient	3	3	V/var
A	injected voltage amplitude	3.5	3.5	V
f^*	rated injected frequency	50	50	Hz
ω_c	cut-off frequency	35	35	rad/s

First, the proposed control strategy was verified with two equal converters in parallel. The frequency-current droop coefficients d_{fk} were both set as 0.2 Hz/A, and the results are shown in Figure 13.

In the figure, u_{bus} is the bus voltage, u_{o1} and i_{o1} were the output voltage and current of DC#1, i_{o2} was the output current of DC#2. Figure 13a,b show the bus voltage and output current waveforms under load variations from 80 Ω to 40 Ω, and from 40 Ω to 80 Ω, respectively. Figure 13c shows the detailed waveforms under the 40 Ω load. It can be seen that the small signal of 3.5 V ac voltage could be better injected into the output voltage of each converter. In the process of load variations, both voltage and current had good dynamic performance, and the dynamic recovery times were both less than 100 ms. Moreover, the influence of load variations on bus voltage could be neglected, and the dc bus voltage was always maintained at the rated value. As shown in Figure 13a, when the load was 80 Ω, the output currents of the two converters were about 0.9 ± 0.15 A, and when the load was 40 Ω, the output currents were about 1.8 ± 0.3 A. Combining with Figure 13c, it is not difficult to find that the load current could be equally shared between the two converters, and the output dc currents had the same value. Furthermore, the phase between the two ac current components was approximately inversed, which is consistent with the theoretical analysis and simulation results.



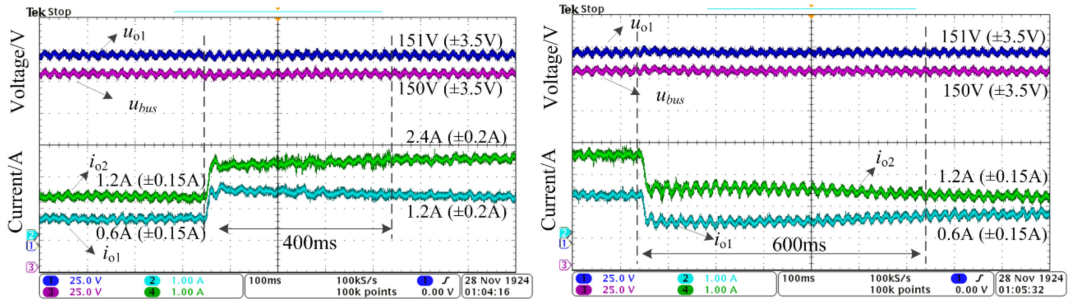
(a) Load switching from 80 Ω to 40 Ω

(b) Load switching from 40 Ω to 80 Ω

(c) Detailed waveforms under the load of 40 Ω

Figure 13. Experimental results of two parallel converters with equal rating.

Figure 14 shows the experiment results of two unequal converters in parallel. The power rating of DC#1 and DC#2 is 1:2, and the frequency-current droop coefficients d_{fk} were set as 0.3 and 0.15 Hz/A. As shown in the figure, when the load was 80 Ω, the output currents of the two converters were 0.6 ± 0.15 A and 1.2 ± 0.15 A, when the load was 40 Ω, the output currents were 1.2 ± 0.2 A and 2.4 ± 0.2 A. So in steady state, the current ratio is approximately 1:2 and the current sharing accuracy can be guaranteed. At the same time, it can found that the influence of load variations on voltage can be neglected, just the same as the case of two equal converters in parallel. When the load resistance decreased, as shown in Figure 14a, the dynamic recovery time of output currents was about 400 ms. When the load resistance increased, as shown in Figure 14b, the dynamic recovery time was about 600 ms. Compared with Figure 13, the dynamic performance of output currents was relatively poor, but it also met the dynamic requirements. Further, the experimental results are basically consistent with the simulation case one.



(a) Load switching from 80 Ω to 40 Ω

(b) Load switching from 40 Ω to 80 Ω

Figure 14. Experiment results of two parallel converters with unequal rating.

Finally, the case of two equal converters with the dc/dc power converter-based load, which is shown in Figure 15, is considered. Figure 16 shows the bus voltage and output current waveforms under load variations between 200 W and 400 W. It can be seen from the figure that the load current could be equally shared between the two converters and the output dc components had the same value. The system dynamic performance was good and similar to that under resistive load. Unlike the

resistive load condition, the phases of the output ac current components were not opposite. This is because the load shown in Figure 15 had a capacitive component, and the injected ac voltage generated reactive power, thus making the sum of the output reactive power a fixed value that was not equal to zero. The experimental results indicate that this did not affect the effectiveness of the proposed control method.

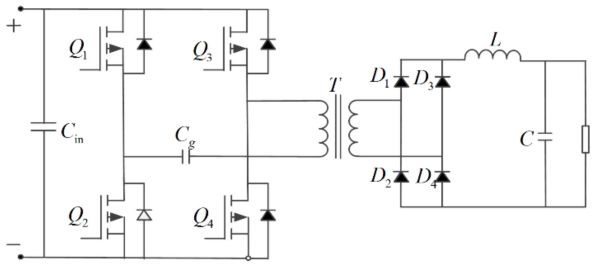
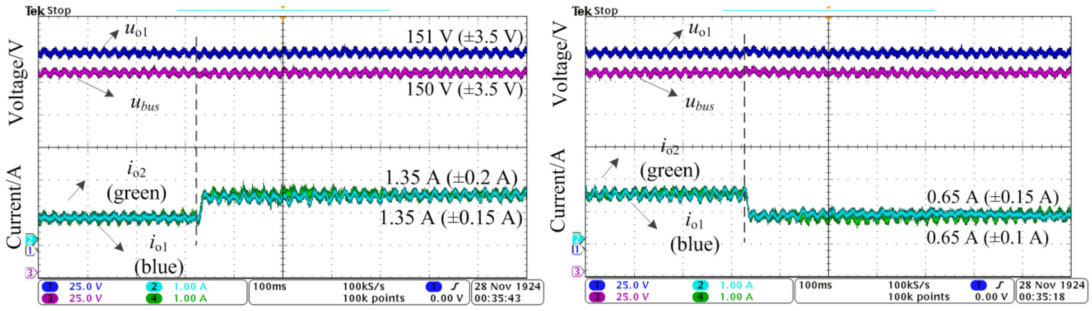


Figure 15. Block diagram of the simplified dc/dc power converter-based load.



(a) Power-converter-based load changing from 200 W to 400 W (b) Power-converter-based load changing from 400 W to 200 W

Figure 16. Experimental results of two parallel converters with equal rating under the dc/dc power-converter-based load.

The experiments above show that the parallel system with the proposed control strategy has better current sharing and dynamic performance, and the bus voltage has better static and dynamic performance without any communication, regardless of whether the converters in parallel have equal or unequal power rating.

7. Conclusions

This paper has presented a novel current-sharing control strategy based on injected small ac voltage for multiple paralleled DC converters. The DC converters are coordinated together with an injected frequency, and hence, accurate current sharing is realized utilizing the feedback mechanism of reactive circuiting power-voltage regulation. On this basis, an autonomous dc bus voltage regulation method has been proposed. Through adding the limiter link and virtual negative impedance, the bus voltage drop caused by line impedance is almost compensated. The basic principle of the proposed control strategy was analyzed in detail, and the stability and dynamic performance were discussed by using small signal modeling. The effectiveness of the proposed control system was evaluated by simulations, including equal and unequal converter ratings, as well as resistive and motor-based constant power load. Finally, the load sharing and bus voltage regulating performance of the proposed method were experimentally verified.

The proposed method is easy to implement without any communication or changing of the hardware structure. However, it is not difficult to find that it also introduces some power quality problems. The output voltage and current ripples of the converter would increase with the injected small ac voltage. Of course, the voltage and current ripples can be controlled within the allowable ranges by reasonably designing the parameters of the proposed controller. Meanwhile, due to the

sensor accuracy, parasitic parameters, external interference, and other reasons, the output current ripple of the experimental results is obviously higher than that of the simulation results. How to further reduce the output ripple and design the injected frequency stopping mechanism after steady state would be the focus research on the proposed control method in the future.

Author Contributions: Conceptualization, Q.Z. and X.Z.; methodology, Q.Z.; validation, Q.Z. and X.Z.; formal analysis, Q.Z.; resources, Y.L.; writing—original draft, Q.Z.; writing—review and editing, Y.L., C.W., and H.G.; project administration, Y.L. and H.G.; funding acquisition, Y.L.

Funding: This research was funded by the National Natural Science Foundation (NNSF) of China under Grant 51709028 and 51979021, the Natural Science Foundation of Liaoning province under Grant 20170540085, and the fundamental research funds for the central universities under Grant 3132018262.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

In this paper, a boost topology was used for the DC/DC converter, and its small signal model of the converter with the voltage and current double-loop controller is shown in Figure A1.

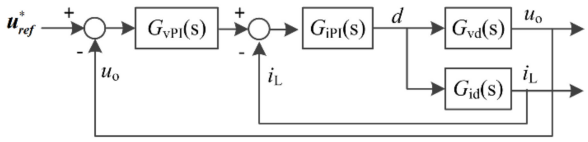


Figure A1. Block diagram of the voltage and current double-loop of boost converter.

$G_{vPI}(s)$ and $G_{iPI}(s)$ are the voltage and current proportional integral controllers, which can be defined as:

$$G_{\mathbf{vPI}}(s) = k_{\mathbf{vp}} + k_{\mathbf{vi}}/s \; G_{\mathbf{iPI}}(s) = k_{\mathbf{ip}} + k_{\mathbf{ii}}/s \tag{A1}$$

where s is Laplace operator, k_{vp} and k_{vi} are the proportional and integral gains of the voltage loop, and k_{ip} and k_{ii} are the proportional and integral gains of the current loop. $G_{\mathbf{vd}}(s)$ is a small signal open-loop transfer function from the control signal (duty cycle d) to the output voltage, and $G_{\mathbf{id}}(s)$ is a small signal open-loop transfer function from the duty cycle d to the output current. The two transfer functions can be defined as follows:

$$G_{\mathbf{vd}}(s) = \frac{U_{\mathbf{o}}}{(1-D)} \cdot \frac{R(1-D)^2 - Ls}{R(1-D)^2 + Ls + RLCs^2} \tag{A2}$$

$$G_{\mathbf{id}}(s) = \frac{2U_{\mathbf{o}}(1+0.5RCs)}{R(1-D)^2 + Ls + RLCs^2} \tag{A3}$$

where L_{dc} and C_{dc} are the inductor and capacitor of the boost converter, U_o is the output voltage, R is the load resistance, and D is the duty cycle of this converter. Then, the closed loop transfer function of the voltage loop can be calculated as follows:

$$G_{\mathbf{closed\_v}}(s) = \frac{G_{\mathbf{vPI}}(s)G_{\mathbf{iPI}}(s)G_{\mathbf{vd}}(s)}{1 + G_{\mathbf{iPI}}(s)G_{\mathbf{id}}(s) + G_{\mathbf{vPI}}(s)G_{\mathbf{iPI}}(s)G_{\mathbf{vd}}(s)}. \tag{A4}$$

The corresponding circuit and control parameters are shown in Table 1. Then, the bode diagram of the closed-loop voltage transfer function is illustrated in Figure A2.

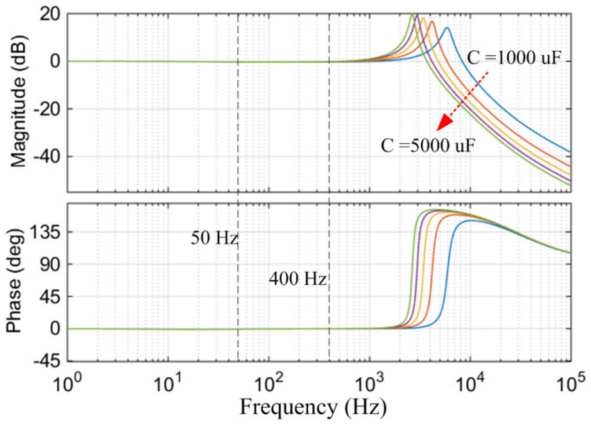


Figure A2. Bode diagram of the closed loop voltage transfer function with the increase of capacitance.

As shown in Figure A2, the voltage controller can effectively track the injected ac signal, whose frequency is less than 400 Hz. The injected frequency is restricted by the bandwidth of the voltage and current double-loop controller. Meanwhile, the selection of injection frequency should also consider the system capacity, because with the increase of the converters, the total capacitance would also increase, resulting in a decrease in bandwidth. Therefore, the maximum frequency should be selected lower than the bandwidth frequency of the inner voltage loop. In order to simplify the analysis and verify the effectiveness of the proposed method, only 50 Hz was selected as the rated injection frequency in the paper.

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