


## Article

# Improvement in Voltage Conversion Ratio of Ultrahigh Step-Down Converter

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**Abstract:** A modified step-down converter is presented herein, which is mainly based on one coupled inductor and several energy-transferring capacitors to improve the voltage conversion ratio as well as to reduce the switch voltage stress. In addition, the portion of the leakage inductance energy can be recycled to the input via the active clamp circuit during the turn-off period and the switches have zero-voltage switching (ZVS) during the turn-on transient. In this paper, the basic operating principles of the proposed converter are firstly described and analyzed, and its effectiveness is finally demonstrated by experiment based on a prototype with input voltage of 60 V, output voltage of 3.3 V and rated output power of 33 W.

**Keywords:** active clamp circuit; coupled inductor; ultrahigh step-down converter; field-programmable gate array; zero-voltage switching; voltage conversion ratio

## 1. Introduction

Recently, with the fast development of the servo power and the cloud, the converter with a high step-down voltage conversion ratio is indispensable. However, regarding the traditional buck converter, if a high step-down voltage conversion ratio is required, the corresponding duty cycle is extremely low, thereby causing the control to be difficult, the power loss on the switch to be increased, and the accompanying efficiency to be decreased. Consequently, there are many researches presented to overcome these problems. The literatures [1,2] apply transformers to half-bridge buck converters so as to improve the step-down voltage conversion ratio. The literatures [3–5] present switched-capacitor converters, whose step-down voltage conversion ratios are enhanced via capacitor voltage dividers. The literatures [6,7] adopt input voltage dividers along with two transformers to improve step-down voltage conversion ratios as well as to cause voltage stresses on switches to be three-level. The circuits shown in [8,9] are improvements of the circuits shown in [7,10]. The literatures [11–16] apply central-tapped coupling inductors to synchronously rectified (SR) buck converters so as to obtain relatively high step-down voltage conversion ratios. In the literatures [17–19], via changing the turns ratios of coupling inductors, not only the voltage stresses on switches can be reduced but also relatively high step-down voltage conversion ratios can be achieved. The literature [20] applies a coupling inductor to an SR buck converter so as to improve the step-down voltage conversion ratio. The literatures [21–24] apply coupling inductors and energy-transferring capacitors to SR buck converters to improve the step-down voltage conversion ratio, and besides, the last employs an active clamp circuit to reduce the switch voltage stress. The circuit shown in [25], with an active clamp circuit included, adopts two forward converters connected in parallel to reduce the voltage conversion ratio.

The literature [26] utilizes multiple voltage-bucking modules and energy-transferring capacitors to improve the step-down voltage conversion ratio as well as to reduce the voltage stresses on switches. However, a large number of modules causes the circuit to be complex and the corresponding size to be relatively huge. The literature [27] employs one buck-boost connected in series with two half-bridge DC transformers and three energy-transferring capacitors so as to improve the step-down voltage conversion ratio. As compared with the literature [21], literature [28] utilizes one additional capacitor and one additional inductor so as to obtain more advantages, such as improvement of core size utilization, reduction of output current ripple, etc. In addition, both have the same voltage conversion ratio.

In this paper, a modified step-down converter is presented. As compared with the work [24], the proposed circuit, based on only one additional capacitor inserted and some circuit connections changed, has a relatively wide voltage conversion ratio as well as relatively small voltage stresses on switches. By the way, both have inherent some merits, such as the voltage clamp during the turn-off period, and the zero-voltage switching (ZVS) for switches during the turn-on transient.

## 2. Circuit Configuration and Its Operating Behavior

Figure 1 shows the proposed converter, which is built up by four switches  $Q_1$ ,  $Q_2$ ,  $Q_3$  and  $Q_4$ , three energy-transferring capacitors  $C_1$ ,  $C_2$  and  $C_3$ , and one coupling inductor with one primary winding  $N_1$ , one secondary winding  $N_2$  and one magnetic inductor  $L_m$ . As for the load, it is constructed by one output resistor  $R_o$ . Figure 2 displays an equivalent circuit model of the proposed converter.

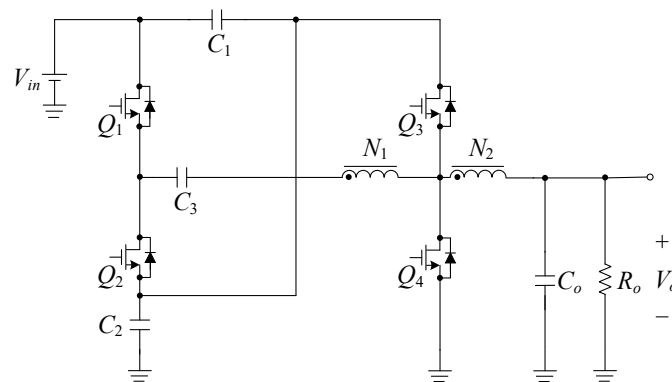


Figure 1. Proposed improved ultrahigh step-down converter.

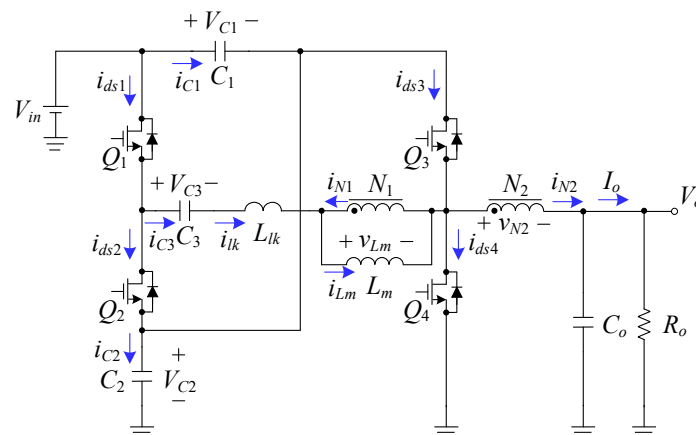


Figure 2. Equivalent circuit model of the proposed converter.

Prior to tackling this section, there are some associated symbols and assumptions in Figure 2, to be described as follows: (i) the input voltage is  $V_i$ ; (ii) the output voltage is  $V_o$ ; (iii) the primary-side

and second-side turns are  $N_1$  and  $N_2$ , respectively; (iv) the currents  $i_{ds1}$ ,  $i_{ds2}$ ,  $i_{ds3}$ ,  $i_{ds4}$ ,  $i_{c1}$ ,  $i_{c2}$ ,  $i_{c3}$ ,  $i_{lk}$ ,  $i_{Lm}$ ,  $i_{N1}$ ,  $i_{N2}$  and  $i_o$  are the currents in  $Q_1$ ,  $Q_2$ ,  $Q_3$ ,  $Q_4$ ,  $C_1$ ,  $C_2$ ,  $C_3$ ,  $L_{lk}$ ,  $L_m$ ,  $N_1$ ,  $N_2$  and  $R_o$ , respectively; (v) the voltages across  $L_m$ ,  $N_2$ ,  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_o$  are  $v_{Lm}$ ,  $v_{N2}$ ,  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$  and  $V_o$ ; (vi) the switching period is signified by  $T_s$ ; (vii) the turn-on times for  $Q_1$  and  $Q_3$  are  $DT_s$ , whereas the turn-on times for  $Q_2$  and  $Q_4$  are  $(1-D)T_s$ , where  $D$  is a duty cycle; (viii) all the switches are ideal, and all the capacitors are ideal without their equivalent series resistances (ESRs) included, that is, the capacitance for each capacitor is assumed to be large enough to keep the voltage on it constant at some value; (ix) the gate driving signals  $v_{gs1}$  and  $v_{gs3}$ , for  $Q_1$  and  $Q_3$  respectively, are identical, whereas the gate driving signals  $v_{gs2}$  and  $v_{gs4}$ , for  $Q_2$  and  $Q_4$  respectively, are identical; and (x) the circuit operates with no negative current. There are six states over one switching period, to be shown in Figure 3.

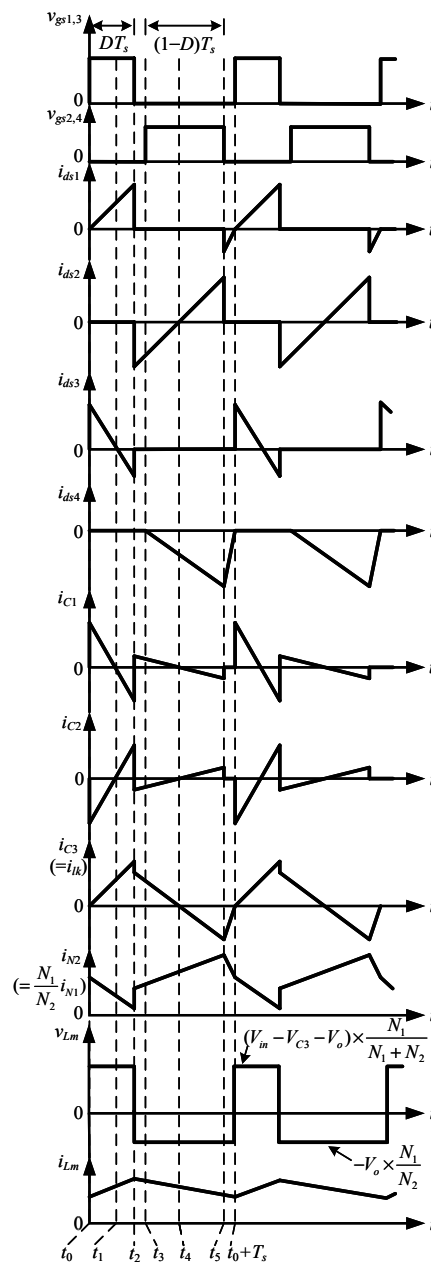


Figure 3. Key waveforms relevant to the proposed converter operating.

## 2.1. Operating Principles

### 2.1.1. State 1: $[t_0 \leq t \leq t_1]$

As shown in Figure 4, the switches  $Q_1$  and  $Q_3$  are in the on-state but the switches  $Q_2$  and  $Q_4$  are in the off-state. The switch  $Q_1$  is turned on with zero-voltage switching (ZVS) because the body diode of  $Q_1$  is switched on before turn-on of  $Q_1$ . During this state, the voltages across the magnetizing inductance  $L_m$  and leakage inductance  $L_{lk}$  are positive voltages, thereby causing  $L_m$  and  $L_{lk}$  to be magnetized. At the same time, the voltage  $V_{in}$  charges the capacitors  $C_1$  and  $C_3$ , and, together with the capacitor  $C_2$ , supplies energy to the load. To speak lucidly, at  $t = t_0$ , the current in  $C_1$  has some positive value and then linearly decreases due to the leakage reflected from the primary-side leakage; at  $t = t_0$ , the current in  $C_2$  has some negative value and then linearly decreases due to the leakage reflected from the primary-side leakage; At  $t = t_0$ , the current in  $C_3$  is zero and then linearly increases due to the primary-side leakage. As soon as  $i_{C1}$  and  $i_{C2}$  reach zero, this mode ends at  $t = t_1$ .

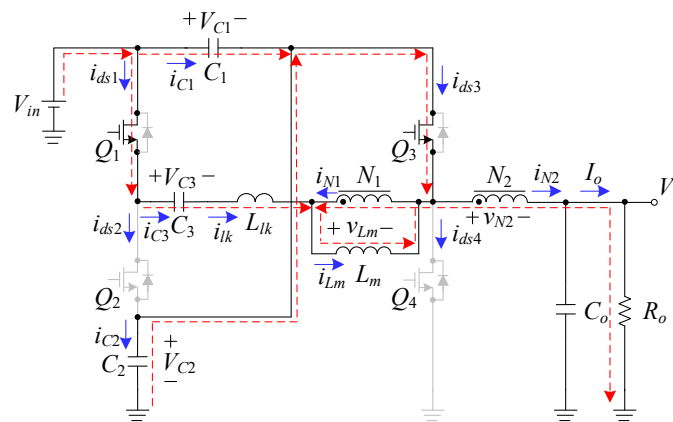


Figure 4. Current flow during state 1.

### 2.1.2. State 2: $[t_1 \leq t \leq t_2]$

As shown in Figure 5, the switches  $Q_1$  and  $Q_3$  are still in the on-state, but the switches  $Q_2$  and  $Q_4$  are still in the off-state. During this state, the magnetizing inductance  $L_m$  and leakage inductance  $L_{lk}$  are still magnetized. At the same time, the input voltage  $V_{in}$  charges the capacitor  $C_2$  and, together with the capacitor  $C_1$ , charges the capacitor  $C_3$  as well as supplies energy to the load. Once  $Q_1$  is turned off, this mode ends at  $t = t_2$ .

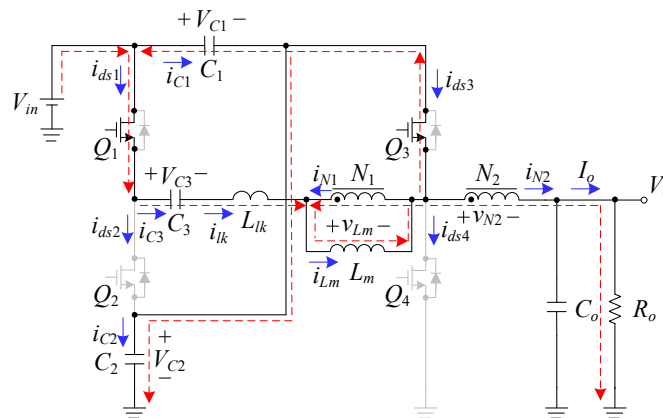


Figure 5. Current flow during state 2.



the capacitor  $C_2$  and, together with the capacitor  $C_1$ , releases energy to the input voltage  $V_{in}$ . Once  $Q_2$  and  $Q_4$  are turned off, this mode ends at  $t = t_5$ .

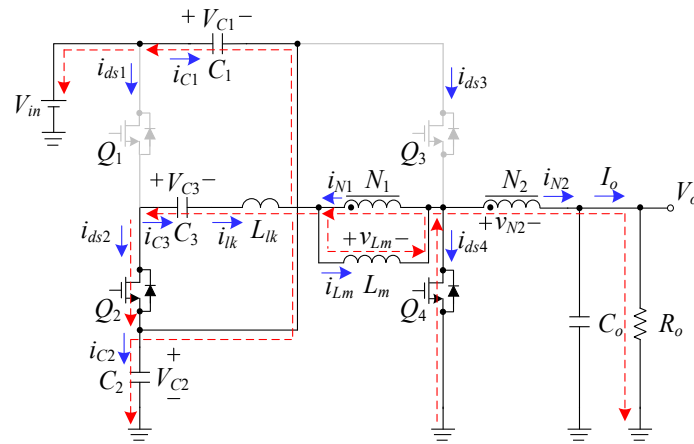


Figure 8. Current flow during state 5.

#### 2.1.6. State 6: $[t_5 \leq t \leq t_0 + T_s]$

As shown in Figure 9, all the switches are turned off with the body diodes of  $Q_1$  and  $Q_4$  turned on and this state is called the other blanking time over one switching period. During such a state, the capacitor  $C_3$  still discharges. At the same time, the magnetizing inductance  $L_m$  and leakage inductance  $L_{lk}$  are still demagnetized, transferring their energy to the load. The moment  $Q_1$  and  $Q_3$  are turned on, this mode ends and the next cycle is repeated.

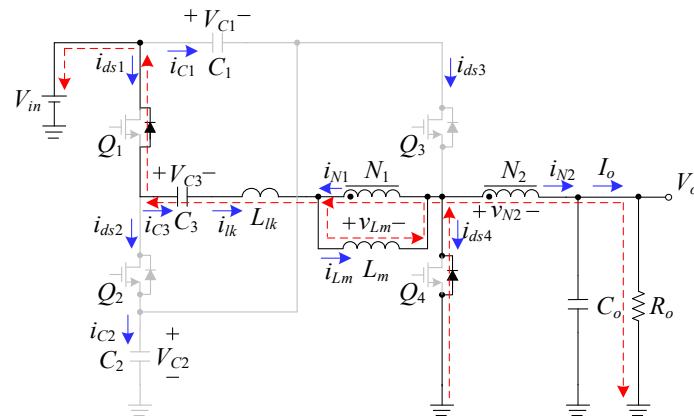


Figure 9. Current flow during state 6.

## 2.2. Voltage Conversion Ratio

In order to obtain the voltage conversion ratio, the voltages across the magnetizing inductance  $L_m$ , the secondary winding  $N_2$ , and the energy-transferring capacitors  $C_1$ ,  $C_2$  and  $C_3$ , that is,  $v_{Lm}$ ,  $v_{N2}$ ,  $V_{C1}$ ,  $V_{C2}$  and  $V_{C3}$ , are first obtained. In the following analysis, the blocking times and the leakage inductance are negligible, and hence only states 1 and 4 are considered. From state 1, the voltages  $v_{Lm}$  and  $v_{N2}$  can be expressed as

$$v_{Lm} = (V_{in} - V_{C3} - V_o) \times \frac{N_1}{N_1 + N_2} \quad (1)$$

$$v_{N2} = V_{C2} - V_o \quad (2)$$

From state 4, the voltages  $v_{Lm}$  and  $v_{N2}$  can be represented by

$$v_{Lm} = -V_o \times \frac{N_1}{N_2} = V_{C2} - V_{C3} \quad (3)$$

$$v_{N2} = -V_o \quad (4)$$

Since the magnetizing inductance  $L_m$  on the primary side can be reflected to the secondary side, the voltage-second balance should be obeyed over one switching period. Therefore, the following equation can be obtained to be

$$(V_{C2} - V_o) \times D = V_o \times (1 - D) \quad (5)$$

From (5), we can obtain

$$V_{C2} = \frac{V_o}{D} \quad (6)$$

Substituting (6) into (3) yields

$$V_{C3} = V_o \times \left( \frac{1}{D} + \frac{N_1}{N_2} \right) \quad (7)$$

In addition, since the magnetizing inductance  $L_m$  on the primary side also needs to obey the voltage-second balance, the following equation can be obtained to be

$$(V_{in} - V_{C3} - V_o) \times \frac{N_1}{N_1 + N_2} \times D = \frac{V_o \times N_1}{N_2} \times (1 - D) \quad (8)$$

By substituting (7) into (8), the voltage conversion ratio can be obtained to be

$$\frac{V_o}{V_{in}} = D \times \left( \frac{n}{1 + 2n} \right) \quad (9)$$

where  $n$  is the turns ratio equal to  $N_2/N_1$ .

### 2.3. Boundary Condition Analysis

The boundary condition for  $L_m$  is described as follows.

$$\begin{cases} 2I_{Lm} \geq \Delta i_{Lm} \Rightarrow L_m \text{ operated without negative current} \\ 2I_{Lm} \leq \Delta i_{Lm} \Rightarrow L_m \text{ operated with negative current} \end{cases} \quad (10)$$

where  $I_{Lm}$  and  $\Delta i_{Lm}$  are the DC and AC values of  $i_{Lm}$ , respectively, and the latter is also called the magnetizing current ripple.

For analysis convenience, it is assumed that there is no power consumption in the converter. According to the voltage-second balance of the inductor and the current second balance of the capacitor, the DC voltage across the coupling inductor and the DC current in the energy-transferring capacitor are zero. Therefore, as shown in Figure 10, the secondary DC current  $I_{N2}$  is equal to the output current  $I_o$ , namely,

$$I_{N1} = \frac{N_2}{N_1} \times I_{N2} = \frac{N_2}{N_1} \times I_o \quad (11)$$

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1} \times I_o \quad (12)$$

$$I_o = \frac{V_o}{R_o} \quad (13)$$

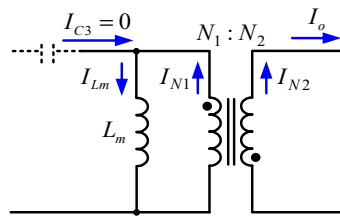


Figure 10. Equivalent model for the coupling inductor under DC analysis.

From (12) and (13), it can be obtained

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1} \times \frac{V_o}{R_o} \quad (14)$$

Since the current ripple  $\Delta i_{Lm}$  can be expressed as

$$\Delta i_{Lm} = \frac{v_{Lm} \Delta t}{L_m} = \frac{\frac{N_1}{N_2} V_o (1-D) T_s}{L_m} \quad (15)$$

Hence, as  $2I_{Lm} \geq \Delta i_{Lm}$ , the magnetizing inductance  $L_m$  will be operated without negative current, that is,

$$\begin{aligned} 2I_{Lm} &\geq \Delta i_{Lm} \\ \Rightarrow 2 \times \frac{N_2}{N_1} \times \frac{V_o}{R_o} &\geq \frac{\frac{N_1}{N_2} V_o (1-D) T_s}{L_m} \\ \Rightarrow \frac{2L_m}{R_o T_s} &\geq \left( \frac{N_1}{N_2} \right)^2 \times (1-D) \\ \Rightarrow K &\geq K_{crit}(D) \end{aligned} \quad (16)$$

where  $K = \frac{2L_m}{R_o T_s}$  and  $K_{crit}(D) = \left( \frac{N_1}{N_2} \right)^2 \times (1-D)$ .

From (16), it can be seen that as  $K \geq K_{crit}(D)$ , the magnetizing inductance  $L_m$  will be operated without negative current; otherwise,  $L_m$  will be operated with negative current. Hence, by assuming that  $N_1/N_2 = 3$ , the boundary curve for  $L_m$  operating mode can be drawn as shown in Figure 11.

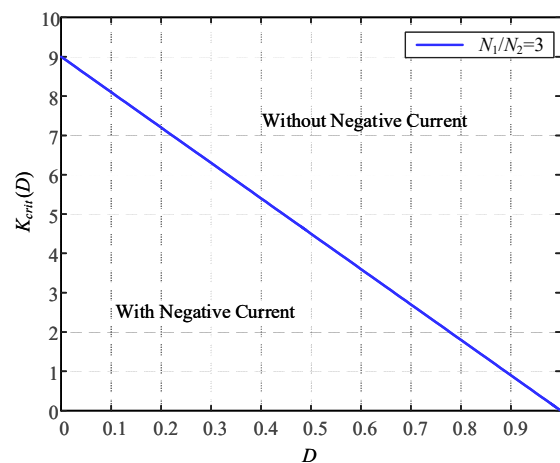


Figure 11. Boundary curve for  $L_m$  operating mode.

#### 2.4. Comparison of Proposed Circuit with Existing Circuits

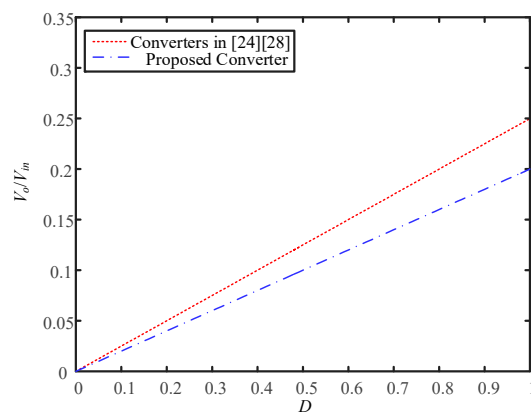
Table 1 shows the comparison of the proposed circuit with the existing circuits, in terms of voltage conversion ratio, component number, switch voltage stress, and output inductor. From Table 1, the proposed circuit has a more component number than the circuits shown in [24,28] have. As shown in Figure 12, the proposed circuit has a lower voltage conversion ratio than the circuits shown in [24,28] have. In practice, the lower the turns ratio  $n (= N_2/N_1)$  is, the larger the leakage inductance.



Consequently, the value of  $n$ , set at  $1/3$  for the comparison in step-down voltage conversion ratio, is reasonable. The proposed circuit has lower voltage stresses on  $Q_1$  and  $Q_2$  than the circuits shown in [24,28] have. In addition, the proposed circuit has lower voltage stresses on  $Q_3$  and  $Q_4$  than the circuits shown in [24,28] have. In addition, only the circuit shown in [28] has an output inductor.

**Table 1.** Comparison of the proposed circuit with the existing circuits.

Converter	Voltage Conversion Ratio	Component Number	Switch Voltage Stress	Output Inductor
Proposed	$D \cdot \left(\frac{n}{1+2n}\right)$	9	$V_{ds1} = V_{ds2} = \frac{1+n}{1+2n} V_{in}$ $V_{ds3} = V_{ds4} = \frac{n}{1+2n} V_{in}$	No
[24]	$D \cdot \left(\frac{n}{1+n}\right)$	8	$V_{ds1} = V_{ds2} = V_{in}$ $V_{ds3} = V_{ds4} = \frac{n}{1+n} V_{in}$	No
[28]	$D \cdot \left(\frac{n}{1+n}\right)$	8	$V_{ds1} = V_{ds2} = V_{in}$ $V_{ds3} = V_{ds4} = \frac{n}{1+n} V_{in}$	Yes



**Figure 12.** Voltage conversion curves of the circuit shown in Table 1 with  $n = 1/3$ .

### 3. Control Strategy

Figure 13 shows the system block diagram for the proposed high step-down converter, including main power stage and feedback control circuit. As for the feedback control circuit, it is constructed by one voltage divider used to obtain the analogue signal of the output voltage, one analogue-to-digital converter (ADC) used to transfer this analogue signal to the digital signal, and one field-programmable gate array (FPGA) chip used to generate four digital pulse-width modulation (DPWM) signals, which are sent to four switches after four gate drivers so as to stabilize the output voltage at the desired value. Speaking lucidly, the digital signal obtained from the ADC is sent to the proportional-integral (PI) controller embedded in the FPGA to create DPWM signals,  $v_{gs1}$ ,  $v_{gs2}$ ,  $v_{gs3}$  and  $v_{gs4}$ , where  $v_{gs1}$  equal to  $v_{gs2}$  is complimentary to  $v_{gs2}$  equal to  $v_{gs4}$ .

#### *How to Set Switching Frequency from FPGA and How to Get DPWM Signal*

The FPGA needs an external oscillator of 20 MHz, and this frequency will be increased to 100 MHz, which will be used as a system clock as well as a subsystem clock of the DPWM generator. As soon as the system get started, the counting value of one counter will be increased from zero to 999, and then be initialized such that the next cycle is to be repeated. That is to say, the switching frequency is 100 MHz divided by 1000, equal to 100 kHz. As the counting value of the counter is smaller than the control force created from the PI controller embedded in the FPGA, the DPWM signal will be “high”; otherwise, the DPWM signal will be “low”.

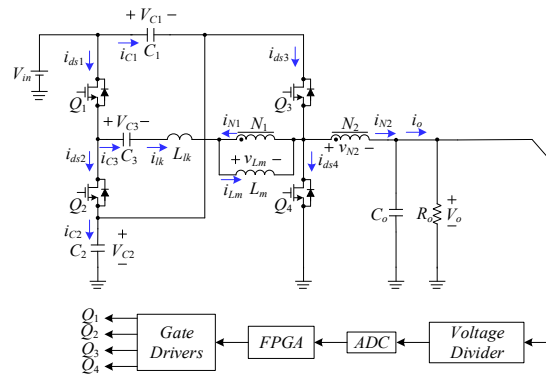


Figure 13. System configuration block diagram.

#### 4. Design Considerations

Prior to this section, system specifications should be given as shown in Table 2. The two blanking times between  $Q_1$  (or  $Q_3$ ) and  $Q_2$  (or  $Q_4$ ) are set at 100 ns and 150 ns, respectively. It is noted that in order to verify that the voltage conversion ratio of the proposed circuit is wider than that of the circuit shown in [24], the former has an input voltage of 60 V and an output voltage of 3.3 V, whereas the latter has an input voltage of 48 V and an output voltage of 3.3 V.

Table 2. System specifications.

Parameters	Specifications
Converter Operating Mode	CCM
Input Voltage ( $V_{in}$ )	60 V
Rated Output Voltage ( $V_{o, rated}$ )	3.3 V
Rated Output Current ( $I_{o, rated}$ )/Power ( $P_{o, rated}$ )	10 A/33 W
Minimum Output Current ( $I_{o, min}$ )/Power ( $P_{o, min}$ )	2 A/6.6 W
Switching Frequency ( $f_s$ )/Period ( $T_s$ )	100 kHz/10 $\mu$ s

##### 4.1. Design of Coupling Inductor

##### 4.1.1. Design of Turns Ratio

From (9), the following equation can be obtained to be

$$D = \frac{V_o}{V_{in}} \times \left( \frac{1+2n}{n} \right) \quad (17)$$

Since the converter mainly transfers energy to the load during the turn-off period of  $Q_1$ , the duty cycle is set between 0.2 and 0.3. According to Table 2, together with this desired duty cycle range, the turns ratio inequality can be obtained to be

$$\begin{aligned} 0.2 &\leq \frac{V_o}{V_{in}} \times \left( \frac{1+2n}{n} \right) \leq 0.3 \\ \Rightarrow 0.2 &\leq \frac{3.3}{60} \times \left( \frac{1+2n}{n} \right) \leq 0.3 \Rightarrow 0.289 \leq n \leq 0.61 \end{aligned} \quad (18)$$

Based on (18), the value of  $n$  is chosen to be

$$n = \frac{1}{3} \quad (19)$$

Substituting (19) and some system specifications shown in Table 2 into (19) yields

$$D = \frac{V_o}{V_{in}} \times \left( \frac{1+2n}{n} \right) = \frac{3.3}{60} \times \left( \frac{1+2 \times \frac{1}{3}}{\frac{1}{3}} \right) = 0.275 \quad (20)$$

#### 4.1.2. Design of Magnetizing Inductance

From (16), it can be seen that if the magnetizing inductance  $L_m$  operates without negative current, the value of  $L_m$  should obey the following inequality:

$$\begin{aligned} L_m &\geq \left(\frac{N_1}{N_2}\right)^2 \times (1-D) \times \frac{R_{o,max} \times T_s}{2} \\ \Rightarrow L_m &\geq \left(\frac{N_1}{N_2}\right)^2 \times (1-D) \times \frac{V_o \times T_s}{2 \times I_{o,min}} \end{aligned} \quad (21)$$

where  $R_{o,max}$  indicates the maximum output resistance.

Substituting the results shown in (19) and (20), and some specifications shown in Table 2 into (21) yields

$$L_m \geq \frac{9 \times (1 - 0.275) \times 3.3 \times 10 \mu}{2 \times 2} \Rightarrow L_m = 53.8 \mu H \quad (22)$$

Before calculating the primary and secondary turns of the coupled inductor,  $N_1$  and  $N_2$ , the peak current of the magnetizing inductance,  $I_{Lm,peak}$ , should be first obtained, namely,

$$I_{Lm,peak} = I_{Lm} + \frac{\Delta i_{Lm}}{2} \quad (23)$$

By substituting (14) and (15) into (23), the following equation can be obtained to be

$$\begin{aligned} I_{Lm,peak} &= I_{Lm} + \frac{\Delta i_{Lm}}{2} \\ &= \frac{N_2}{N_1} \times I_o + \frac{\frac{N_1}{N_2} \times V_o \times (1-D)}{2 \times L_m \times f_s} \end{aligned} \quad (24)$$

By substituting the results shown in (19) and (20), and some specifications shown in Table 2 into (30), the value of  $I_{Lm,peak}$  can be obtained to be

$$I_{Lm,peak} = \frac{1}{3} \times 10 + \frac{3 \times 3.3 \times (1 - 0.275)}{2 \times 53.8 \mu \times 100 k} = 4 \text{ A} \quad (25)$$

After this, via the Faraday law, the value of  $N_1$  can be represented by

$$N_1 = \frac{L_m \times I_{Lm,peak}}{A_e \times B_{max}} \times 10^8 \quad (26)$$

where  $A_e$  is the effective area of the core size and  $B_{max}$  is the maximum flux density.

Since the saturation flux density  $B_s$  will be reduced due to the temperature rising, the value of  $B_{max}$  is designed to be 80% of  $B_s$ . By the way, the high- $\mu$  core is used herein, whose product name is PQ20/16-3C90, made by FERROXCUBE Co. Table 3 shows the specifications of this core.

**Table 3.** Core specifications.

Parameters	Specifications
Product name	PQ20/16-3C90
Inductor constant ( $A_L$ )	3250 nH/N <sup>2</sup> $\pm$ 25%
Saturation flux density ( $B_s$ )	380 mT
Residual flux density ( $B_r$ )	60 mT
Effective area ( $A_e$ )	0.619 cm <sup>2</sup>
Effective volume ( $V_e$ )	2.33 cm <sup>3</sup>
Effective magnetic length ( $l_e$ )	3.76 cm

By substituting the results shown in (22) and (25), and some specifications shown in Table 3 into (26), the value of  $N_1$  can be obtained to be

$$N_1 = \frac{53.8 \mu \times 4}{0.619 \times 0.8 \times 3800} \times 10^8 \approx 12 \text{ Turns} \quad (27)$$

Since the value of  $n$  is  $1/3$ , the value of  $N_2$  is set at four turns. However, by substituting the result of (27) and the value of  $A_e$  shown in Table 3 into the following equation, the corresponding value of  $L_m$ , much larger than the value of  $L_{min}$  shown in (22), can be obtained to be

$$L_m = N_1^2 \times A_L = 12^2 \times 3250 \times 10^{-9} = 468 \mu\text{H} \quad (28)$$

Consequently, the air gap needs to be adjusted in order to obtain the desired value of  $L_m$ . Without considering the fringing effect, the desired value of the airgap  $l_g$  can be obtained according to the following two equations:

$$L_m = \frac{4\pi A_e N_1^2 \mu_e}{l_e} \times 10^{-8} \quad (29)$$

$$\mu_e \cong \frac{l_e}{l_a} \quad (30)$$

where  $\mu_e$  is the equivalent magnetic permeability.

Combining (29) and (30) yields

$$l_a = \frac{4\pi A_e N_1^2}{L_m} \times 10^{-8} \quad (31)$$

By substituting the result shown in (22) and some specifications shown in Table 3 into (31), the required value of  $l_a$  can be obtained to be

$$l_a = \frac{4\pi \times 0.619 \times 144}{53.8 \mu} \times 10^{-8} \approx 0.21 \text{ mm} \quad (32)$$

Finally, the actual value of  $L_m$  is designed and measured to be  $81.6 \mu\text{H}$ .

#### 4.2. Component Specifications

In the following, the specifications of the used components are listed in Table 4.

**Table 4.** Specifications of the components used in the proposed converter.

Components	Specifications	
MOSFET	$Q_1, Q_2$ $Q_3, Q_4$	STP120NF10 IRF3205Z
Energy-Transferring Capacitor	$C_1$	220 $\mu\text{F}/100 \text{ V}$ Rubycon Electrolytic Capacitor
	$C_2, C_3$	680 $\mu\text{F}/35 \text{ V}$ Rubycon Electrolytic Capacitor
Capacitor	$C_o$	1000 $\mu\text{F}/16 \text{ V}$ Rubycon Electrolytic Capacitor
Coupled Inductor	Core: PQ20/16-3C90 $N = 1/3, L_m = 81.6 \mu\text{H}, L_{lk} = 0.82 \mu\text{H}$	

### 5. Experimental Results

#### 5.1. Test Bench for Measuring Efficiency and Waveforms

In the following, how to measure the efficiency will be described. First, as shown in Figure 14, the input current is obtained by measuring the voltage across one current sensing resistor based on one digital meter. After this, the input voltage is obtained also by another digital meter. Hence, the input

power can be attained. Regarding the output power, the output current is read from one electronic load and the output voltage is obtained also by the other digital meter. Therefore, the output power can be attained. Finally, the corresponding efficiency can be obtained. As for measured waveforms, they are obtained by the instruments shown in Figure 14, along with two additional current amplifiers, two additional current probes and one additional isolated oscilloscope.

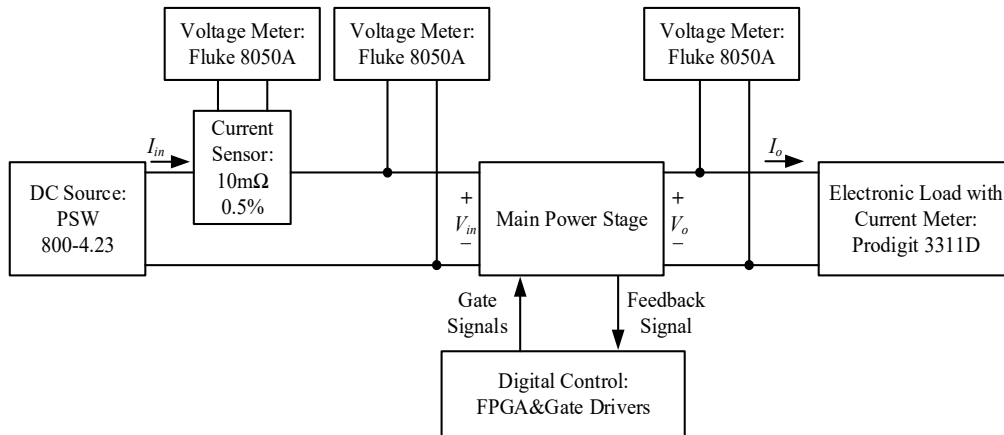


Figure 14. Test bench for measuring efficiency.

## 5.2. Measured Waveforms and Efficiency

The waveforms shown in Figures 15–21 are measured at rated load. Figure 15 shows the gate driving signal for  $Q_1$ ,  $v_{gs1}$ , the voltage across  $Q_1$ ,  $v_{ds1}$ , the gate driving signal for  $Q_3$ ,  $v_{gs3}$ , and the voltage across  $Q_3$ ,  $v_{ds3}$ . Figure 16 shows the gate driving signal for  $Q_2$ ,  $v_{gs2}$ , the voltage across  $Q_2$ ,  $v_{ds2}$ , the gate driving signal for  $Q_4$ ,  $v_{gs4}$ , and the voltage across  $Q_4$ ,  $v_{ds4}$ . Figure 17 shows the voltages on  $C_1$ ,  $V_{C1}$ , the voltage on  $C_2$ ,  $V_{C2}$ , and the voltage on  $C_3$ ,  $V_{C3}$ . Figure 18 shows the gate driving signal for  $Q_1$ ,  $v_{gs1}$ , the gate driving signal for  $Q_2$ ,  $v_{gs2}$ , the current flowing through  $L_{lk}$ ,  $i_{lk}$ , and the current in  $N_2$ ,  $i_{N2}$ . Figure 19 shows the input voltage  $V_{in}$  and the output voltage  $V_o$ . Figures 20 and 21 show the turn-on ZVS of  $Q_1$  and  $Q_2$ , respectively. Figure 22 shows load transient responses and Figure 23 displays a curve of efficiency versus load current percentage.

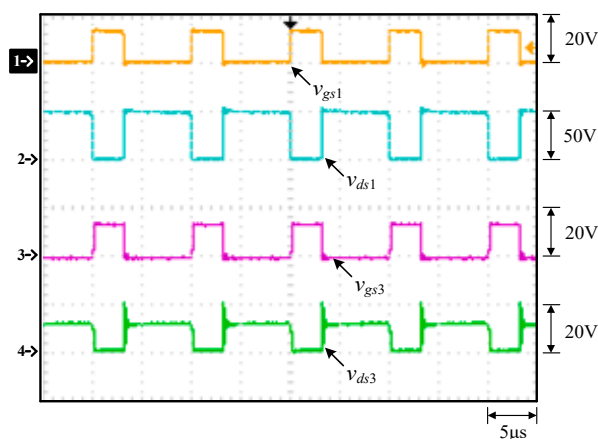


Figure 15. Measured waveforms at rated load: (1)  $v_{gs1}$ ; (2)  $v_{ds1}$ ; (3)  $v_{gs3}$ ; (4)  $v_{ds3}$ .

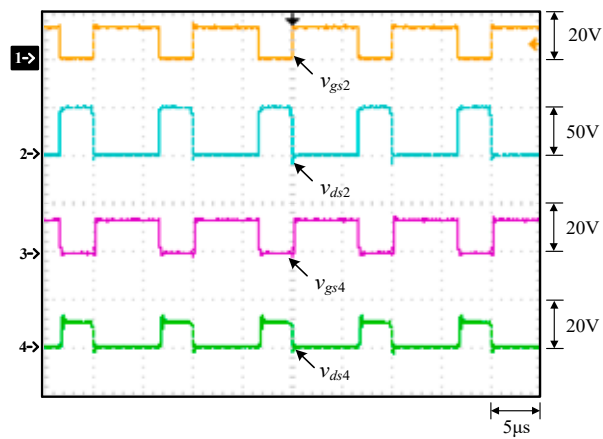


Figure 16. Measured waveforms at rated load: (1)  $v_{gs2}$ ; (2)  $v_{ds2}$ ; (3)  $v_{gs4}$ ; (4)  $v_{ds4}$ .

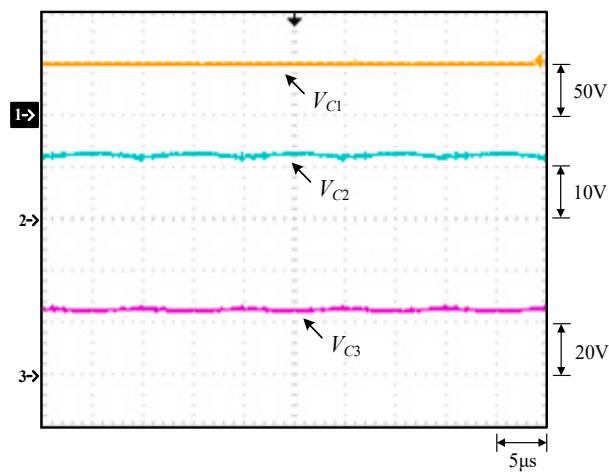


Figure 17. Measured waveforms at rated load: (1)  $V_{C1}$ ; (2)  $V_{C2}$ ; (3)  $V_{C3}$ .

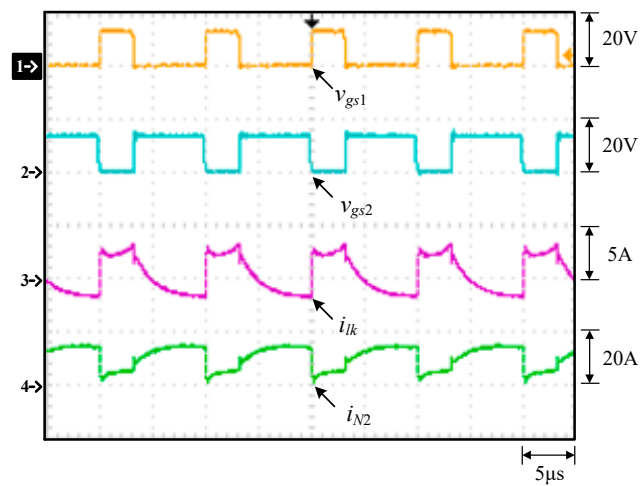


Figure 18. Measured waveforms at rated load: (1)  $v_{gs1}$ ; (2)  $v_{gs2}$ ; (3)  $i_{lk}$ ; (4)  $i_{N2}$ .

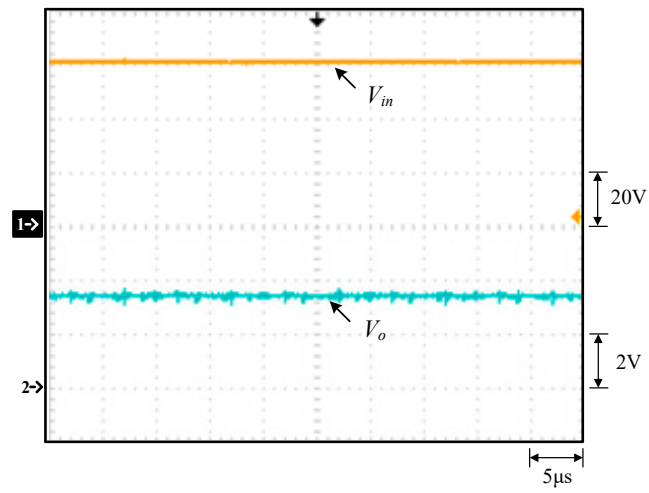


Figure 19. Measured waveforms at rated load: (1)  $V_{in}$ ; (2)  $V_o$ .

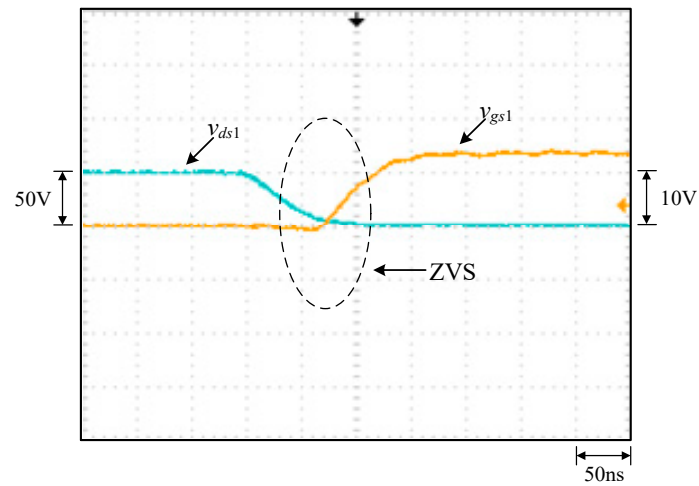


Figure 20. Zoom-in of the turn-on transient of  $Q_1$ .

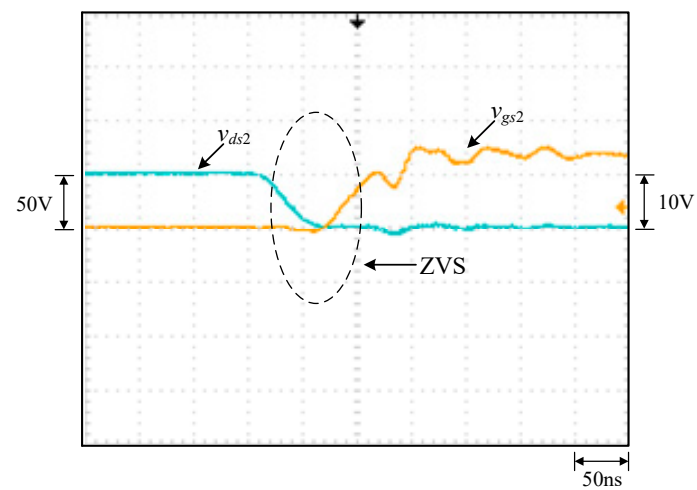
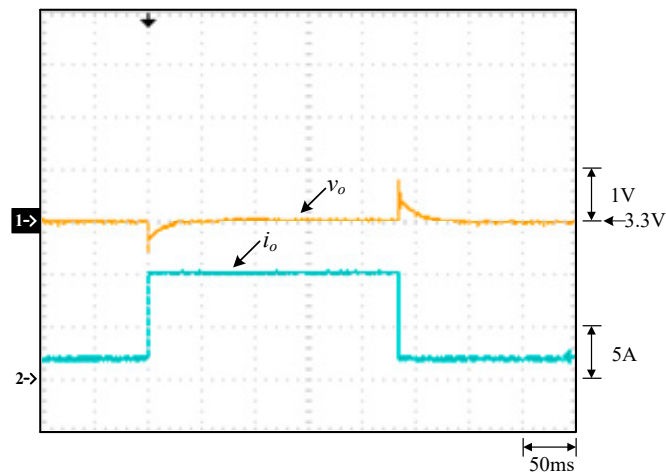
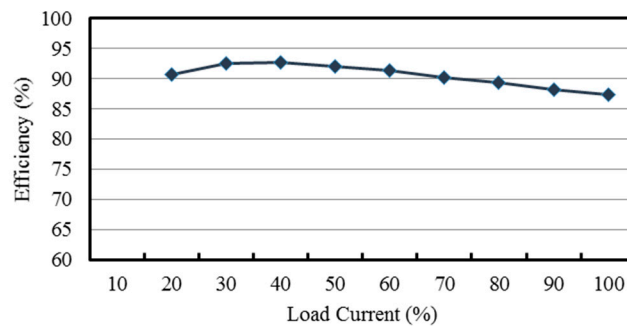


Figure 21. Zoom-in of the turn-on transient of  $Q_2$ .



**Figure 22.** Output voltage responses due to load transients from light/rated load to rated/light load.



**Figure 23.** Curve of efficiency versus load current percentage.

From Figure 15, it can be seen that the voltage stress across  $Q_1$  is 48 V, equal to  $V_{in}$  minus  $V_{C2}$  ( $= 60 \text{ V} - 12 \text{ V}$ ), whereas it can be seen that the voltage stress across  $Q_3$  is 12 V, equal to  $V_{in}$  minus  $V_{C1}$  ( $= 60 \text{ V} - 48 \text{ V}$ ) with the voltage spike on  $Q_3$  due to the parasitic capacitance of the switch resonating with the line parasitic inductance and the leakage inductance of the coupling inductor. From Figure 16, it can be seen that the voltage stress across  $Q_2$  is 48 V, equal to  $V_{in}$  minus  $V_{C2}$  ( $= 60 \text{ V} - 12 \text{ V}$ ), whereas it can be seen that the voltage stress across  $Q_4$  is 12 V, equal to  $V_{in}$  minus  $V_{C1}$  ( $= 60 \text{ V} - 48 \text{ V}$ ). From Figure 17, the voltages on  $C_1$ ,  $C_2$  and  $C_3$ , namely,  $V_{C1}$ ,  $V_{C2}$  and  $V_{C3}$ , are almost kept constant at some values. From Figure 18, it can be seen that there are some differences in  $i_{lk}$  and  $i_{N2}$  between the waveforms shown in Figure 4 and these measured waveforms. This is because the leakage inductance of the coupled inductor will resonate with the energy-transferring capacitors. From Figure 19, it can be seen that the output voltage can be stably kept at 3.3 V under the input voltage of 60 V. From Figures 20 and 21, it can be seen that the switches  $Q_1$  and  $Q_2$  have ZVS turn-on since these two switches are switched on after individual body diodes are turned on, corresponding to states 1 and 4 in Section 2. Figure 22 shows the load transient response from light load to rated load with a undershoot of 600 mV and a recovery time of 30 ms, and the load transient response from rated to light load with an overshoot of 800 mV and a recovery time of 55ms. Figure 23 shows that the overall efficiency is above 87.4% and can be up to 92.7%.

## 6. Conclusions

The proposed step-down converter comes from the converter [28]. Although the former, with one additional capacitor, has larger number of components than the latter has, the former has a higher voltage conversion ratio and lower voltage stresses on the switches than the latter has if the value of turns ratio is chosen reasonably. In addition, the portion of the leakage inductance energy in the former can be recycled to the input via the active clamp circuit during the turn-off period.



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