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An Output Capacitor-Less Low-Dropout Regulator with 0–100 mA Wide Load Current Range

Jihoon Park [1], Woong-Joon Ko [2], Dong-Seok Kang [1], Yoonmyung Lee [1,*] and Jung-Hoon Chun [1,*]

[1] College of Information and Communication Engineering, Sungkyunkwan University, Suwon 16419, Korea; jhpark09@skku.edu (J.P.); naviation@skku.edu (D.-S.K.)
[2] Samsung Electronics Co. Ltd., Hwaseong 18448, Korea; woongjun.ko@samsung.com
* Correspondence: yoonmyung@skku.edu (Y.L.); jhchun@skku.edu (J.-H.C.); Tel.: +82-31-299-4596 (J.-H.C.)

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Abstract: An output capacitor-less low-dropout (OCL-LDO) regulator with a wide range of load currents is proposed in this study. The structure of the proposed regulator is based on the flipped-voltage-follower LDO regulator. The feedback loop of the proposed regulator consists of two stages. The second stage is turned on or off depending on the variation in the output load current. Hence, the regulator can retain a phase margin at a wide range of load currents. The proposed regulator exhibits a better regulation performance compared to the ones in previous studies. The test chip is fabricated using a 65-nm CMOS process.

Keywords: low-dropout regulator; flipped voltage follower; wide load current range; output capacitor-less low-dropout regulator

1. Introduction

Power management of mobile devices and communication networks have been advancing with the growing number of mobile consumer electronics and Internet of Things (IoT) devices. To improve their power efficiency and battery life, multiple levels of engineering efforts have been conducted from system-level optimization [1–4] to device-level power management such as dynamic voltage and frequency scaling [5–8]. Digital systems and system-on-chip devices usually have multiple voltage domains that need to be adjusted reflecting dynamic variations of load conditions. As a result, there is a great demand of power management integrated circuits (PMICs) with a high energy efficiency and accuracy across wide load ranges.

A PMIC takes battery power as input and provides clean power to core blocks such as an application processor (AP). Generally, core blocks require multiple levels of power, therefore, the PMICs contain several low-dropout (LDO) regulators to provide them. Because analog LDO regulators are generally targeted for sensitive circuits, it is important to attain a high power supply rejection (PSR) and fast response while maintaining a high energy efficiency and sound stability. A popular method of retaining the loop stability of an LDO regulator is by connecting a large off-chip capacitor to the output node. As PMICs contain a large number of LDO regulators, the loss of PCB area due to multiple off-chip capacitors cannot be ignored, particularly in mobile applications that require a small form factor. To overcome this problem, output capacitor-less LDO (OCL-LDO) regulators have been studied. One of the previous studies on the OCL-LDO regulator is an ultra-fast load-transient LDO regulator [9]. However, it uses a 600-pF decoupling capacitor, which consumes a large silicon area and may not be suitable for mobile PMICs. A full on-chip LDO regulator was introduced by Milliken et al., but it has a low loop gain resulting in a low power supply rejection ratio (PSRR) [10]. An ultra-low-power OCL-LDO regulator proposed in Reference [11] shows the best performance.

However, its performance is susceptible to process variations. Flipped voltage follower (FVF) based LDO regulator designs have been developed [12–15]. A basic FVF-based LDO regulator has a simple folded structure, but it exhibits poor regulation characteristics [12,13]. In Reference [14], a dynamic biasing technique was acquired to improve the poor regulation characteristics, but its loop gain and PSR characteristics still required improvements. In Reference [15], the feedback loop of the LDO regulator has an additional second stage for a better PSR and regulation characteristics. However, it demands a minimum load current of 1–3 mA to maintain loop stability, thereby degrading the power efficiency under a light load condition. This study presents an FVF-based LDO regulator, which is stable even under a light load condition (0–1 mA).

This paper is organized as follows. The design challenges of conventional LDO regulators are described in Section 2. Section 3 presents the overall architecture of the proposed LDO with a detailed explanation of the implemented circuits. Section 4 shows the chip measurement results. Finally, Section 5 presents the conclusions.

2. Conventional LDO Regulators

2.1. Output Capacitor-Less LDO Regulator

Regulators can be classified as linear and switching regulators. Among these, linear regulators can supply clean power without noise, but they have a poor power efficiency due to a voltage drop (dropout voltage) in the variable resistor. The regulator structure that minimizes the dropout voltage is called an LDO regulator. Figure 1 shows the structure of a conventional LDO regulator. It takes input power at V_{IN} and allows V_{OUT} to provide clean output power. V_{OUT} is designed to maintain a constant value through the negative feedback path consisting of an op-amp and a variable resistor R_P. R_{OUT} and C_{LOAD} refer to the resistance and capacitance of the output stage, respectively. The variable resistor R_P is implemented using a transistor called a power transistor. Because the feedback loop in Figure 1 is a system with at least two poles, frequency compensation is necessary for ensuring loop stability. In this case, a common method is to connect the output stage with the capacitor C_{OUT} that has a large value in μF, so that the pole of the output is always dominant. Although this method can easily perform frequency compensation, there exists the disadvantage of PCB area loss due to C_{OUT}. The LDO regulator introduced in Reference [9] succeeded in ensuring loop stability without external capacitors but used a 600-pF MIM capacitor to achieve a fast response. Although the PCB area was reduced successfully, a large amount of silicon area had to be used for the MIM capacitor, making it unsuitable for LDO regulators in mobile applications.

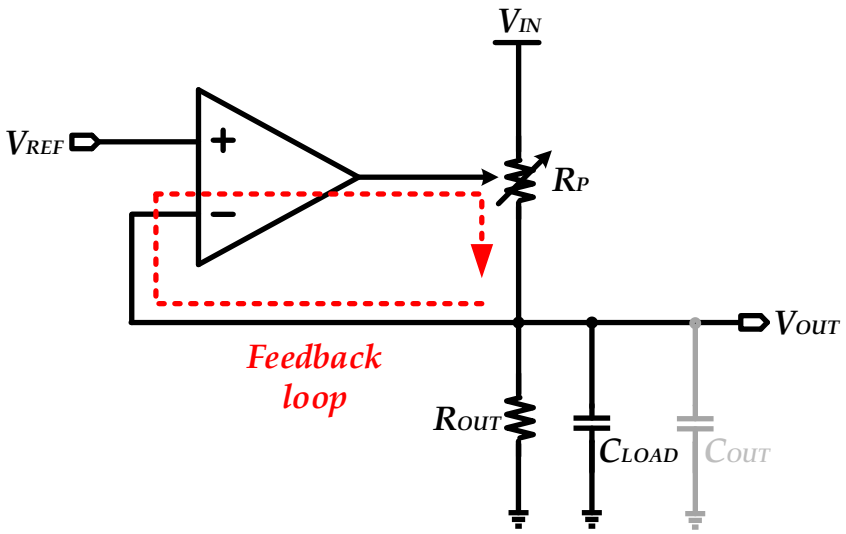


Figure 1. Conventional low-dropout (LDO) regulator.

2.2. FVF-Based LDO Regulator

Figure 2 shows the basic structure of an FVF-based LDO regulator [12]. The regulator is composed of M_P, the power transistor of the regulator, M_{C1}, which senses the output voltage and adjusts the gate voltage of M_P through the negative feedback, and I_{BIAS1}, the current source. The biasing circuit on the right side determines V_{CTRL}, the gate bias voltage of M_{C1}. The source voltage of M_{C2} is fixed at V_{REF} by the negative feedback of the biasing circuit. As M_{C1} and M_{C2} have the same bias current ($I_{BIAS1} = I_{BIAS2}$) and aspect ratio, they have the same source voltage. Therefore, in the steady state, V_{OUT} is determined as follows:

$$V_{OUT} = V_{CTRL} + V_{SG}\,(of\ M_{C1}) = V_{REF} \tag{1}$$

If output current increases abruptly, V_{OUT} will decrease momentarily. M_{C1} will detect this variation of V_{OUT} and the voltage at node X, which is the gate voltage of the power transistor M_P, decreases accordingly. That is, the current flowing through M_P will increase and recover V_{OUT} to its initial level. In contrast, if the output current decreases rapidly, the gate voltage of M_P will increase and restrain V_{OUT} from increasing. The output load capacitance of the output capacitor-less LDO is primarily attributed to the parasitic capacitance of the power lines and it is typically less than 50 pF. Because the output impedance of the FVF-based LDO regulator is reduced drastically by the loop gain of the regulator feedback path, this feedback pushes the pole created at the output node away from a unit gain frequency of the regulator. As a result, the dominant pole is determined by the gate capacitance of the power transistor M_P, not by the output load parasitic capacitor.

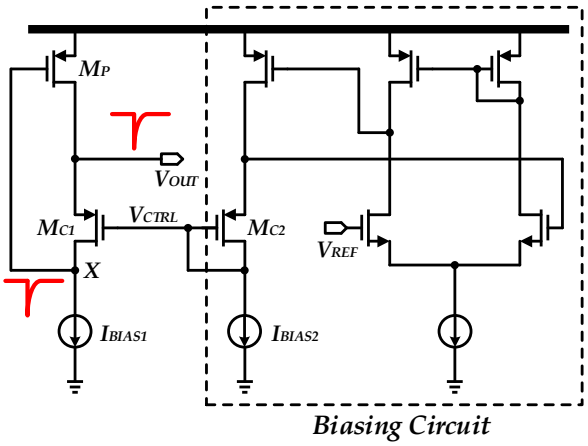


Figure 2. Flipped voltage follower (FVF)-based LDO regulator [12].

2.3. Voltage Spike Detection of FVF-Based LDO Regulator

A major disadvantage of the FVF-based LDO regulator is its poor load regulation characteristics. To overcome this, Milliken et al. [9] used a very large bias current (6 mA) to achieve the maximum bandwidth of the regulator. However, this technique is not applicable in mobile applications using limited battery power. Or et al. [14] proposed a dynamic bias method that drives the circuit with a minimum operating current with a maximum operating current only when a high driving current is required. The waveform of the relationship between output current and quiescent current is shown in Figure 3.

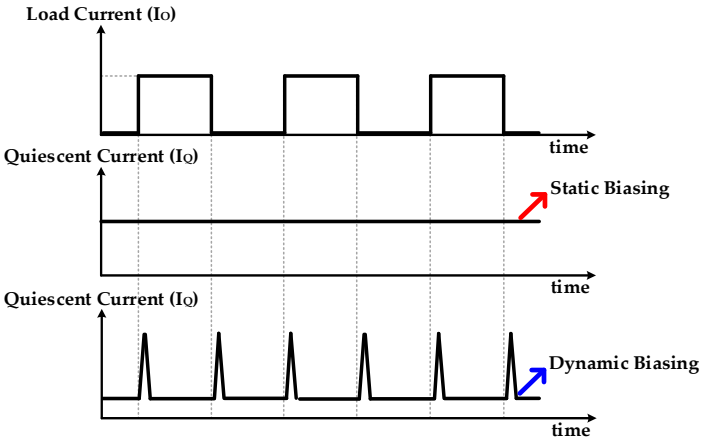


Figure 3. Relationship between output current and quiescent current of an LDO regulator.

Figure 4 shows the structure and operating waveform of the voltage spike detecting current mirror [14]. A sudden change in the amount of current flowing through the output stage results in an abrupt change of the output voltage (emulated with a pulse voltage source in Figure 4). During this, only the high frequency component of the output voltage variation passes through C_1 and affects node X leading to a rise in its voltage. Afterwards, the node X voltage is gradually recovered to the original value due to the R-C time constant of node X. Because the voltage at node X is the gate-source voltage of M_2, the bias current (I_{BIAS}) instantaneously increases, as shown in Figure 4 and then returns to its original value.

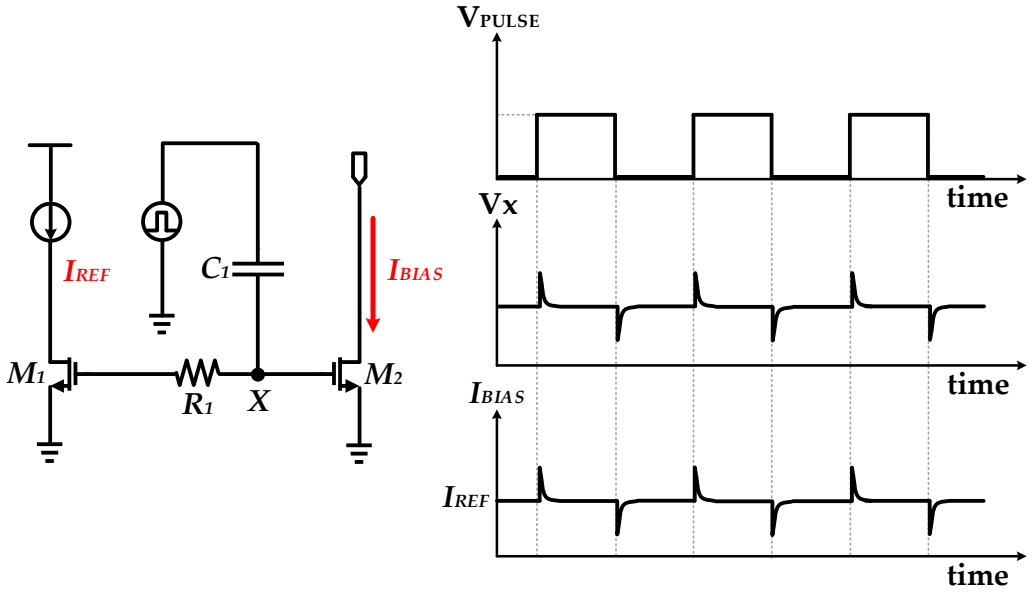


Figure 4. Operation principle of voltage spike detection circuit.

Figure 5 shows a structure that combines a FVF-based LDO regulator with a current mirror that detects voltage spikes. C_{PAR} refers to the gate-stage parasitic capacitance of power transistor M_P. To respond to abrupt voltage changes at the output stage, it is necessary to rapidly charge or discharge the C_{PAR}. When a voltage overshoot occurs in the output stage, the C_{PAR} can be charged quickly through the overshoot detection circuit consisting of $M_{UP1,2,3}$, C_{UP}, and R_{UP} as shown in Figure 5a. Conversely, as shown in Figure 5b, when an undershoot occurs, the C_{PAR} gets discharged fast through the M_{DN3} which is triggered by the undershoot detection circuit consisting of $M_{DN1,2,3}$, C_{DN}, and R_{DN}. The bandwidth of the overshoot detection circuit can be adjusted by changing the $R_{DN/UP}$ and $C_{DN/UP}$ values. Owing to a fast loop response, this structure can respond faster to sudden V_{OUT} changes than a

conventional FVF-based LDO regulator. However, because the main loop of the regulator is composed of only one stage, the loop gain is too small to achieve a sufficient PSRR.

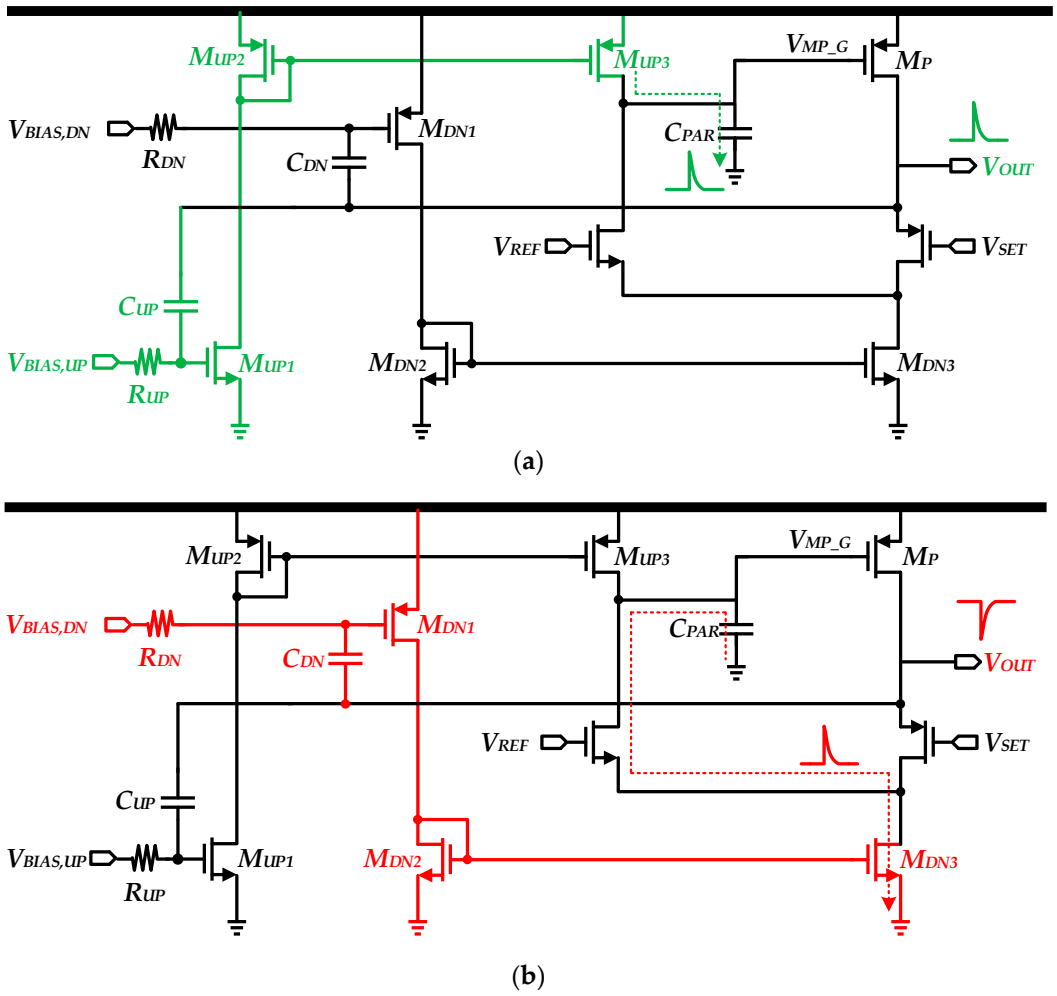


Figure 5. Operation principle of voltage spike detection FVF-based LDO regulator. (**a**) under overshoot condition; (**b**) under undershoot condition.

2.4. Loop-Gain-Enhanced FVF-Based LDO Regulator

Comparing to the conventional FVF-based LDO regulator, the circuit in Figure 6 has an additional stage to increase the loop gain. However, as the number of stages increases, the frequency compensation of the loop becomes complicated. Similar to the voltage spike detection regulator described earlier, this architecture also uses a dynamic bias current source. C_M in Figure 6 serves as a Miller capacitor for frequency compensation and it detects the undershoot voltage at the output stage and discharges the gate capacitor of M_P through M_{DISC}. On the other hand, C_1 senses the overshoot of V_{OUT} and allows a large amount of current to flow to the gate capacitor of M_P through M_C. Adding this second stage increases the loop gain, which improves regulator performance such as the load and line regulation and PSRR. However, the disadvantage of this regulator is that a certain amount of output current must always flow through the output stage to ensure loop stability. According to a study [15], this minimum driving current should be at least a few milliamperes in a 90-nm process. As a result, although the regulation characteristics are improved through the loop gain enhancement and frequency compensation, the power efficiency in a low-power state still needs to be improved.

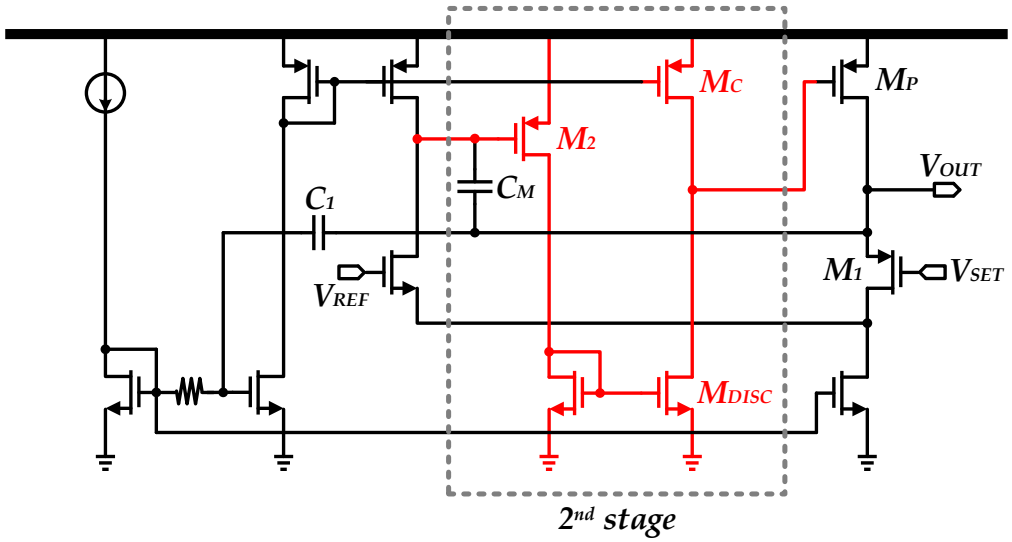
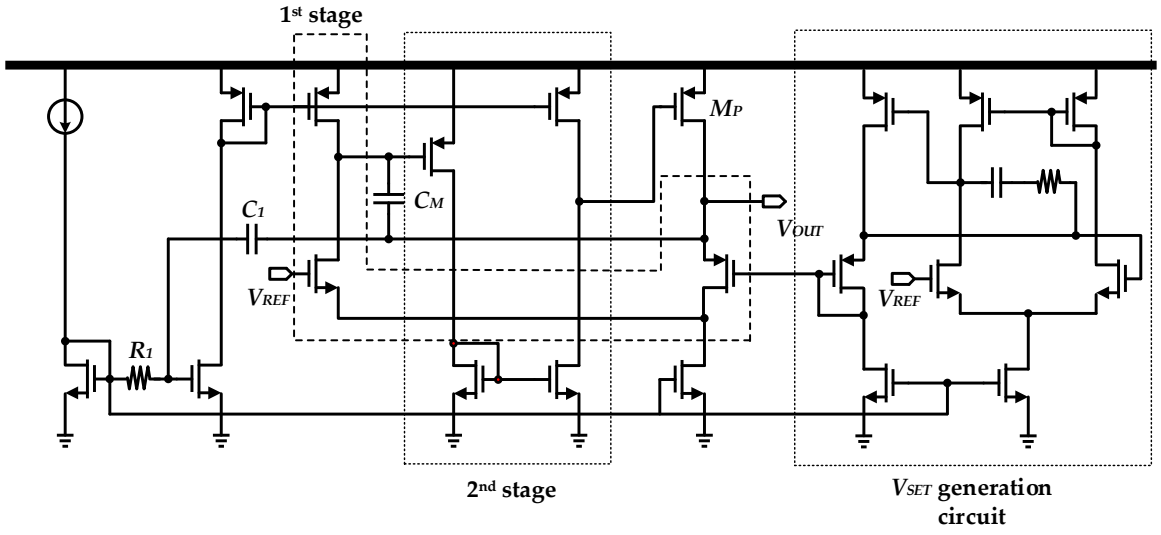


Figure 6. Structure of an LDO regulator based on a loop-gain-enhanced FVF [15].

3. Proposed LDO Regulator

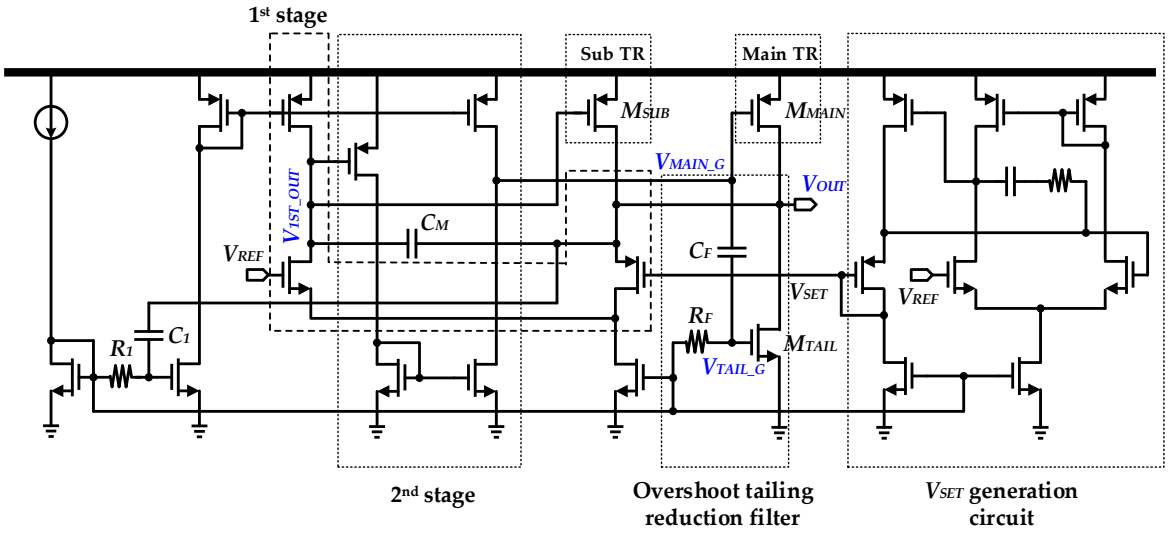
Figure 7a shows a full schematic representation of the enhanced loop gain FVF-based LDO regulator [15] originated from a basic FVF-based LDO regulator [12]. When compared with the basic regulator [12], the enhanced loop gain regulator has an additional second gain stage to boost the total loop gain of the regulator. However, this LDO regulator requires a certain amount of load current to achieve loop stability. If the regulator is under a light load condition, a complex pole is generated, degrading the stability of the loop and causing a long settling behavior.

Figure 7b shows a full schematic representation of the proposed LDO regulator. The main idea of this regulator is that its operating mode is altered based on the level of the load current. If the load current is low, the regulator operates as a basic FVF-based LDO regulator [12]. However, if the load current is increased, the proposed regulator operates as an enhanced loop gain FVF-based LDO regulator [15]. As shown in Figure 7b, the proposed regulator mainly comprises a simple folded FVF as its first stage, a common-source structure as its second stage, a main power transistor (M_{MAIN}), and a subsidiary power transistor (M_{SUB}). In this circuit, the second stage and M_{MAIN} are adaptively turned on or off depending on the output load current.



(**a**)

Figure 7. *Cont.*



(**b**)

Figure 7. Full schematic representations of LDO regulators: (**a**) loop gain enhanced FVF-based LDO regulator [15] and (**b**) proposed LDO regulator.

The operating mechanism of the proposed regulator is illustrated in Figure 8. Figure 8a shows the case where the load current reduces to less than 1 mA. It should be noted that this light load condition is not easily supported by the regulator in Reference [15]. In the proposed regulator, the gate voltage of M_{SUB} is reduced by the first stage and M_{SUB} is weakly turned on. M_{SUB} is designed to have a small size (144 µm/0.06 µm), yet it can afford to drive the current under a light load condition. However, the second stage is almost turned off when the load current is extremely low. Even if the second stage is weakly turned on, the response of M_{MAIN} is much slower than that of M_{SUB}. In other words, when the regulator is under a light load condition, we can consider that only M_{SUB} is turned on while the second stage and M_{MAIN} are turned off. The proposed regulator operates like a basic FVF-based LDO regulator.

If the load current of the regulator is increased, the voltage level of node X (the gate of M_{SUB}) is further reduced. Therefore, the second stage is turned on and it adds a considerable gain as M_1 enters the saturation region. Under a heavy load condition, the first stage, second stage, M_{MAIN}, and M_{SUB} are fully turned on. However, the driving current of M_{SUB} is one-tenth of that of M_{MAIN}. Therefore, the effect of M_{SUB} can be ignored as in Figure 8b. Consequently, under a heavy load condition, the proposed regulator operates as an enhanced loop gain FVF-based LDO regulator [15]. Moreover, it switches its operating mode depending on the amount of output load current. Hence, it can achieve stability even if the output load current is extremely low.

The proposed regulator is not a push-pull regulator. Therefore, it is difficult to recover the overshoot voltage at the output node. In this proposed circuit, an overshoot tailing reduction filter is introduced to prevent the output tailing voltage. The drain of M_{TAIL} is connected to the output node and the gate voltage of M_{MAIN} is filtered once and then connected to the gate node of M_{TAIL}. When the output current is switched from a heavy to a light load, a high pass filter, which consists of R_F and C_F, detects the gate voltage of M_{MAIN} and it momentarily increases the discharging current flowing through M_{TAIL}. As a result, the output overshoot voltage is suppressed.

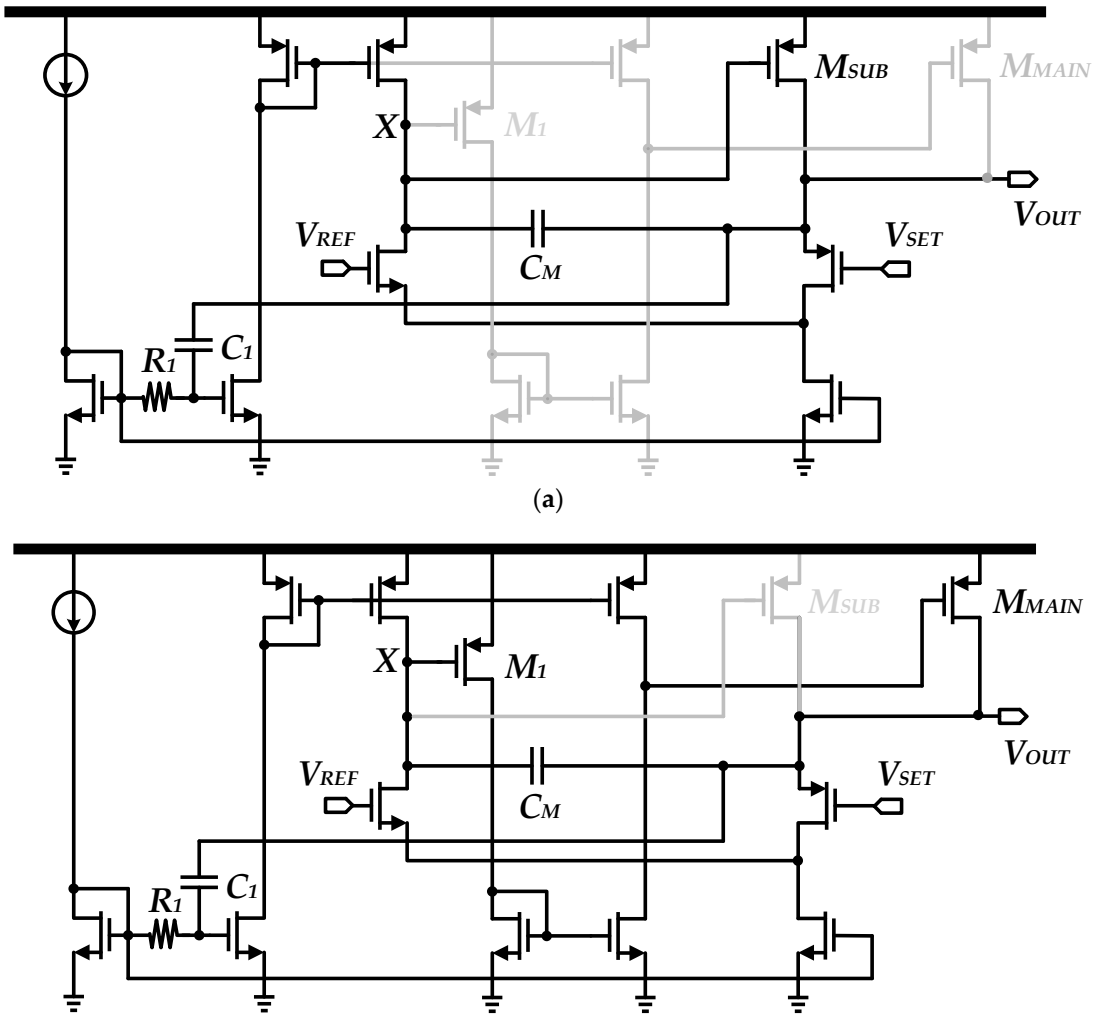


Figure 8. Operation principle of the proposed LDO. (**a**) with a light load current; (**b**) with a heavy load current.

Figure 9 shows the simulated transient responses of the proposed and conventional FVF-based LDO regulators. The constant input voltage of 1.2 V is supplied and the load current is changed from 0 to 100 mA and vice versa. The rising and falling time of the load current is approximately 100 ns. Both LDO regulators have a constant output voltage of 1 V. The undershoot voltages of the proposed and conventional LDO regulators are 183 and 432 mV, respectively, and the overshoot voltages are 108 and 215 mV. We could confirm that the transient characteristics are significantly improved by the additional gain stage and the overshoot tailing reduction filter of the proposed LDO regulator.

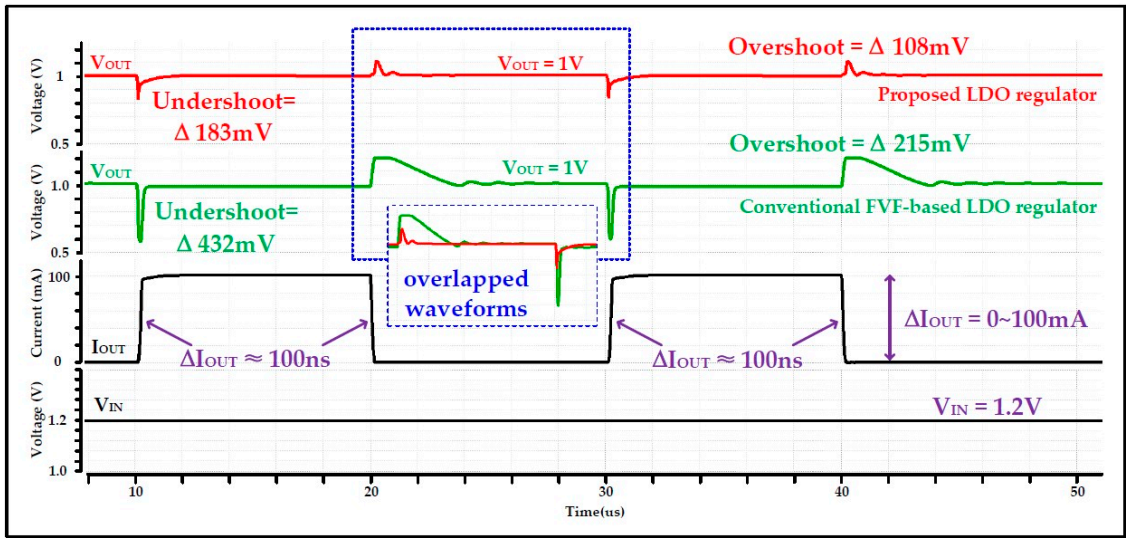


Figure 9. Simulation results of transient responses with load current variations.

Figures 10 and 11 show how the internal nodes of the proposed and conventional FVF-based LDO regulators behave while the load conditions abruptly change. Figure 10a shows the simulated voltage waveforms of the two important nodes of a conventional FVF-based LDO regulator: V_{OUT} (the output node of the LDO regulator) and V_{MP_G} (the gate node of the power transistor, M_P in Figure 5). When the load current is changed from 0 to 100 mA, V_{OUT} drops first, but it is finally recovered to the initial voltage owing to the negative feedback circuit described in Figure 5. That is, V_{OUT} rises again to the desired target as the gate voltage of the power transistor drops with approximately 487-ns delay. This delay is significantly shortened by inserting an additional stage in the proposed LDO regulator. Figure 10b shows the simulated waveforms of the proposed LDO regulator's internal nodes: V_{OUT}, V_{1ST_OUT} (the output of the 1st stage), and V_{MAIN_G} (the output of 2nd stage). When the load current is changed from light to heavy, V_{1ST_OUT} and V_{MAIN_G} ramps down approximately 1.8 times faster than V_{MP_G} of the conventional FVF-based LDO regulator and achieving 1.8 times smaller undershoot.

The simulation results in Figure 11 explain how the overshoot voltage is further suppressed by the overshoot tailing reduction filter. When the load current changes from 100 to 0 mA, V_{OUT} is instantaneously increased. Almost simultaneously, V_{TAIL_G} (the gate node of M_{TAIL} in Figure 7b) also ramps up because of the coupling through the overshoot tailing filter and it momentarily increases the discharging current flowing through M_{TAIL}. As a result, the output overshoot voltage is suppressed effectively and the duration of overshoot is reduced by approximately 3.5 times.

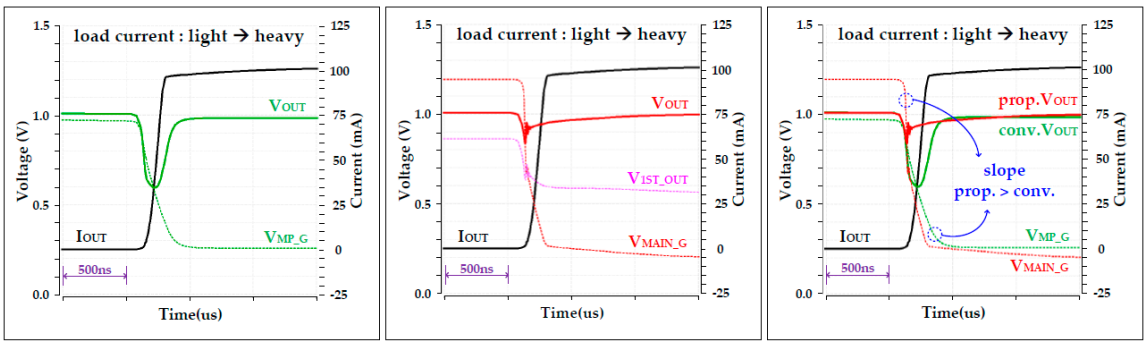


Figure 10. Simulation results of internal nodes' transient responses: (**a**) conventional LDO regulator, (**b**) proposed LDO regulator and (**c**) comparison between conventional and proposed LDO regulators. (The load current is changed from 0 to 100 mA with 100-ns rising time).

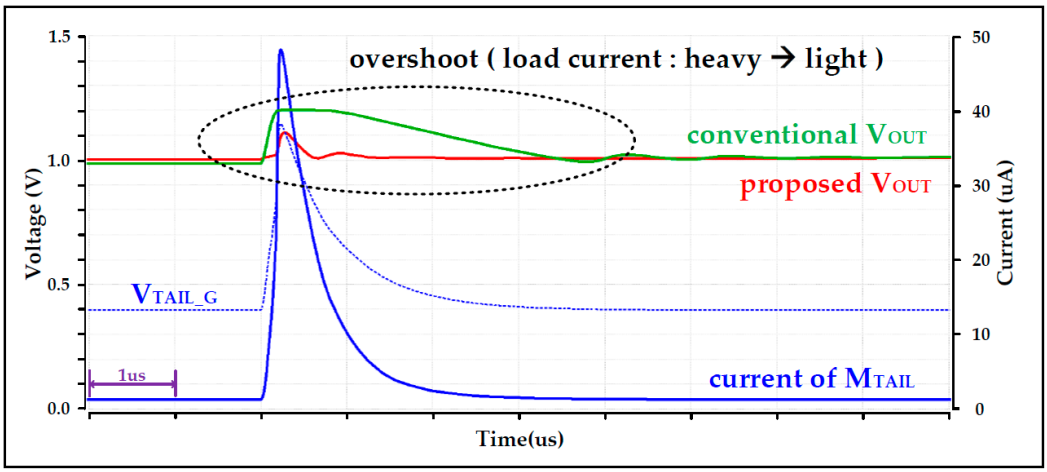


Figure 11. Simulation results of the overshoot tailing reduction filter. (The load current is changed from 100 to 0 mA with 100-ns falling time).

4. Measurement Results and Comparison

The proposed OCL-LDO regulator was fabricated using a 65-nm CMOS process. The chip micrograph is shown in Figure 12. Because of the metal filling in the process, it is difficult to distinguish the active area of the LDO in the micrograph. Therefore, we superimposed the layout with the micrograph. The LDO block occupies only 0.027 mm^2 (270 µm × 100 µm). The additional blocks such as the 2nd gain stage and the overshoot tailing reduction filter occupy approximately 10% of the total area.

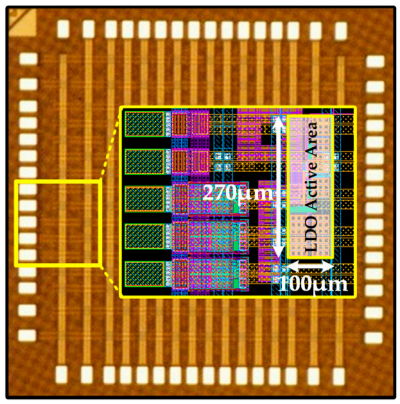


Figure 12. Micrograph of proposed LDO regulator.

Figure 13 illustrates the measured load-transient responses. The waveform at the top shows the output voltage when the load current is changed from 0 to 100 mA and vice versa. The waveform at the bottom shows an enlarged image of the undershoot and overshoot that occur when the load current is changed from 0 to 100 mA and 100 to 0 mA, respectively. The target output voltage of the proposed LDO regulator is 1 V. The measured output voltage is 1 V ± 18 mV. The maximum undershoot and overshoot voltages are 228 and 112 mV, respectively. In [15], the overshoot time delay of the LDO regulator based on the enhanced loop gain is approximately 5 µs, whereas, in the proposed LDO regulator, the overshoot tailing reduction filter (Figure 7b) reduces the overshoot time delay to approximately 1.5 µs.

In Table 1, the performance of the proposed LDO regulator is compared with that of the previous capacitor-less LDO regulators. First, the proposed LDO has a wider range of load current, from 0 mA to 100 mA, whereas References [12,16] have a limited range of less than 50 mA and Reference [15] does

not support ultra-light load conditions. The proposed LDO regulator is also competitive in terms of the quiescent current, response time, settling time, PSR, and load regulation capability.

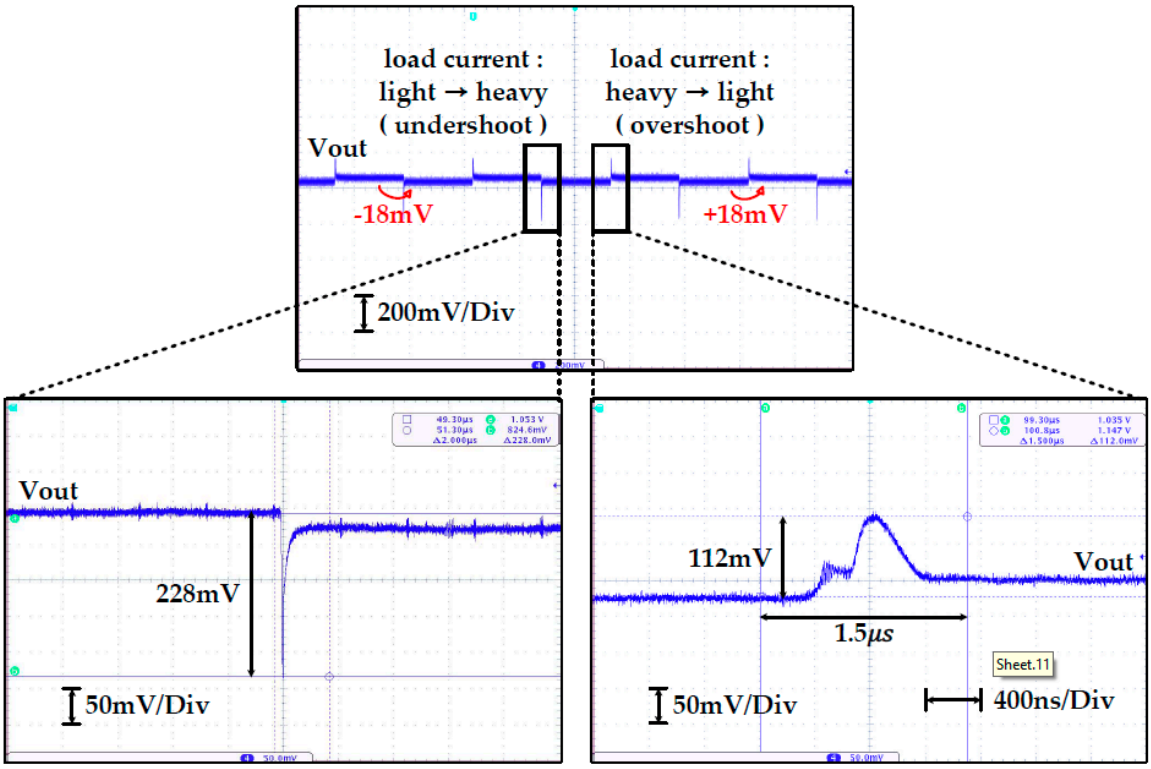


Figure 13. Measured load–transient response of the proposed LDO regulator with load current variation (0–100 mA).

Table 1. Performance comparison of capacitor-less LDOs.

Parameters	TCAS-I 2008 [12]	JSSC 2010 [15]	TCAS-I 2015 [16]	This Work
Process [nm]	350	90	65	65
LDO Type	Analog	Analog	Analog	Analog
Input Voltage [V]	1.2	0.75–1.2	1.2	1.2
Output Voltage [V]	1	0.5–1	1	1
Load Current Range [mA]	0–50	3–100	0–10	0–100
Max Load Current, I_{MAX} [mA]	50	100	10	100
Quiescent Current, I_Q [μA]	95	8	50–90	30
Peak Current Efficiency [%]	99.81	99.99	n/a	99.97
PSR [dB] @ 10 MHz	n/a	25 @ 10 kHz	<20	26
ΔV [mV] @ Load Step [mA]	164 @ 50	114 @ 97	82 @ 10	228 @ 100
Response Time, T_R [ns] [1]	3.28	0.057	1.15	0.228
Settling Time [ns]	<300	5000	>100	<2000
Load Regulation [mV/mA]	0.28	0.1	1.1	0.18
Total On-chip Capacitor [nF]	Not required	Not required	0.14	Not required
Active Area [mm^2]	0.0448	0.019	0.023	0.027
FOM1 [ps] [2]	6.232	0.005	5.74	0.068

[1] $T_R = C_{OUT} \times \Delta V / I_{MAX}$ [9]; [2] FOM1 = $T_R \times I_Q / I_{MAX}$ [9].

5. Conclusions

We proposed a 65 nm CMOS OCL-LDO regulator, which is stable even under a light load condition. Under a heavy load condition, this regulator operates as an enhanced loop gain FVF-based LDO regulator. However, under the light load condition, the second stage is turned off and the proposed regulator operates as a basic FVF-based LDO regulator. As a result, the proposed regulator can achieve

a full-range stability from 0 to 100 mA. Furthermore, the overshoot tailing reduction filter helps the regulator to achieve a better transient response. Compared to the previous literature, the proposed LDO regulator supports a wider range of load current and has a better transient regulation performance.

Author Contributions: J.P. and W.-J.K. proposed and designed the overall architecture of proposed output capacitor-less low-dropout (LDO) regulator. D.-S.K. contributed in test chip design and layout. J.P. performed experiments and evaluated results. Y.L. and J.-H.C. guided and directed the authors for this work.

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Conflicts of Interest: The authors declare no conflicts of interest.

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