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A Study on Improving Switching Characteristics According to a Circuit Analysis Technique in Converter Applications Using Gallium Nitride Field Effect Transistors

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Abstract: In this paper, we studied how the switching characteristics of a power conversion system could be improved using gallium nitride (GaN) devices. To this end, a circuit system applying GaN field effect transistors (FETs) was modeled to derive a mathematical differential equation, and the transfer function of the system was obtained through the modeled equation to propose the analysis model. The frequency response of the system where the GaN FET device was applied was analyzed through the proposed modeling circuit, and the method to compensate for characteristics of the system was proposed. The applied method and the proposed model were validated through the comparative analysis on the frequency responses before and after the frequency response. This study's results were proposed that the problem occurring in systems with GaN FETs could be solved through this theoretical and systematic method.

Keywords: GaN FET; WBG; frequency response; DC-DC converter; switching characteristics

1. Introduction

The development of silicon semiconductor devices has been steadily increasing over the last few decades. In the power conversion system field, significant advances have been made in power conversion system technology alongside the development of various structures, circuit topologies, and control technologies by the use of power switching devices. However, the limitations to the technical development of silicon semiconductors have appeared, no further technical improvements to silicon semiconductor devices are expected. More than ever, today's power systems require high power and density. The high density has been achieved alongside the development of packaging and bonding technologies. Since some 10 years ago, gallium nitride (GaN) technology has been spotlighted as representing next-generation power semiconductor devices that can replace silicon semiconductor devices. In particular, GaN devices have many advantages, such as a wide bandgap (WBG), low on-resistance, high electron transfer speed due to their heterostructure, high on-off speed due to their high electron mobility transistor (HEMT) structures, and excellent high-temperature characteristics. Thus, GaN devices are suitable for using in high-density and high-power systems, and this can be accomplished with a much smaller size than that of a silicon semiconductor device in high-speed switching operations. Since GaN devices have a wider bandgap than other devices do, they have had an electric breakdown field 10 times stronger than that of silicon semiconductor devices, thus, they can be used even at high voltages and high temperatures. GaN devices have a heterostructure that bonds the materials of differing bandgaps. A two-dimensional (2D) channel is formed by creating a 2D electron gas (2DEG) induced by polarization, thereby isolating impurities and minimizing the scattering effect, and resulting in a high electron density and a high electron mobility [1]. Thus, the

high frequency switching can be accomplished because high-speed operations are possible, and low on-resistance characteristics can be maintained, thereby enabling high-density and high-power system development, which follow the current trends of the power system development.

Further studies on power system development using WBG devices have been undertaken, and the GaN device market has grown, particularly in Asia [2]. A variety of studies on GaN devices have also been accomplished. For example, a study was conducted on quantitatively extracting the transient characteristics of GaN semiconductors, as this information was not explicitly given by suppliers, and another study analyzed GaN devices' loss characteristics compared to those of metal-oxide-semiconductor field-effect transistors (MOSFETs) [3]. A study has also been conducted on reduction in parasitic inductance components by ensuring that the bonded wires inside field-effect transistors (FETs) are as close together as possible. Notably, the ringing phenomenon, which occurs in the transient state of GaN devices, is the result of the low turn-on threshold voltage and the small parasitic capacitance of GaN devices. A fast switching operation can be achieved due to this small parasitic capacitance, but GaN devices have a relatively large dV/dt ratio, thereby generating noise due to the parasitic capacitance and the stray inductance resonance of the FET, and the printed circuit board (PCB). Thus, Faulty turn-on may be occurred as a result, which creates a serious problem. Therefore, the study to address this issue was accomplished [4–7].

Most studies have been focused on hardware improvements for GaN devices. However, since their improvements depend on the experiences and the know-how of PCB designers, or circuit designers, they do not lead to universal technical advancements. To overcome this limitation, a study has been proposed to remove input signal noise and resonance frequency signals by applying a noise removal circuit to improve the frequency response, thereby compensating for the phase delay through software [8]. The present study derived a system as a theoretical mathematical modeling equation by which the systematic noise removal circuit could be applied and the frequency response characteristics could be analyzed. This study then presented a model through which the system's characteristics could be analyzed theoretically rather than by applying to a general low-pass filter to blindly remove high-frequency signals, as was attempted in previous studies, and proposed the method of applying to the optimal filter to the system by analyzing its frequency response characteristics. This study also proved the validity of the proposed method through their results using the presented method.

2. Derivation of the System Characteristics

Figure 1 shows the process of designing and manufacturing a conventional power conversion system. First, the circuit design is started as shown in Figure 1, and then the system is completed through the PCB design and fabrication. As mentioned in Section 1, GaN devices have unwanted high frequency noise due to the GaN properties and the stray inductance components in the circuit. This increases switching losses, resulting in lower system efficiency.

Figure 1. The traditional WBG device system design and compensation flow.

To solve this, you can compensate by adding a filter. However, simply just applying a filter that removes high frequency noise without considering the characteristics of the system will not only achieve the desired results, but also slow down the dynamics of the system. This causes problems such as phase delay. It also causes faulty turn-on problem in other power conversion systems (especially, complementary output devices). Therefore, in order to solve these problems, we proposed a method for compensating the above problems in domestic papers. However, this method was not a perfect compensation method after all.

Therefore, as shown in Figure 2, we propose a modeling method with a theoretical and mathematical using circuit analysis technique (CAT). In addition, we propose a method to improve the characteristics of power conversion system using GaN devices by analyzing the frequency response of the system and designing the filters using the results. First, separate the converter's topology into two circuits. To do this, the capacitors coupled to input and output are separated using Miller's theorem, and we model it as a dependent current source to reflect the operation at the gate stage as the drain stage. After that, the voltage-current relationship was derived by using the operation mode in each circuit, and the transfer function of the system was derived. The derived transfer function obtains the frequency response using an analysis tool such as MATLAB, and uses this information to design appropriate filters and predict the results. Thus we can design optimized filters and add it to the actual circuit, effectively removing high frequency noise, reducing switching losses, and increasing system efficiency. Therefore, as compared with the conventional compensation method, it is possible to ensure quick response characteristics with little phase delay of the signals.

Figure 2. The proposed WBG device system design and compensation flow in this paper.

2.1. System Modeling

Figure 3 shows a step-down converter, the most basic power conversion topology. Here, GaNFETs are modeled as FETs with stray inductance and parasitic capacitance as highlighted in blue. The sensing and control parts are not considered in this study. The gate driver can be configured with various types

of drives, such as totem-pole, bootstrap, transformer-coupled, and direct drive, as shown in Figure 3, depending on the needs and design of the circuits. However, this diversity and design freedom make up the unwanted RLC resonant circuit in the system, which may cause the unsuspected operation and noise. In Figure 3, in order to theoretically analyze the frequency response, the parasitic capacitance are separated by the Miller effect and divided into two parts to reflect the operating characteristics. A simple concept circuit for this was shown in Figure 4.

Figure 3. The step-down power conversion system structure with GaN FET, internal parameters and stray components.

Figure 4. The concept of circuit separation to divide into two parts.

Conceptually, this is similar to conventional MOSFET small-signal equivalent circuits, but in contrast to finding AC components, this study separated the circuit into two parts, taking into account the circuit's operating characteristics and the Miller effect. Therefore, we propose a method of analyzing

both small and large signals at the same time and obtaining a transfer function for analyzing the frequency response. The GaN FET has fast electron moving speed and wide band gap, which is advantageous for high speed operation compared to existing FETs, and has the advantage of operating at high temperature without heat radiation design. However, compared to MOSFETs the switching is unstable due to relatively small parasitic capacitance components and low threshold voltages. These can be further exacerbated when high frequency noise components have frequencies near the resonance point in the system. Therefore, through the analysis and method proposed in this study, the frequency response analysis and filter design can be approached more theoretically and practically to ensure stable operation of the system.

Next, the circuit of a GaN FET system was modeled in two parts: the gate-source and the drain-source, from which a mathematical differential equation was derived, thereby deriving the transfer function. The frequency response of the system was analyzed using the derived transfer function, and the filter that removes the section where unnecessary response characteristics are displayed was designed. Then, the system's response after the filter was applied was then analyzed.

To analyze the characteristics of the power conversion system using the GaN FET, the system of the step-down converter using a GaN FET was firstly modeled. As described in the introduction, the system is characterized by being unstable in a transient state due to their low turn-on threshold voltage and low parasitic capacitance. Considering this, the power conversion circuit was modeled and divided into gate and drain sources [9–11]. Figure 5 shows how the drain source circuit was modeled as a circuit device. The operation was divided by time according to the switching operation order (from Mode 0 to 3).

Figure 5. Modeling the drain-source circuit in the GaN FET system: (a) Free-wheeling, powering and resonant mode at transient state at turn on; (b) Powering mode at turn on; (c) Resonant mode at transient state at turn off; (d) Free-wheeling mode at turn off.

Here $i_d = (v_{gs} - v_{gs(th)} \pm \Delta v_{gs-r}) \cdot g_{fs} = k \cdot \Delta i_g$ and g_{fs} is forward transfer conductance, it is for reflecting to drain-source that the gate voltage resonated by the LC at the gate stage. Here, we used information about the current flowing, Δi_g is defined by the component due to the voltage variation of the gate stage with the transfer conductance. k is an adjustment gain constant, and is a proportional constant that adjusts to reflect the change of the voltage at the gate and drain stages. In Figure 5, because the circuit was modeled the drain-source operation, the source and the components (V_{gs} , C_{gs} , L_g and R_g) at the gate stage are short-circuited. However, the operation due to the voltage variation of the gate stage is considered in the drain-source stage by $k \cdot \Delta i_g$. In Figure 6, a gate-source modeling circuit, uses Miller's theorem to isolate C_{gd} capacitance while bringing it to the gate stage. Here C_{ds} can be omitted:

$$\frac{d}{dt} i_d(t) = -\frac{1}{L_d} v_{c1}(t) + \frac{1}{L_d} v_d(t) \quad (1)$$

$$\frac{d}{dt} i_{L_s}(t) = -\frac{R_{ds_on}}{(L_s + L_{dc})} i_{L_s}(t) - \frac{1}{(L_s + L_{dc})} v_{c_o}(t) + \frac{1}{(L_s + L_{dc})} v_{c1}(t) \quad (2)$$

$$\frac{d}{dt} v_{c1}(t) = \frac{1}{(C_{gd} + C_{ds})} i_d(t) - \frac{1}{(C_{gd} + C_{ds})} i_{L_s}(t) \quad (3)$$

$$\frac{d}{dt} v_{c_o}(t) = \frac{1}{C_o} i_{L_s}(t) - \frac{1}{C_o R_L} v_{c_o}(t) \quad (4)$$

Figure 6. Modeling the gate-source circuit in the GaN FET system.

Equations (1)–(4) present the differential equations by which voltage-current equations are derived for the modeled circuit upon being switched on. Please refer Appendix A for the mathematical development process to derive the relational and transfer function equations at the time of switching off. Appendix A will be useful for deriving the transfer function for your system by adding or removing parameters to your system that are different from those proposed in this paper. Through the above defined equation and Appendix A, the final transfer function of the drain-source stage is defined as Equation (5):

$$G(s) = \frac{b_{14}}{\det(\mathbb{F})} \cdot \frac{1}{L_d} = \frac{k_5}{L_d(s^4 + k_1 s^3 + k_2 s^2 + k_3 s + k_4)} \quad (5)$$

Figure 6 shows the gate-source circuit represented as an equivalent circuit. Through this figure, the transfer function can be calculated via Equations (6)–(8) equivalently by the transfer function expansion process between the drain and the source, as calculated above. Please see Appendix A for further details of the mathematical process. We can derive the system transfer function of gate-source circuit as Equation (9) using Equations (6)–(8) and Appendix A:

$$\frac{d}{dt} i_g(t) = -\frac{R_g}{(L_g + L_s + L_{dc})} i_g(t) - \frac{1}{(L_g + L_s + L_{dc})} v_{gs}(t) - \frac{1}{(L_g + L_s + L_{dc})} v_o(t) + \frac{1}{(L_g + L_s + L_{dc})} v_g(t) \quad (6)$$

$$\frac{d}{dt} v_{gs}(t) = \frac{1}{(A_v C_{gd} + C_{gs})} i_g(t) - \frac{1}{(A_v C_{gd} + C_{gs}) \cdot (r'_s)} v_{gs}(t) \quad (7)$$

$$\frac{d}{dt} v_o(t) = \frac{1}{C_o} i_{L_s}(t) - \frac{1}{C_o R_L} v_o(t) \quad (8)$$

$$G(s) = \frac{m_4}{s^3 + m_1 s^2 + m_2 s + m_3} \quad (9)$$

2.2. System Response Characteristic

The system's frequency response characteristics were calculated using the transfer function obtained in Section 2.1. These transfer functions are Equation (5) and Equation (9). The all factors ($k_1 \sim k_5$ and $m_1 \sim m_4$) in Equation (5) and Equation (9) are derived from Table 1 and Appendix A. Figure 7 shows the frequency response of the system as the L_g changes with L_d fixed. It can be seen that the resonance occurs at about 2.08 MHz by the currently designed L_g . As can be seen from the table in Figure 7, the smaller L_g was, the larger the resonant frequency was, and the larger L_g was, the smaller the resonant frequency was. The maximum gain on the system is the largest at 78.6 dB at about 658 kHz. Afterwards, whether L_g is large or small, the maximum gain is reduced. Because parasitic capacitance is not controllable, it is not considered. Capacitance can be added externally, but, since this has the effect of increasing the capacitance component, the resonance frequency band is substantially lowered to the left of the graph. This results in a state where the switching becomes extremely unstable.

Table 1. The parameters of the dc-dc converter system.

Parameter	Value	Parameter	Value
v_{in}	24 V	v_{out}	12 V
i_{in}	7.5 A	i_{out}	15 A
C_{gd}	0.44 nF	k	10
C_{gs}	9.36 nF	r'_s	1 m Ω
C_{ds}	0.01 nF	r_g	0.7 Ω
L_g	0.2 μ H	R_L	1.6 Ω
L_s	0.5 nH	R_{ds_on}	16 m Ω
L_d	0.2 nH	A_v	4.8
L_{dc}	400 μ H	C_o	1 μ F

Figure 7. The system frequency response with variation of gate-inductance (L_g).

Figure 8 shows the frequency response characteristics of the system as the L_d changes with L_g fixed. In the present state, L_d causes resonance at about 105 MHz, but the gain is -84.2 dB, which does not affect the system significantly. In particular, since it is a far away from the switching frequency band, it

means that the state of L_d does not need to be considered much. However, if the L_d value becomes larger according to the design, the resonant frequency band of the drain-source stage is also lowered.

Figure 8. The system frequency response with variation of drain-inductance (L_d).

We can confirm this again in Figures 7 and 8. The PCB design causes resonance due to the stray inductance component of the gate and drain stages. The smaller the stray inductance was, the more stable the system becomes. ΔF_{r_Lg} and ΔF_{r_Ld} in Figures 7 and 8 represent the range of variation of the resonant frequency that can vary depending on the PCB design. Therefore, based on this result, we can also choose the method of reducing inductance, referring to Appendix B. If this is not possible, there is a need for a way to attenuate the gain of a particular frequency band. In this paper, the band-stop filter (BSF) and low-pass filter (LPF) are used to improve the response characteristics of the system (please note that this study does not intend to discuss the characteristics of the filter, but to show that it is possible to improve the characteristics of a power conversion device utilizing GaN devices by applying the filter).

The square wave pulse width modulation (PWM) signal contains the high-frequency component. Both ideal PWM signals and PWM signals that contain noise include the high-frequency component, which will contain the signals in the frequency, the gains of which increase suddenly around the resonance point in the system. This causes system instability or large signal fluctuation upon switching. Consequently, it is necessary to lower or limit the response to this frequency component. Thus, the system's response characteristics can be improved by combining a band-stop filter and a low-pass filter that removed the specific frequency component.

2.3. Filter Design and Response Results

The frequency response analysis results have been demonstrated that the center frequency of the resonance point was approximately 2.08 MHz. The most profound effect on switching performance is exhibited by the gate-source inductance. There are two sources for parasitic source inductance in a typical circuit, one is the bond wire neatly integrated into the FET package and another is the printed circuit board wiring inductance. Furthermore, the inductor and the parasitic capacitor form a resonant RLC circuit as we know. The resonant circuit is excited by the steep edges of the gate drive voltage waveform and it is the fundamental reason for the oscillatory spikes observed in most gate drive circuits. This resonance can be damped by series resistive components of the loop, which include the driver output impedance, the external gate resistor, and the internal gate resistor, but a reduction of the

overall gain is inevitable, so effectively, to remove the resonance frequency and high-frequency signals, a band-stop filter and a low-pass filter were designed. The frequency responses are shown in Figure 9. This figure shows the filter and system's frequency response curve, in which the band-stop, low-pass filters and converter system, respectively.

Figure 9. The frequency response of the band-stop, low-pass filters and converter system.

In Figure 10, the gain of the BSF is set to -55 dB to attenuate 52.1 dB at the 2.08 MHz frequency, and the attenuating frequency band is defined as F_{cp} . F_{cp} band is 1.5 – 2.8 MHz, about 1.3 MHz. F_{cp} can be changed and adjusted according to the filter's corner frequency, number of poles and the type of filter. The results has been showed that the gain was raised suddenly at approximately 2.08 MHz in Figure 9 was attenuated to under 0 dB by the band-stop filter, as verified in Figure 10.

Figure 10. The comparison of the frequency response between the original converter system and the compensated system.

After the system's cut-off frequency, it was reached the response was rolled off to -20 dB/decade and then attenuated to a -120 dB/decade slope around the resonance point. Thus, an optimized filter was designed and applied to the system using the frequency response analyzed through the system modeling to improve the system's response characteristics [12]. The switching characteristics can be improved by reducing the switching loss of the FET.

Figure 11 shows the circuit of the designed filter and power conversion part. It is the circuit that was an active second-order band-stop filter for preventing a 2.08 MHz frequency signal, and then a low-pass filter for attenuating a response of higher frequency signal. The filter circuit may be located before and after the gate. However, based on the experimental results, it is better that it be located in front of the gate driver in terms of energy efficiency and effect (however, this is an experimental result and was not accurately analyzed).

Figure 11. The proposed filter circuit and the power conversion topology with GaN FET. (Second order band-stop and low-pass filters).

3. Experiments and Results

Experiments were conducted using the GaN FET converter module to verify the proposed method that improved the system's switching characteristics. Using a TI GaN FET (LMG5200), the DC-DC converter module was self-made, and for the controller, a TMS320F28335 module was used. The filter manufactured by us was applied and interfaced. In this experiment, most parameters were chosen by referring to the data sheet provided by TI, and the value of the PCB stray inductance was estimated and applied through measurements.

3.1. Stray Inductance Measurement

The stray inductance in the PCB was divided into resistance and inductance components in the path between two points, as shown in Figure 12, calculated, and estimated based on the voltage value between the two points by injecting a current that changed according a constant time. Figure 13 shows

a picture of a real test step-down converter using a GaN FET. The path of stray inductance that can occur on the PCB is shown. The filter circuit was added to the bottom of the board. Refer to the table attached in Figure 13 for wiring information.

Figure 12. The measurement method for the PCB stray inductance.

Figure 13. The stray inductance path in the self-manufactured PCB.

3.2. Test and Analysis

Table 1 presents the parameters chosen for the model analysis through applying the TI data sheet information and measured values. The experiment's results were verified through their applications to an approximately 200 W converter system, which represented around 50% of the rated capacity.

Figure 14a shows the voltage and current measurement results at both switching ends in the GaN FET converter system. Figure 14b shows the expanded figure of the voltage and the current at both switch ends upon turn-off. As you can be seen in Figure 14, because the voltage is ringing by resonance, so current is also ringing.

Figure 14. The drain-source voltage and current signals at the time of switching. (a) 1 cycle turn on-off waveform; (b) A zoomed view.

Figure 15 shows the PWM waveform when the proposed filter is applied to the noise-containing PWM driving signals. A filter analyzed through system modeling was applied for improving the frequency response characteristic. And the results were verified that most frequency components that affected the system had been removed.

Figure 15. The gate-source voltage signals (original and filtered).

Figure 16a shows the voltage and current switching waveforms in the GaN FET conversion system due to the noise-containing PWM signals. Figure 16b shows how the voltage and current switching waveforms in the GaN FET conversion system looked after the filtered signals are applied. The results has been indicated that the ringing waveform's size and the time upon on–off switching were significantly reduced.

Figure 16. The switching waves of drain-source voltage and current in system. (a) The voltage and current switching waveforms before method applied; (b) The voltage and current switching waveforms after method applied.

Consistent with the findings of previous studies, when a low-pass filter was applied without the system characteristics being identified, not only was high-frequency noise removed but needed signals were also attenuated, resulting in a significant phase delay. However, if unnecessary signals were removed through the application of the optimal filter after the system's frequency response was identified through the proposed system modeling analysis, both signal attenuation and phase delay were reduced significantly.

Figure 17 shows an expanded view of the switching time to see how switching losses happened. In Figure 17a, the voltage does not drop to zero at the time of switching turn-on, but rings due to resonance. These eventually result in switching losses. In addition, as shown in Figure 17b, voltage and current were ringing during turn-off. As mentioned in the paper, these are the results of a combination of GaN's low threshold voltage and LC resonance. Figure 17c,d show that the switching properties were improved when the method proposed in this paper was applied, but there is a slight delay, and small ripples still exist. This is analyzed as a slight phase delay caused by the filter, although it has much less delay and ripple than conventional methods.

By improving the characteristics of this switching, the switching losses are different before and after method is applied as analyzed in Figure 18. Switching is repeated every 5 μ s, with increasing loss. Other sections increase little by little with the gradient of conduction losses. In particular, at turn-on time, a large amount of losses occur due to a large ringing voltage when the current is conducted. On the other hand, at turn-off time, the current does not have much ringing in the zero section, so this loss is analyzed to be less than the loss at turn-on. Figure 18 shows the graph of the switching loss calculated using the above two methods. As shown, the method in which the optimized filter was applied was proposed by this study, the switching loss due to ringing was considerably attenuated, as shown by the dotted circles. It can be seen that the proposed method improves the switching loss by about 36.7% compared with the conventional method. Therefore, we proved the validity of the proposed method which improves switching characteristics.

Figure 17. The comparison of switching waveform before and after applying the proposed method. (a) The voltage and current switching waveforms at turn-on before method applied; (b) The voltage and current switching waveforms at turn-off before method applied; (c) The voltage and current switching waveforms at turn-on after method applied; (d) The voltage and current switching waveforms at turn-off after method applied.

Figure 18. The comparison of switching losses before and after applying the proposed method.

In Figure 19, we have compared simulations and the measured results. Figure 19c,d show simulation results of the spectrum of the signal before and after applying the method proposed in this

paper and Figure 19a,b show the measured results. It can be seen that the derived experimental results are similar to the analysis results, but, while the resonance frequency was analyzed as 2.08 MHz in the actual experiment, it could be seen that resonance occurs at about 2.5 MHz due to some parameter measurement error. However, because it exists in the attenuation band (1.5–2.8 MHz), it can be seen that the resonance frequency element was attenuated as the experimental result.

Figure 19. The comparison of signal spectrum before and after applying the proposed method. (a) System response spectrum measurement results before method applied; (b) System response spectrum measurement results after method applied; (c) System response spectrum simulation results before method applied; (d) System response spectrum simulation results after method applied.

4. Discussion and Conclusions

This study modeled a system and induced a mathematical relationship equation for verifying the frequency response characteristics involved in solving major problems in GaN FET power conversion systems. Through the verification of the frequency response characteristics, a filter-applied method was presented to limit frequency responses in a specific range and to improve response characteristics in a high-frequency range. This study has been contributed to facilitating the analysis of system characteristics through theoretical models, through which systems' characteristics could be analyzed by applying them to various power conversion systems using GaN devices. This study proved that the ringing and faulty turn-on problems in GaN FETs could be solved by designing and adding a filter through the theoretical response characteristics of the system. As a result, switching loss was reduced by about 36.7%, peak voltage by about 37.2%, and current ripple by 49.6% when the proposed method was applied to the existing system.

In the author's previous paper, q method that compensated for the phase delay problem occurring when a filter was applied was proposed, which was verified through simulations and experiments. The results of our studies are expected to be widely used in GaN systems in the future, as GaN FET power conversion systems may run in higher frequency ranges, and their undesirable characteristics can be compensated for by software. If the function that can control filter characteristics is added to gate drivers in the future, GaN device applications are expected to advance technologically.

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Appendix A

This appendix shows the process of deriving the transfer function of the system through a mathematical process according to the modeling equations of Equations (A1)–(A4):

$$\frac{d}{dt}i_d(t) = -\frac{1}{L_d}v_{c_1}(t) \quad (\text{A1})$$

$$\frac{d}{dt}i_{L_s}(t) = -\frac{R_{ds_on}}{(L_s + L_{dc})}i_{L_s}(t) - \frac{1}{(L_s + L_{dc})}v_{c_o}(t) + \frac{1}{(L_s + L_{dc})}v_{c_1}(t) \quad (\text{A2})$$

$$\frac{d}{dt}v_{c_1}(t) = \frac{1}{(C_{gd} + C_{ds})}i_d(t) - \frac{1}{(C_{gd} + C_{ds})}i_{L_s}(t) \quad (\text{A3})$$

$$\frac{d}{dt}v_{c_2}(t) = \frac{1}{C_o}i_{L_s}(t) - \frac{1}{C_o R_L}v_{c_o}(t) \quad (\text{A4})$$

Equations (A1)–(A4) present the differential equations by which voltage-current equations are derived for the modeled circuit upon being switched off. As presented in Equation (A5), variables are substituted to calculate a transfer function after the variables expressed with each of the differential equations are designated as state variables:

$$\mathbf{x} = \begin{bmatrix} i_d(t) \\ i_{L_s}(t) \\ v_{c_1}(t) \\ v_{c_o}(t) \end{bmatrix} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} \quad \dot{\mathbf{x}} = \begin{bmatrix} \dot{i}_d(t) \\ \dot{i}_{L_s}(t) \\ \dot{v}_{c_1}(t) \\ \dot{v}_{c_o}(t) \end{bmatrix} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} \quad (\text{A5})$$

The on and off transfer functions are expressed considering the system operation to calculate the transfer functions, which are divided into Equations (A6) and (A7):

$$\dot{\mathbf{x}}_{on} = \mathbf{A}_{on}\mathbf{x} + \mathbf{B}_{on}\mathbf{U} \quad (\text{A6})$$

$$\dot{\mathbf{x}}_{off} = \mathbf{A}_{off}\mathbf{x} + \mathbf{B}_{off}\mathbf{U} \quad (\text{A7})$$

Since the on–off duty is defined as presented in Equation (A8), a transfer function for a single cycle can be expressed as Equation (A9):

$$D_{on} + D_{off} = 1 \quad (\text{A8})$$

$$\dot{\mathbf{x}}_{(on+off)} = (D_{on}\mathbf{A}_{on} + D_{off}\mathbf{A}_{off})\mathbf{x} + (D_{on}\mathbf{B}_{on} + D_{off}\mathbf{B}_{off})\mathbf{U} \quad (\text{A9})$$

$$\mathbf{A}_{on} = \mathbf{A}_{off} = \begin{bmatrix} 0 & 0 & -1/L_d & 0 \\ 0 & -(R_{ds_on})/(L_s + L_{dc}) & 1/(L_s + L_{dc}) & -1/(L_s + L_{dc}) \\ 1/(C_{gd} + C_{ds}) & -1/(C_{gd} + C_{ds}) & 0 & 0 \\ 0 & 1/C_o & 0 & -1/C_o R_L \end{bmatrix} \quad (\text{A10})$$

$$\mathbf{B}_{on} = \begin{bmatrix} 1/L_d \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{B}_{off} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (\text{A11})$$

Here, since the vector that represents the state variable parameter satisfies $\mathbf{A}_{on} = \mathbf{A}_{off}$ and the output voltage is a voltage applied to the output capacitor C_2 , it can be expressed in Equation (A12):

$$v_o = v_{c_o}(t) = x_4 = [0 \ 0 \ 0 \ 1]\mathbf{X} \quad (\text{A12})$$

By arranging the above equation, the input and output transfer function equations of the system can be expressed as Equations (A13) and (A14):

$$\dot{\mathbf{X}} = \mathbf{A}\mathbf{X} + \mathbf{D}_{on}\mathbf{B}_{on}\mathbf{U} \quad (\text{A13})$$

$$\dot{\mathbf{Y}} = \mathbf{C}\mathbf{X} + \mathbf{D}\mathbf{U} = [0 \ 0 \ 0 \ 1]\mathbf{X} \quad (\text{A14})$$

By substituting the parameter values that are not zero for all variables and arranging the equations, the state equations can be expressed in Equations (A15) and (A16):

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & a_{13} & 0 \\ 0 & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & 0 & 0 \\ 0 & a_{42} & 0 & a_{44} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} Db_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_d \quad (\text{A15})$$

$$y = [0 \ 0 \ 0 \ 1] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} \quad (\text{A16})$$

The transfer function in the above state equations can be expressed as Equation (A17) and the Laplace inverse matrix of the transfer function is defined in Equation (A18). Then, the 4×4 determinant of $(s\mathbf{I} - \mathbf{A})$ can be calculated via Equation (A19):

$$G(s) = \frac{Y(s)}{U(s)} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} = [0 \ 0 \ 0 \ 1] \begin{bmatrix} s & 0 & -a_{13} & 0 \\ 0 & s - a_{22} & -a_{23} & -a_{24} \\ -a_{31} & -a_{32} & s & 0 \\ 0 & -a_{42} & 0 & s - a_{44} \end{bmatrix}^{-1} \begin{bmatrix} 1/L_d \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (\text{A17})$$

$$(s\mathbf{I} - \mathbf{A})^{-1} = \frac{1}{\det(s\mathbf{I} - \mathbf{A})} \text{Adj}(s\mathbf{I} - \mathbf{A}) \quad (\text{A18})$$

$$\begin{aligned} \det(s\mathbf{I} - \mathbf{A}) = & s \left\{ (s - a_{22}) \begin{vmatrix} s & 0 \\ 0 & s - a_{44} \end{vmatrix} - (-a_{23}) \begin{vmatrix} -a_{32} & 0 \\ -a_{42} & s - a_{44} \end{vmatrix} \right. \\ & \left. + (-a_{24}) \begin{vmatrix} -a_{32} & s \\ -a_{42} & 0 \end{vmatrix} \right\} \\ & - a_{12} \left\{ (a_{21}) \begin{vmatrix} s & 0 \\ 0 & s - a_{44} \end{vmatrix} - (-a_{23}) \begin{vmatrix} -a_{31} & 0 \\ 0 & s - a_{44} \end{vmatrix} \right. \\ & \left. + (-a_{24}) \begin{vmatrix} -a_{31} & s \\ 0 & 0 \end{vmatrix} \right\} \\ & + (-a_{13}) \left\{ (a_{21}) \begin{vmatrix} -a_{32} & 0 \\ -a_{42} & s - a_{44} \end{vmatrix} - (s - a_{22}) \begin{vmatrix} -a_{31} & 0 \\ 0 & s - a_{44} \end{vmatrix} \right. \\ & \left. + (-a_{24}) \begin{vmatrix} -a_{31} & -a_{32} \\ 0 & -a_{42} \end{vmatrix} \right\} \\ & - (a_{14}) \left\{ (a_{21}) \begin{vmatrix} -a_{32} & s \\ -a_{42} & 0 \end{vmatrix} - (s - a_{22}) \begin{vmatrix} -a_{31} & s \\ 0 & 0 \end{vmatrix} \right. \\ & \left. + (-a_{23}) \begin{vmatrix} -a_{31} & -a_{32} \\ 0 & -a_{42} \end{vmatrix} \right\} \end{aligned} \quad (\text{A19})$$

Equation (A19) can be expressed by the Laplace function, as presented in Equation (A20), through determinant expansion, and the coefficients of each order are defined in Equations (A21)–(A24). By those equations, the determinant, which is a denominator of the transfer function, can be calculated:

$$\det(s\mathbb{I} - \mathbb{A}) = s^4 + k_1s^3 + k_2s^2 + k_3s + k_4 \quad (\text{A20})$$

$$k_1 = (R_{ds_on}) / (L_s + L_{dc}) + 1/C_o R_L \quad (\text{A21})$$

$$k_2 = (R_{ds_on}) / ((L_s + L_{dc}) \cdot C_o R_L - 1 / (L_s + L_{dc})^2) + 1 / (L_d (C_{gd} + C_{ds})) \quad (\text{A22})$$

$$k_3 = -1 / ((L_s + L_{dc}) \cdot C_o R_L - 1 / (L_d (C_{gd} + C_{ds}))) \cdot \left\{ -(R_{ds_on}) / (L_s + L_{dc}) - 1 / C_o R_L \right\} \quad (\text{A23})$$

$$k_4 = 1 / (L_d (C_{gd} + C_{ds})) \cdot (R_{ds_on}) / ((L_s + L_{dc}) \cdot C_o R_L - 1 / (L_d C_o (L_s + L_{dc}) (C_{gd} + C_{ds}))) \quad (\text{A24})$$

To calculate the adjoint matrix, which is a numerator of the transfer function, it is expressed in vector **F**, as presented in Equation (A25), thereby calculating the cofactor of the matrix and the transposed matrix to calculate the adjoint of the matrix through Equations (A26) and (A27). Accordingly, Equation (A18) can be defined as Equation (A28):

$$(s\mathbb{I} - \mathbb{A}) = \mathbb{F} = \begin{bmatrix} f_{11} & f_{12} & f_{13} & f_{14} \\ f_{21} & f_{22} & f_{23} & f_{24} \\ f_{31} & f_{32} & f_{33} & f_{34} \\ f_{41} & f_{42} & f_{43} & f_{44} \end{bmatrix} \quad (\text{A25})$$

$$\mathbb{F} \text{ cofactor} = \mathbb{B} = \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} \\ b_{21} & b_{22} & b_{23} & b_{24} \\ b_{31} & b_{32} & b_{33} & b_{34} \\ b_{41} & b_{42} & b_{43} & b_{44} \end{bmatrix} \quad (\text{A26})$$

$$\mathbb{B}^T = \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} \\ b_{21} & b_{22} & b_{23} & b_{24} \\ b_{31} & b_{32} & b_{33} & b_{34} \\ b_{41} & b_{42} & b_{43} & b_{44} \end{bmatrix} \quad (\text{A27})$$

$$(s\mathbb{I} - \mathbb{A})^{-1} = \mathbb{F}^{-1} = \frac{1}{\det(\mathbb{F})} \mathbb{B}^T = \begin{bmatrix} \frac{b_{11}}{\det(\mathbb{F})} & \frac{b_{21}}{\det(\mathbb{F})} & \frac{b_{31}}{\det(\mathbb{F})} & \frac{b_{41}}{\det(\mathbb{F})} \\ \frac{b_{12}}{\det(\mathbb{F})} & \frac{b_{22}}{\det(\mathbb{F})} & \frac{b_{32}}{\det(\mathbb{F})} & \frac{b_{42}}{\det(\mathbb{F})} \\ \frac{b_{13}}{\det(\mathbb{F})} & \frac{b_{23}}{\det(\mathbb{F})} & \frac{b_{33}}{\det(\mathbb{F})} & \frac{b_{43}}{\det(\mathbb{F})} \\ \frac{b_{14}}{\det(\mathbb{F})} & \frac{b_{24}}{\det(\mathbb{F})} & \frac{b_{34}}{\det(\mathbb{F})} & \frac{b_{44}}{\det(\mathbb{F})} \end{bmatrix} \quad (\text{A28})$$

Equation (A28) is substituted into Equation (A17), which is the transfer function equation, and calculated with matrices **C** and **B**, thereby obtaining the equation of the transfer function, as presented in Equation (A29):

$$\begin{aligned} \mathbb{C}(s\mathbb{I} - \mathbb{A})^{-1} \mathbb{B} &= [0 \ 0 \ 0 \ 1] \begin{bmatrix} \frac{b_{11}}{\det(\mathbb{F})} & \frac{b_{21}}{\det(\mathbb{F})} & \frac{b_{31}}{\det(\mathbb{F})} & \frac{b_{41}}{\det(\mathbb{F})} \\ \frac{b_{12}}{\det(\mathbb{F})} & \frac{b_{22}}{\det(\mathbb{F})} & \frac{b_{32}}{\det(\mathbb{F})} & \frac{b_{42}}{\det(\mathbb{F})} \\ \frac{b_{13}}{\det(\mathbb{F})} & \frac{b_{23}}{\det(\mathbb{F})} & \frac{b_{33}}{\det(\mathbb{F})} & \frac{b_{43}}{\det(\mathbb{F})} \\ \frac{b_{14}}{\det(\mathbb{F})} & \frac{b_{24}}{\det(\mathbb{F})} & \frac{b_{34}}{\det(\mathbb{F})} & \frac{b_{44}}{\det(\mathbb{F})} \end{bmatrix} \begin{bmatrix} 1/L_d \\ 0 \\ 0 \\ 0 \end{bmatrix} \\ &= \frac{b_{14}}{\det(\mathbb{F})} \cdot \frac{1}{L_d} \end{aligned} \quad (\text{A29})$$

Here, b_{14} , the cofactor coefficient of the transfer function, can be calculated through the determinant, as presented in Equation (A30):

$$b_{14} = \det \begin{vmatrix} f_{21} & f_{22} & f_{23} \\ f_{31} & f_{32} & f_{33} \\ f_{41} & f_{42} & f_{43} \end{vmatrix} = f_{21} \begin{vmatrix} f_{32} & f_{33} \\ f_{42} & f_{43} \end{vmatrix} - f_{22} \begin{vmatrix} f_{31} & f_{33} \\ f_{41} & f_{43} \end{vmatrix} + f_{23} \begin{vmatrix} f_{31} & f_{32} \\ f_{41} & f_{42} \end{vmatrix} \quad (\text{A30})$$

$$= f_{23} \cdot f_{31} \cdot f_{42}$$

Here, as $f_{21} = 0$, $f_{43} = 0$, $f_{41} = 0$, and the cofactor function coefficients are defined as presented in Equation (A31). Their values can be calculated as Equation (A32):

$$\begin{vmatrix} f_{21} & f_{22} & f_{23} \\ f_{31} & f_{32} & f_{33} \\ f_{41} & f_{42} & f_{43} \end{vmatrix} = \begin{vmatrix} 0 & s - a_{22} & -a_{23} \\ -a_{31} & -a_{32} & s \\ 0 & -a_{42} & 0 \end{vmatrix} \quad (\text{A31})$$

$$f_{23} \cdot f_{31} \cdot f_{42} = (-a_{23}) \cdot (-a_{31}) \cdot (-a_{42}) = -\frac{1}{(L_s + L_{dc})} \cdot \frac{1}{(C_{gd} + C_{ds})} \cdot \frac{1}{C_o} = k_5 \quad (\text{A32})$$

Through the above defined equation, the final transfer function of the system is defined as Equation (A33):

$$G(s) = \frac{b_{14}}{\det(\mathbb{F})} \cdot \frac{1}{L_d} = \frac{k_5}{L_d(s^4 + k_1s^3 + k_2s^2 + k_3s + k_4)} \quad (\text{A33})$$

$$\mathbf{x} = \begin{bmatrix} i_g(t) \\ v_{gs}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} x_5 \\ x_6 \\ x_7 \end{bmatrix} \quad \dot{\mathbf{x}} = \begin{bmatrix} \dot{i}_g(t) \\ \dot{v}_{gs}(t) \\ \dot{v}_o(t) \end{bmatrix} = \begin{bmatrix} \dot{x}_5 \\ \dot{x}_6 \\ \dot{x}_7 \end{bmatrix} \quad (\text{A34})$$

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{D}_{on}\mathbf{B}_{on}\mathbf{U} \quad (\text{A35})$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} = [0 \ 1 \ 0]\mathbf{x} \quad (\text{A36})$$

$$\begin{bmatrix} \dot{x}_5 \\ \dot{x}_6 \\ \dot{x}_7 \end{bmatrix} = \begin{bmatrix} a_{55} & a_{56} & a_{57} \\ a_{65} & a_{66} & 0 \\ a_{75} & 0 & a_{77} \end{bmatrix} \begin{bmatrix} x_5 \\ x_6 \\ x_7 \end{bmatrix} + \begin{bmatrix} b_{51} \\ 0 \\ 0 \end{bmatrix} v_g \quad (\text{A37})$$

$$\det(s\mathbb{I} - \mathbf{A}) = s^3 + m_1s^2 + m_2s + m_3 \quad (\text{A38})$$

$$m_1 = \left(R_g / (L_g + L_s + L_{dc}) + (1 / (A_v C_{gd} + C_{gs})) (r'_s) \right) + (1 / C_o R_L) \quad (\text{A39})$$

$$m_2 = 1 / (L_g + L_s + L_{dc}) \cdot C_o R_L + (R_g / (L_g + L_s + L_{dc})) (1 / (A_v C_{gd} + C_{gs})) (r'_s) + (R_g / (L_g + L_s + L_{dc})) / C_o R_L + (1 / (L_g + L_s + L_{dc})) / (A_v C_{gd} + C_{gs}) + (1 / (L_g + L_s + L_{dc}) \cdot C_o) \quad (\text{A40})$$

$$m_3 = (1 / (L_g + L_s + L_{dc})) / (A_v C_{gd} + C_{gs}) \cdot C_o R_L + (1 / (L_g + L_s + L_{dc})) (1 / (A_v C_{gd} + C_{gs})) (r'_s) / C_o + (R_g / (L_g + L_s + L_{dc})) (1 / (A_v C_{gd} + C_{gs})) / (r'_s \cdot C_o R_L) \quad (\text{A41})$$

$$m_4 = -\frac{1}{(A_v C_{gd} + C_{gs})} \cdot \frac{1}{C_o R_L} \cdot \frac{1}{(L_g + L_s + L_{dc})} \quad (\text{A42})$$

$$G(s) = \mathbf{C}(s\mathbb{I} - \mathbf{A})^{-1}\mathbf{B} = [0 \ 1 \ 0] \begin{bmatrix} \frac{b_{11}}{\det(\mathbb{F})} & \frac{b_{21}}{\det(\mathbb{F})} & \frac{b_{31}}{\det(\mathbb{F})} \\ \frac{b_{12}}{\det(\mathbb{F})} & \frac{b_{22}}{\det(\mathbb{F})} & \frac{b_{32}}{\det(\mathbb{F})} \\ \frac{b_{13}}{\det(\mathbb{F})} & \frac{b_{23}}{\det(\mathbb{F})} & \frac{b_{33}}{\det(\mathbb{F})} \end{bmatrix} \begin{bmatrix} 1 / (L_g + L_s + L_{dc}) \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (\text{A43})$$

$$= \frac{b_{12}}{\det(\mathbb{F})} \cdot \frac{1}{(L_g + L_s + L_{dc})} = \frac{m_4}{s^3 + m_1s^2 + m_2s + m_3}$$

Appendix B

PCB wiring is plate inductance. Therefore, the inductance can be adjusted using the following equation:

$$L = \mu_0 2\ell \left(\ln \frac{2\ell}{t+w} + 0.5 \right) \quad (t : \text{thickness}, w : \text{width}, \ell : \text{length})$$

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