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Flux-Balance Control for LLC Resonant Converters with Center-Tapped Transformers

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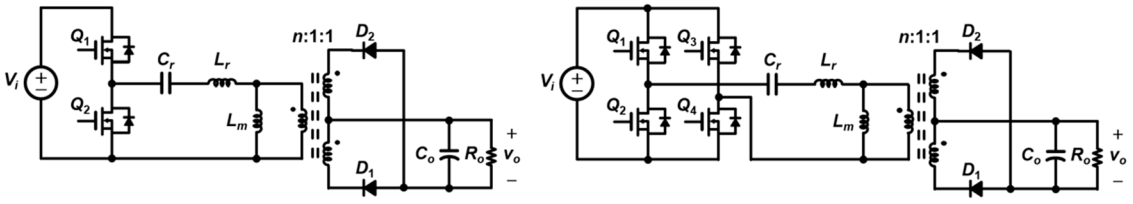
Received: 9 July 2019; Accepted: 19 August 2019; Published: 21 August 2019

Abstract: LLC resonant converters with center-tapped transformers are widely used. However, these converters suffer from a flux walking issue, which causes a larger output ripple and possible transformer saturation. In this paper, a flux-balance control strategy is proposed for resolving the flux walking issue. First, the DC magnetizing current generated due to the mismatched secondary-side leakage inductances, and its effects on the voltage gain are analyzed. From the analysis, the flux-balance control strategy, which is based on the original output-voltage control loop, is proposed. Since the DC magnetizing current is not easily measured, a current sensing strategy with a current estimator is proposed, which only requires one current sensor and is easy to estimate the DC magnetizing current. Finally, a simulation scheme and a hardware prototype with rated output power 200 W, input voltage 380 V, and output voltage 20 V is constructed for verification. The simulation and experimental results show that the proposed control strategy effectively reduces the DC magnetizing current and output voltage ripple at mismatched condition.

Keywords: LLC resonant converter; center-tapped transformer; flux walking; flux-balance control loop; magnetizing current estimation

1. Introduction

The LLC resonant converter is widely used in many different applications such as onboard chargers, server power systems, laptops, desktops, photovoltaic regeneration systems. Owing to the characteristics of zero-voltage-switching (ZVS) at the primary side and zero-current-switching (ZCS) at the secondary side, high efficiency and high power density of the LLC converter are achieved [1–7]. The half-bridge (HB) and full-bridge (FB) with the center-tapped transformer rectifier topologies shown in Figure 1 are the most commonly used topologies of the LLC resonant converter. Thanks to the center-tapped transformer, only two rectifying diodes are necessary at the secondary side [8–11]. Without the center-tap, it would be required to implement a full-wave rectifier.



(**a**) (**b**)

Figure 1. Different topologies of the LLC resonant converter (**a**) half-bridge and (**b**) full-bridge.

Figure 2a shows the key waveforms of the LLC resonant converter operating below the resonant frequency with the matching leakage inductances in both secondary side windings, where v_{gs1} and v_{gs2} are the driving signals of the MOSFET Q_1 and Q_2, respectively. Figure 2a reveals that the current waveforms of the diode 1 (i_{D1}) and diode 2 (i_{D2}) are symmetrical, and energy flows through the diode 1 and diode 2 in the positive and negative cycles, respectively. In Figure 2a, the magnetizing current will have no DC component.

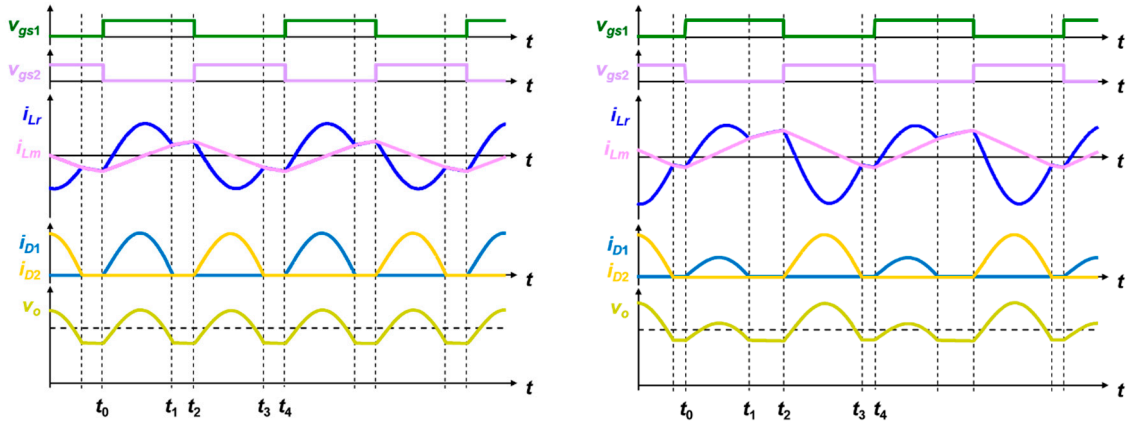


Figure 2. Key waveforms of the LLC resonant converter operating below the resonant frequency with the different leakage inductances in the secondary side windings (**a**) matched leakage inductances and (**b**) mismatched leakage inductances.

However, practical LLC resonant converters with center-tapped transformers contain a flux walking issue, which causes a larger output ripple and possible transformer saturation [12–14]. This is because the secondary side windings are usually not symmetrical in practical manufacture. The mismatched leakage inductances are generated in the secondary side windings, which causes an imbalance in the secondary side currents, resulting in a larger output voltage ripple. The secondary side currents imbalance will reflect upon the magnetizing inductance on the primary side. Therefore, the magnetizing current will have a DC component, which will lead to the flux walking and possible transformer core saturation.

Figure 2b shows the key waveforms of the LLC resonant converter operating below the resonant conditions with the mismatched leakage inductances in the secondary side windings. In Figure 2b, the current waveforms of the diode 1 and diode 2 are not symmetrical. The magnetizing current (i_{Lm}) will, therefore, contain a DC component. Since the resonant capacitance is in series with the primary side, the resonant current (i_{Lr}) will not have a DC component from charge balance concept. Besides, the mismatched condition considers not only the leakage inductances of the secondary side windings of the transformer but also the parasitic inductances of the printed-circuit-board (PCB) traces on the secondary side.

To improve the flux walking issue in the LLC resonant converter, improved winding structures for the secondary side were proposed [12–14]. The coupling coefficients between the primary side and two secondary sides were increased to mitigate the flux walking issue [12]. The further improved method is used in the Bifilar winding structure to overcome this problem [13]. The flux distribution of the non-symmetrical structure of the secondary side windings were analyzed in [14]. However, they cannot consider the mismatch problems caused by the PCB circuit traces.

According to abovementioned issue, a flux-balance control strategy, which is based on the original output-voltage control loop, is proposed in this paper. The flux-balance control is added to improve the magnetizing current imbalance problem caused by the secondary side mismatches.

Besides, the DC magnetizing current of the LLC resonant converter is difficult to sense directly. An indirect method to sense the magnetizing current was used [15], which involved sensing the currents at the primary and secondary side, simultaneously and subtracting them to obtain the magnetizing current. Then, the DC component was obtained using a low-pass filter. This solution, however, required several current sensing devices, which increased the circuit cost; moreover, the low-pass filter produced a slow dynamic response. Therefore, this paper proposes a simple magnetizing current sensing strategy with a DC current estimation scheme to overcome the abovementioned issue.

Moreover, for small-signal model, the mathematical methods for deriving the small-signal dynamic model of the LLC resonant converter were developed [16–19]. However, these works focused only on the switching frequency to output voltage transfer function. Besides, matching with circuit ac sweep simulation occurs only under specific operating conditions. Nevertheless, system identification [20,21] is a useful method to obtain the small-signal model of the system without using any complex mathematical model. Therefore, the system identification [21] is used to obtain the small-signal models of the LLC resonant converter for controllers design in this paper.

The remainder of this paper is organized as follows. Section 2 analyzes the mismatched leakage inductances effects of the secondary side on the DC magnetizing current and voltage gain. Section 3 describes the proposed control strategy with the magnetizing current sensing and the DC magnetizing current estimation. Section 4 describes the controller designs for the flux-balance loop and output-voltage loop, which are based on the transfer functions obtained by using the system identification tool of MATLAB (R2018b, MathWorks, Natick, MA, USA). Section 5 presents the simulated and experimental results, to verify the effectiveness of the proposed control strategy. Finally, Section 6 provides the conclusions.

2. Analysis of Secondary Side Mismatched Leakage Inductances Effects

2.1. Analysis of the Magnetizing Current DC Value

Figure 3 shows the DC current path in the LLC resonant tank when the leakage inductances at the secondary side are mismatched. It is assumed that the leakage inductance of the positive-cycle loop at the secondary side ($L_{lk2,pos}$) is smaller than the leakage inductance of the negative-cycle loop at the secondary side ($L_{lk2,neg}$). According to Kirchhoff's current law (KCL), the relationship among i_{Lr}, i_{Lm}, and i_{Dx} can be expressed as follows

$$i_{Lr} = i_{Lm} + \frac{i_{Dx}}{n} \tag{1}$$

$$x = \begin{cases} 1 : \text{duringthepositivecycle} \\ 2 : \text{duringthenegativecycle} \end{cases} \tag{2}$$

where n is the turns ratio of the transformer. Since the resonant capacitance is in series with the input of the transformer, the DC current of the resonant inductor is zero. That is, the average resonant inductor current in a switching period is zero in steady-state, and can be expressed as follows

$$I_{Lr,DC} = \frac{1}{T_s}\int_0^{T_s} i_{Lr}dt = \frac{1}{T_s}\int_0^{T_s}\left(i_{Lm} + \frac{i_{Dx}}{n}\right)dt = 0\text{A}. \tag{3}$$

Based on (3), the relationship between the magnetizing DC current and difference in the DC currents of both diodes can be expressed as follows

$$\begin{aligned} I_{Lm,DC} &= \tfrac{1}{T_s}\int_0^{T_s} i_{Lm}dt = -\tfrac{1}{nT_s}\int_0^{T_s} i_{Dx}dt \\ &= -\tfrac{1}{nT_s}\left(\int_0^{T_s/2} i_{D1}dt - \int_{T_s/2}^{T_s} i_{D2}dt\right) = \tfrac{1}{n}(I_{D2,DC} - I_{D1,DC}) \end{aligned} \tag{4}$$

where $I_{D1,DC}$ and $I_{D2,DC}$ are the DC currents of the diodes at secondary side. Equation (4) shows that the magnetizing DC current is proportional to the difference between $I_{D1,DC}$ and $I_{D2,DC}$ with the turns ratio n. Therefore, the largest $I_{Lm,DC}$ would be induced for the largest current mismatch in the secondary side condition.

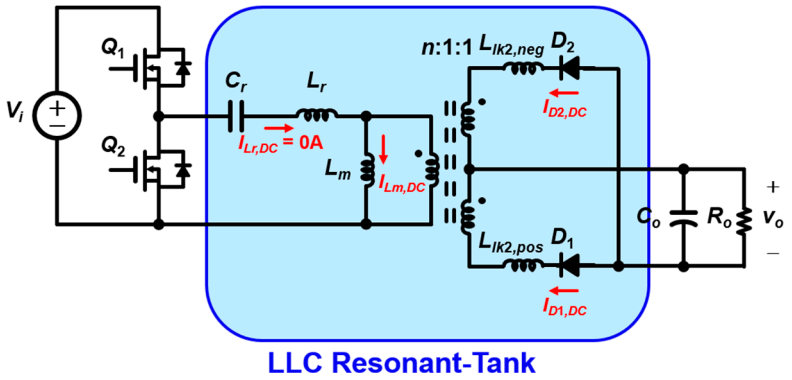


Figure 3. The DC current path in the LLC resonant tank when the leakage inductances at the secondary side are mismatched ($L_{lk2,pos} < L_{lk2,neg}$).

2.2. Analysis of the Voltage Gain under Mismatched Condition

A non-ideal transformer equivalent circuit can be expressed by the model shown in Figure 4a, which is called the "T model" [22,23]. In Figure 4a, the leakage inductances are distributed at the primary and secondary sides, separately. This circuit is not suitable for the analysis of the LLC resonant converter. On the other hand, Figure 4b shows the "L model" [22,23]. In this model, the leakage inductance at the secondary side is removed. Therefore, it is suitably used in the LLC resonant tank for analysis.

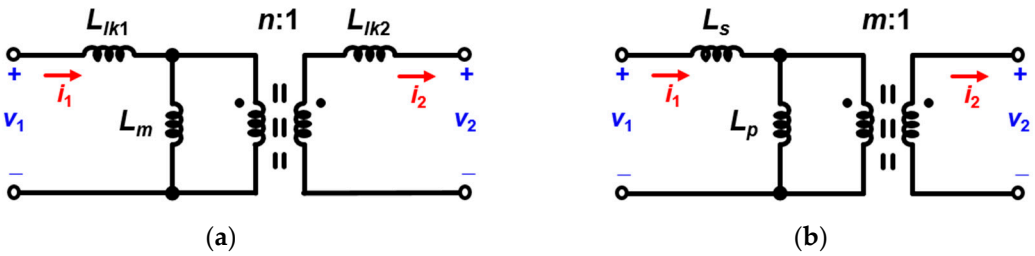


Figure 4. Different equivalent circuit models of the transformer (**a**) T model and (**b**) L model.

For center-tapped applications, the L model of the transformer can be separated into the positive and negative cycle models. For a matched condition, the parameters of the L model for the positive and negative cycle will be the same. This will not be the case for the mismatched condition because the leakage inductances at the secondary side would affect the resonant parameters during the positive and negative cycles.

Figure 5 shows the equivalent circuit models of the LLC resonant tank for the positive (lower left) and negative (lower right) cycles. The relative parameters of the L model during the positive and negative cycles can be derived from Figure 4 and is presented as follows

$$m_h = \frac{nL_m}{L_m + n^2 L_{lk2,h}} \tag{5}$$

$$L_{p,h} = \frac{{L_m}^2}{L_m + n^2 L_{lk2,h}} \tag{6}$$

$$L_{r,h} = L_{ext} + L_{lk1} + L_m \| n^2 L_{lk2,h} \tag{7}$$

$$h = \begin{cases} pos : \text{duringthepositivecycle} \\ neg : \text{duringthenegativecycle} \end{cases} \tag{8}$$

where L_m indicates the magnetizing inductance of the transformer, L_{lk1} and $L_{lk2,h}$ express the leakage inductances at the primary and secondary sides of the transformer, respectively, m_h indicates the equivalent turns ratio of the L model, L_{ext} represents the external resonant inductance, $L_{p,h}$ expresses the equivalent paralleled inductance of the L model, and $L_{r,h}$ is the total equivalent resonant inductance of the L model. Therefore, the parameters of the L model during the positive and negative cycles can be obtained using (5)–(8).

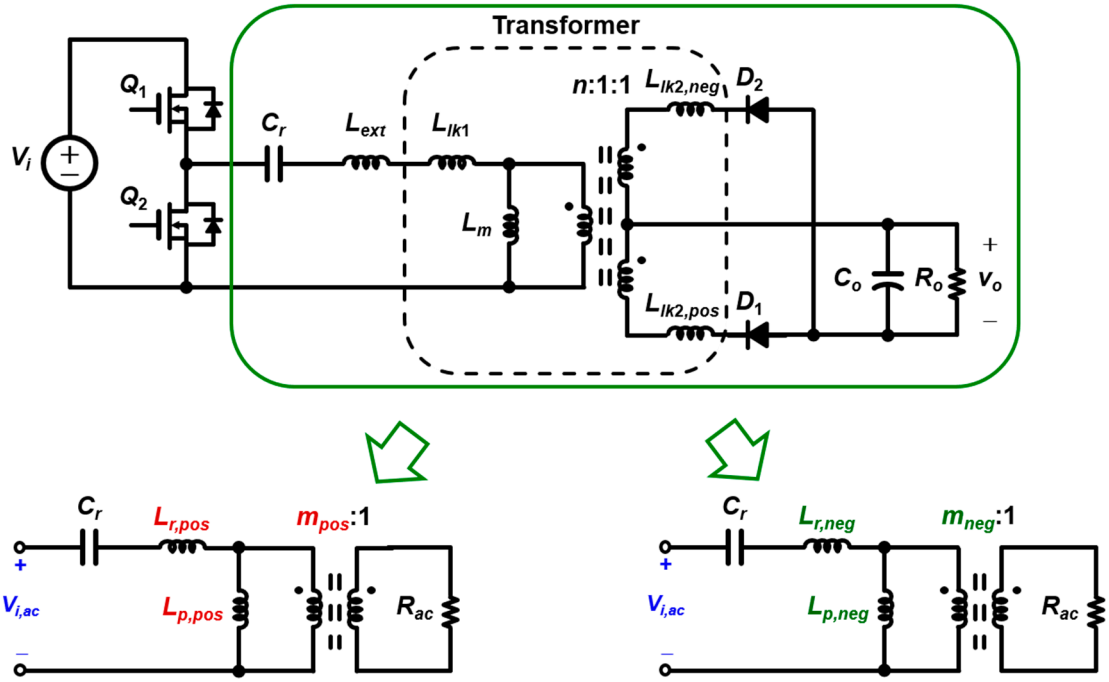


Figure 5. Equivalent circuit models of the resonant tank during the positive cycle (lower left) and negative cycle (lower right).

The voltage gain during the positive and negative cycles can be expressed as follows

$$M(f_{n,h}) = \frac{m_h V_o}{V_i} = \frac{1}{\sqrt{\left[1 + \frac{1}{L_{n,h}}\left(1 - \frac{1}{f_{n,h}{}^2}\right)\right]^2 + \left[Q_h\left(f_{n,h} - \frac{1}{f_{n,h}}\right)\right]^2}} \tag{9}$$

$$f_{r,h} = \frac{1}{2\pi\sqrt{L_{r,h}C_r}} \tag{10}$$

$$Q_h = \frac{1}{m_h{}^2 R_{ac}}\sqrt{\frac{L_{r,h}}{C_r}} \tag{11}$$

$$R_{ac} = \frac{8}{\pi^2}R_o \tag{12}$$

$$f_{n,h} = \frac{f_s}{f_{r,h}} \tag{13}$$

$$L_{r,h} = \frac{L_{p,h}}{L_{r,h}} \tag{14}$$

where f_r indicates the resonant frequency, C_r is the resonant capacitance, Q_h is the qualify factor, R_{ac} is the equivalent ac load resistance, R_o is the load resistance, f_s is the switching frequency, $f_{n,h}$ is the normalized frequency, and $L_{n,h}$ is the ratio between $L_{p,h}$ and $L_{r,h}$.

Based on (9)–(14), the voltage gain curves during the positive and negative cycles can be drawn as shown in Figure 6. The solid lines represent the nominal Q-value condition and dashed lines express the high Q-value condition. Assuming the normal leakage inductance $L_{lk,2n} = L_{lk,2,pos} = L_{lk,2,neg}$ at the secondary side, i.e., at matched condition, $f_{n,pos}$ and $f_{n,neg}$ would be one as indicated by the curve **a** (i.e., maroon solid line) with the normal operating point indicated by the sky blue circle in Figure 6. When operating under the mismatched condition and assuming the leakage inductances at the secondary side are satisfying $L_{lk,2n} = L_{lk,2,pos} < L_{lk,2,neg}$, the voltage gain during the positive cycle follows the original curve **a** (i.e., maroon solid line); during the negative cycle, the voltage gain curve moves toward the left as shown by the curve **b** (i.e., light blue solid line). Under the mismatched condition, the voltage gain also operates at $M = 1.05$, because of the voltage loop regulation, and the operating point shifts to the point indicated by the pink circle.

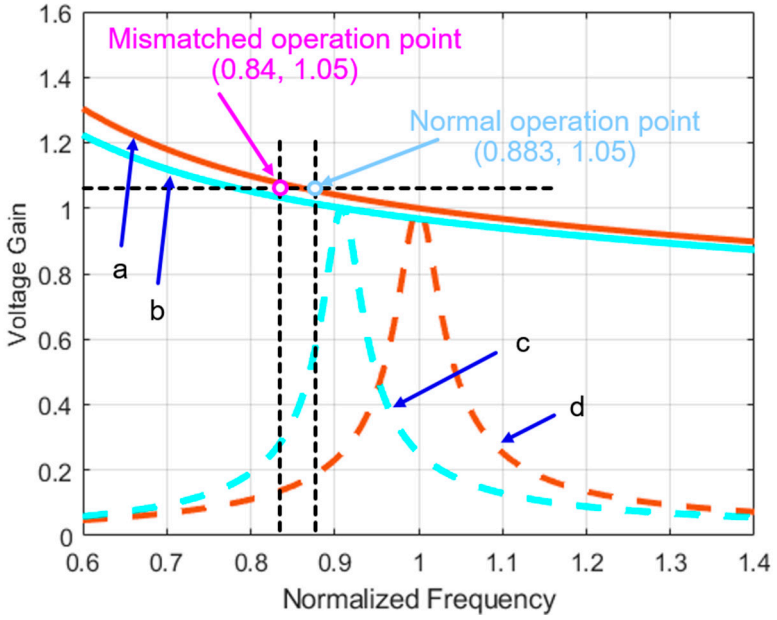


Figure 6. Voltage gain curves during the positive and negative cycles, curve **a**: Nominal Q-value condition with the matched leakage inductance $L_{lk,2n}$ at the secondary side; curve **b**: Nominal Q-value condition with the mismatched leakage inductance $L_{lk,2,neg}$ at the secondary side during the negative cycle; curve **c**: High Q-value condition with the matched leakage inductance $L_{lk,2n}$ at the secondary side; curve **d**: High Q-value condition with the mismatched leakage inductance $L_{lk,2,neg}$ at the secondary side during the negative cycle.

The operations of the curve **a** (i.e., maroon solid line) during the positive cycle and curve **b** (i.e., light blue solid line) during the negative cycle can be mapped to time-domain operated waveforms shown in Figure 2b. They are matched precisely between the voltage gains and time domain waveforms.

3. Proposed Flux-Balance Control Architecture

3.1. Description of the Proposed Control Architecture

Figure 7 shows the block diagram of the proposed control architecture to solve the flux walking issue caused by the mismatched condition on the secondary side. The proposed control is based on the original output-voltage control loop with the addition of the flux-balance loop. The flux-balance loop includes the sampling setup for the magnetizing current, a DC current estimator, a flux-balance loop

controller, and a variable-frequency-variable-duty-pulse-width-modulator (VFVDPWM). The output of the voltage loop controller controls the switching period of the MOSFETs Q_1 and Q_2. The output of the flux-balance loop controller offsets the duty ratio of the MOSFETs Q_1 and Q_2 from 0.5. The input of the flux-balance loop controller is the error between $i_{Lm,DC}$ and $i_{Lm,DC,ref}$, which is zero in steady-state. Thus, the flux-balance loop forces the DC magnetizing current to zero and solves the flux walking issue. The DC estimator estimates the DC magnetizing current, and the i_{Lm} sampling scheme samples relative information of the magnetizing current from the resonant current i_{Lr}. The relationship between the DC magnetizing current and the duty ratio are not direct, because the resonant capacitance is in series between the half-bridge switches and the input of the transformer. According to the proposed flux-balance control, when the duty is regulated, the resonant capacitance to hold the charge balance in steady-state, the DC current of the resonant inductance, therefore, keeps zero, and the rectifier diodes turned off time, therefore, be changed when the duty ratio be regulated. Finally, the magnetizing DC current would be regulated. Detailed descriptions of the functional blocks of the magnetizing current sampling scheme, the DC current estimator, and the VFVDPWM are provided below.

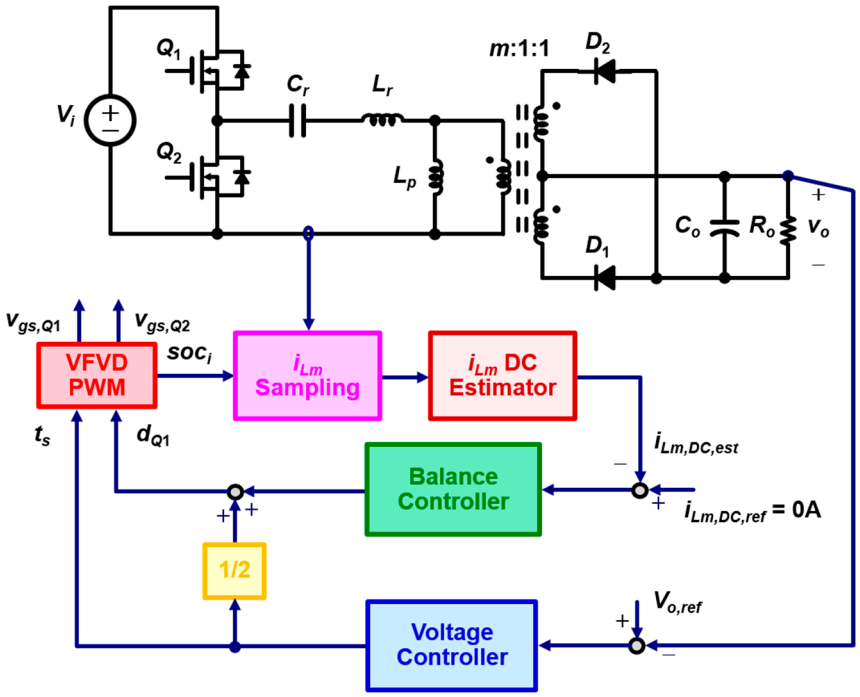


Figure 7. Overall block diagram of the proposed control architecture.

3.2. Magnetizing Current Sampling Scheme

Figure 8 shows the magnetizing current sampling scheme, where i_{Lr} is the resonant current, i_{Lm} is the magnetizing current, $i_{Lm,p}$, and $i_{Lm,n}$ are the peak values of the magnetizing current during the positive and negative cycles, respectively. The magnetizing current of the LLC resonant converter cannot be measured directly because the magnetizing inductance is an equivalent element in the transformer. However, owing to the LLC resonant converter usually operates with the switching frequency below the resonant frequency, the resonant current is equal to the magnetizing current when the diodes on the secondary side are turned off. As shown in Figure 8, during these intervals, the peak values of the magnetizing current during the positive and negative cycles occur when the respective MOSFET Q_1 and Q_2, are turned off. According to the previous statement, the sampling pluses of $SOC_{i,p}$ and $SOC_{i,n}$ can be applied from the VFVDPWM, which are generated when the driving signals of MOSFET Q_1 and Q_2 are turned off, respectively. After that, $i_{Lm,p}$ and $i_{Lm,n}$ can be sampled during each switching period.

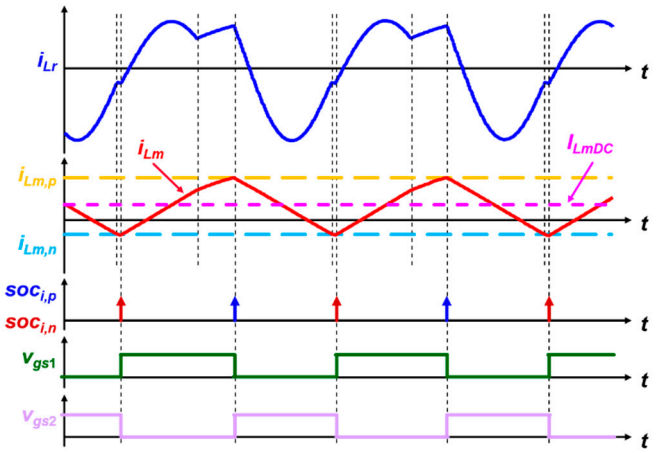


Figure 8. Magnetizing current sampling timing, where $i_{Lm,p}$ ($i_{Lm,n}$) is sampled at the timing of v_{gs1} (v_{gs2}) from high to low.

3.3. DC Value Estimation of the Magnetizing Current

This paper proposes the DC value estimation scheme to obtain the DC magnetizing current, which will be used as one of the inputs of the flux-balance controller. Figure 9 shows the magnetizing current waveform (red line), which is similar to a triangular wave (shown by the blue dashed line). The magnetizing DC current can be estimated after the $i_{Lm,p}$ and $i_{Lm,n}$ are sampled, and is expressed as follows

$$\begin{aligned} i_{Lm,DC,est}[n] &= \text{DCvalueoftriangularwave} \\ &= \tfrac{1}{2}(i_{Lm,p}[n] + i_{Lm,n}[n]) \\ &\approx \tfrac{1}{T_s}\int_0^{T_s} i_{Lm}dt \end{aligned} \tag{15}$$

where $i_{Lm,DC,est}[n]$ represents the estimated magnetizing DC current. Equation (15) reveals that the estimated magnetizing DC current can be approximated as the sum of $i_{Lm,p}[n]$ and $i_{Lm,n}[n]$, divided by 2, which is a very simple method to obtain the magnetizing DC current. The block diagram of the DC magnetizing current estimator is shown in Figure 10.

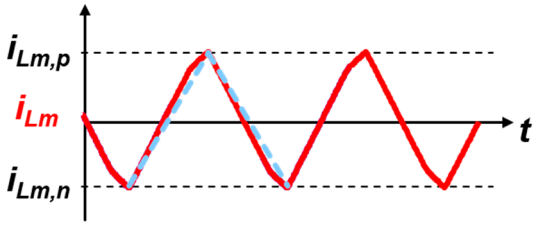


Figure 9. The magnetizing current waveform (red line) and the approximate triangular waveform (blue dashed line).

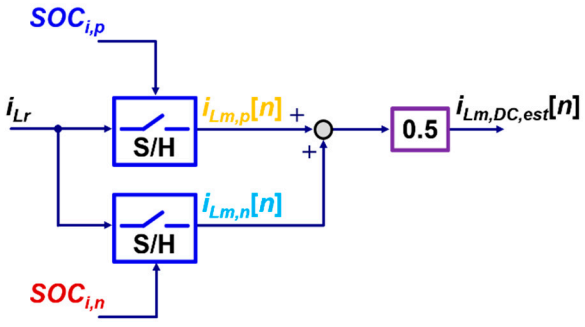


Figure 10. Block diagram of the magnetizing DC current estimator.

3.4. Variable-Frequency-Variable-Duty-Pulse-Width-Modulator

In conventional LLC resonant converters, the output voltage regulation is achieved by controlling the switching frequency and maintaining the duty ratios of MOSFET Q_1 and Q_2 at 50%. The proposed flux-balance control scheme utilizes the controlled duty ratio for MOSFET Q_1 for the magnetizing DC current regulation. Figure 11 shows the operating timing of the VFVDPWM, where v_{carr} is the carrier waveform, d_{Q1} is the duty ratio control signal of MOSFET Q_1, t_s is the switching period control signal. In Figure 11, the slope of v_{carr} is fixed. t_s can therefore control the magnitude of v_{carr} to control the switching period. d_{Q1}, which is equal to $0.5t_s$ in the matched condition, controls the duty ratio of MOSFET Q_1 for the flux-balance loop regulation. $SOC_{i,p}$ is generated when d_{Q1} equals v_{carr} and $SOC_{i,n}$ is generated when t_s equals v_{carr}. Thus, the control signal and magnetizing current sampling pulses of the proposed flux-balance loop can be obtained from Figure 11.

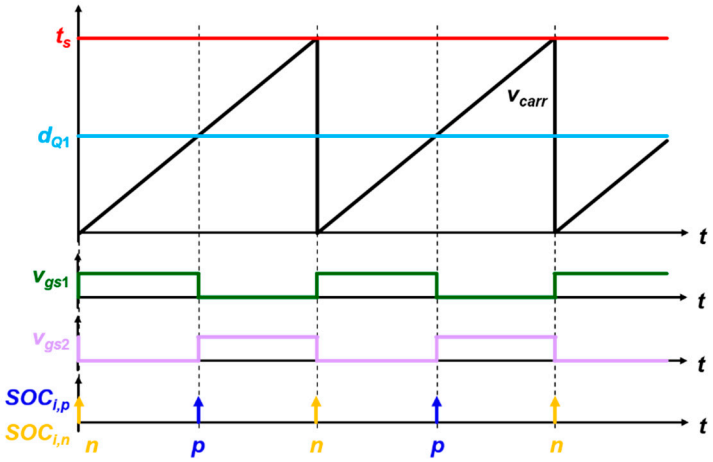


Figure 11. VFVDPWM operating timing.

4. Small-Signal Model and Controllers Design

4.1. Small-Signal Models Built Using System Identification

Unlike the pulse-width-modulation (PWM) converter, the LLC resonant converter is a complex nonlinear system. Therefore, it is difficult to obtain its small-signal model through mathematical derivation. Previously, researchers had developed the mathematical methods for deriving the small-signal dynamic model of the LLC resonant converter [16–19]. However, these works focused only on the matching with circuit ac sweep simulation occurs only under specific operating conditions. At the same time, the flux-balance loop proposed in this paper, there is no more literature to discuss. The system identification tool of MATLAB [21] is a useful tool to obtain the small-signal model transfer function without using any complex mathematical model derivation. Figure 12 shows the processing flow windows of the system identification of MATLAB. The transfer function of the system can be obtained from the simulated or measured system data such as time response or frequency response. Therefore, the system identification tool of MATLAB [21] is used to obtain the small-signal model for controller design, in this paper.

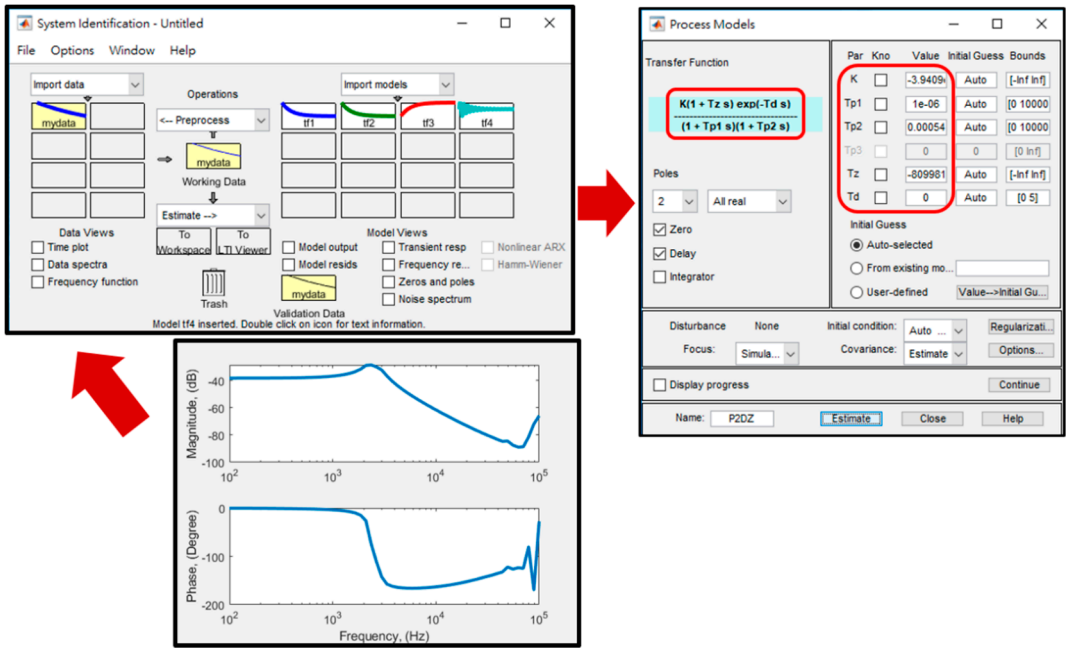


Figure 12. Processing flow windows of the system identification tool of MATLAB.

4.2. Flux-Balance Loop Controller Design

Figure 13 shows the control block diagram of the flux-balance loop, for which the loop gain can be expressed as

$$T_b(s) = G_{comp,b}(s)G_{PWM,b}(s)G_{bc}(s) \tag{16}$$

where $G_{bc}(s)$ represents the transfer function of the controlled plant, which is the duty ratio of MOSFET Q_1 (d_1-tilde) to the magnetizing DC current ($i_{Lm,DC}$-tilde), $G_{PWM,d}(s)$ represents the transfer function of the duty ratio control signal ($v_{con,d}$-tilde) to the duty ratio of MOSFET Q_1, and $G_{comp,b}(s)$ indicates the controller of the flux-balance loop.

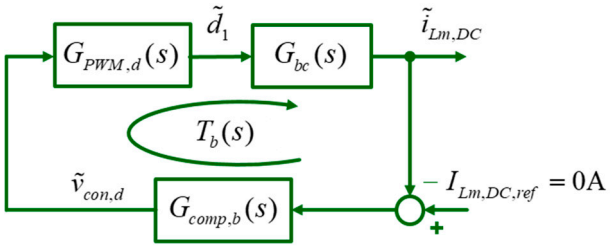


Figure 13. Control block diagram of the flux-balance loop.

Using the system identification tool of MATLAB, the uncompensated loop gain from the duty ratio control signal to the magnetizing DC current under full load operation condition can be expressed as follows. The parameters of the LLC resonant converter are shown in Table 1, which will be shown in Section 5.

$$\begin{aligned} \frac{\tilde{i}_{Lm,DC}}{\tilde{v}_{con,d}} &= G_{PWM,d}(s)G_{bc}(s) \\ &= \frac{1.452\times10^9}{s^2+487.1\times10^3 s+41.49\times10^9}. \end{aligned} \tag{17}$$

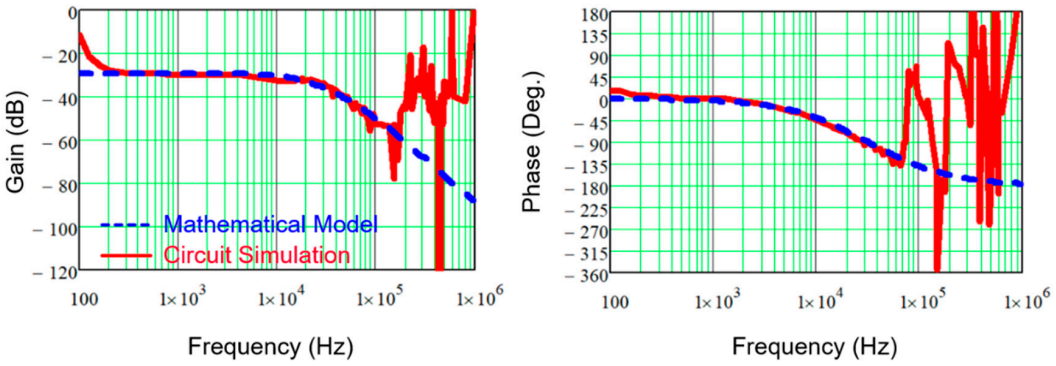
The characteristic equation in (17) has two real poles at 110 krad/s (17.5 kHz) and 377 krad/s (60 kHz), respectively. Figure 14a shows the bode plots of the uncompensated flux-balance loop gains obtained from the mathematical model in (17) (blue dashed line) and Simplis circuit simulation (red solid line). Figure 14a reveals that the dominate pole is at 17.5 kHz. The controller of the flux-balance loop $G_{comp,b}(s)$ can, therefore, be chosen as a PI-type controller and can be expressed as follows

$$G_{comp,b}(s) = K_{pb}\frac{s+z_b}{s} = 20\cdot\frac{s+62.8\times10^3}{s} \quad (18)$$

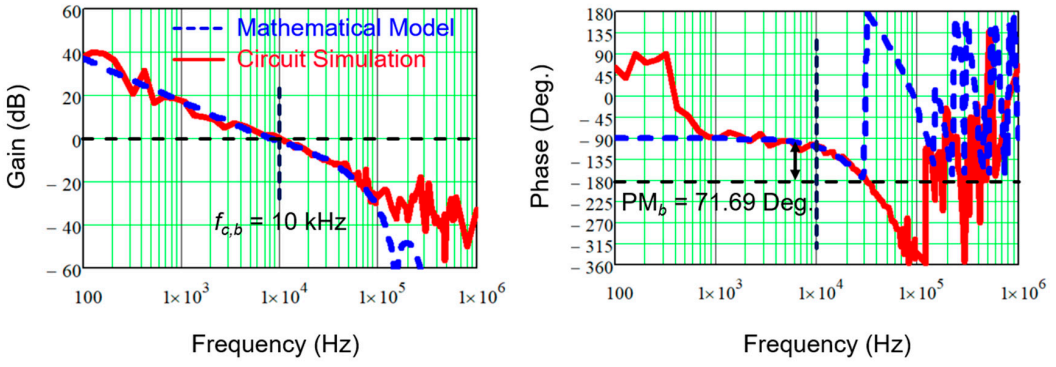
where K_{pb} is the DC gain, which is determined according to the crossover frequency sets as $f_{c,b}$ = 10 kHz, and z_b is the zero, which is set at 17.5 kHz for pole/zero cancellation. The phase margin (PM) is set as 72° to ensure stability. The bode plot of the compensated flux-balance loop gain, after the addition of the controller, is shown in Figure 14b.

Table 1. Parameters of the LLC resonant converter.

Symbol	Description	Quantity
V_i	input voltage	380 V
V_o	output voltage	20 V
$P_{o,\text{rated}}$	rated output power	200 W
n	transformer turns ratio	10
L_m	magnetizing inductance	310 µH
L_{lk1}	leakage inductance in the primary side	6.386 µH
$L_{lk2,pos}$	leakage inductance in the secondary side during the positive cycle	53 nH
$L_{lk2,neg}$	leakage inductance in the secondary side during negative cycle (matched condition)	53 nH
$L_{lk2,neg}$	leakage inductance in the secondary side during negative cycle (mismatched condition)	167.77 nH
L_{ext}	external resonant inductance	42 µH
C_r	resonant capacitance	20 nF
C_o	output capacitance	1000 µF
r_{Co}	equivalent-series-resistance of the output capacitance	40 mΩ



(**a**)



(**b**)

Figure 14. Bode plot of the flux-balance loop gain (**a**) uncompensated and (**b**) compensated.

4.3. Output-Voltage Loop Controller Design

Figure 15 shows the control block diagram of the output-voltage loop, the loop gain of which can be expressed as follows

$$T_v(s) = G_{comp,v}(s)G_{PWM,f}(s)G_{fv}(s) \tag{19}$$

where $G_{fv}(s)$ represents the transfer function of the controlled plant, which is the switching frequency of MOSFET Q_1 (f-tilde) to the output voltage (v_o-tilde), $G_{PWM,d}(s)$ represents the transfer function of the switching frequency control signal ($v_{con,f}$-tilde) to the switching frequency of MOSFET Q_1, and $G_{comp,v}(s)$ is the controller of the output-voltage loop.

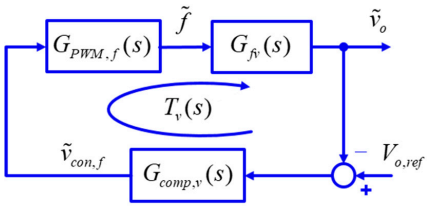


Figure 15. Control block diagram of the output voltage loop.

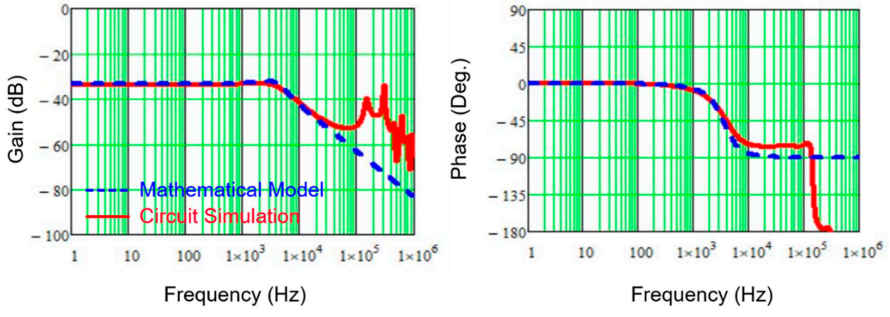
Using the system identification tool of MATLAB, the uncompensated loop gain from the switching frequency control signal to the output voltage under full load operation condition can be expressed as follows. The parameters of the LLC resonant converter are shown in Table 1.

$$\begin{aligned} \frac{\tilde{v}_o}{\tilde{v}_{con,f}} &= G_{PWM,f}(s)G_{fv}(s) \\ &= \frac{594\times(s+30.97\times10^3)}{s^2+42.84\times10^3 s+795.4\times10^6}. \end{aligned} \tag{20}$$

The characteristic equation in (20) has a complex pole pair at 21.42 ± j18.346 krad/s (3.41 ± j2.9 kHz) and a zero at 30.97 krad/s (4.93 kHz). Figure 16a shows the bode plots of the uncompensated output-voltage loop gains obtained from the mathematical model in (20) (blue dashed line) and Simplis circuit simulation (red solid line). Figure 16a reveals that the phase down to −90°, due to the zero, is very close to complex pole pair. Thus, (20) can be simplified as a first-order system. The controller of the output voltage $G_{comp,v}(s)$ can also be chosen as a PI-type controller and can be expressed as follows

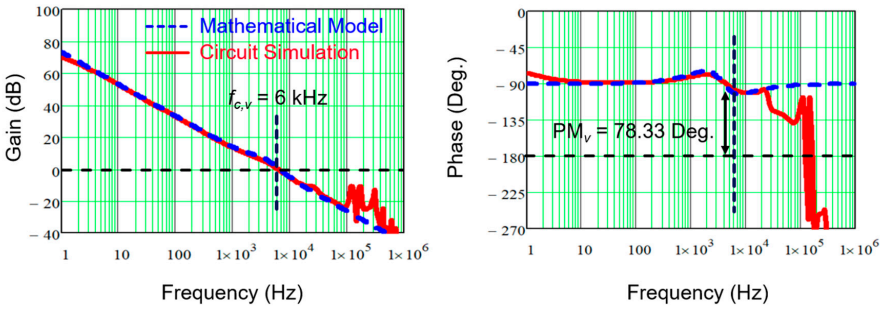
$$\begin{aligned} G_{comp,v}(s) &= K_{pv}\frac{s+z_v}{s} \\ &= 70\cdot\frac{s+18.85\times10^3}{s} \end{aligned} \tag{21}$$

where K_{pv} is the DC gain, which is determined according to the crossover frequency sets as $f_{c,v}$ = 6 kHz, z_v is the zero, which is set at 18.85 kHz for pole/zero cancellation, and the phase margin at $f_{c,v}$ is 78.33° to ensure stability. The bode plot of the compensated output-voltage loop gain, after the addition of the controller, is shown in Figure 16b.



(**a**)

Figure 16. *Cont.*



(**b**)

Figure 16. Bode plot of the output-voltage loop gain (**a**) uncompensated and (**b**) compensated.

5. Simulation and Experimental Verification

To verify the proposed approach, Simplis software was used to construct the simulation, and an experimental platform was built as shown in Figure 17. In this paper, the center-tapped model constructed in Simplis is similar to Figure 5. Two ideal transformers, where the primary side is connecting in parallel, and the secondary side connecting in series, are used. The magnetizing inductance and leakage inductances are added in the primary side and secondary sides, respectively. The advantage of this method is that all of branches current and nodes voltages can easily be measured for observation and analysis.

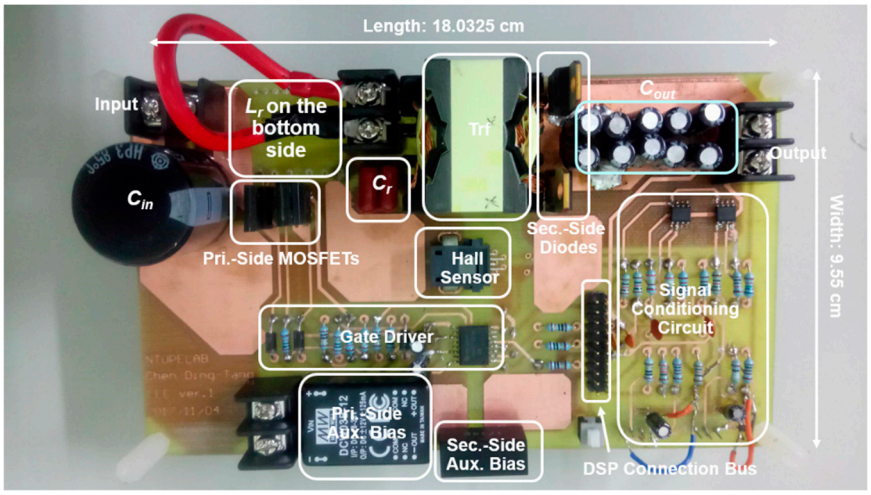


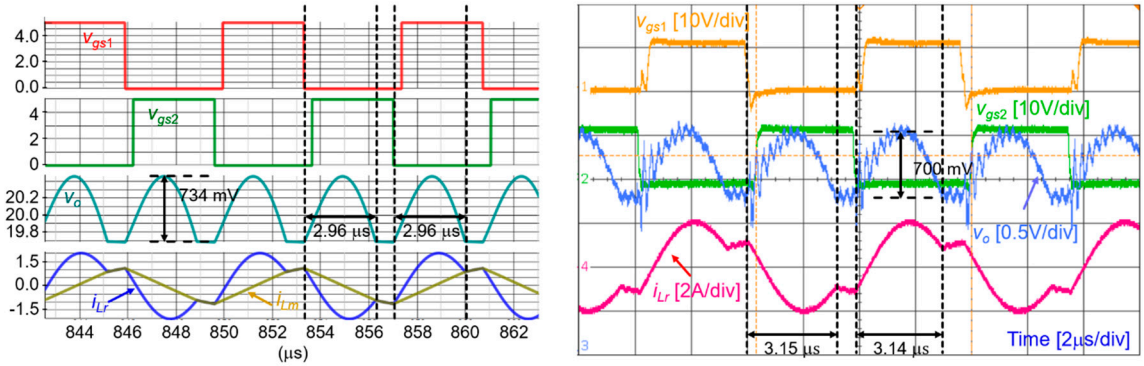
Figure 17. Experimental prototype of LLC resonant converter.

The proposed flux-balance control strategy was implemented by using Texas Instrument C2000 Piccolo 28035 digital signal processor. For experimental equipment, Agilent Technologies InfiniiVision DSO-X 3054A oscilloscope (BW = 500 MHz) was used; Keysight Technologies 1147B current probe (BW = 50 MHz) was used for i_{Lr} measurement, and Sapphire Instrument LDP-6002 (BW = 25 MHz) differential voltage probes were used for differential voltage measurement (v_{gs1}). Table 1 lists the related parameters of the LLC resonant converter. The leakage inductance at the secondary side, during the negative cycle, covers the matched condition ($L_{lk2,neg}$ = 53 nH) and mismatched condition ($L_{lk2,neg}$ = 167.77 nH). The set switching frequency is less than the resonant frequency, i.e., $f_s < f_r$, for an input voltage V_i = 380 V.

5.1. Steady-State Operation

Figure 18 shows the simulated and experimental results of the LLC resonant converter at full load in steady-state operation with the matched secondary-side leakage inductances, i.e., $L_{lk2,pos} = L_{lk2,neg}$

= 53 nH. In Figure 18a, the peak-to-peak ripple of the output voltage is approximately 734 mV. The conduction times of the secondary side diodes are 2.96 µs. The resonant frequency is f_r = 168.9 kHz, and switching frequency is f_s = 134.78 kHz. In Figure 18b, the peak-to-peak ripple of the output voltage is 700 mV and conduction times of the secondary-side diodes are approximately 3.14 µs during the positive and negative cycles. Therefore, the resonant frequency is f_r = 159.23 kHz and switching frequency is f_s = 130.11 kHz. The simulated and experimental results show that the magnetizing current is almost balanced between horizontal axis, i.e., $I_{Lm,DC}$ = 0 A, but some parasitic effects in the secondary side of the hardware cause a mismatch between the simulated and experimental results.



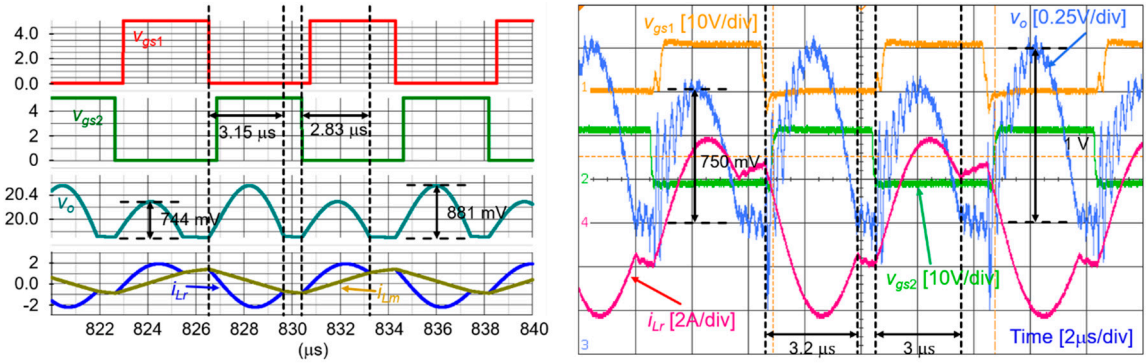
(**a**) (**b**)

Figure 18. Matched secondary side leakage inductances at full load in steady-state operation (**a**) simulation results and (**b**) experiment results.

Figure 19 shows the simulated and experimental results of the LLC resonant converter at steady-state, when operating at full load with the mismatched secondary side leakage inductances, i.e., $L_{lk2,pos}$ = 53 nH and $L_{lk2,neg}$ = 167.77 nH. In Figure 19a, the peak-to-peak ripples of the output voltage during the positive and negative cycles are 744 mV and 881 mV, respectively. The conduction time of the secondary side diode during the positive cycle is 2.83 µs. Therefore, the resonant frequency during the positive cycle is $f_{r,pos}$ = 176.67 kHz. The conduction time of the secondary side diode during the negative cycle is 3.15 µs. Hence, the resonant frequency during the negative cycle is $f_{r,neg}$ = 158.73 kHz. The switching frequency is f_s = 127.98 kHz and magnetizing DC current is $I_{Lm,DC}$ = 436 mA. In Figure 19b, the peak-to-peak ripples of the output voltage during the positive and negative cycles are 750 mV and 1 V, respectively. The conduction time of the secondary side diode during the positive cycle is 3 µs. Hence, the resonant frequency during positive cycle is $f_{r,pos}$ = 166.67 kHz. The conduction time of the secondary side diode during the negative cycle is 3.2 µs; therefore, the resonant frequency during the negative cycle is $f_{r,neg}$ = 156.25 kHz. The switching frequency is f_s = 127.01 kHz. The magnetizing DC current can be estimated as $I_{Lm,DC,est}$ = 400 mA using (15), which is approximately the same as the simulated result, although the experimental result does not measure the magnetizing DC current directly.

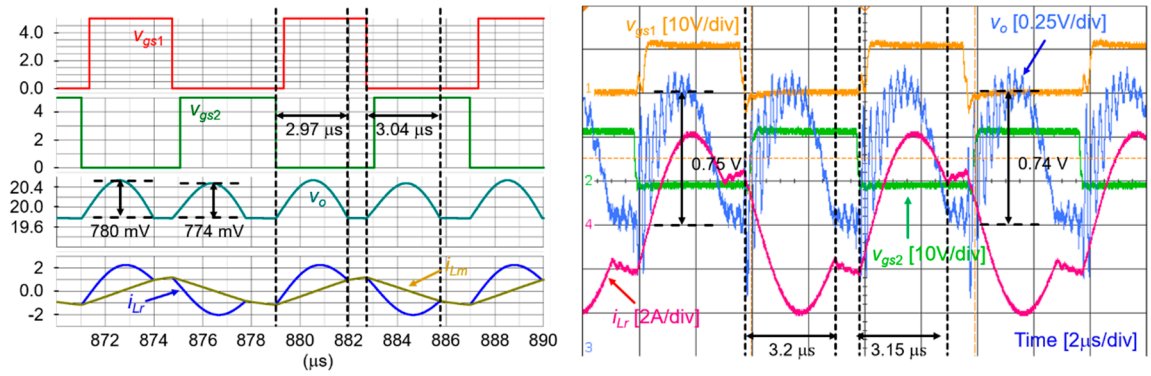
Figure 20 shows the simulated and experimental results of the LLC resonant converter at full load in steady-state with the flux-balance loop control, for the same mismatched condition as that in Figure 19. In Figure 20a, the peak-to-peak ripples of the output voltage during the positive and negative cycles are 780 mV and 774 mV, respectively. The conduction time of the secondary side diode during the positive cycle is 2.97 µs; therefore, the resonant frequency during positive cycle is $f_{r,pos}$ = 168.35 kHz. The conduction time of the secondary side diode during the negative cycle is 3.04 µs; hence, the resonant frequency during the negative cycle is $f_{r,neg}$ = 164.47 kHz. The switching frequency is f_s = 125.37 kHz and magnetizing DC current is $I_{Lm,DC}$ = 19 mA. In Figure 20b, the peak-to-peak ripples of the output voltage during the positive and negative cycles are 750 mV and 740 mV, respectively. The conduction time of the secondary side diode during the positive cycle is 3.15 µs; hence, the resonant frequency

during positive cycle is $f_{r,pos}$ = 158.73 kHz. The conduction time of the secondary side diode during the negative cycle is 3.2 µs; therefore, the resonant frequency during negative cycle is $f_{r,neg}$ = 156.25 kHz. The switching frequency is f_s = 126.21 kHz. The magnetizing DC current can be estimated to be $I_{Lm,DC,est}$ = 20 mA, using (15). The magnetizing DC current estimated from the experimental result is close to the value obtained from the simulations, which confirms the effectiveness of the approach proposed in this paper.



(**a**) (**b**)

Figure 19. Mismatched secondary side leakage inductances at full load in steady-state operation (**a**) simulation results and (**b**) experiment results.



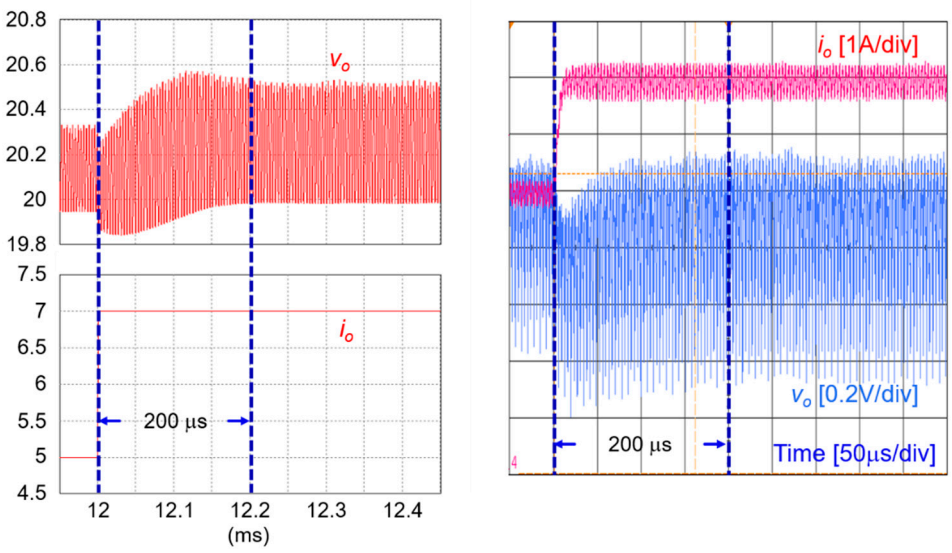
(**a**) (**b**)

Figure 20. Mismatched secondary side leakage inductances at full load in steady-state operation with the flux-balance loop control (**a**) simulation results and (**b**) experiment results.

5.2. Dynamic-State Operation

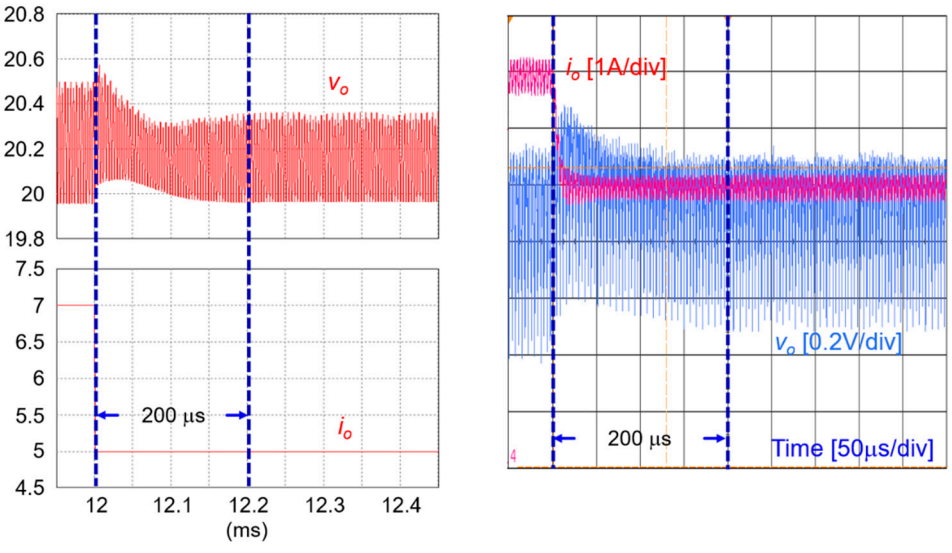
Figure 21 shows the simulated and experimental results of the transient response of the LLC resonant converter, which compensates for the mismatched secondary side leakage inductances using the flux-balance loop, for load changes from 50% to 70%. The transient time is approximately 200 µs, as shown in the simulated and experimental results. Figure 21 reveals that the voltage loop and the flux-balance loop operate simultaneously, without affecting each other in the transient state. Figure 22 shows the simulated and experimental results of the transient response of the LLC resonant converter, which compensates for the mismatched secondary side leakage inductances with the flux-balance loop, for load changes from 70% to 50%. The simulated and experimental results show that the transient time is 200 µs. Figure 22 shows that the voltage loop and flux-balance loop do not affect each other, even during the load step down. Figure 23 shows the experimental results of the disabled and enabled flux-balance loop at 70% load, considering the mismatched secondary side leakage inductances. When the flux-balance loop is disabled, the maximum peak-to-peak ripple of the output voltage is

818.75 mV. Once the flux-balance loop is enabled, the maximum peak-to-peak ripple of the output voltage reduces to 731.25 mV.



(**a**) (**b**)

Figure 21. Transient response of load change from 50% to 70% with the mismatched secondary side leakage inductances and the flux-balance loop control (**a**) simulation results and (**b**) experiment results.



(**a**) (**b**)

Figure 22. Transient response of load change from 70% to 50% with the mismatched secondary side leakage inductances and the flux-balance loop control (**a**) simulation results and (**b**) experiment results.

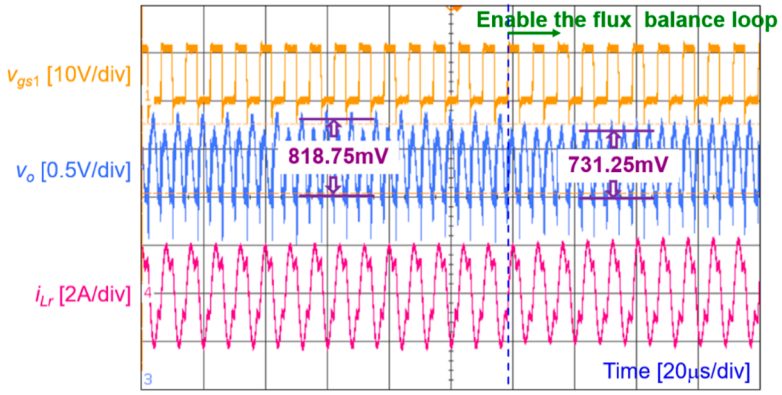


Figure 23. Experiment results of the disabled/enabled flux-balance loop at 70% load, considering the mismatched secondary side leakage inductances.

6. Conclusions

In this paper, a flux-balance loop control strategy was proposed to solve the flux walking issues of the center-tapped transformer in the LLC resonant converter, which were caused by mismatched leakage inductances at the secondary side. The magnetizing DC current effect and voltage gain parameter variation caused by the mismatched conditions at the secondary side were analyzed. Based on these analyses, the flux-balance control loop combining with the original output-voltage control loop, was proposed to resolve the issues. Besides, a magnetizing DC current sampling strategy and estimation scheme was also proposed to overcome the difficulties in measuring the magnetizing DC current. The simulation and experimental results confirmed the effectiveness of the proposed control strategy.

Author Contributions: Y.-C.L. substantially contributed to literature search, control strategy design, examination and interpretation of the results, development of the overall system, and review and proofreading of the manuscript. D.-T.C. substantially contributed to implement the control strategy, production and analysis of the results, and preparation and revision of the manuscript. C.-J.C. substantially contributed to the review and proofreading of the manuscript.

Funding: This work was supported by the Ministry of Science and Technology (MOST) in Taiwan under grants MOST 107-2221-E-002-054-MY2 and National Taiwan University under grants NTU-CC-108L890701.

Acknowledgments: The authors want to thank SIMPLIS Technologies Corporation, U.S.A, for providing SIMPLIS simulation tool.

Conflicts of Interest: The authors declare no conflict of interest.

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