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A Si-FET-Based High Switching Frequency Three-Level LLC Resonant Converter

Jung-Woo Yang and Sang-kyoo Han *

POELSA, Power Electronics System Laboratory, Kookmin University, Seoul 100-011, Korea
* Correspondence: djhan@kookmin.ac.; Tel.: +82-910-5467

Received: 16 July 2019; Accepted: 6 August 2019; Published: 9 August 2019

Abstract: This paper highlights the proposed silicon field-effect transistor (Si-FET)-based high switching frequency three-level (TL) LLC resonant converter. It provides a detailed operational analysis of the converter; the multilevel (ML) organization of cells; voltage-balancing principles; current-balancing principles; loss comparison between Si-FETs and gallium-nitride (GaN)-FETs; and an optimal design consideration based on loss analysis. This analysis reveals that the switching losses of all power switches can be considerably reduced as the voltage across each switch can be set to half of the input voltage without an additional circuit or control strategy. Moreover, the current of each resonant inductor is automatically balanced by a proposed integrated magnetic (IM)-coupled inductor. Therefore, the operating frequency can be easily increased to near 1 MHz without applying high-performance switches. In addition, the resonant tanks of the converter can be a group of cells for multilevel operation, which indicates that the voltage across each switch is further reduced as more cells are added. Based on the results of the analysis, an optimal design consideration according to the resonant tank and switching frequency is discussed. The proposed converter was validated via a prototype converter with an input of 390 V, an output of 19.5 V/18 A, and a frequency of 1 MHz.

Keywords: three-level LLC resonant converter; 1 MHz operation; Si-FET; voltage balancing; current balancing; multilevel; voltage stress

1. Introduction

Size minimization of modern power systems, including those for communications, TV, and electric vehicle (EV) systems, has become an increasingly important objective. Size reduction of converters is oftentimes accompanied by high-frequency minimization of magnetics, i.e., inductors and transformers. Unfortunately, during the process, the high switching loss causes a serious thermal problem and a large heat sink, which can be resolved by the application of a soft-switching technique or the use of high-performance switches.

Some studies have proposed certain kinds of high-frequency DC–DC topologies with soft-switching [1–7]. Practically, employing soft-switching methods on the main switches can reduce the switching loss and achieve higher efficiency, higher power density, and lower system costs. Nonetheless, these cannot achieve zero-voltage switching (ZVS) in all load conditions, aside from the fact that an additional circuit potentially degrades the power density.

A number of LLC resonant converters can easily solve the abovementioned problems [8–9]. Under all load conditions, all switches can operate with the ZVS without additional circuits. Moreover, zero-current switching (ZCS) of output rectifier diodes can be ensured, thereby removing the need for snubber circuits to prevent voltage spikes and reverse recovery problems. The LLC resonant converter achieves high efficiency during high-frequency operation. However, with these converters, increasing the switching frequency is restrained by the higher turned-off loss of silicon field-effect transistors (Si-FETs). To improve the performance of the high-frequency operation, high-

performance switches, i.e., gallium–nitride field-effect transistors ((GaN)-FETs) can be employed instead of Si-FETs [10–13]. These switches feature low on-state resistance, fast rise-and-fall time, and small drain–source capacitance, which favor the dramatic decrease in the switching and conduction losses. On the other hand, they are costly and require an additional gate driver and a voltage source near 5 V.

Among the various means of switching losses reduction, various three-level (TL) resonant converters with half of the input voltage for the voltage across the main switches have been utilized in some studies [14–19]. The principle behind the practicality of such converters is the possible utilization of high-performance switches due to the reduced rated voltage on the switches, mainly as a consequence of the lower drain–source resistance relative to the lower breakdown voltage [18]; moreover, the lower drain–source voltage can reduce the switching power loss [19]. In [14], although the voltage stress of all switches was found to be half the input voltage, additional dead time was required, leading to more complex gate driving, smaller effective duty, and larger additional circulating current. A fixed-frequency TL LLC resonant converter was presented in [15]. For this converter, although the voltage across switches was half of the input voltage, two clamp diodes were required. Moreover, the main switches cannot be guaranteed to be at half the input voltage when there is a slight difference in the parasitic capacitance of switches or the gate-driving signal.

Figure 1 shows a conventional TL LLC resonant converter [17]. It consists of two half-bridge (HB) LLC resonant converters arranged in series and sharing a transformer and a resonant inductor. Switches Q_1 and Q_3 are operated complementarily to Q_2 and Q_4 at a constant duty (D =0.5). When Q_1 and Q_3 are turned on, the current flows through the input capacitor C_{in1} are as shown in Figure 1a, and the voltage is determined by the equation:

$$V_{Cin1} = V_{Cr1} + V_{Cr2}. \tag{1}$$

Alternatively, when Q_2 and Q_4 are on, the current flows through the other input capacitor, C_{in2}, are as shown in Figure 1b, and the voltage is determined by the equation:

$$V_{Cin2} = V_{Cr1} + V_{Cr2}. \tag{2}$$

Therefore, the voltage across the switches is set to half of the input voltage. Moreover, capacitors C_{r1} and C_{r2} are implemented as the resonant capacitors.

However, given different capacitance, the resonant capacitor currents i_{Cr1} and i_{Cr2} are imbalanced due to the impedance difference of each resonant capacitor. Thus, the voltages of each input capacitor V_{Cin1} and V_{Cin2} cannot be guaranteed to be at half the input voltage because of the current imbalance. Consequently, the voltage across the switches cannot be guaranteed to be at half the input voltage. To confirm these issues, the Power SIM (PSIM) (Rockville, MD, USA) simulation results are presented in Figure 2, considering the following parameters:

1. Input voltage: V_{IN} = 390 V
2. Output voltage: V_O = 19.5 V
3. Output power: P_O = 350 W
4. Turn ration: n = 5

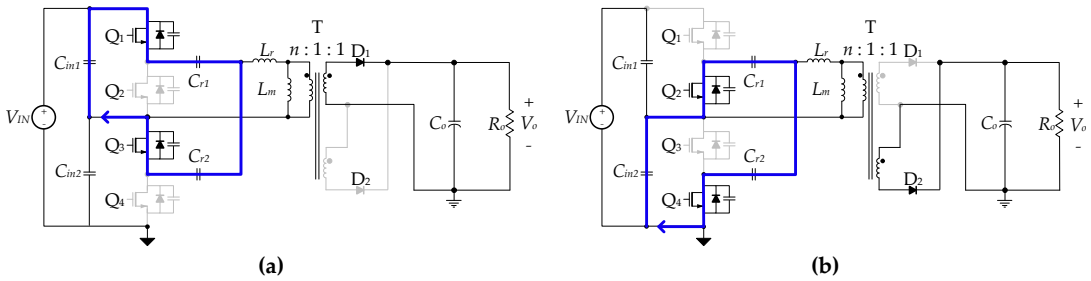


Figure 1. A conventional three-level (TL) LLC resonant converter resonant converter voltage clamping by (**a**) C_{in1} and (**b**) C_{in2}.

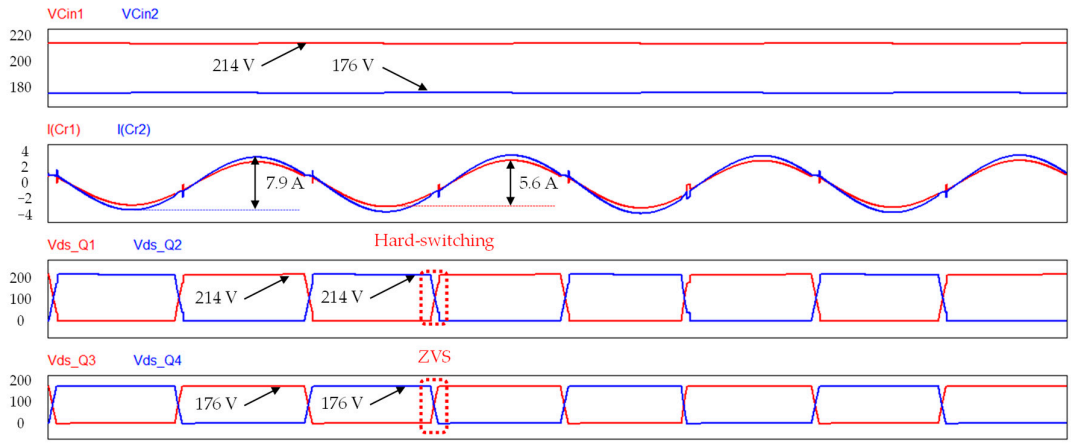


Figure 2. PSIM simulation results of the conventional TL LLC resonant converter with –10% C_{r1}, +10% C_{r2} tolerance.

Figure 2 displays the PSIM simulation waveforms of the voltage across input capacitors, the currents through resonant capacitor, and the drain–source voltage of the conventional TL LLC resonant converter. Assuming different capacitance for the resonant capacitors, the voltage of the input capacitor gets imbalanced, together with the drain–source voltage of switches. Furthermore, switches Q_1 and Q_2 operate under hard switching because they have higher voltage stress than Q_3 and Q_4. Therefore, the conventional TL LLC resonant converter cannot ensure the voltage balance and ZVS of all switches.

This paper proposes a Si-FET-based high switching frequency TL LLC resonant converter, with a discussion of its mode analysis, voltage-balancing principles, current balancing principles, and optimal design considerations for high efficiency. Structurally, it consists of four stacked switches in series, two resonant tanks, and a balancing capacitor connected to each resonant tank. Switches Q_1 and Q_3 in the converter operate with a constant duty ratio, with the other pair (Q_2 and Q_4) complementing their operation. This converter is especially important as it ensures the balance of the voltage across each switch and the current through the IM-coupled inductor. First, the balancing capacitor ensures that the voltage across each switch is half that of the input voltage, without any additional dead time or clamp diodes required. Here, because only the balancing capacitor is required to ensure the balance in voltage, there is no need for an additional circuit or digital IC. Moreover, the offset voltage of the resonant capacitors is a quarter of the input voltage, allowing the use of low-voltage rating capacitors. Secondly, the IM-coupled inductor in the converter ensures the current balance of each resonant inductor without adding a balancing circuit or control strategy.

The rest of the paper is structured as follows. The detailed circuit operation is presented in Section 2. An analysis of the voltage balancing principles, current balancing principles, voltage conversion ratio, performance comparison between Si-FETs and GaN-FETs, and optimal design consideration based on loss comparison is given in Section 3. The validity of the TL LLC resonant converter is confirmed through the experimental results of a prototype converter from an input of 390 V and an output of 19.5 V/18 A, as shown in Section 4. Conclusions are provided in Section 5.

2. Operating Mode Analysis

2.1. Circuit Operation

Figure 3 is a schematic representation of the proposed TL LLC resonant converter, which consists of four stacked switches in parallel and two resonant tanks. The converter's key waveforms in a steady state are depicted in Figure 4; here, Q_1 and Q_3 are operated with a constant duty ratio (D = 0.5), with the complementary Q_2 and Q_4. Thus, the converter has six switching period modes, with each detailed operating circuit illustrated in Figure 5. To illustrate the operation of the proposed converter, several assumptions are considered:

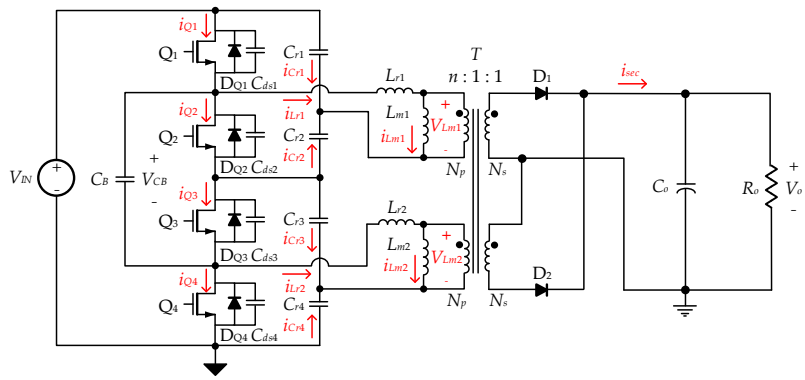


Figure 3. Analysis circuit of the TL LLC resonant converter.

1. Output capacitor C_O is large enough to maintain a constant voltage.
2. The four resonant capacitors, C_{r1}, C_{r2}, C_{r3}, and C_{r4}, have the same capacitance of C_r.
3. The balancing capacitor C_B is larger than the resonant capacitors (C_{r1}, C_{r2}, C_{r3}, and C_{r4}) to be considered as a voltage source of $V_{IN}/2$.
4. The output capacitance of all Si-FETs is the same as the capacitance of C_{ds}.
5. All Si-FETs and main switches have parasitic diodes of D_{Q1}, D_{Q2}, D_{Q3}, and D_{Q4}.
6. The two resonant inductors, L_{r1} and L_{r2}, have the same inductance L_r.
7. The two magnetizing inductors, L_{m1} and L_{m2}, have the same inductance L_m.
8. The turn ratio of the main transformer T is $n = N_p/N_s$.

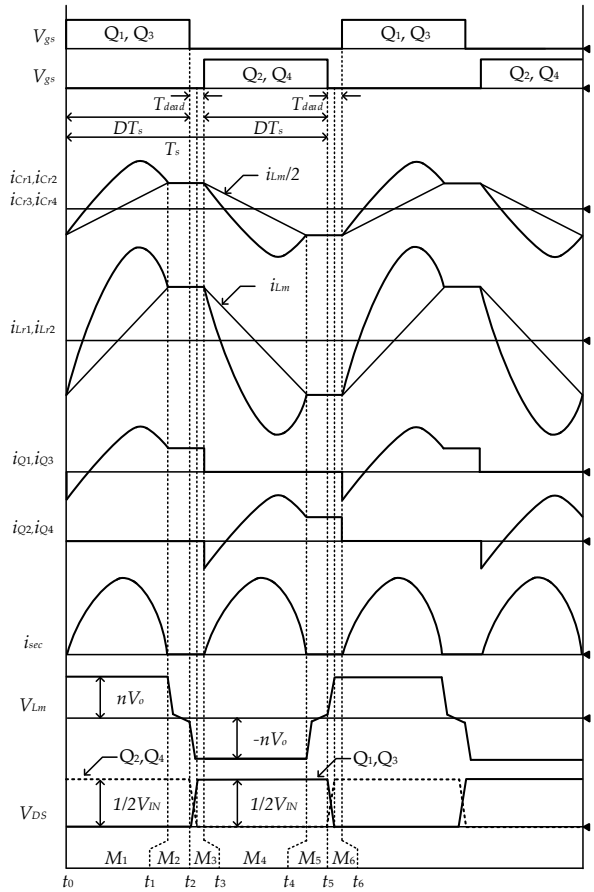


Figure 4. Key waveforms of the converter in a steady state.

2.1.1. Circuit Operation in a Steady State

Mode 1 [$t_0 - t_1$]: This mode begins when Q_1 and Q_3 are turned on with ZVS at t_0. Figure 6a shows the equivalent circuit during Mode 1. Resonant inductors L_{r1} and L_{r2} have a positive current flow with sinusoidal waveform by the resonance of C_{r1}, C_{r2}, C_{r3}, and C_{r4}, as follows:

$$i_{Lr1}(t) = i_{Lr2}(t) = i_{Q1}(t) = i_{Q3}(t) = \frac{V_{T1}}{z_1}\cos[\omega_1(t - t_0) + \alpha_1] \tag{3}$$

$$i_{Cr1}(t) = i_{Cr2}(t) = i_{Cr3}(t) = i_{Cr4}(t) = \frac{V_{T1}}{2z_1}\cos[\omega_1(t - t_0) + \alpha_1]. \tag{4}$$

As the rectifier diode D_1 is conducting, the output voltage V_O is reflected in the turn ratio, n. Therefore, the primary voltage of transformer $V_T(t)$ is set to nV_O. Subsequently, the magnetizing inductor L_m is built up, and its current $i_{Lm}(t)$ is linearly raised from negative to positive:

$$i_{Lm1}(t) = i_{Lm2}(t) = i_{Lr1}(t_0) + \frac{nV_O}{L_m}(t - t_0) \tag{5}$$

$$i_{sec}(t) = 2n[i_{Lr}(\mathrm{t}) - i_{Lm}(\mathrm{t})]. \tag{6}$$

Voltages across the main switches V_{DSQ2} and V_{DSQ4} are set to half the input voltage. The offset voltage of the resonant capacitor can also be set to half the input voltage, and the balancing capacitor has a constant voltage of half the input voltage. The equivalent circuit during Mode 1 is shown in Figure 6a, with the equations of voltage being:

$$V_{Cr1}(t) = V_{Cr3}(t) = \frac{V_{IN}}{2} - nV_O + V_{T1}\sin[\omega_1(t - t_0) + \alpha_1] \tag{7}$$

$$V_{cr2}(t) = V_{cr4}(t) = V_{Cr1}(t) - \frac{V_{IN}}{2} \tag{8}$$

$$V_{DSQ2}(t) = V_{DSQ4}(t) = \frac{V_{IN}}{2}, \tag{9}$$

where $V_{T1} = \sqrt{(z_1 i_{Lr}(t_0))^2 + (-V_{IN}/2 + nV_O + V_{Cr}(t_0))^2}$, $\alpha_1 = tan^{-1}[(z_1 i_{Lr}(t_0))/(-V_{IN}/2 + nV_O + V_{Cr}(t_0))]$, $\omega_1 = 2\pi f_1 = (1/\sqrt{2L_r C_r})$, and $z_1 = \sqrt{L_r/(2C_r)}$.

Mode 2 [$t_1 - t_2$]: At the end of Mode 2, the primary currents $i_{Lr1}(t)$ and $i_{Lr2}(t)$ reach the same current level as the magnetizing currents $i_{Lm1}(t)$ and $i_{Lm2}(t)$. Thus, the magnetizing inductors L_{m1} and L_{m2} take part in the resonance with two resonant tanks:

$$i_{Lr1}(t) = i_{Lr2}(t) = i_{Q1}(t) = i_{Q3}(t) = \frac{V_{T2}}{z_2}\cos[\omega_2(t - t_1) + \alpha_2] \tag{10}$$

$$i_{Lm1}(t) = i_{Lm2}(t) = i_{Lr}(t) \tag{11}$$

$$i_{Cr1}(t) = i_{Cr2}(t) = i_{Cr3}(t) = i_{Cr4}(t) = \frac{V_{T2}}{2z_2}\cos[\omega_2(t - t_1) + \alpha_2]. \tag{12}$$

Accordingly, the voltages across the main switches, V_{DSQ2} and V_{DSQ4}, are set to half of the input voltage, with the offset voltage of the resonant capacitor also set to half of the same input voltage, as the balancing capacitor has a constant voltage that is half of the input voltage. In addition, output rectifier D_1 is turned off with ZCS and becomes reverse-biased. During this mode, with the output being higher than the secondary voltage of the transformer, it is separated from the transformer primary side. Therefore, the output capacitor supplies to the load:

$$V_{Cr1}(t) = V_{Cr3}(t) = \frac{V_{IN}}{2} + V_{T2}\sin[\omega_2(t - t_1) + \alpha_2] \tag{13}$$

$$V_{cr2}(t) = V_{cr4}(t) = V_{Cr1}(t) - \frac{V_{IN}}{2} \tag{14}$$

$$V_{DSQ2}(t) = V_{DSQ4}(t) = \frac{V_{IN}}{2}, \tag{15}$$

where $V_{T2} = \sqrt{(z_2 i_{Lr}(t_1))^2 + (-V_{IN}/2 + nV_O + V_{Cr}(t_1))^2}$, $\alpha_2 = tan^{-1}[(z_2 i_{Lr}(t_1))/(-V_{IN}/2 + nV_O + V_{Cr}(t_1))]$, $\omega_2 = 2\pi f_2 = (1/\sqrt{2C_r(L_r+L_m)})$, and $z_2 = \sqrt{(L_r + L_m)/(2C_r)}$.

Mode 3 [$t_2 - t_3$]: This mode begins when Q_1 and Q_3 are turned off. Subsequently, the voltages of parasitic capacitors C_{ds1} and C_{ds3} are charged from 0 to half of the input voltage $V_{IN}/2$; linearly, the voltages of parasitic capacitor C_{ds2} and C_{ds4} are discharged from $V_{IN}/2$ to 0 by $i_{Lm}(t_1)$. After i_{Lm} fully charges C_{ds1} and C_{ds3}, and discharges C_{ds2} and C_{ds3}, D_{b2} and D_{b4}, the anti-parallel diodes of Q_2 and Q_4, are forward-biased, and then the resonant tank of C_{r1}, C_{r2}, and L_{r1} and another resonant tank of C_{r3}, C_{r4}, and L_{r2} conduct simultaneous resonance. In addition, as the rectifier diode D_2 is conducting, the primary voltage of transformer $V_T(t)$ decreases to $-nV_O$. The current and voltage for this mode are expressed as follows:

$$V_{Cr1}(t) = V_{Cr3}(t) \cong V_{Cr1}(t_2) - \frac{i_{Lm}(t_0)}{2C_r}(t - t_2) \cong V_{Cr1}(t_2) + \frac{i_{Lm}(t_1)}{2C_r}(t - t_2) \tag{16}$$

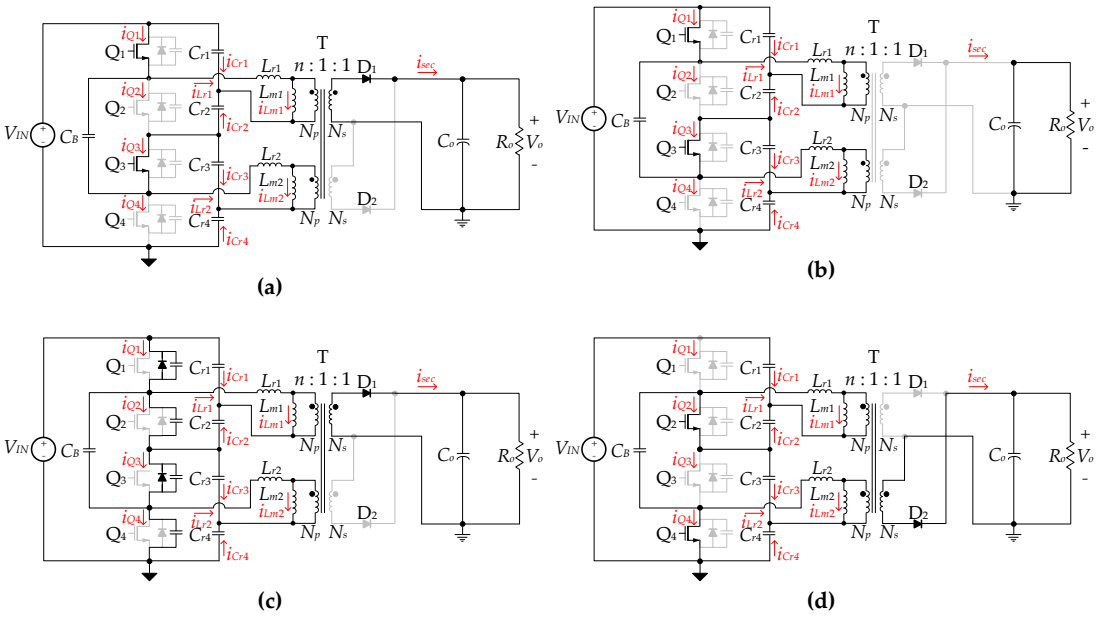
$$V_{Cr2}(t) = V_{Cr4}(t) = \frac{i_{Lm}(t_1)}{2C_r} - \frac{V_{IN}}{2} V_{Cr1}(t_2) \tag{17}$$

$$i_{Cr1}(t) = i_{Cr2}(t) = i_{Cr3}(t) = i_{Cr4}(t) = -\frac{i_{lm}(t_0)}{2} \cong \frac{i_{lm}(t_1)}{2} \tag{18}$$

$$V_{DSQ1}(t) = V_{DSQ3}(t) = -\frac{i_{lm}(t_0)}{2C_{ds}}(t - t_2) \cong \frac{i_{lm}(t_1)}{2C_{ds}}(t - t_2) \tag{19}$$

$$V_{DSQ2}(t) = V_{DSQ4}(t) = \frac{V_{IN}}{2} + \frac{i_{lm}(t_0)}{2C_{ds}}(t - t_2) \cong \frac{V_{IN}}{2} - \frac{i_{lm}(t_1)}{2C_{ds}}(t - t_2). \tag{20}$$

Figure 5d–f describes the operation principle of Modes 4–6, the equivalent circuit, and the operating circuit, which are the same as for Modes 1–3; thus, no further description is needed.



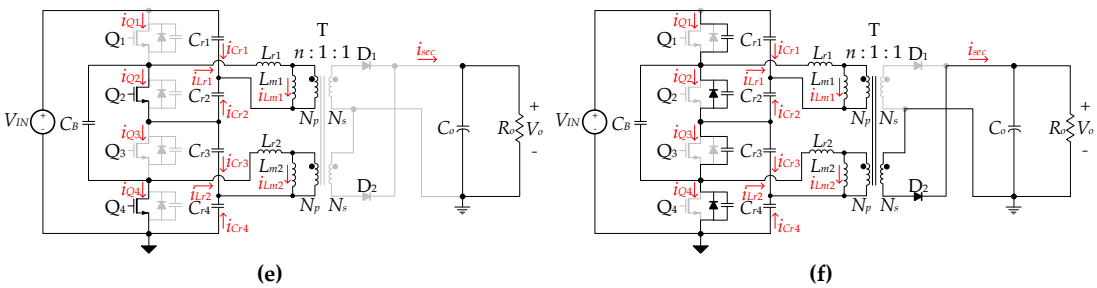


Figure 5. Operating mode according to switching period: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; and (**f**) Mode 6.

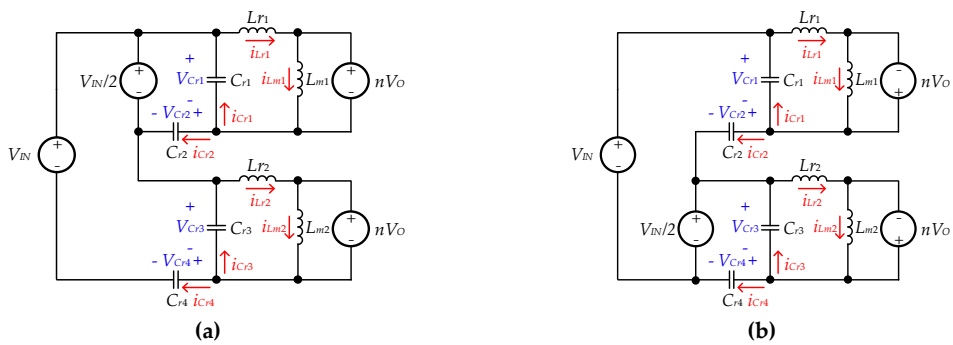


Figure 6. Equivalent circuit according to switching period: (**a**) Mode 1 and (**b**) Mode 3.

3. Analysis and Design Considerations

3.1. Principle of Voltage Balancing

To ensure that the voltage across the main switches is half of the input voltage, the balancing capacitor voltage V_{CB}, should be maintained. The TL LLC resonant converter can maintain V_{CB} at half of the input voltage with no additional components or digital control. Nonetheless, the capacitance of the balancing capacitor should be 10 times that of the converter, large enough to not have any effect on the resonance:

$$C_B > 10C_r(C_r = C_{r1} = C_{r2} = C_{r3} = C_{r4}). \tag{21}$$

Figure 7 shows the voltage-balancing principle according to the switch operation. Firstly, as soon as Q_1 and Q_3 are turned on, the current flow through the balancing capacitor C_B is as shown in Figure 7a, with its voltage represented by:

$$V_{CB} = V_{Cr1} + V_{Cr2}. \tag{22}$$

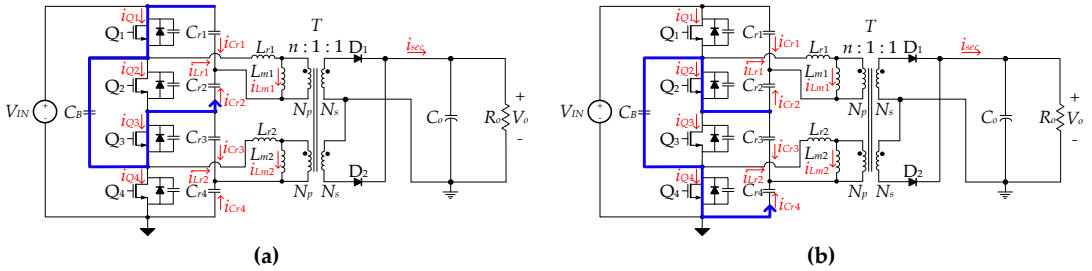


Figure 7. Voltage-balancing principle according to switching period: (**a**) Q_1 and Q_3 turned on; and (**b**) Q_2 and Q_4 turned on.

Secondly, when Q_2 and Q_4 are turned on, the current flow through the balancing capacitor is as shown in Figure 7b, with the voltage as follows:

$$V_{CB} = V_{Cr3} + V_{Cr4}. \tag{23}$$

Finally, the sum of voltages of all the resonant capacitor are the same as the input voltage:

$$V_{IN} = V_{Cr1} + V_{Cr2} + V_{Cr3} + V_{Cr4}. \tag{24}$$

Therefore, the voltage across the main switches is set to half the input voltage. In addition, when the capacitance of the resonant capacitors has a different value in the conventional TL LLC resonant converter mentioned in earlier sections, the voltage across the main switches cannot be guaranteed to be half of the input voltage. However, with the proposed voltage-balancing method, the offset voltage of each resonant capacitor is fixed at nV_O regardless of the value of the resonant capacitor. Consequently, as the voltage of the balancing capacitor clamps the voltage across the main switches, the voltage across them is also set to half of the input voltage.

Moreover, the proposed TL LLC resonant converter can be extended into a multi-level (ML) LLC resonant converter by organization of the cells. Figure 8a shows an example of the proposed TL LLC resonant converter with the organization of cells. The basic cell unit consists of two switches, Q_{2k} and Q_{2k-1}; a resonant capacitor, C_{r_2k} and C_{r_2k-1}; a resonant inductor, L_{r_k}; and a transformer, T_k, as shown in Figure 8b. The ML LLC resonant converter with n cells is shown in Figure 9. It consists of n cells and n balancing capacitors, which are connected to the node A_n of each cell. Through the addition of the n cells, the voltage across the main switches can be proportionally reduced to V_{IN}/n according to the number of cells.

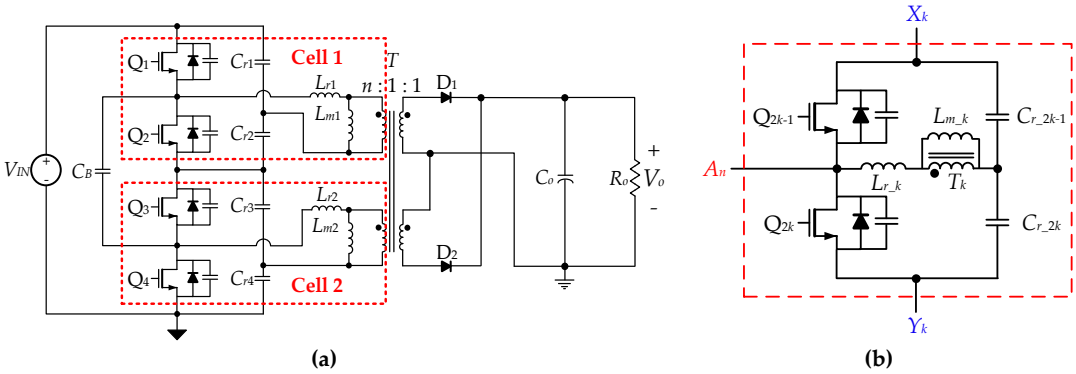


Figure 8. A TL LLC resonant converter with the organization of cells: (**a**) Organization of cells for the converter; and (**b**) a basic cell unit of the converter.

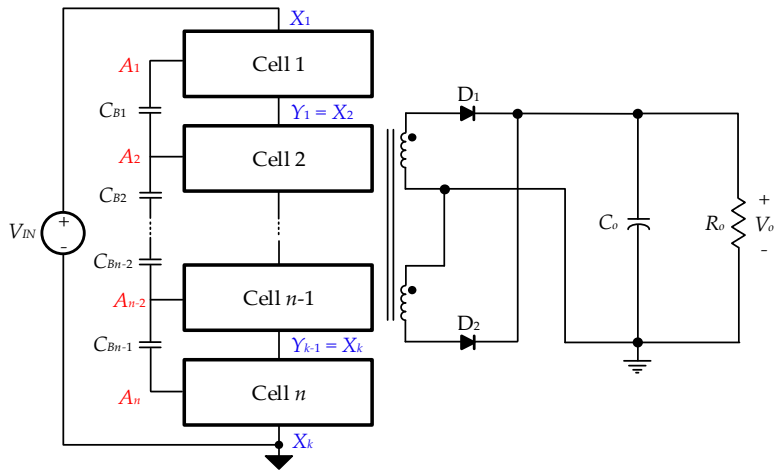


Figure 9. The proposed multi-level (ML) LLC resonant converter resonant converter.

When group Q_{2k-1} is turned on, V_{Cbm} is the same as the sum of V_{cr_2k-1} and V_{cr_2k}. In contrast, when the group Q_{2k} is turned on, V_{Cbm} is the same for the sum of V_{Cr_2x}, V_{Cr_2x-1}, V_{Cr_4x}, and V_{Cr_4x-1} for $m = 1, 2, \cdots n-2, n-1$, and $k = 1, 2, \cdots n-1, n$. V_{Cbm} is obtained as follows:

$$V_{Cbm} = V_{Cr\_2k} + V_{Cr\_2k-1} = V_{Cr\_4k} + V_{Cr\_4k-1}. \tag{25}$$

Based on Equation (25), all balancing capacitors can implement the voltage balancing of each cell. In addition, the sum of all resonant capacitor voltages is the same for the input voltage. Considering Equation (24), the voltage stress of all switches is set to V_{IN}/n:

$$V_{IN} = V_{Cr1} + V_{Cr2} + V_{Cr3} + \cdots + V_{Cr\_2k-2} + V_{Cr\_2k-1} + V_{Cr\_2k} \tag{26}$$

$$V_{IN}/2 = V_{Cr1} = V_{Cr2} = V_{Cr3} = \cdots = V_{Cr\_2k-2} = V_{Cr\_2k-1} = V_{Cr\_2k}. \tag{27}$$

3.2. Principle of Current Balancing

The resonant inductor is generally implemented with the leakage inductor of the transformer. Nonetheless, the transformer of the proposed TL LLC resonant converter has a very small leakage inductance due to the strongly coupled structure of the planar transformer; therefore, the proposed converter must have either two additional inductors or one differential mode (DM)-coupled inductor at each primary side of the transformer. In this case, the current balance of each primary side is very important. Assuming that the parameters of the transformer and gate signals are ideal, the average current of magnetizing inductors $\langle i_{Lm1} \rangle$ and $\langle i_{Lm2} \rangle$ is 0. Subsequently, the magnetizing current of each resonant tank assumes the same value:

$$i_{Lm1} = i_{Lm2}. \tag{28}$$

In addition, the primary currents i_{Lr1} and i_{Lr2} have the same value:

$$i_{Lr1}(= i_{Lm1} + i_{sec}/n) = i_{Lr2}(= i_{Lm2} + i_{sec}/n). \tag{29}$$

However, with every component having a tolerance, each resonant capacitor yields a different practical value. Likewise, the practical impedance of each DM-coupled inductor becomes different, because of the different wire lengths and air gaps. Therefore, when the abovementioned conditions occur, the current of each resonant inductor, as well as the current stress of each power switch, becomes imbalanced. Figure 10 shows the PSIM simulation waveforms of each resonant inductor and drain–source voltage. When the value of each resonant capacitor has ±10% tolerance, the drain–source voltage can be set to half of the input voltage by the balancing capacitor, but the current of each resonant inductor is imbalanced, as shown in Figure 10a. In addition, when the value of the resonant inductor has ±10% tolerance, the voltage across each power switch can be set to half of the input voltage with the aid of the balancing capacitor. On the other hand, Figure 10b shows that the current of each resonant inductor is imbalanced, which can induce destruction of the switches and thermal imbalance problems.

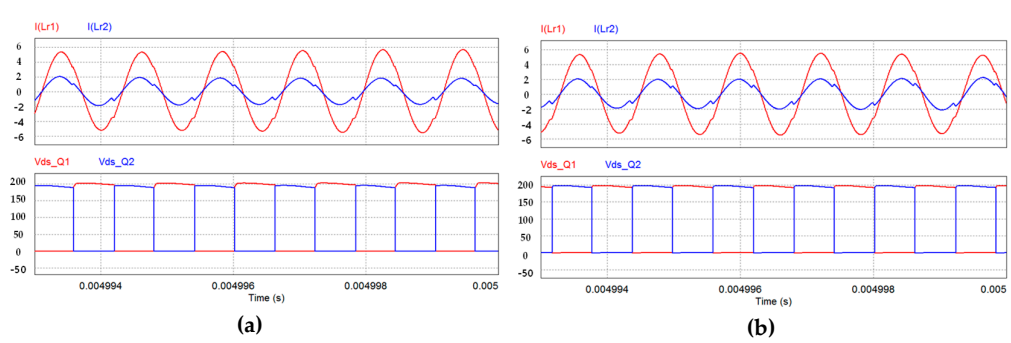


Figure 10. PSIM simulation results of the proposed TL LLC resonant converter: (**a**) In the case of increased C_{r1} and C_{r2} by 10%, and decreased C_{r3} and C_{r4} by 10%; and (**b**) in the case of increased L_{r1} by 10%, and decreased L_{r2} by –10%.

To overcome the practical current imbalance, common-mode (CM)-coupled inductor is inserted into the transformer primary side as shown in Figure 11. Despite the existence of the tolerances of resonant capacitors and inductors, the CM-coupled inductor achieves the exact current balance of each transformer primary side. However, as there is the need for an additional CM-coupled inductor besides the resonant inductors, the converter size may be increased.

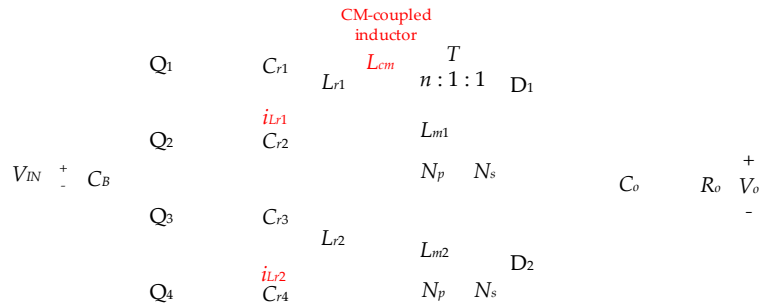


Figure 11. The proposed TL LLC resonant converter with the CM-coupled inductor.

Figure 12a shows the proposed single-core IM capable of replacing the CM-coupled inductor and resonant inductors. Apparently, the proposed IM-coupled inductor not only achieves current balance, but also makes the converter more compact. The reluctance model of the proposed IM-coupled inductor based on the proposed structure of the CM-coupled inductor in Figure 12a is as shown in Figure 12b. The equivalent circuit is similar to the magnetic structure; the magneto-motive force (mmf) F [A] is produced by n-turn windings, N_{Lr1} and N_{Lr2} and carrying currents of i_{Lr1} and i_{Lr2}, and each reluctance of $\mathcal{R} = \mu_o(\ell_g + \ell/\mu_r)/A[H^{-1}]$, where ℓ is the magnetic path length, ℓ_g is the air-gap of the core, μ_r is the relative permeability, μ_o is the absolute permeability, and A is the cross-sectional area of the core. Figure 13a illustrates the proposed IM inductance model based on the reluctance model. Also, the IM inductance model in Figure 13a can be represented as the equivalent IM-coupled inductor, as shown in Figure 14.

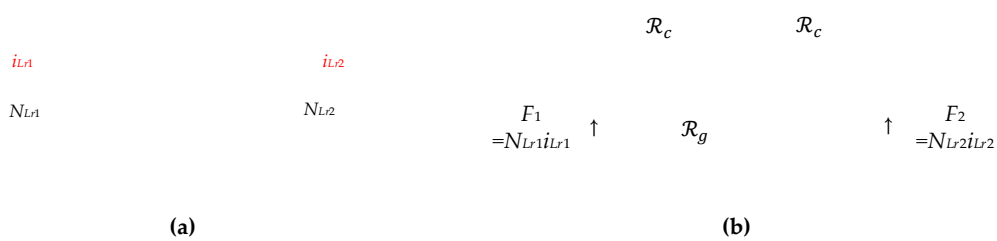


Figure 12. The proposed integrated magnetics (IM)-coupled inductor: (**a**) Structure of the proposed integrated magnetics (IM) for the CM-coupled inductor including resonant inductors; (**b**) reluctance model.

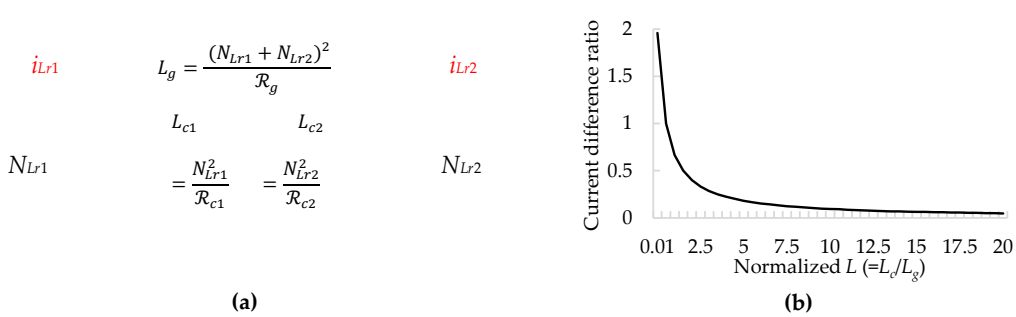


Figure 13. The proposed integrated magnetics (IM)-coupled inductor: (**a**) Inductance model; and (**b**) current balancing ratio by the normalized L.

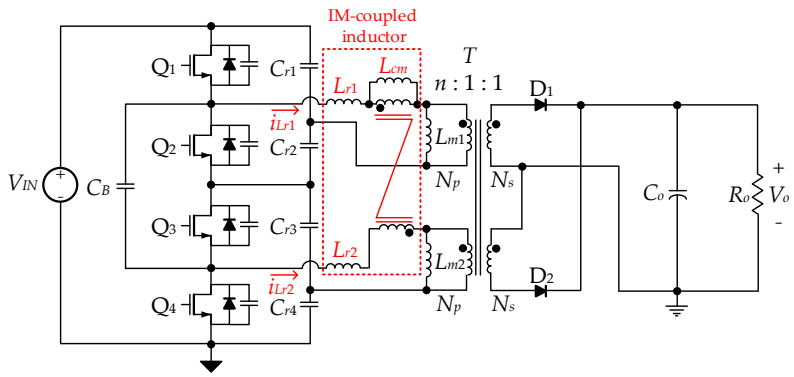


Figure 14. The proposed TL LLC resonant converter with the IM-coupled inductor.

The equivalent inductance model of the proposed IM-coupled inductor can be expressed as the equivalent two resonant inductors, L_{r1} and L_{r2}, and CM-coupled inductor. Consequently, the inductance of each inductor can be derived as follows:

$$L_{cm} = \frac{L_c(L_c + L_g)}{2L_c + L_g} = \frac{n^2\mu_0 A_c(\frac{A_c\,\ell_g}{\ell_c} + 4A_g)}{2\,A_c\ell_g + 4A_g\ell_c} \left(\because L_c = L_{c1} = L_{c2},\ \ell_g \gg \frac{\ell}{\mu_r},\ \ell_c \gg \frac{\ell}{\mu_r}\right) \tag{30}$$

$$L_r = L_{r1} = L_{r2} = \frac{L_c L_g}{2L_c + L_g} = \frac{2n^2\mu_0 A_c A_g}{2A_g\ell_c + A_c\ell_g}, \tag{31}$$

where A_c is the cross section area of the core outer legs, A_g is the cross section area of the core center leg, ℓ_c is the air gap of the core outer legs, and ℓ_g is the air gap of the core center leg.

Assuming that the air gaps of the outer legs are 0, as the value of inductors L_{c1} and L_{c2} are very large, the current of each resonant is almost same. However, small air gaps is required to prevent the core saturation and improve the core loss. Therefore, there is a current difference between each resonant inductor according to the ratio of L_c and L_g. Figure 13b shows the current difference ratio according to the normalized L (= L_c/L_g), where the current difference ratio is defined as $|i_{Lr1} - i_{Lr2}|/[(i_{Lr1} + i_{Lr2})/2]$. As shown in Figure 13b, the larger normalized L produces a smaller current difference. In summary, the resonant inductors L_{r1} and L_{r2} are implemented as the leakage inductances of the proposed IM inductor, which can be adjusted mainly by the air gap of the core center leg. In addition, the CM-coupled inductor for current balancing is implemented as the magnetizing inductance of the proposed IM inductor, which is determined mainly by the reluctance of core outer legs.

3.3. Voltage Conversion Ratio

If the TL LLC resonant converter operates at the resonant frequency, the resonant current flow follows a nearly sinusoidal waveform pattern, which would validate the use of fundamental harmonic approximation to derive the DC characteristic of the LLC resonant converter. The simplified equivalent circuit, which includes a single resonant tank to easily obtain the voltage conversion ratio, is derived as shown in Figure 15.

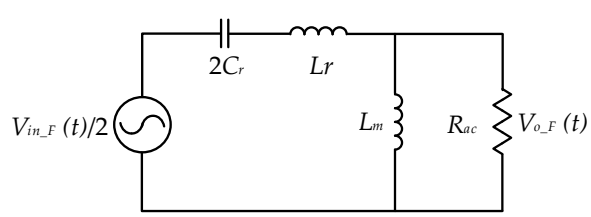


Figure 15. The simplified equivalent circuit of the TL LLC resonant converter.

To obtain mathematical expressions, the total load resistance, R_{ac}, and the fundamental input and output voltage of the resonant tank can be expressed as follows:

$$V_{in\_F}(\mathrm{t}) = \frac{V_{IN}}{\pi}\sin(\omega_r \mathrm{t}) \tag{32}$$

$$V_{o\_F}(\mathrm{t}) = n\frac{4V_O}{\pi}\sin(\omega_r \mathrm{t}) \tag{33}$$

$$R_{ac} = \frac{8n^2}{\pi^2}R_{eq}. \tag{34}$$

Meanwhile, the voltage conversion ratio of the proposed converter can be expressed as follows:

$$M = \frac{V_{o\_F}(\mathrm{t})}{V_{in\_F}(\mathrm{t})} = \frac{1}{4n\sqrt{\{1+1/L_n(1-1/F^2)\}^2+\{1/Q_e(F-1/F)\}^2}}, \tag{35}$$

where

$f_r = 1/(2\pi\sqrt{2C_rL_r})$,
$\omega_r = 2\pi f_r$,
$Z_o = \sqrt{L_r/(2C_r)}$,
$L_n = L_m/L_r$,
$F = f_{sw}/f_r$,
$R_{eq} = V_O/I_O$
$Q_e = R_{ac}/\sqrt{L_r/(2C_r)}$.

3.4. ZVS Condition

To ascertain that the ZVS operates in a steady state, the stored energy of the magnetizing inductors L_{m1} and L_{m2} should be sufficiently large to charge and discharge the parasitic capacitors of switches during Modes 3 and 6. In the TL LLC resonant converter, because the voltage stress of switches is half the input voltage, the ZVS condition can be expressed as follows:

$$\frac{L_m i_{Lm}^2(t_1)}{2} f_r t_{dead} \geq \frac{2C_{ds}(0.5V_{IN})^2}{2}. \tag{36}$$

3.5. Maximum Gain Analysis

With the TL LLC resonant converter operating at the resonant frequency, the magnetizing current during the dead time i_{Lm} and the limit of the magnetizing inductance can be expressed as follows:

$$i_{Lm}(t_1) = \frac{0.5(0.5V_{IN})}{2L_m f_r} \tag{37}$$

$$L_{m1} = L_{m2} \leq \frac{t_{dead}}{16C_{ds}f_r} = \frac{\pi\sqrt{2L_rC_r}t_{dead}}{16C_{ds}}. \tag{38}$$

Accordingly, when the TL LLC resonant converter is utilized behind the power factor correction (PFC) converter, the resonant tank is designed to operate at the resonant frequency for load regulation under a nominal operation. Nonetheless, the link voltage of PFC converter is lower during the hold-up time, but the TL LLC resonant converter requires a higher voltage gain. Thus, the resonant tank is designed to obtain an output voltage under the minimum link voltage, V_{link_min}, and frequency ratio, F_{min}. From Equation (35), the resonant tank can be expressed as follows:

$$L_m = \frac{4n^2R_OL_n \parallel F_{min}(F_{min}^2-1) \parallel}{\pi^3 f_r}\sqrt{\left\|(\frac{V_{link\_min}}{4nV_O})^2 - [1+\frac{1}{L_n}\left(1-\frac{1}{F_{min}^2}\right)]^2\right\|} \tag{39}$$

$$C_r = \frac{1}{L_r(2\pi f_r)^2} \tag{40}$$

$$L_r = \frac{L_m}{L_n} \tag{41}$$

where, $F_{min} = f_{sw\_min}/f_r$.

Furthermore, for assumed values of parameters F_{min}, and L_n, the resonant tank of L_m, L_r, and C_r is determined from Equations (39)–(41). For example, if P_o = 350 W, n = 5, V_{link_min} = 320 V, L_n = 7, and F_{min} = 0.7, the output voltage can be obtained under the minimum link voltage according to the switching and resonant frequency from Figure 16.

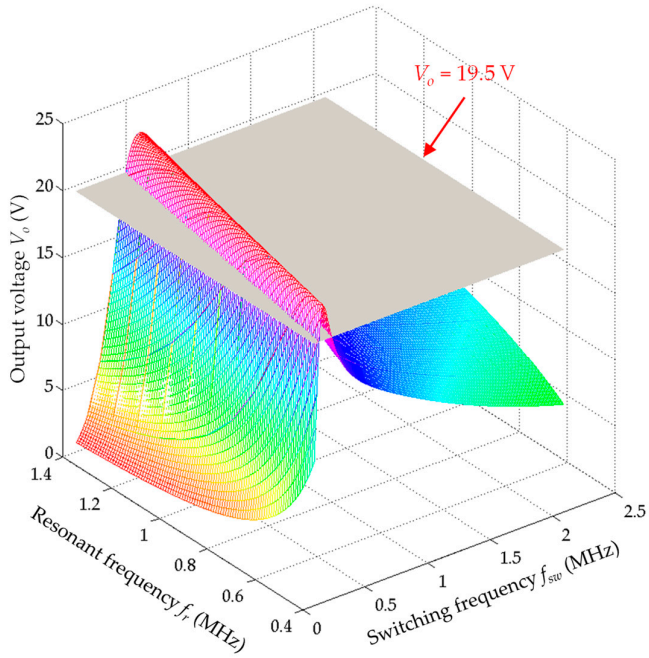


Figure 16. Output voltage gain graph at the minimum link voltage.

3.6. Comparison of Major Components

3.6.1. Stress Comparison

Table 1 provides a list of equations for the maximum voltage of a Si-FET and a resonant capacitor between the TL LLC resonant converter and a HB LLC resonant converter. Here, although the TL LLC resonant converter has two additional switches, compared with the HB LLC resonant converter for the same resonant tank condition, the voltage across the main switches is half that of the HB LLC resonant converter.

Table 1. Stress comparison for the two converters.

Components	Symbols	Equations	
		TL LLC resonant converter	**HB LLC resonant converter**
Si-FET	V_{Q_peak}	$\frac{V_{IN}}{2}$	V_{IN}
Resonant capacitor	V_{Cr_peak}	$\frac{V_{IN}}{2} - nV_O + \frac{V_O}{8\sqrt{2}nC_rR_O}\sqrt{T_r^2 + \frac{n^4R_O^2}{4\pi^2L_n^2L_r^2}}$	$V_{IN} - nV_O + \frac{V_O}{4nC_rR_O}\sqrt{T_r^2 + \frac{n^4R_O^2}{4\pi^2L_n^2L_r^2}}$

3.6.2. Comparison of Switch Loss

To elucidate the distinction between the TL LLC resonant converter with Si-FETs and the HB LLC resonant converter with GaN-FETs, their switch losses are compared under the same resonant tank conditions and specifications of main parameters, as shown in Table 2. When the LLC resonant converter operates at the resonant frequency with enough dead time, the main switches can operate with ZVS. Thus, turned-on and output capacitor losses are not considered.

Consequently, the loss sources of FETs deal with the conduction, turned-off, dead time, and gate driver losses. From Table 3, the Si-FETs, with lower rated voltage than the GaN-FETs, have similar drain–source resistance, fall time, and input capacitance as the GaN-FETs. This demonstrates that the proposed converter is applicable to high-performance switches, which has a lower rated voltage compared with switches for the HB LLC resonant converter.

Table 2. Specifications of the main parameters.

Parameters	Value		Unit
	TL LLC resonant converter	HB LLC resonant converter	
Input voltage V_{IN}	390		V_{DC}
Output voltage V_O	19.5		V_{DC}
Output power P_O	350		W
Gate-to-source voltage V_{drv}	15		V_{DC}
SR Gate-to-source voltage V_{SR_drv}	10		V_{DC}
Dead time t_{dead}	100		ns
Resonant capacitances C_r	5.5	1.375	nF
Resonant inductance L_r	2.6	10.4	uH
Magnetizing inductance L_m	14.5	58	uH
Turn ratio n	5:5:1:1	10:1	
Switching frequency f_{sw}	1		MHz

Table 3. Specifications of Si-FETs and GaN-FETs.

Parameters	Value		Unit
	BSC16DN25NS3 (Si-FET)	TPH3206PD (GaN-FET)	
Drain–source breakdown voltage	250	600	V
Continuous drain current	10.9	17	A
Drain–source on-state resistance	0.16	0.18	ohm
Input capacitance	920	760	pF
Output capacitance	59	44	pF
Rise time	4	4.5	ns
Fall time	4	4	ns
Source–drain diode forward voltage	0.9	2.6	V

Figure 17 displays the switch losses in both converters under the assumption that the resonant converter operates at the resonant frequency. Figure 17a, b illustrates the specified switch losses of the TL LLC resonant converter and two switches of the HB LLC resonant converter based on Table 3, at the point of switching frequency f_{sw} = 1 MHz. Apparently, as the TL LLC resonant converter has four switches in series, the conduction loss is approximately twice that of the HB LLC resonant converter. Overall, a slight difference of 0.7 W is obtained for the total switch losses of each converter.

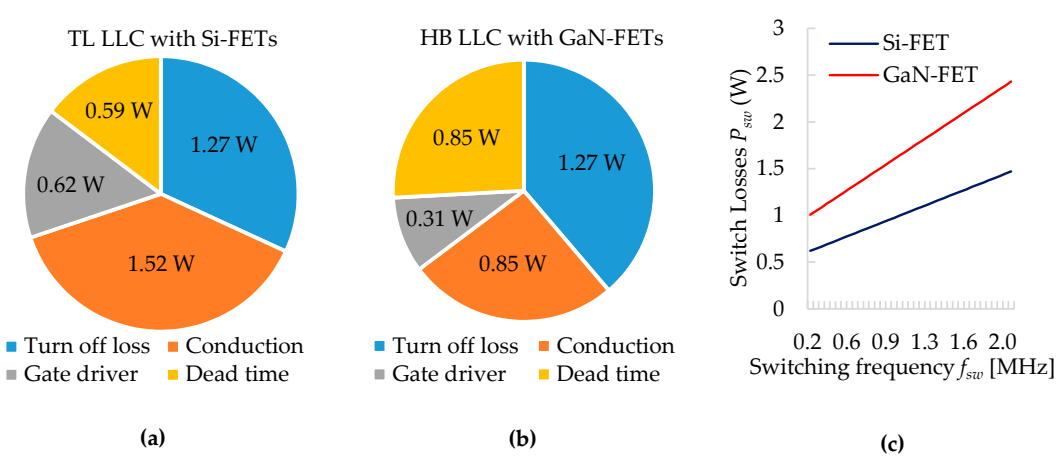


Figure 17. Comparison of switch losses for the two converters under the same resonant tank conditions: (**a**) Total switch loss of the TL LLC resonant converter; (**b**) total switch loss of the HB LLC resonant converter; and (**c**) single-switch loss comparison according to the switching frequency.

Figure 17c displays the single-switch losses of the GaN-FET and Si-FET. Although both increase with a higher switching frequency, the single-switch losses of the TL LLC are smaller than those of the HB LLC, mainly due to its reduced turned-off loss and the lower voltage across the switches. Moreover, the proposed TL LLC resonant converter can use the high-performance Si-FETs, which have lower drain–source resistance and source–drain diode forward voltage, owing to the low rated voltage. Therefore, each switch of the TL LLC resonant converter exhibits lower conduction, turned-off, and dead time losses, indicating its ability to reduce the heat sink size of the main switches, as switch losses can be dissipated.

3.7. Optimal Design through the Loss Analysis

A converter's efficiency is relative based on various components, including the value of resonant tank, switching frequency, and so on. Based on the loss analysis, the highest efficiency for the TL LLC resonant converter can be obtained via optimization of the design components. General loss sources include Si-FET conduction loss and switching loss, copper and core loss of magnetics, and conduction loss of synchronous (SR)-FETs. The parameters used are based on the assumption that the converter operates at a switching frequency in a steady state.

3.7.1. Loss Analysis for Switching Components

The switching components of the TL LLC resonant converter are four Si-FETs in the primary side and two SR-FETs in the secondary side as the output rectifier. For the comparison of power losses, equations for the main parameters can be consulted as provided in Table 4.

Most of the Si-FET loss components for the TL resonant converter are similar to those of a conventional HB LLC resonant converter. Switches for the TL LLC and HB LLC resonant converters operate with ZVS as mentioned in the switch loss comparison; as such, the loss sources of Si-FETs deal with the conduction, turned-off, dead time, and gate driver losses. The conduction loss of Si-FETs can be expressed as follows:

$$P_{conduction} = 4R_{ds(on)}I_{Q\_rms}^2, \tag{42}$$

where $R_{ds(on)}$ is the drain–source on-state resistance, whereas I_{Q_rms} is the drain–source root mean square (RMS) current of the switch.

The drain–source voltage of the converter and the maximum current of the magnetizing inductance at the turned-off point affect the transition loss of Si-FETs. Moreover, because the drain–source voltage of the converter is half the input voltage, the turn-off loss of each switch is equally reduced. Therefore, the TL LLC resonant converter can reduce the heat sink size. Relatively, the turned-off loss of Si-FETs can be expressed as follows:

$$P_{turn\_off} = 2V_{Q\_peak}I_{Lm\_peak}f_{sw}t_f, \tag{43}$$

where V_{Q_peak} is the drain–source voltage, I_{Lm_peak} is the maximum current of the magnetizing inductor, f_{sw} is the switching frequency, and t_f is the fall time. The gate driver loss of Si-FETs can be expressed as follows:

$$P_{gate\_driver} = 4C_{iss}V_{drv}^2f_{sw}, \tag{44}$$

where C_{iss} is the parasitic input capacitance of SR-FETs, and V_{drv} is the gate driver supply voltage. The dead time loss of Si-FETs can be expressed as follows:

$$P_{dead} = 8I_{Lm\_peak}V_{SD}t_{dead}f_{sw}, \tag{45}$$

where V_{SD} is the source–drain diode forward voltage drop, and t_{dead} is the dead time of Si-FETs.

The SR-FETs operate with ZVS and ZCS due to the 0 current at the turned-on and turned-off point. Thus, the loss sources of SR-FETs are the conduction and gate driver losses. The conduction loss of SR-FETs can be expressed as follows:

$$P_{SR\_conduction} = 2R_{SR\_ds(on)}I_{do\_rms}^2, \tag{46}$$

where $R_{SR\_ds(on)}$ is the drain–source on-state resistance of SR-FETs, and I_{do_rms} is the drain–source RMS current of SR-FET.

The gate driver loss of SR-FETs can be expressed as follows:

$$P_{SR\_gate\_driver} = 2C_{SR\_iss}V_{SR\_drv}^2 f_{sw}, \tag{47}$$

where C_{iss} is the parasitic input capacitance of SR-FETs, and V_{drv} is the supply voltage of the gate driver.

Table 4. Equations for calculation of switching loss.

Components	Symbols	Equations
Si-FET	I_{Q_rms}	$\frac{V_O}{16nR_O}\sqrt{4\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$
	I_{Q_peak}	$\frac{V_O}{8nR_O}\sqrt{4\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$
Transformer	I_{Lm_peak}	$\frac{nV_OT_r}{8L_m}$
SR-FET	I_{do_rms}	$\frac{V_O}{8\sqrt{3}R_O}\sqrt{12\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$

3.7.2. Loss Analysis for Magnetics

The magnetics of the TL LLC resonant converter are two resonant inductors and two transformers in the primary side. For comparison of the magnetics losses, the RMS and peak current equations for the magnetics of the TL LLC resonant converter are shown in Table 5.

Table 5. Equations for the calculation of magnetic loss.

Components	Symbols	Equations
Resonant inductor	I_{Lr_rms}	$\frac{V_O}{8\sqrt{2}nR_O}\sqrt{4\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$
	I_{Lr_peak}	$\frac{V_O}{8nR_O}\sqrt{4\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$
Transformer	I_{pri_rms}	$\frac{V_O}{8\sqrt{2}nR_O}\sqrt{4\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$
	I_{sec_rms}	$\frac{V_O}{4\sqrt{6}R_O}\sqrt{12\pi^2 + \frac{n^4R_O^2T_r^2}{L_n^2L_r^2}}$
	I_{Lm_peak}	$\frac{nV_OT_r}{8L_m}$

A common technique for calculating loss is employed in the magnetic analysis. The waveforms of the TL LLC resonant converter are first assumed to be sinusoidal. Cores used for magnetics of the TL LLC resonant converter are planar cores aimed at minimizing the converter height. The core losses of the inductor and the transformer are determined by the modified Steinmetz equation [20–21]:

$$P_{T\_core} = 2kB_{T\_pk}^{\alpha}f_{sw}^{\beta}V_{e\_T}, \tag{48}$$

where k, α, and β are the core loss coefficients, dependent on the core material; B_{T_pk} is the peak flux density of the transformer; and V_{e_T} is the volume of the transformer.

The total wire loss of the transformer is expressed as follows:

$$P_{T\_wire} = 2(P_{pri} + P_{sec}) = 2(R_{pri\_AC}I_{pri\_rms}^2 + R_{\mathrm{sec\_AC}}I_{sec\_rms}^2), \tag{49}$$

where R_{pri} is the primary winding resistance, I_{pri_rms} is the rms current of the primary wire, R_{sec} is the secondary winding resistance, and I_{sec_rms} is the RMS current of the secondary wire.

Inductor core loss is determined by using the modified Steinmetz equation:

$$P_{Lr\_core} = 2kB_{Lr\_pk}^{\alpha} f_{sw}^{\beta} V_{e\_Lr}, \tag{50}$$

where k, α, and β are the core loss coefficients, dependent on the core material; B_{Lr_pk} is the peak flux density; and V_{e_Lr} is the volume of the transformer.

Inductor wire loss is expressed as follows:

$$P_{Lr\_wire} = 2R_{Lr\_AC} I_{Lr\_rms}^2, \tag{51}$$

where R_{Lr} is the winding resistance of the resonant inductor and I_{Lr_rms} is the rms current of the resonant inductor.

3.7.3. Results of Loss Analysis

To achieve a highly efficient converter, the optimal design based on loss analysis is required to choose a switching frequency and a value of the resonant tank that minimizes power losses. In this respect, the power losses are relative to the switching frequency and L_n of the converter.

For the loss analysis, the following parameters are used and the proposed converter is designed to be operated at f_r, as the resonant frequency:

1. Input voltage: V_{IN} = 390 V
2. Output voltage: V_O = 19.5 V
3. Output power: P_O = 350 W

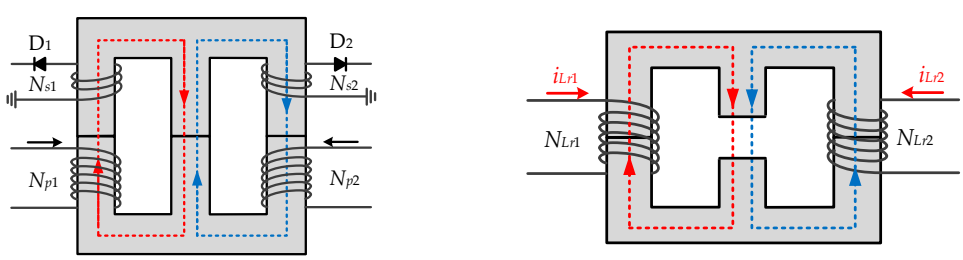
The TL LLC resonant converter operates at f_r as the switching frequency; thus, the transformer turn ratio can be obtained using the following equation, where the voltage conversion gain is equal to 1:

$$M_{f_r} = \frac{4nV_O}{V_{IN}} = 1. \tag{52}$$

Using Equation (52), the turn ratio is about 5.

Moreover, the proposed converter requires two inductors and two transformers. To reduce its size, a planar transformer and a resonant inductor with 12 layers are selected with the two oz. width for the pattern, relative to the core window area. Also, two resonant tanks, a transformer and an inductor, consist of a single core with winding of the pattern on the outer legs of the core, thereby increasing the power density, as shown in Figure 18.

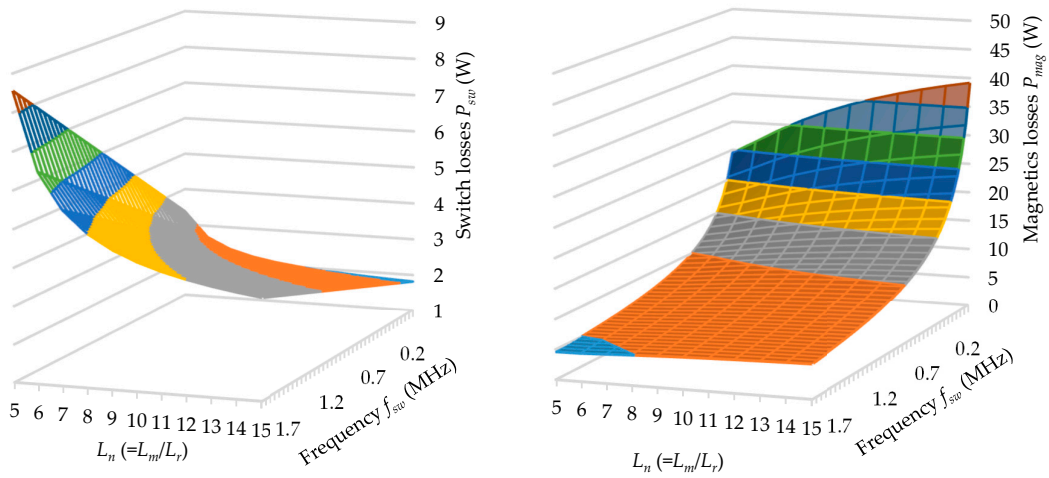
The transformer has five primary turns and one secondary turn, whereas by core saturation, the resonant inductor has five turns. Figure 19a shows the total switch losses, including those of Si-FETs and SR-FETs according to L_n (= L_m/L_n) and the switching frequency. Here, when L_n is higher than 7 with a high switching frequency, there is a slight difference in the switch losses. Figure 19b depicts the total magnetic component losses according to L_n and the switching frequency; there is also a slight difference in the switch losses when L_n is higher than 7 with a high switching frequency.



(a) **(b)**

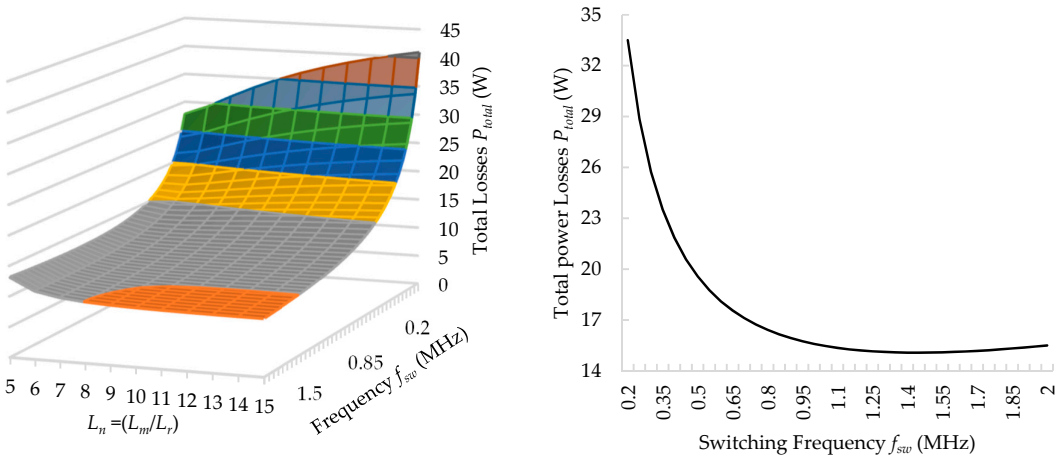
Figure 18. The winding method of magnetic components: (**a**) A planar transformer and (**b**) a planar inductor.

Figure 20 shows a comparison of the total losses based on Figure 19. A comparison of total loss by L_n and f_{sw} is shown in Figure 20a, mainly describing a slight difference in total losses when $f_{sw} > 1$ MHz and $L_n > 7$. Figure 20b described a detailed total loss comparison according to the switching frequency with $L_n = 7$ and $P_o = 350$ W. Note that when the switching frequency is higher than 1 MHz, the value of the total losses is almost the same value as at 16 W. Consequently, the switching frequency is set to 1 MHz, and L_n to 7.



(a) **(b)**

Figure 19. Comparison of main components relative to L_n (= L_m/L_r) and switching frequency: (**a**) Switch losses and (**b**) magnetic losses.

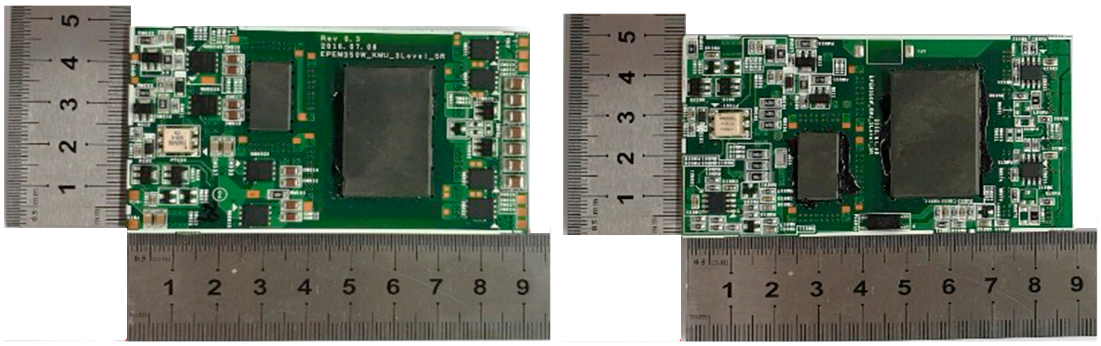


(a) **(b)**

Figure 20. Total losses comparison: (**a**) according to L_n and the switching frequency: and (**b**) according to $L_n = 7$ and the switching frequency.

4. Experimental Results

A 350 W prototype of the TL LLC resonant converter was created to verify its performance, operational principle, and advantages, as depicted in Figure 21. Table 3 and 6 provide the main parameters and components of the prototype.



(a) **(b)**

Figure 21. The TL LLC resonant converter: (**a**) Top side and (**b**) bottom side.

Table 6. Specification of the main components.

Components	Name
Si-FETs Q_1, Q_2, Q_3, Q_4	BSC16DN25NS3
Output rectifier D_1, D_2	BSC061N08NS5
Controller	SEM3150
Thickness of pattern	2oz (= 0.7 mm)
Planar resonant inductor core	EE 0909 (ML-91S)
Relative permeability	900
Turns	5
Air gap of center leg	0.31 mm
Air gap of outer leg	0.03 mm
Planar transformer core	EE 2012 (ML-91S)
Relative permeability	900
Primary turns	5
Secondary turns	1
Air gap of center leg	0.55 mm

4.1. Practical Voltage Balancing under Soft Start-Up Conditions

Under soft start-up conditions, the voltage of all capacitors in the TL LLC resonant converter was discharged to 0. The voltage of the balancing capacitor V_B was also 0 at the point of start-up, as shown in Figure 22a. After Q_1 and Q_3 were turned on during Mode 1 or Q_2 and Q_4 were turned on during Mode 4, the input voltage was applied to the balancing capacitor and the resonant capacitor, C_{r3} and C_{r4} by the Kirchhoff voltage law. At this moment, the sums of the resonant capacitor voltages, $V_{cr1} + V_{Cr2}$ and $V_{cr3} + V_{cr4}$, could not be guaranteed to be half of the input voltage. Figure 23a shows the experimental waveforms at V_{IN} = 200 V, which are due to the voltage imbalance. From Figure 22a, the switches could be destroyed at V_{IN} = 390 V due to the voltage imbalance.

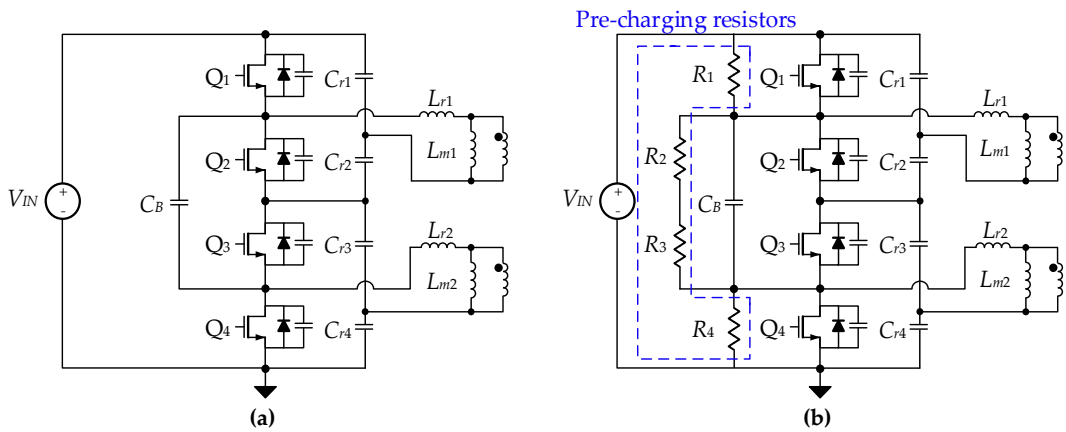


Figure 22. Primary side of the proposed TL LLC resonant converter: (**a**) Conventional circuit without balancing resistors and (**b**) improved circuit with balancing resistors.

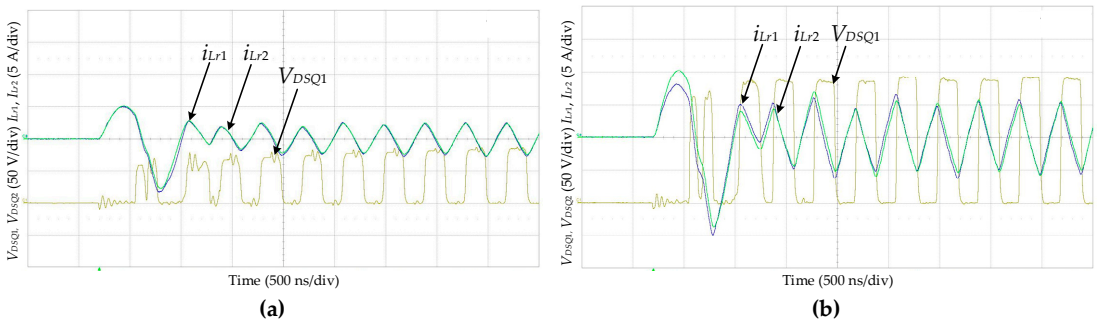


Figure 23. Experimental waveforms at soft start-up: (**a**) without balancing resistors under V_{IN} = 200 V; and (**b**) with balancing resistors under V_{IN} = 390 V.

These problems could be resolved by configuring the current flow path with pre-charging resistors to charge the balancing capacitor before soft start-up. However, as the location of resistors enables the current and included input voltage to assume a steady state, as depicted in Figure 22b, the power consumption can be as large as the standby power. However, if the value of the resistors was too high to reduce the standby power, the pre-charging time would be longer. As such, the resistor value has to be properly selected. With the resistors of 1 MOhm, the voltage across switches can be set to half the input voltage at the point of soft start-up, as shown in Figure 23b.

4.2. Waveforms

The experimental balancing waveforms of each resonant component with P_O = 350 W and normalized L = 30 in the steady state are shown in Figure 24. In Figure 24a, the voltage of the balancing capacitor V_{CB} and the sum of the resonant capacitor voltage $V_{Cr1} + V_{Cr2}$ and $V_{Cr3} + V_{Cr4}$ maintained the voltage balance. Moreover, the resonant currents i_{Lr1} and i_{Lr2} exhibited the same waveforms and maintained the current balance for each resonant tank, as depicted in Figure 24b. Figure 24 shows the main experimental waveforms with output power from P_O = 0 W to 350 W, with drain-to-source voltage V_{Q_ds}, gate-to-source voltage V_{Q_gs}, and resonant current i_{Lr} in Figure 25a–d. All switches were turned on with ZVS under every load condition, and the voltage stress was set to half the input voltage.

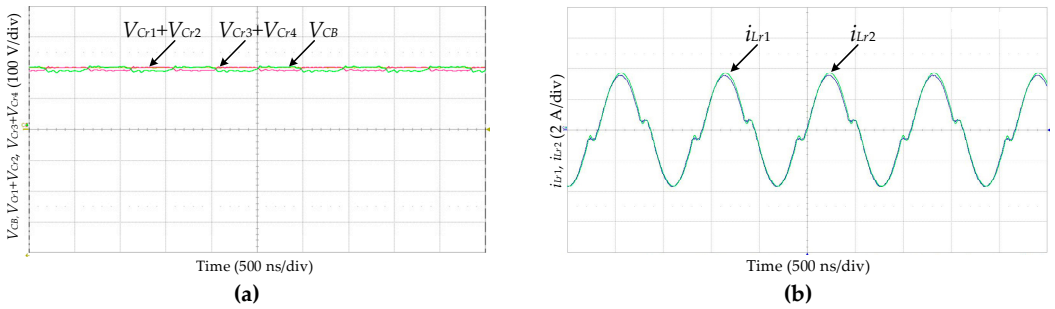


Figure 24. Experimental balancing waveforms of the TL LLC resonant converter with P_O = 350 W: (**a**) Voltage balancing of capacitors; and (**b**) current balancing of IM-coupled inductors.

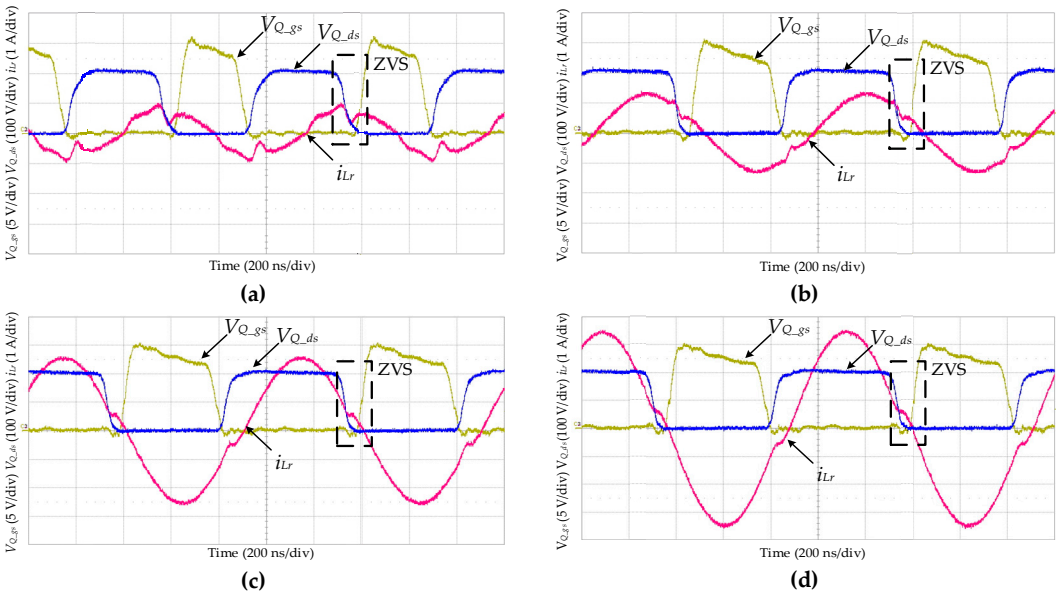
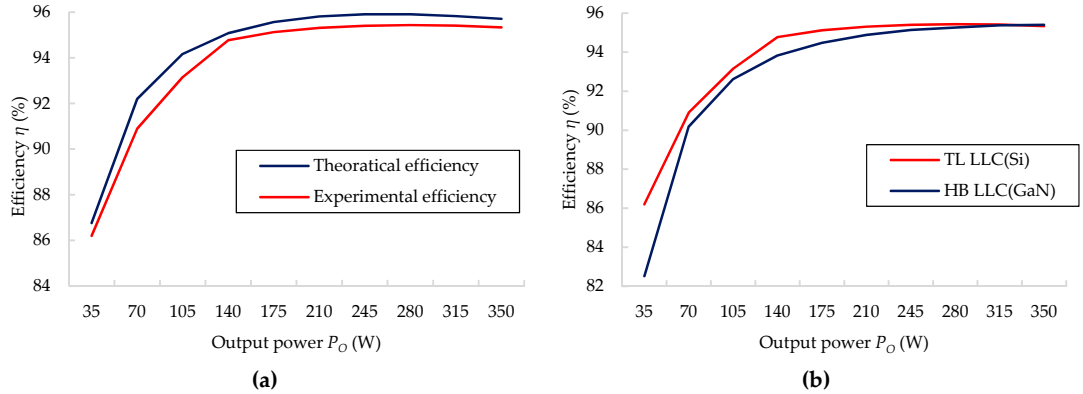


Figure 25. Experimental waveforms of the TL LLC resonant converter: (**a**) P_o = 0 W, f_{sw} = 1.3 MHz; (**b**) P_o = 100 W, f_{sw} = 1.07 MHz; (**c**) P_o = 250 W, f_{sw} = 1.0 MHz; and (**d**) P_o = 350 W, f_{sw} = 0.97 MHz.

4.3. Efficiency

Figure 26a shows efficiency comparison curves between the theoretical and experimental results measured by YOKOGAWA : Tokyo, Japan, WT1804E under different load conditions. The efficiency curves were the same, with slight differences. The maximum efficiency was 95.43% at an 80% load condition. Figure 26b is an efficiency comparison between TL LLC with Si-FETs and HB LLC with GaN-FETs. From Figure 26b, we see that, while the proposed TL LLC resonant converter has the higher efficiency under the light load condition, the difference in efficiency is further reduced as the output power increases. Because the turn-off loss forms a large portion of the total loss at a light load, the proposed TL LLC resonant converter has less total loss due to low voltage across the switches. However, as the conduction loss gets larger as the output power increases, the difference in efficiency is further reduced because the drain–source on-state resistance of GaN-FETs is smaller than that of the proposed converter. As a result of the efficiency comparison, although the proposed TL LLC resonant converter uses relatively low-cost Si-FET switches, it shows superior performance to the conventional HB LLC resonant converter using the high-performance and high-cost GaN-FETs.



(a) **(b)**

Figure 26. Efficiency comparisons: (**a**) between the experimental and theoretical results; and (**b**) between the TL LLC and HB LLC results.

5. Conclusions

A proposed Si-FET-based high switching frequency three-level LLC resonant converter was presented herein, with a discussion of its operational principle, loss analysis, and optimal design consideration based on loss analysis to those of another converter. The results demonstrated the ability of the proposed converter to achieve voltage balancing without additional circuits or control strategy and to ensure that the voltage across the main switches is set to half of the input voltage. Moreover, it was shown that the voltage stress of the main switches could be further reduced via the application of a modular system. Based on analysis and design considerations, the converter's operating frequency was over 1 MHz, with a high efficiency of 95.33% under a full load (350 W).

Author Contributions: Conceptualization, J.Y. and S.H.; Methodology, J.Y.; Validation, J.Y.; Formal analysis, J.Y. and S.H.; Resources, S.H.; Writing—original draft preparation, J.Y.; Writing—Review, J.Y. and S.H.; Supervision, S.H.;

Funding: This work supported by the Ministry of Trade, Industry and Energy (MOTIE) (Grant # 2018201010650A), and Korea Institute of Energy Technology Evaluation and Planning (KETEP) (Grant # 2018201010650A).

Conflicts of Interest: The authors declare no conflict of interest.

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