An Approach to Natural Sampling Using a Digital Sampling Technique for SPWM Multilevel Inverter Modulation

Mauricio Muñoz-Ramírez [1], Hugo Valderrama-Blavi [1,*] , Marco Rivera [2] and Carlos Restrepo [2]

[1] Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Escola Tècnica Superior d'Enginyeria, Universitat Rovira i Virgili, 43007 Tarragona, Spain

[2] Department of Electromechanics and Energy Conversion, Universidad de Talca, 3340000 Curicó, Chile

* Correspondence: hugo.valderrama@urv.cat; Tel.: +34-977-558-523

Abstract: This paper introduces an approach that applies a digital sampling technique for a sinusoidal pulse width modulation (SPWM) multilevel inverter modulation that reduces the total harmonic contents in the output voltage compared to that of classical regular sampling techniques. This new modulation emulates with a high degree of fidelity a natural sampling pulse width modulation (PWM). The theoretical analysis of this new digital technique compared with natural sampling has been validated by simulations and through experiments with a built prototype that performed five–level inverter modulations with vertically displaced carriers in phase disposition. Both simulation and experimental results generate a SPWM output voltage with higher fidelity than classic regular sampling techniques, allowing a reduction of the filtering demands on the inverter output, which in turn can decrease the converter size and its manufacturing costs. As the presented technique is digital, the resulting modulation is more robust against switching noise, jitter, and other system perturbations and the modulation parameters can be changed easily, even in an automated way. For this reason, the modulation introduced here can be a useful tool to perform spectral analysis for different multilevel modulations and systems.

Keywords: carrier shape ratio; level distribution; multilevel inverter; phase disposition; sampling methods

1. Introduction

A multilevel inverter (MI) is a power converter with switching components that enables diverse input voltages to be combined to generate a sinusoidal output waveform. The MIs that are most frequently cited in the literature are characterized by lower harmonic distortion and conduction losses than classic two-level inverters supplied at the same input voltage. Furthermore, the harmonic reduction is aligned with switching frequency reduction [1–3].

Several examples found in the literature demonstrate that the study about new topologies, new modulation and control techniques, as well applications are the focus of research nowadays [4,5]. Among recent multilevel topologies, a Hybrid Single T-Type Double H-Bridge Multilevel Inverter (STDH-MLI) has been proposed and produces 15 levels at the output using three DC voltage sources [6]. A 13-level topology is presented in Reference [1] with a reduced number of switches and DC voltage sources providing flexibility for higher voltage and power requirement based on the way the DC sources are connected. Hybrid multilevel configurations such as hybrid clamped, cascaded, flying capacitor based, and others have been also discussed and studied in Reference [4]. All these new multilevel power converter configurations have common features such as fewer switches devices, low total harmonic distortion (THD), easy circuit expansion, and better electromagnetic compatibility, among others [7–9]. The asymmetrical full bridge multilevel inverter (AFBMI) [10] is one type of diode-clamp MI, which is the converter under study in this work (see Figure 1). This topology is

able to perform any multilevel modulation from 2 to 5 levels. When operating with 4 and 5 levels, the AFBMI converter uses less active or controllable switches than any other five-level converter and, therefore, is the most suitable to reduce conduction and switching losses. In addition, this topology can work with unbalanced power supplies, yielding a nonuniform level distribution [11].
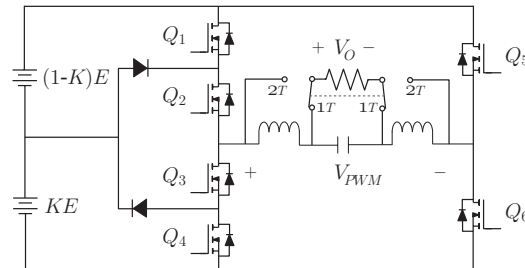

Figure 1. Asymmetric full-bridge multilevel inverter (AFBMI).

Regarding modulation and control techniques for multilevel converters, one-cycle-control method [5], PWM strategies [12], selected harmonic elimination [13], predictive control [14], and others [15] have become the most studied strategies in the last years for several applications such as photovoltaic applications [16], wind energy conversion systems [17], active power filters [18], motor drives [19], and others [20].

This work will discuss the application of the sinusoidal pulse width modulation (SPWM) technique with AFBMI. The main contribution of this article is the discussion of several alternatives for calculating the switching instants, the analysis and a theoretical and experimental comparison of different sampling methods and the proposal of a novel sampling method [21–24].

2. Sampling Methods for Multilevel Converters

Vertically shifted carrier or multicarrier schemes have $N - 1$ carriers signals to generate N-level inverter output voltages. Also, $N - 1$ switching zones occur during one fundamental cycle. Carriers are organized as phase disposition (PD), phase opposition disposition (POD), alternative phase opposition disposition (APOD), and phase shift (PS) depending on their phases [25]. PD has been reported as the best method in most cases when compared against other methods, e.g., POD and APOD [26–28], mainly in diode clamped inverters. Nevertheless, an analysis of simulations and expressions should be complemented by an analysis of experimental data that considers the vast range of conditions in modulation techniques. Some conditions such as sampling methods [29,30], the modulation frequency ratio F_C/F_O (Switching frequency/Fundamental frequency), and the nonlinear characteristics of switching devices influence the resultant waveform and its spectrum. Here, we discuss the sampling methods for both the modulator signal and the carriers.

A SPWM modulating circuit can be analog or digital. In an analogical modulator, the modulating signal M_a and the carriers are continuously generated and the switching moments are computed instantaneously for each active carrier within the interval $[t_0, t_0 + T_C]$. The analogical method is known as natural sampling modulation. In a simple way, the carriers can be displaced by offset adjustments and their amplitudes modified in order to apply feed-forward compensation when the DC input supplies change in time. However, synchronization between the $N - 1$ carriers is not easily achieved because the switching frequency F_C is not easy to adjust and is also susceptible to the tolerances of the oscillator. Furthermore, the carriers are susceptible to jitters. Sawtooth-shaped carriers have been used; however, symmetrical triangular carriers (standard carriers, Figure 2) are generally preferred because the ratio r_i between the falling slope and the rising slope is equally distributed in time. This ratio r_i of the carrier is also susceptible to tolerances, and it cannot be easily modified to different values. See Figure 3 for representations of nonstandard carriers.
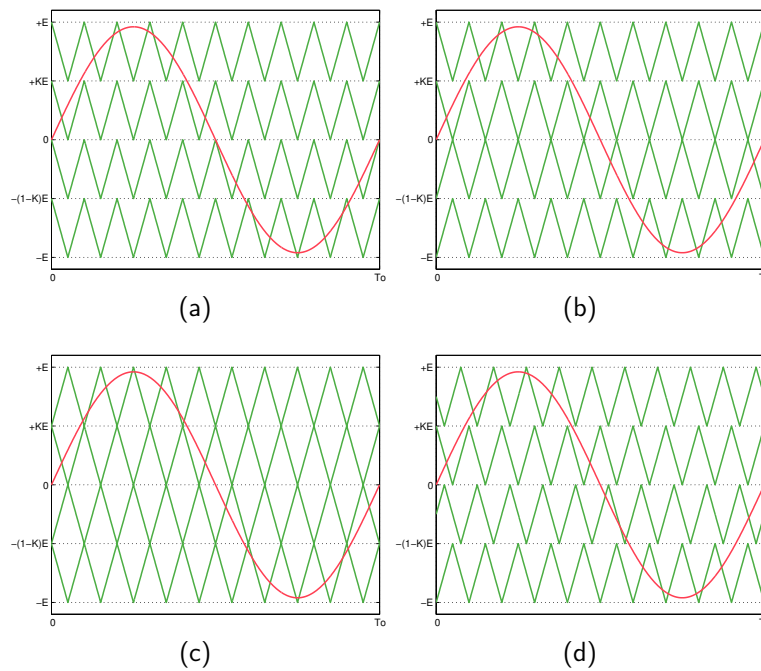
Figure 2. Types of disposition for vertical multicarrier sinusoidal pulse width modulation (SPWM): (**a**) phase disposition (PD), (**b**) phase opposition disposition (POD), (**c**) alternative phase opposition disposition (APOD), and (**d**) phase shift (PS). In the vertical axis, there are $N - 1$ carriers for N levels. $M_f = 10$ is selected for the horizontal axis for the sake of easiness. Note that there are M_f switching intervals. Only one of the carriers is active for comparison with the modulating signal M_a.
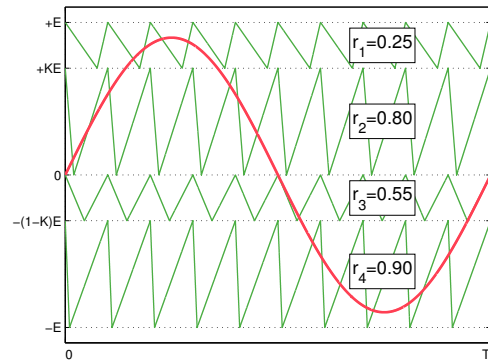

Figure 3. Five-level PD-SPWM with modified carrier slopes: Note that the carrier ratios do not represent standard carriers. Each carrier controls one switching zone as follows: $r_1[+E, +KE]$, $r_2[+KE, 0]$, $r_3[0, -(1-K)E]$, and $r_4[-(1-K)E, -E]$.

In digital modulators, the carriers are produced by counters and comparators and switching moments are determined after comparing the regular sampled modulating signal. Among the diverse digital modulation techniques, both symmetrical regular sampling and asymmetrical regular sampling are well-known [31]. The first goal of a SPWM modulator is to create a waveform that contains the exact frequency component F_O and amplitude M_a. The second target is to reduce the harmonic components resulting from modulation. This harmonic content is not easy to verify when comparison has to be done with different criteria such as phase disposition, level distribution K, and modulation indexes M_a and M_f. However, in the time domain, the differences between the aforementioned criteria can be inspected by measuring the error in the switching instants X_D and X_U and eventually the pulse width $D = X_D - X_U$ (see the red projection of natural sampling in Figure 4).
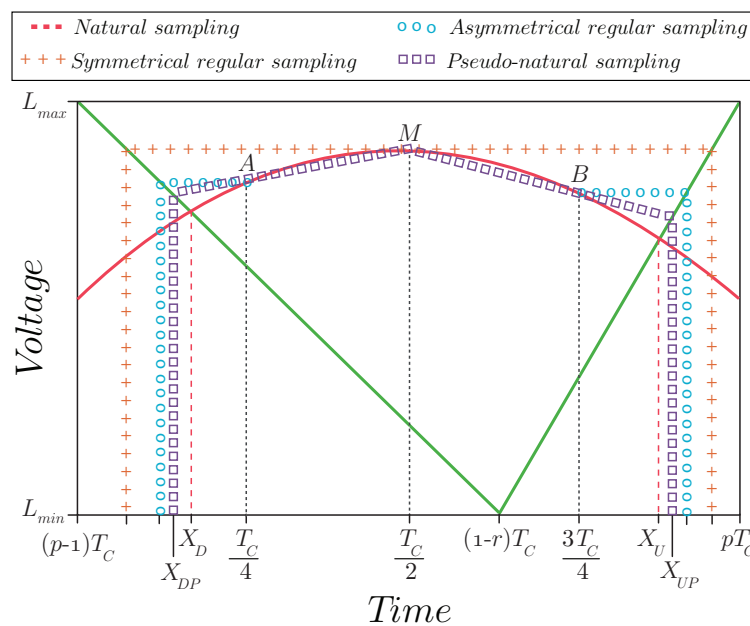
Figure 4. Sampling methods for a given switching interval: Comparison of natural, symmetrical regular, asymmetrical regular, and pseudo-natural sampling methods for SPWM.

Since pulse width modulation is an approach to a continuous reference using discrete DC voltage supplies, the multilevel conversion can be examined by comparing the use of natural sampling, symmetrical regular sampling, and asymmetrical regular sampling. Natural sampling occurs when the modulator signal is continuously compared with the triangular carrier. Symmetrical regular sampling occurs when the reference is sampled by M in Figure 4 at the center of the carrier ($T_C/2$) and is held constant to be compared with the triangular carrier. Asymmetrical regular sampling handles the two samples A and B at time $T_C/4$ and time $3T_C/4$. The respective projections are seen in Figure 4. In these sampling methods, X_D and X_U are respectively the times of the rising and the falling slopes of the carrier. Although natural sampling implementation becomes more complicated as the levels of the inverter increase, this is the most suitable method for synthesizing a multilevel waveform with a high degree of fidelity. On the other hand, if one sample (symmetrical sampling) or two samples (asymmetrical sampling) of the reference signal are taken and a projection to the falling and rising slopes of the carrier is plotted, the switching moments can be easily computed with acceptable accuracy although the resultant harmonic contents is higher than in natural sampling.

3. Pseudo-Natural Modulation

3.1. Natural and Regular Sampling Methods for SPWM

The double Fourier series (DFS) expression is a helpful tool that can be used to validate harmonics calculations with a SPWM circuit based on the natural sampling method. Thus, the output waveform contains a spectrum that can be predetermined in advance by using a DFS expression. However, when obtaining the exact solution for switching moments, this analog modulator can encounter certain obstacles when it needs to modify the shape ratio of its carrier signals. Also, an analog modulation has disadvantages such as tolerance in passive elements and susceptibility to noise and temperature dependence. Additionally, there is no flexibility for configurations as there are for POD and APOD.

Because of its nature, a digital circuit is intended to implement regular sampling. SPWM is widely implemented digitally because this option offers low noise levels for carriers and modulator comparisons limited to the quantization error and has no temperature dependence. Also, fast configuration, in our particular case, enables the carrier slopes to be programmed. Furthermore, the digital modulator can be reconfigured to perform POD and APOD.

Digitally determined switching moments were previously implemented [29,30]. Basically, the method resampled the modulator signal using the resampling ratio $rsr = F_S/2F_C$, that is, when $rsr = 4$, four modulator samples were taken in one-carrier period T_C. Therefore, for symmetrical sampling, the resampling ratio is $rsr = 1$, whereas for asymmetrical sampling, it is $rsr = 2$. Such carriers were standard shaped. Another precedent was the approach reported in References [32] and [33] where the curve of the sinusoidal modulating signal was assumed to be one single secant line during the carrier period; for every carrier interval, there was an elementary cell that represented the states of the inverter and their respective switching moments. On the basis of this elementary cell, a harmonic predictive model was elaborated to study in advance different PWM strategies digitally implemented later with standard carriers. In this paper, we propose an alternative method for modeling and carrying out SPWM that is as accurate and as close as possible to natural sampling methods. This method is pseudo-natural sampling and enables the harmonic contents to be predicted by modeling and then experimentally implementing SPWM using either a simulation tool or a digital control board whilst also allowing the carriers slopes to be modified.

3.2. Definition of Pseudo-Natural Sampling SPWM

We discuss the concept of pseudo-natural sampling that can be seen in Figure 4 which compares the switching instant decisions of pseudo-natural sampling with those of the previously mentioned sampling methods. The pseudo-natural sampling method is carried out by using three samples (Figure 4): one sample at the carrier period T_C midpoint, namely sample M; one sample from the left side at the falling slope interval midpoint, namely sample A; and one sample from the right side at the rising slope interval midpoint, namely sample B. The secant segments AM and MB replace the modulating signal. The pair of segments AM and the falling slope are intersected to find X_{DP}. In the same way, the pair of segments MB and the rising slope are intersected to find X_{UP} [21].

Table 1 shows the comparison among switching instants and duty cycles with four sampling methods, including the introduced pseudo-natural method. The switching values are delimited in the first carrier period, that is, $0 \leq t \leq T_C < T_O$ for a switching ratio $M_f = 50$. Taking this example is very illustrative, since the first carrier period is in the boundary of zero-crossing and the sinusoidal reference presents a high derivative. Table 1 also demonstrated how the duty cycle D in a carrier period can have different widths and be modulated at different instants if the four sampling methods are compared among them. The differences rely on the fact that the input signal is not constant during a carrier period, especially on the boundary of zero-crossing where the high derivative property implies that any digital sampling method should synthesize the incoming modulating signal as natural sampling does. Pseudo-natural sampling method is the option that best fits replacing natural sampling by means of a digital modulator.

Tables 2–4 compare the switching moments and duty cycles of the referred four sampling methods, including our novel pseudo-natural method. The switching values are delimited in the first carrier period, that is, $0 \leq t \leq T_C < T_O$ for a switching ratio $M_f = 50$. This example is very illustrative because the first carrier period is on the zero-crossing boundary and the sinusoidal reference presents a high derivative. Figure 5 shows the switching interval and switching instants obtained by four sampling techniques that correspond with the square shown in Table 2 for case (a). The duty cycles of three techniques are compared with the resultant duty cycle of natural sampling in Tables 2–4. Such comparison results in the duty cycle error presented in the middle columns of these tables. Both the switching instants and the duty cycle of each switching interval contribute to the harmonic output spectrum. Table 1 also demonstrated how the duty cycle D in a carrier period can have different widths and be modulated at different times depending on which sampling method is used.

We noted that pseudo-natural sampling produces a duty cycle that is sufficiently close to that obtained with natural sampling. This enables us to use digital hardware to implement a SPWM modulation in which an experimental output waveform has a low degrading effect on the expected spectrum.

Table 1. Comparison of sampling methods when the modulator is within the angle $0 < \theta < 2\pi/M_f$. $A = 0.9 \cdot \sin(1.8°)$, $M = 0.9 \cdot \sin(3.6°)$, and $B = 0.9 \cdot \sin(5.4°)$. Switching instants are obtained from MATLAB and Pspice simulations.

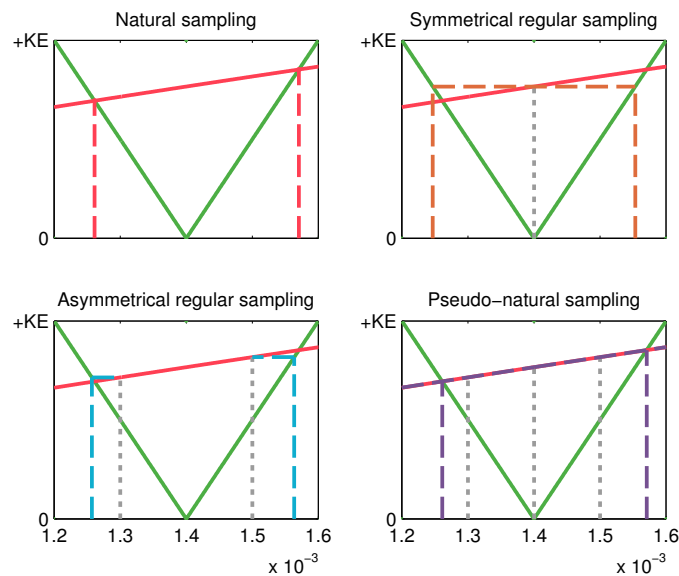| Switching Time	Natural Sampling	Pseudo-Natural Sampling		Symmetrical Regular Sampling		Asymmetrical Regular Sampling	
		Value	Percent Error	Value	Percent Error	Value	Percent Error
X_d	179.74 µs	179.7 µs	0.022%	177.43 µs	1.29%	188.73 µs	5.00%
X_u	225.54 µs	225.48 µs	0.027%	222.66 µs	1.28%	233.93 µs	3.72%
$D = X_d - X_u$	45.8 µs	45.78 µs	0.044%	45.23 µs	1.25%	45.2 µs	1.31%

Figure 5. Switching interval and switching instants yield by four sampling techniques corresponds with the square shown in Table 2 for case (a).

Table 2. Comparison of sampling methods in the time and frequency domains with $E = 50$ V, $M_f = 50$, $M_a = 0.9$, $K = 0.5$, and $r_1 = r_2 = r_3 = r_4 = 0.5$ for (**a**) PD-SPWM, (**b**) POD-SPWM, and (**c**) APOD-SPWM.
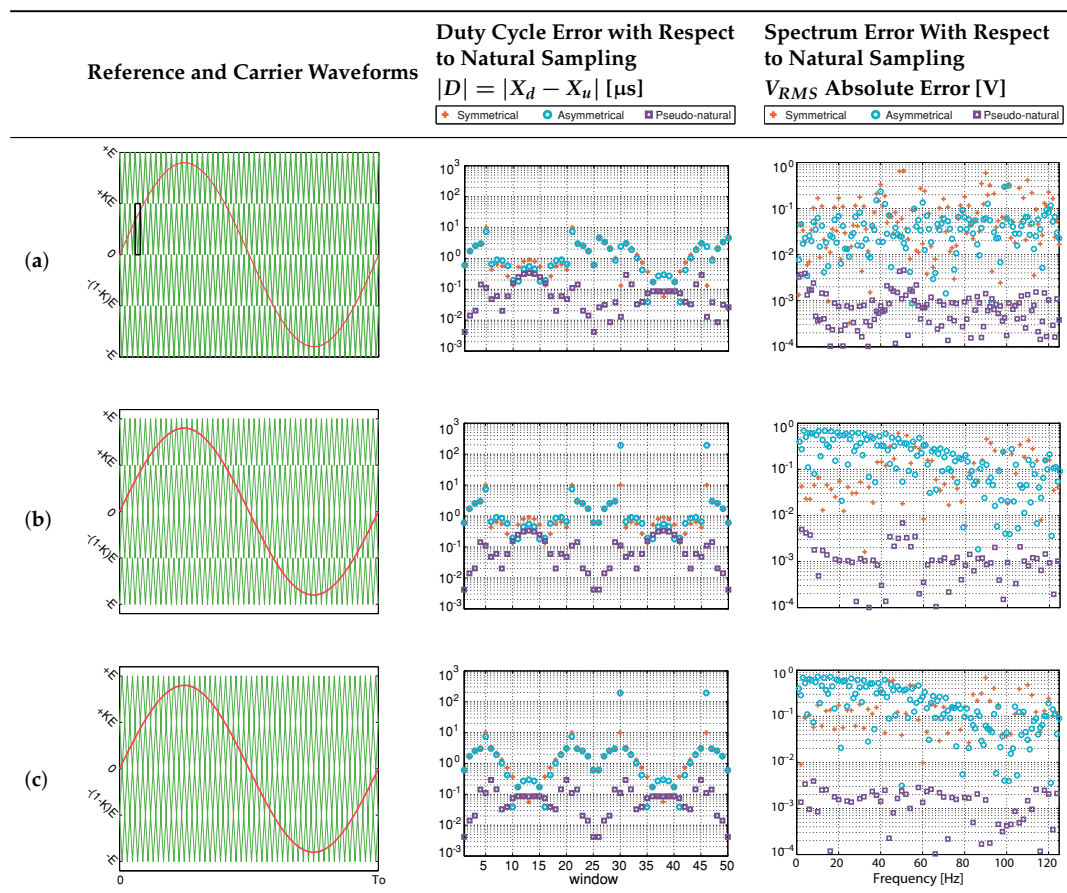
Table 3. Comparison of sampling methods in the time and frequency domains: Regular symmetrical, regular asymmetrical, and pseudo-natural against natural sampling with PD-SPWM, $E = 50$ V, $M_f = 50$, $M_a = 0.9$, and $r_1 = r_2 = r_3 = r_4 = 0.5$ for (**a**) $K = 0.3$, (**b**) $K = 0.5$, and (**c**) $K = 0.8$.
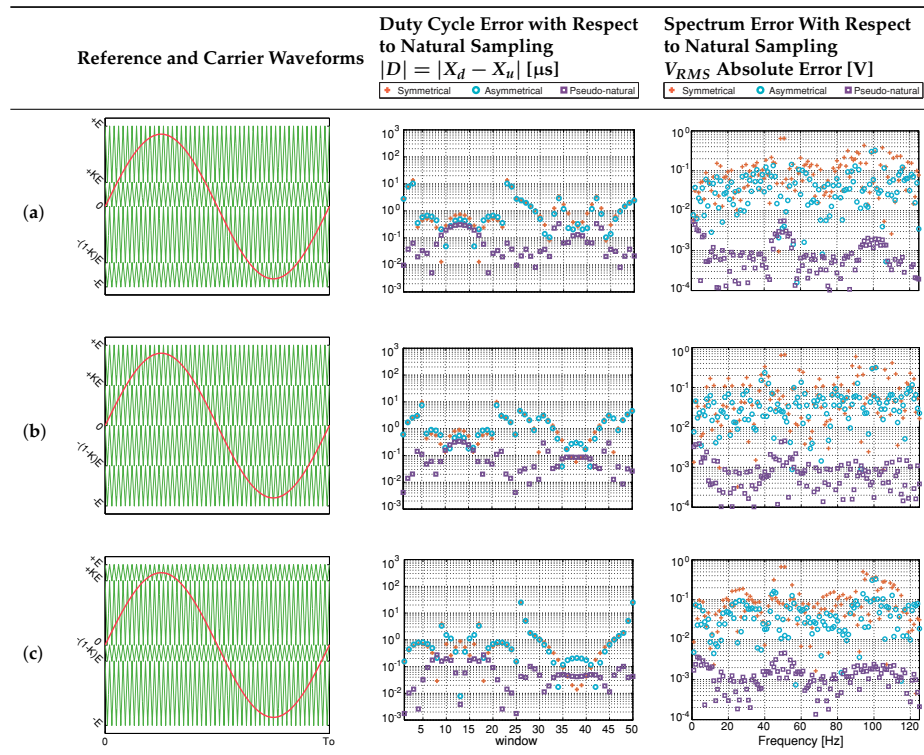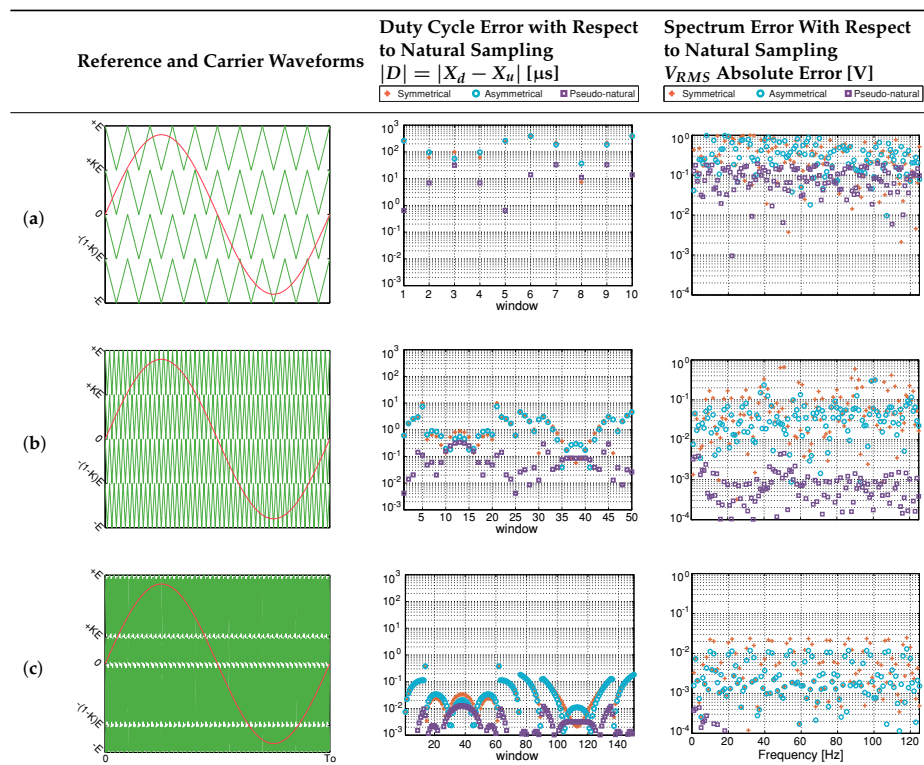

Table 4. Comparison of sampling methods in the time and frequency domains: Regular symmetrical, regular asymmetrical, and pseudo-natural against natural sampling with PD-SPWM, $E = 50$ V, $K = 0.5$, $M_a = 0.9$, and $r_1 = r_2 = r_3 = r_4 = 0.5$ for (**a**) $M_f = 10$, (**b**) $M_f = 50$, and (**c**) $M_f = 150$.

4. Experimental Results

4.1. Experimental Prototype Description

The experimental prototype encompassed three main sections, namely the power stage circuit, the driving circuitry, and the modulation controller system, as illustrated in Figure 6. The power stage section contains the power switching components, the connection plugs for input and output voltages, and the group of reservoir capacitors to stiffen the input voltages. In the second section, the pulses calculated and created by the digital signal processor (DSP) are optically isolated and conditioned for each metal–oxide–semiconductor field-effect transistor (MOSFET). A multiple output transformer is used in order to obtain the AC supplies for seven auxiliary DC sources: one for the optical isolators and six more for each dedicated buffering circuit that transmits the pulses to their respective MOSFETs. Finally, the modulation controller system is where we implemented the pseudo-natural sampling method in a phase disposition PWM controller built into a TMS320F2812 DSP Development Kit. This kit tool is an embedded system including a hardware/software platform in which a PWM algorithm can be written, compiled, and executed as a program. In the TMS320F2812 DSP Development Kit, the configuration of output and input ports and internal hardware is flexible and the switching pulses of the asymmetric full bridge multilevel inverter can be transferred through an optically isolated driving circuit. Table 5 summarizes the binary values for each MOSFET in every switched level or status at the output of the inverter.
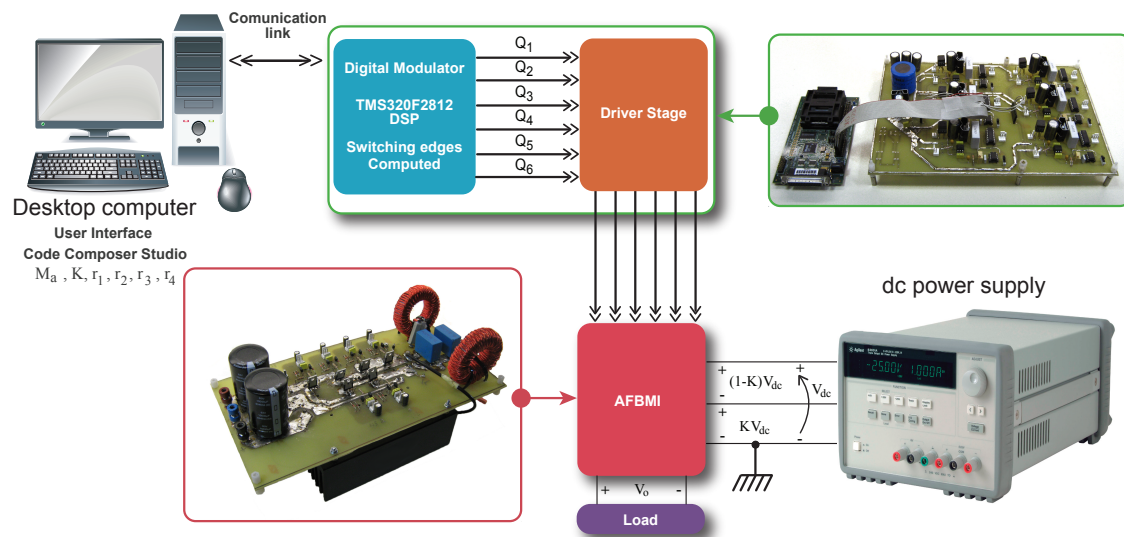

Figure 6. Block diagrams of the open loop system prototype.

Table 5. Switching states and voltage levels.

State	Level	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	D_1	D_2
S_1	E	1	1	X	0	0	1	0	0
S_2	KE	0	1	1	0	0	1	1	1
S_3	0	0	0	1	1	0	1	0	0
S_4	0	1	1	0	0	1	0	0	0
S_5	$(K{-}1)E$	0	1	1	0	1	0	1	1
S_6	$-E$	0	X	1	1	1	0	0	0

X: do not care.

According to Table 5, to drive the multilevel inverter switches, three complementary pairs of driving signals are required. To take advantage of the available hardware in the DSP, the two DSP timers $T0$ and $T1$ are used. The master timer $T0$ is used as the carrier period generator with a fixed value of $T_C = 400$ μs. The slave timer $T1$ is updated every T_c seconds by means of a master timer $T0$

interruption. Then, *T1* is refreshed by changing the values of its registers, namely "Dnhold" (XDP) and "Uphold" (XUP), according the values depicted in Figure 7.

The operating procedure is as follows. The counter starts from zero, increasing its value until the actual value of "Uphold" register is reached. At the same time, the counter value is compared with the value of the "Dnhold" register. While the counter value is bigger than the "Dnhold", the timer *T1* output state is high; on the contrary, *T1* state is low [21]. Due to the internal clock configuration in the DSP, the maximum count value for the "Uphold" is 30,000, which corresponds to the maximum XUP value, 400 μs.
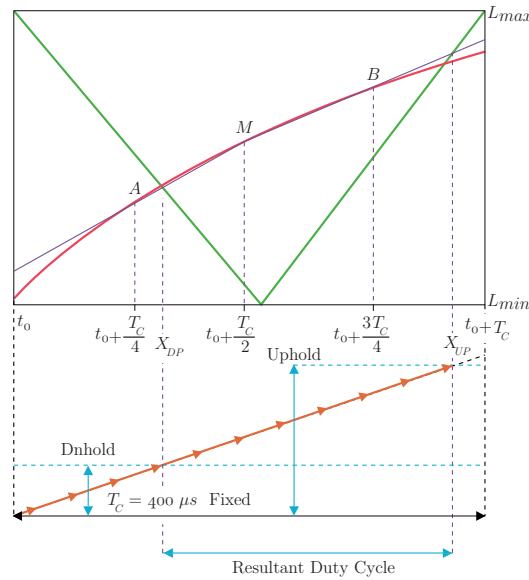

Figure 7. Generation of switching edges X_{DP} and X_{UP}.

As described in Section 3.2, pseudo-natural modulation requires only three samples per cycle, namely *A* at $T_c/4$, *M* at $T_c/2$, and finally *B* at $3T_c/4$, to be implemented. This approximation of the analog modulation (natural sampling) consists of replacing the analog modulating signal with two secant segments *AM* and *MB*. The intersection of the segment *AM* and the carrier falling slope gives the expression of X_{DP}. In the same way, the intersection of segment *MB* and the rising slope delivers X_{UP}. According to that, Equation (1) gives the value of both switching instants expressed in counts.

$$X_{DP}(counts) = 30{,}000 \; \frac{M - L_{max} + \dfrac{A - M}{r_i}}{\dfrac{L_{min} - L_{max}}{1 - r_i} + 2\dfrac{A - M}{r_i}}$$

$$X_{UP}(counts) = 30{,}000 \; \frac{M - L_{max} + \dfrac{M - B}{1 - r_i} + \dfrac{L_{max} - L_{min}}{r_i}}{\dfrac{L_{max} - L_{min}}{r_i} + 2\dfrac{M - B}{1 - r_i}}$$

(1)

However, after several tests, some wrong frequency components on the base-band zone were detected in certain cases. It was found that the dependence of *r* (and $1 - r$) in the denominators of Equation (1) produced overflow conditions in the DSP at some particular cases. To solve this problem, Equation (1) was rewritten to eliminate these factors from the fraction denominators, leading to Equation (2) [21].

$$X_{DP}(counts) = 30,000 \ \frac{(1 - r_i)(2A - M - L_{max})}{L_{min} - L_{max} + 4 \ (1 - r_i)(M - A)}$$

$$X_{UP}(counts) = 30,000 \ \frac{r_i \ (3M - 2B - L_{max}) + L_{max} - L_{min}}{L_{max} - L_{min} + 4 \ r_i(B - M)} \tag{2}$$

4.2. Performance of Diverse Sampling Methods

Despite our focus on PD-SPWM, as shown in Tables 2–4, we have presented in the preceding section the results of other types of modulation to demonstrate the flexibility of our DSP-based modulator. The error in pseudo-natural sampling and in both symmetrical and asymmetrical regular sampling were calculated considering the natural sampling switching instants as the correct or idieal ones. These comparisons have included different criteria such as the phase disposition, the level distribution of input DC supplies, the modulation frequency index, and the use of different carrier shape ratios. In all these scenarios, the pseudo-natural sampling has proved to be a reliable method with improved accuracy over symmetrical and asymmetrical regular samplings (see the resemblance between the theoretical and the experimental results in Table 6). Different performance figures can be used to evaluate the quality of an inverter output waveform, and normally, total harmonic distortion (THD) is a common performance figure. In case of stand-alone inverters, the harmonic content can be evaluated with the voltage THD_V, whereas for grid-connected inverters, the injection of current harmonics in the grid can be quantified with THD_I. A common expression to calculate THD is given in Equation (3), where V_h and I_h are the hth-order harmonic amplitudes and V_1 and I_1 are the amplitudes of the fundamental components, which are 50 Hz.

$$THD_V = \frac{1}{V_1} \sqrt{\sum_{h=2}^{\infty} V_h^2} = \sqrt{\sum_{h=2}^{\infty} \left(\frac{V_h}{V_1}\right)^2}$$

$$THD_I = \frac{1}{I_1} \sqrt{\sum_{h=2}^{\infty} I_h^2} = \sqrt{\sum_{h=2}^{\infty} \left(\frac{I_h}{I_1}\right)^2} \tag{3}$$

Nevertheless, in any modulation, the number of harmonics produced is infinite, and for practical reasons, when THD is calculated with only a limited number of harmonics N, Equation (3) gives only an approximated value of THD. An alternative proposed in Reference [34] calculates the THD value using the *rms* value of the voltage instead of its harmonics:

$$THD_V = \sqrt{\frac{V_{rms}^2}{V_{1,rms}^2} - 1} \approx \frac{1}{V_1} \sqrt{\sum_{h=2}^{\infty} V_h^2} \approx \frac{1}{V_1} \sqrt{\sum_{h=2}^{N} V_h^2} \tag{4}$$

where

$$V_{1,rms}^2 = \frac{V_1^2}{2} \tag{5}$$

and

$$V_{rms}^2 = V_{DC}^2 + V_{1,rms}^2 + \frac{1}{2} \sqrt{\sum_{h=2}^{\infty} V_h^2} \tag{6}$$

This rms-based THD expression has also the advantage of including the THD caused by the DC component, different from Equation (4), where the DC effect in inverter THD is not considered. As has been shown throughout the paper, the pseudo-natural modulation presented here reproduces with more fidelity the switching instants X_{DP} and X_{UP} of a natural modulation than conventional symmetrical and asymmetrical regular modulations because, among other things, it uses three samples. The higher fidelity of this modulation guarantees that pseudo-natural modulation signal V_{PWM} will have less THD_V than the other digital modulations. The THD_V value has been calculated and

measured in many cases and is always far below the 5% reference code given by the European and American standards, IEC 61000 and IEEE 519-1992, respectively.

Table 6. Pseudo-natural against natural sampling with PD-SPWM, $E = 50$ V, $M_f = 50$, and $M_a = 0.9$ for (**a**) $K = 0.5$ and $r_1 = r_2 = r_3 = r_4 = 0.5$; (**b**) $K = 0.5$ and $r_1 = r_2 = r_3 = r_4 = 1$; abd (**c**) $K = 0.3, r_1 = 0.2, r_2 = 0.6, r_3 = 0.7$, and $r_4 = 0.4$.
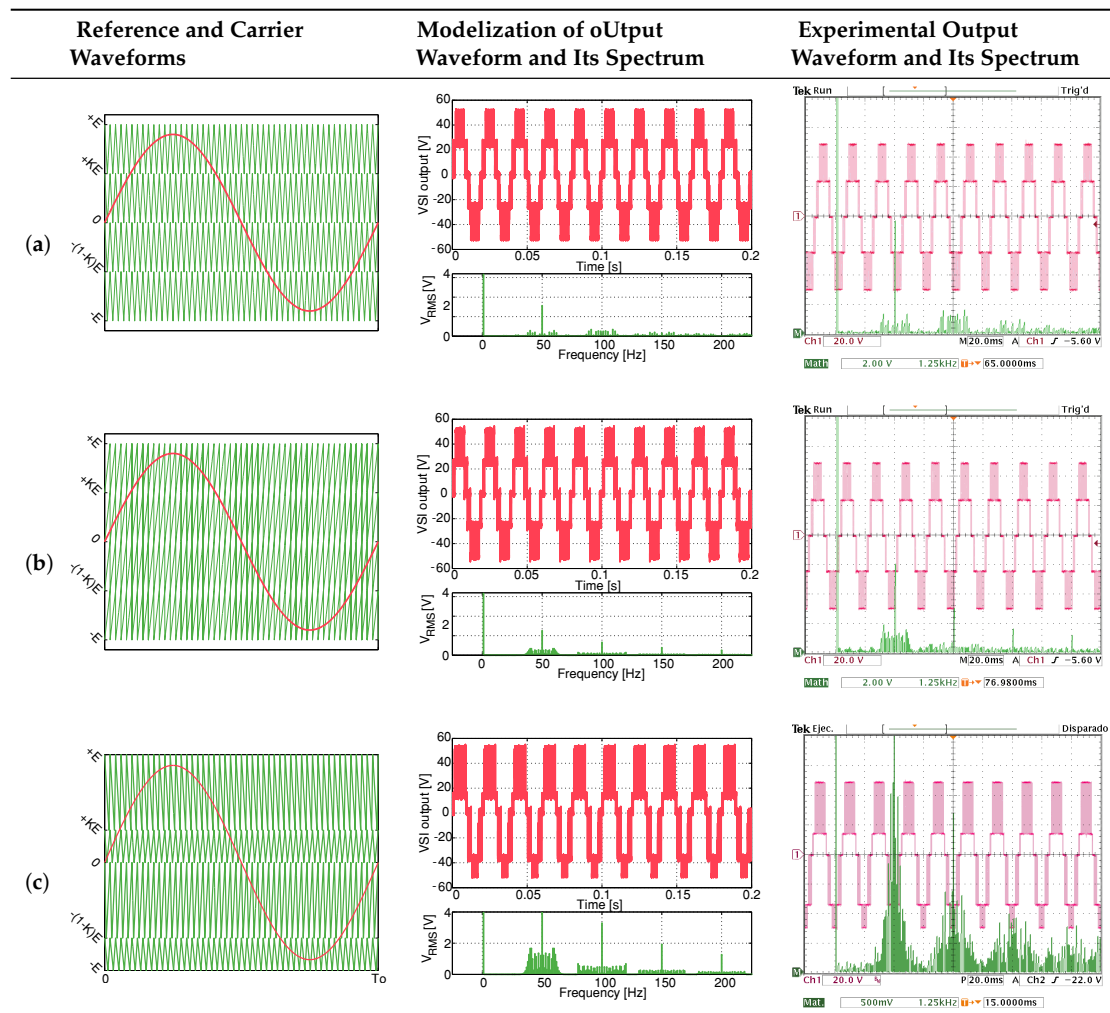
As a matter of example, in Figure 8, five different modulations are presented for a given level distribution $K = 0.5$; a symmetrical carrier set, which is a carrier slope factor $r = 0.5$ for all the carriers; and four different amplitude modulation indexes from $M_a = 0.6$ to $M_a = 0.9$. The figure represented here is the cumulative THD_V. The horizontal axis of the four graphs given in Figure 8 is the number of harmonics N that have been considered calculating THD_V.

Although the inverter prototype has a switching frequency of $F_S = 2.5$ kHz with a frequency modulation index $M_F = 50$, the inverter output low-pass filter has a corner frequency at $F_C = 2$ kHz. For this reason, no more than 40 harmonics are considered to calculate the cumulative THD_V of the inverter output voltage V_{PWM} before the output filter effect. Beyond the switching frequency, the effect of the output filter reduces the negative effects of high-order harmonics, namely, the lateral-bands around the switching frequency and its multiples $2F_S$, $3F_S$, and so on.
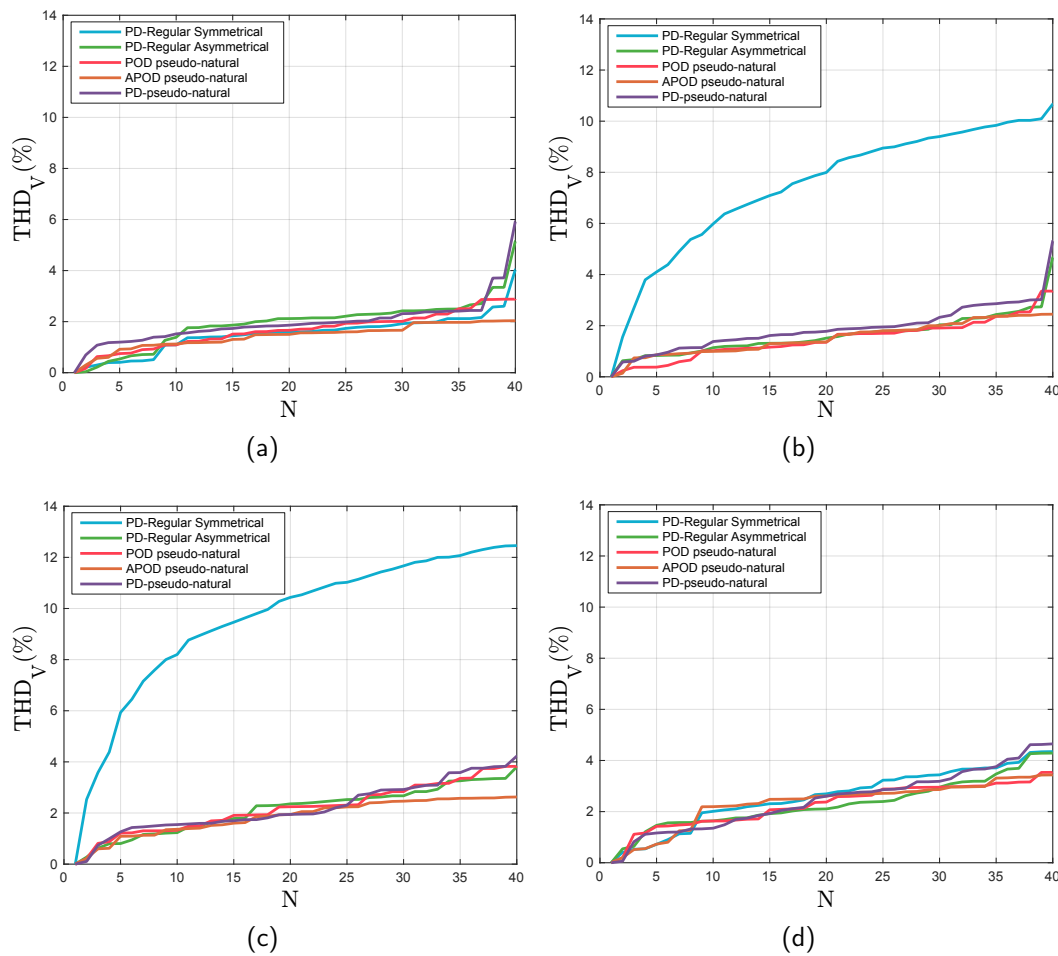
Figure 8. THD_V of PD, POD, and APOD with pseudo-natural sampling and of PD with regular symmetrical and asymmetrical sampling with level distribution $K = 0.5$, $r1 = r2 = r3 = r4 = 0.5$, and modulation index Ma: (**a**) 0.9, (**b**) 0.8, (**c**) 0.7, and (**d**) 0.6.

5. Conclusions

Several modulation techniques have been reviewed to determine the sampling methods used to create the switching instants. MATLAB was used to simulate the switching times calculation. Symmetrical regular sampling and asymmetrical regular sampling have been compared with natural sampling by calculating their respective switching instants. The error of the resultant duty cycle and the error of the output harmonics with respect to the output modulation obtained by natural sampling have been presented. Pseudo-natural sampling has been introduced as a digital approach that takes advantage of digital modulator circuits and, at the same time, yields high fidelity outputs similar to that of an analog modulator. This makes the pseudo-natural modulation an interesting and reliable choice for modulating output waveforms with a high degree of fidelity and low distortion. The error in the duty cycle and the resultant output harmonic by pseudo-natural sampling is small if compared with those classical techniques.

Pseudo-natural sampling requires three samples per cycle, namely A at $T_c/4$, M at $T_c/2$, and finally B at $3T_c/4$. Although when compared to other digital modulations, symmetrical regular sampling requires a sample per cycle (M at $T_c/2$) and asymmetrical sampling requires two (A at $T_c/4$, and B at $3T_c/4$), the fidelity emulating the analog natural sampling is clearly superior, as shown in the experimental results of this paper, with little additional computational and hardware cost, considering, for example, the enormous speed of actual sampler circuits and digital platforms.

On the other hand, substituting an analogical modulation by a digital equivalent has two main advantages. The first one is the suppression of switching noise and jitter effects that can affect the comparators of any PWM analogical modulation. The second one is the easy reconfiguration of the modulation parameters and the repeatability of the experiments. These two issues are especially important if a spectral study of a multilevel modulation for spectral optimization purposes must be carried out. In a multilevel modulation, the amplitude modulation index as well as the carrier frequencies, amplitudes, and slopes have a direct impact on the inverter output spectrum. The possibility of having a digital modulation practically equivalent to a analog one but with all its parameters easily changeable, even in an automated way, not only represents a good tool to carry the spectral analysis but also can be used by itself to simplify the realization of the multilevel inverters modulators, making them more robust to switching noise and other perturbations.

The modulation research has been applied to the AFBMI converter presented in this paper. This circuit topology has the smallest number of switching devices for five-level modulation and as a suitable alternative for carrying out the experimental verification of SPWM using pseudo-natural sampling. The experimental results confirm the feasibility and good performance of pseudo-natural sampling. Among all the common advantages of multilevel modulation, there is the possibility of making high-power and high-voltage inverters for traction applications. Here, using low switching frequency devices (2.5 kHz to 5 kHz) like the insulated-gate bipolar transistors (IGBT's) becomes mandatory, the lateral bands of a sinusoidal modulation become very near to the main component at 50–60 Hz, and then a clean output spectrum modulation is desirable to simplify the inverter output filter design.

In this context, the modification of carrier slopes or nonstandard carriers opens up the possibility of research into alternatives in which the set of carrier slopes can be reconfigured or programmed in order to reduce the harmonic components.

Author Contributions: Conceptualization, H.V.-B.; methodology, H.V.-B. and M.M.-R.; software, M.M.-R.; validation, H.V.-B., M.M.-R., and C.R.; formal analysis, H.V.-B., M.M.-R., and C.R.; investigation, H.V.-B. and M.M.-R.; resources, H.V.-B., M.M.-R., and C.R.; data curation, M.M.-R.; writing—original draft preparation, H.V.-B., M.M.-R., and C.R.; writing—review and editing, H.V.-B., M.M.-R., M.R., and C.R.; visualization, H.V.-B., M.M.-R., M.R., and C.R.; supervision, H.V.-B.; project administration, H.V.-B.; funding acquisition, H.V.-B.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

AFBMI	Asymmetric full bridge multilevel inverter
APOD	Alternative phase opposition disposition
MI	Multilevel inverter
PD	Phase disposition
POD	Phase opposition disposition
PS	Phase shift
SPWM	Sinusoidal pulse width modulation
E	Total DC supply
K	Level distribution coefficient in a five level inverter, $\{-1, K-1, 0, K, 1\} \cdot E$
N	Number of levels in a multilevel modulation scheme
i	An integer number of carriers between 1 and $N-1$ levels in a vertically shifted carrier scheme
T_C	Period of a triangular carrier
t_0	The start time of a switching interval
$t_0 + T_C$	The end time of a switching interval

DSP	Digital signal processor
$T0$, $T1$	DSP counters
T_O	Fundamental period
F_O, F_C	Fundamental and switching frequencies, $F_O = 50$ Hz and $F_C = 2.5$ kHz
$V_O(t)$	Inverter output voltage, $V_O(t) = V_O \cdot \sin(2\pi F_O t)$
M_a	Amplitude modulation index, $M_a = V_O / E$
M_f	Frequency modulation indexes that define the integer number of switching intervals of the AFBMI modulation, $M_f = F_C / F_O$
L_{max}, L_{min}	For an active carrier, the adjacent levels when $L_{min} < V_O(t) < L_{max}$
t_{rise}	Rise time in a carrier signal
r_i	Carrier shape ratio of a triangular carrier, where $r_i = t_{rise} / T_C$
r_1, r_2, r_3, r_4	Set of shape ratios in a five level inverter
rms	Root mean square
THD	Total harmonic distortion

References

1. Bassi, H.; Salam, Z. A New Hybrid Multilevel Inverter Topology with Reduced Switch Count and dc Voltage Sources. *Energies* **2019**, *12*, 977. [CrossRef]
2. Vozikis, D.; Adams, G.; Rault, P.; Despouys, O.; Holliday, D.; Finney, S. Enhanced Multilevel Modular Converter with Reduced Number of Cells and Harmonic Content. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**. [CrossRef]
3. Samajdar, D.; Bhattacharya, T.; Dey, S. A Reduced Switching Frequency Sorting Algorithm for Modular Multilevel Converter with Circulating Current Suppression Feature. *IEEE Trans. Power Electron.* **2019**. [CrossRef]
4. Zhang, J.; Xu, S.; Din, Z.; Hu, X. Hybrid Multilevel Converters: Topologies, Evolutions and Verifications. *Energies* **2019**, *12*, 615. [CrossRef]
5. Tian, X.; Ma, Y.; Yu, J.; Wang, C.; Cheng, H. A Modified One-Cycle-Control Method for Modular Multilevel Converters. *Energies* **2019**, *12*, 157. [CrossRef]
6. Rawa, M.; Siddique, M.D.; Mekhilef, S.; Mohamed Shah, N.; Bassi, H.; Seyedmahmoudian, M.; Horan, B.; Stojcevski, A. Design and Implementation of a Hybrid Single T-Type Double H-Bridge Multilevel Inverter (STDH-MLI) Topology. *Energies* **2019**, *12*, 1810. [CrossRef]
7. Vo, D.V.; Nguyen, M.K.; Do, D.T.; Choi, Y.O. A Single-Phase Nine-Level Boost Inverter. *Energies* **2019**, *12*, 394. [CrossRef]
8. Thiruvengadam, A.; Udhayakumar, K. An Enhanced H-Bridge Multilevel Inverter with Reduced THD, Conduction, and Switching Losses Using Sinusoidal Tracking Algorithm. *Energies* **2018**, *12*, 81. [CrossRef]
9. Khodaparast, A.; Azimi, E.; Azimi, A.; Adabi, M.E.; Adabi, J.; Pouresmaeil, E. A New Modular Multilevel Inverter Based on Step-Up Switched-Capacitor Modules. *Energies* **2019**, *12*, 524. [CrossRef]
10. Valderrama-Blavi, H.; Munoz-Ramirez, M.; Maixe, J.; Giral, R.; Calvente, J. Low frequency multilevel inverters for renewable energy systems. In Proceedings of the IEEE International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20–23 June 2005; Volume 3, pp. 1019–1024. [CrossRef]
11. Valderrama-Blavi, H.; Bosque, J.M.; Barrado, J.A.; Munoz, M.; Calvente, J. Design of a sinusoidal current source using a sliding-mode-controlled asymmetrical full-bridge multilevel converter. *IET Power Electron.* **2008**, *1*, 203–213. [CrossRef]
12. Akhmetov, Z.; Hammami, M.; Grandi, G.; Ruderman, A. On PWM Strategies and Current THD for Single- and Three-Phase Cascade H-Bridge Inverters with Non-Equal DC Sources. *Energies* **2019**, *12*, 441. [CrossRef]
13. Gong, Z.; Cui, Q.; Zheng, X.; Dai, P.; Zhu, R. An Improved Imperialist Competitive Algorithm to Solve the Selected Harmonic Elimination Pulse-Width Modulation in Multilevel Converters. *Energies* **2018**, *11*, 3080. [CrossRef]
14. Guan, W.; Huang, S.; Luo, D.; Rong, F. A Reverse Model Predictive Control Strategy for a Modular Multilevel Converter. *Energies* **2019**, *12*, 297. [CrossRef]
15. Ishfaq, M.; Uddin, W.; Zeb, K.; Khan, I.; Ul Islam, S.; Adil Khan, M.; Kim, H. A New Adaptive Approach to Control Circulating and Output Current of Modular Multilevel Converter. *Energies* **2019**, *12*, 1118. [CrossRef]

16. Acharya, A.B.; Ricco, M.; Sera, D.; Teodorescu, R.; Norum, L.E. Arm Power Control of the Modular Multilevel Converter in Photovoltaic Applications. *Energies* **2019**, *12*, 1620. [CrossRef]

17. Liu, Z.; Li, K.; Sun, Y.; Wang, J.; Wang, Z.; Sun, K.; Wang, M. A Steady-State Analysis Method for Modular Multilevel Converters Connected to Permanent Magnet Synchronous Generator-Based Wind Energy Conversion Systems. *Energies* **2018**, *11*, 461. [CrossRef]

18. Liu, J.; Xu, Z.; Xiao, L. Comprehensive Power Flow Analyses and Novel Feedforward Coordination Control Strategy for MMC-Based UPFC. *Energies* **2019**, *12*, 824. [CrossRef]

19. Foti, S.; Testa, A.; De Caro, S.; Scimone, T.; Scelba, G.; Scarcella, G. Multi-Level Open End Windings Multi-Motor Drives. *Energies* **2019**, *12*, 861. [CrossRef]

20. Leite, R.; Afonso, J.; Monteiro, V. A Novel Multilevel Bidirectional Topology for On-Board EV Battery Chargers in Smart Grids. *Energies* **2018**, *11*, 3453. [CrossRef]

21. Muñoz-Ramírez, M. Contributions on Spectral Control for the Asymetrical Full Bridge Multilevel Inverter. Ph.D. Thesis, Universitat Rovira i Virgili, Tarragona, Spain, 2010.

22. Ventosa-Cutillas, A.; Montero-Robina, P.; Umbría, F.; Cuesta, F.; Gordillo, F. Integrated Control and Modulation for Three-Level NPC Rectifiers. *Energies* **2019**, *12*, 1641. [CrossRef]

23. Marquez Alcaide, A.; Monopoli, V.G.; Leon, J.I.; Ko, Y.; Buticchi, G.; Vazquez, S.; Liserre, M.; Franquelo, L.G.G. Sampling-Time Harmonic Control for Cascaded H-Bridge Converters with Thermal Control. *IEEE Trans. Ind. Electron.* **2019**. [CrossRef]

24. Vasiladiotis, M.; Christe, A.; Geyer, T. Model Predictive Pulse Pattern Control for Modular Multilevel Converters. *IEEE Trans. Ind. Electron.* **2019**, *66*, 2423–2431. [CrossRef]

25. Kouro, S.; Lezana, P.; Angulo, M.; Rodriguez, J. Multicarrier PWM With DC-Link Ripple Feedforward Compensation for Multilevel Inverters. *IEEE Trans. Power Electron.* **2008**, *23*, 52–59. [CrossRef]

26. McGrath, B.; Holmes, D. Multicarrier PWM strategies for multilevel inverters. *IEEE Trans. Ind. Electron.* **2002**, *49*, 858–867. [CrossRef]

27. McGrath, B.; Holmes, D. An analytical technique for the determination of spectral components of multilevel carrier-based PWM methods. *IEEE Trans. Ind. Electron.* **2002**, *49*, 847–857. [CrossRef]

28. Agelidis, V.; Calais, M. Application specific harmonic performance evaluation of multicarrier PWM techniques. In Proceedings of the PESC 98 Record, 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196), Fukuoka, Japan, 22 May 1998; Volume 1, pp. 172–178. [CrossRef]

29. Walker, G.R. Modulation and Control of Multilevel Converters. Ph.D. Thesis, University of Queensland, Brisbane, Australia, 1998.

30. Walker, G. Digitally-implemented naturally sampled PWM suitable for multilevel converter control. *IEEE Trans. Power Electron.* **2003**, *18*, 1322–1329. [CrossRef]

31. Holmes, D.; Lipo, T. *Pulse Width Modulation for Power Converters, Principles And Practice*, 1st ed.; Wiley-IEEE Press: New York, NY, USA, 2003.

32. Mariéthoz, S.; Rufer, A. A New Single-Phase Multilevel Modulator—A Fast and Accurate Method to Compute the Modulator Harmonic Spectra. In Proceedings of the EPE-PEMC 2004: 11th International Conference on Power Electronics and Motion Control, Riga, Latvia, 2–4 September 2004; pp. 172–178.

33. Mariéthoz, J.S. Étude Formelle Pour la Synthèse de Convertisseurs Multiniveaux Asymétriques: Topologies, Modulation et Commande. Ph.D. Thesis, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2005.

34. Farokhnia, N.; Vadizadeh, H.; Fathi, S.H.; Anvariasl, F. Calculating the Formula of Line-Voltage THD in Multilevel Inverter With Unequal DC Sources. *IEEE Trans. Ind. Electron.* **2011**, *58*, 3359–3372. [CrossRef]