

Review

MDPI

Gallium-Nitride Semiconductor Technology and Its Practical Design Challenges in Power Electronics Applications: An Overview

Mauricio Dalla Vecchia^{1,2,*}, Simon Ravyts^{1,2}, Giel Van den Broeck^{1,2}, and Johan Driesen^{1,2}

¹ Departement Elektrotechniek, KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven, Belgium

² EnergyVille, Thor Park 8310, 3600 Genk, Belgium

* Correspondence: mauricio.dallavecchia@kuleuven.be

Received: 7 June 2019; Accepted: 9 July 2019; Published: 11 July 2019



Abstract: This paper will revise, experimentally investigate, and discuss the main application challenges related to gallium nitride power semiconductors in switch-mode power converters. Gallium Nitride (GaN) devices are inherently gaining space in the market. Due to its high switching speed and operational switching frequency, challenges related to the circuit design procedure, passive component selection, thermal management, and experimental testing are currently faced by power electronics engineers. Therefore, the focus of this paper is on low-voltage (<650 V) devices that are used to assemble DC-DC and/or DC-AC converters to, for instance, interconnect PV generation systems in the DC and/or AC grids. The current subjects will be discussed herein: GaN device structure, the advantages and disadvantages of each lateral gallium nitride technology available, design challenges related to electrical layout and thermal management, overvoltages and its implications in the driver signal, and finally, a comprehensive comparison between GaN and Si technology considering the main parameters to increase the converters efficiency.

Keywords: gallium nitride semiconductors; practical challenges; power electronics

1. Introduction

The power electronics field is known for its extensive range of applications, e.g., from power converters, semiconductors, electric machines, and generation/storage systems to analog and digital circuits, ICs, and RF [1]. Most of these applications are currently in vogue, e.g., distributed generation with renewable energy sources and its control [2–5] and storage systems [6,7], since decreasing the CO₂ emissions generated by some of the centralized power plants is now required. Building Applied Photovoltaics (BAPV) and Building Integrated Photovoltaics (BIPV) and their connection to the system are the focus of much research currently. Researchers aim at improving the efficiency of the PV panels in the range of 1% pt; however, an important feature is often forgotten: the interconnection of these PV systems in the grid. Figure 1 illustrate this interconnection in the AC system. As can be seen in Figure 1, power electronics converters are also a key factor to achieve a higher system efficiency, since these devices are responsible for the interface between solar generation (in DC) and DC or AC systems.

Power converters, for most researchers, are a black-box. These devices, among other components, are made by passive components, e.g., capacitors, inductors, and transformers, and power semiconductors (diodes and FETs). High efficiency and power density are the main goal in these applications since the maximum amount of PV generation should be injected into the grid with a minimal size space occupied by these devices [8–10] because of the costs of the m² in highly-populated areas. For instance, a regular BAPV installation in a building environment is interconnected with the AC system via IGBT-based high-power inverters. This building needs a dedicated room of around

 50 m^2 to place the inverters to interconnect a medium-sized (100 kWp) BAPV system. If, instead of high power inverters, the system is interconnected via DC-DC Module Level Converters (DC-DC MLC) or micro-inverters applying low-voltage/low-power semiconductors (GaN or even Si) connected directly at the back of the modules, the 50-m² room space is saved and can further be used for other purposes. Notice that, for these type of applications, both technologies (GaN and Si) can still be used. Furthermore, the size of the magnetics, passive components, and heat sinks will directly influence the size of these MLC or micro-inverters. The size of the magnetics and passives, the bulkiest components, together with heat sinks, in a power converter, are directly related to the operational switching frequency of the converter [8]. Reported in the literature, for DC-DC MLC, GaN-based converters perform a size reduction of three times compared with the same structure in Si [11]. Finally, this approach can also mitigate the partial shading problem when a few PV panels are connected in strings. Wide-Band Gap (WBG) [12,13] semiconductors are known to have faster transitions compared to Silicon (Si) switches, which determines the first project question: Do Wide Band Gap (WBG) devices present better overall performance than Silicon (Si) switches in terms of efficiency and power density in power electronics applications? To answer this question, a comprehensive analysis comparing these devices' characteristics should be done in order to evaluate each technology available on the market.



Figure 1. Interconnection of PV panels into the grid and emphasis on the basic components of power electronics converters.

As mentioned above, the power semiconductor operational switching frequency essentially determines the volume of the passive components in a power electronics converter. Currently, most of the applications and converters on the market are made based on Si power semiconductors. Silicon MOSFETs started to be used in power electronics applications in the early 1960s after its invention in 1960 at Bell Labs [14]. This component started to gain more attention since it presented a high switching speed (at that time), which enabled its usage in application where BJTs suffer because of its internal characteristics and, eventually, even replacing BJTs in regular applications. From that point on, the field dramatically evolved, since with the dissemination of the power Si-MOSFET, operational frequencies of tens or hundreds of Hertz (Hz) migrated to tens or few hundreds of kiloHertz (kHz), enabling the shrinkage of the passive components and still achieving considerably high efficiencies.

Additionally, the MOSFET implementation opens the door for new DC-DC, DC-AC, AC-DC, and AC-AC topology proposals, since the converters can switch faster with lower overall losses. This breakthrough also pushes other components, e.g., capacitors, wires, cores, and isolation material, to become more reliable and to have better characteristics, whereas an optimization to achieve better performance and power density can be realized for higher switching frequencies [15–18].

Since then, silicon technology has evolved, and now, the Si material is close to its technological limits. Figure 2, with Baliga's Figure-Of-Merit (BFOM) [19,20], highlights the common materials' theoretical limits. BFOM calculates and compares, based on the materials' mobility (μ_r), permissivity (ϵ_r), voltage breakdown (V_B), and band gap (E_G) (check Equation (1)), the on-resistance of each material per surface area. As can be seen in Figure 2, Gallium Nitride (GaN) and Silicon Carbide (SiC) present much better BFOM than the current state-of-the-art silicon material, since higher breakdown voltages can be achieved with lower on-resistance for the same surface area (decreasing conduction losses) if compared with Si technology, which enable its usage in the new generation of power converters.



Figure 2. Baliga's figure-of-merit to show the technological limit of each semiconductor material.

Is silicon, after many years of dominating the power electronics semiconductors market, in danger of being massively replaced? The answer to this question is yet unknown, but one statement can be made: silicon technology has a promising competitor, as happened with BJTs in the early stage, so-called WBG semiconductors. Research companies and groups worldwide are investigating this new technology currently.

As previously mentioned, the most common WBG materials used currently to assemble power devices are Gallium Nitride (GaN) and Silicon Carbide (SiC) in commercial applications, although variations and other materials are also being explored in research, e.g., Ge, GeSn, AlGaN, GaAs, 4H-SiC, 2H-GaN, Ga₂O₃, diamond, and 2H-AlN, materials listed in [21,22]. It was proven that, for high-voltage applications (>1200 V), SiC is a better option compared to GaN [23]. Lateral GaN devices present limitations in terms of voltage and current capability because of the lateral structure, which limits the technology application to a lower voltage level. Comparatively, GaN material presents better characteristics than SiC, but due to the aforementioned limitation, GaN components are on the market for a voltage range up to 650 V.

GaN is a promising WBG technology for the applications in, e.g., BAPV/BIPV and in low-voltage DC networks, since the limited DC or AC voltage range is within the boundaries of this device. Therefore, the aims of this paper are the following: (1) present a brief review of the current state-of-the-art WBG GaN technology available on the market for low-voltage applications (<650 V); (2) give to power electronics engineers insights about the design and application challenges/recommendations that this new technology offers; and (3) discuss, based on different figures-of-merit, which technology, between GaN and Si, is the possible candidate for the next generation of power electronics converters. In the end, it is expected that the reader will have a clear vision about the different GaN technologies and which option suits better its specific applications.

The GaN devices on the market typically present different packages and characteristics, which lead to distinct circuit designs and thermal management challenges. In order to have a better understanding about the aforementioned criteria, the document will discuss, in Section 2, the GaN's internal structure (enhancement-mode (e-mode), cascode, depletion-mode (d-mode)) and the advantages and disadvantages of each technology available on the market. This discussion is relevant to situate specific applications of each technology, and based on this selection, different approaches, for instance, in terms of driver stage and heat sink selection, can be taken into consideration for final integration. Practical design challenges in terms of layout and cooling strategies will be further discussed in

(1)

Section 3. Finally, a qualitative comparison between similar 650/600-V and 100-V GaN and Si power semiconductors is provided in Section 4 in order to discuss the important figures-of-merit that should be considered by designers when projecting its converters for such applications.

2. Device Configuration

According to [24], semiconductors with high band gap properties allow for higher operating temperatures, since a lower leakage current will be generated once these components present stronger chemical bonds at the lattice band. Internally, each GaN has its own layer structure [25–28]. More specifically, GaN components can be made by GaN-on-GaN [29,30] or GaN-on-Si [31–33] substrates, for instance.

From the power electronics engineer perspective, special attention to understand the physical limits of the devices that will be applied in the circuit is necessary in order to select and project driver and power stages correctly. For instance, parasitic components and switch characteristics, e.g., threshold voltage, maximum/minimum gate voltages, and gate storage energy, constitute the essential information in order to project the driver stage accordingly for the selected switch. R_{ds-on} is the parasitic element that defines the equivalent circuit of the device when conducting; hence, conduction losses can be calculated using this parameter. Tests under controlled conditions are also important to measure the transition times between on/off states. This information is important to calculate the switching losses under hard-switching applications.

GaN semiconductors, from the power electronics point of view, are divided into three main categories: depletion-mode, cascode-mode, and enhancement-mode. The category in which the device will be included is dependent on the internal structure and layout during its production, as mentioned above. These devices will be briefly discussed in this section.

2.1. Depletion-Mode

Depletion-mode devices are inherently "normally-on". Normally-on semiconductors present better $R_{ds-on} * Area$ if compared with normally-off GaN (cascode-mode and e-mode) and Si semiconductors, although it becomes more challenging for implementation, since its default state is "ON". This characteristic leads to the adoption of additional protection [34] and/or a soft-start synchronization at the driver stage in order to guarantee the switch operability before system connection, otherwise short-circuits may occur depending on the topology implemented.

This device turns-on with 0 V between gate-source terminals. Positive voltages can also be applied to turn-on the device, although extra circuitry or an extra voltage source needs to be used to achieve this requirement. To commute the semiconductor to the "OFF" state, a negative voltage of -15 V-20 V has been reported in the literature [35,36] for d-mode devices. Figure 3a shows the representation of a d-mode device with its gate-source voltage levels.



Figure 3. Different structures for GaN devices on the market: (**a**) normally-on GaN device; (**b**) cascode GaN device; and (**c**) normally-off GaN device.

Additionally, application of d-mode devices also brings challenges for the gate-driver circuitry of these devices. Since its creation, many gate driver circuits have been proposed to overcome the issue with the voltage level. Some of these driver circuits are adjustable [37], depending on the threshold and full turn-on/-off voltages of the devices. Resonant drivers [38] are also reported in the literature. Ishibashi et al. [39,40] proposed a new driver solution based on the connection of a capacitor in series

with the output gate-driver resistor. This capacitor is previously charged before it starts the device operation and is responsible for applying the required voltage between gate-source terminals of the semiconductor.

2.2. Cascode-Mode

The cascode structure was created to overcome the normally-on behavior of the d-mode GaN devices, since normally-on devices are not desirable in most power electronics applications that require a fail-safe operation. To do so, a Low-Voltage (LV) Si-based MOSFET (typically 30 V) is implemented in series with the High-Voltage (HV) GaN device [41–44]. The device structure is shown in Figure 3b. The drain and source of the LV Si device are connected, respectively, to the source and gate of the HV GaN.

The switching behavior of this device will be briefly described. When the devices are in the off-state, the drain-source parasitic capacitance of the LV Si MOSFET is charged. Considering no internal parasitic inductances between the above-mentioned terminals and the HV GaN gate-source terminals (no delay included in the analysis), the voltage applied in the HV GaN gate-source is the negative value of the drain-source voltage of the LV Si device, characterizing the normally-on behavior of the HV GaN (off-state with negative voltage). When it is applied a gate-signal to turn the LV Si switch "ON", the channel of the Si switch is closed, and both Si drain-source and GaN gate-source capacitances discharge through the Si channel, decreasing and increasing the terminals voltage, respectively. When the drain-source voltage of the Si device is 0 V, the gate-source voltage of the HV GaN device is at the same voltage level, and the GaN device is fully-on (normally-on characteristics).

The LV Si MOSFET now drives the GaN semiconductor, adapting the control signals of the device, which previously needed a negative power supply to drive the normally-on GaN, and now, with the cascode structure, a positive voltage is used to turn-on the device. Conventional Si drivers can be implemented in this circumstance. An adaptation on the cascode control was proposed by Texas Instruments in [45], when the LV Si MOSFET was used only to start the device and remained in the on-state during the entire operation, instead of switching together with the HV GaN, for normal cascode operation.

In its internal structure, d-mode GaN devices do not have an anti-parallel body-diode, which brings the benefit of mitigating the reverse recovery losses during the switching transient. When an LV Si MOSFET is connected in series, adapting the device to become normally-off, the Si anti-parallel diode is internally inevitable and is added to the switch structure (check Figure 3b), which leads to an increase of reverse recovery losses at the device level. Moreover, the implementation of an LV Si MOSFET in series with an HV GaN device also increases the switch on-resistance, increasing the overall losses under the device's conduction stage. Hence, this technique was adopted only for GaN devices in the range of 600–650 V, when the on-resistance of the cascode device was not strongly affected by the introduction of the LV Si MOSFET.

An advantage of cascode-mode is related to the threshold voltage of the devices, since the LV Si MOSFET the responsible for driving the HV GaN. This configuration allows the application of a regular gate-driver circuit, once the LV Si switch is the component that drives the HV GaN. The gate driver and normally-on characteristics of the d-mode devices are bypassed by the cascode-mode, although the reverse recovery of the device increases by the application of a Si MOSFET, which also negatively affects the overall speed of the device.

2.3. Enhancement-Mode

The enhancement-mode device is structurally similar to the depletion-mode, since no LV Si MOSFET is implemented. The main difference between d-mode and e-mode devices is that the e-mode GaN is internally adapted to be able to turn-on with a positive voltage and turn-off with 0 V or negative voltages. This adaptation is made by introducing, for instance, an additional layer of p-doped GaN or

AlGaN in between the gate and the AlGaN surface of the device. This addition shifts the threshold voltage, making it into a normally-off device, in which a positive voltage turns-on the device and a 0 V or negative voltages turns-off, as shown in Figure 3c.

Enhancement-mode devices add the advantages of the depletion-mode (no LV Si MOSFET in series) and the cascode-mode (normally-off structure) devices, which leads to a better switching behavior with less losses and a simpler driver implementation. The main drawback of the structure is related to the low threshold voltage of the device (check Table 1), in which it makes the component susceptible to ringing, since its voltage margin between 0 V and V_{th} is extremely low. Additionally, to fully turn-on the device, the voltage level should be between 5–6 V (depending on the manufacturer), and the maximum allowed voltage between gate-source terminals is in the order of 7 V, which leads to an extremely low margin between fully turned-on and maximum gate voltages. Therefore, the gate channel can collapse if the voltage is not controlled to stay under the device limits.

CaN Tachnology	Criteria								
Gain Technology	Ref.	V (V)	I (A)	$R_{ds-on}\left(\Omega\right)$	Q_{rr} (nC)	V_{th} (V)	Package	Q_g (nC)	
Normally on	[40]	600	2	0.16	6		-	-	
Normany-on	[35]	650	100	0.017	-	-10	SMD	-	
Cascode	[46]	650	20	0.110	54	2.1	TO-220	10	
Normally off	[47]	650	22.5	0.067	0	1.1/1.3	SMD	5.8	
Normany-on	[48]	650	120	0.012	-	-	-	25	

Table 1. Application KPIs for comparison of normally-on, cascode and normally-off GaN devices.

2.4. Comparison between GaN Structures

To be able to compare the different structures, some Key Performance Indicators (KPIs) are defined for the 600–650-V GaN devices (components available on the market or tested as samples). For an application point of view, the important parameters that should be verified before component selection are shown in Table 1. Comparing the three structures, it can be noticed that the normally-off devices present lower values in terms of drain-source on-resistance compared with the cascode structure, for similar current levels. This KPI is directly related to the conduction losses performed during normal operation. Additionally, normally-off devices present zero reverse recovery and lower gate charge compared with cascode devices, decreasing the commutation losses. On the other hand, cascode and normally-on devices are less susceptible to inappropriate turn-on/-off since the threshold voltages are higher than the normally-off GaN devices on the market. This KPI brings an additional challenge for PCB designers, and this will be discussed in Section 3.

2.5. Advantages and Disadvantages of Each GaN Technology

Based on the discussion presented in Section 2, partial conclusions regarding the GaN technologies are depicted:

- The normally-on device brings a cost benefit for manufacturers in terms of production, although presenting a limited amount of applications and gate-driver challenges (synchronization and/or extra safety) in order to have a safe operation. Possible applications include current-fed converters and converters with short-circuit protection schemes integrated.
- Cascode GaNs bring the benefit of normally-off devices with a higher threshold voltage. On the other hand, the devices present reverse recovery due to the LV Si MOSFET and higher on-resistance and internal parasitics compared with other GaN technologies. Since this component is more immune against gate oscillations (discussed in Section 3.1.3), this component is suited

better in applications with multiple switches, e.g., multi-level converters and high step-up and step-down applications.

Normally-off GaNs present the lowest gate charge and on-resistance compared with the
aforementioned GaNs, while having the lowest threshold voltage. Thus, this component is
more susceptible to malfunction due to gate-source ringing. Converters with ground connection
to the source of the switch or limited floating points are the structure in which this device
presents better performance, e.g., DC-DC boost converter, DC-DC buck converter, full-bridge, and
half-bridge topologies.

3. Design/Layout Challenges

Since GaN has more and more appeal on the power electronics market and in the research community, topics related to PCB design, thermal loss extraction, and challenges related in how to control overvoltages due to fast switching and, consequently, gate oscillations will be discussed herein. The objective is to highlight the challenges that designers are facing when changing from the conventional Si to GaN devices and to provide insight into how to overcome these issues.

3.1. PCB Layout/Design

3.1.1. Device Package

Available on the market, most of the GaNs are Surface-Mounted Devices (SMD). This trend relates primarily to decreasing the parasitic inductances between the device terminals, since this component can operate at high switching frequencies, and these parameters play a major role in switching performance [49–53]. The GaNs available have much smaller packages as compared to the TO family: 83-times smaller than TO-247-3 and 45-times smaller than TO-220 (considering only the package), which brings the benefit of space reduction, as shown in Figure 4, although the thermal cycle of the device should be addressed carefully. However, some off-the-shelf GaN devices are made in the TO-220 package [46]. SMD components also bring the benefit of decreasing the power loop parasitics, since the drain-source-gate-kelvin pins are directly connected to the PCB and not via external pads, as for the TO family shown in Figure 4.



Figure 4. Size comparison between TO-247, TO-220, and SMDGaNs available on the market.

3.1.2. Internal Parasitics

In Figure 3, ideal devices are depicted. Since GaN semiconductors can operate at high switching frequencies due to their fast transient both to turn-on and turn-off, the internal and external parasitics due to, respectively, internal bond-wire connections and PCB layout need to be considered and minimized during device production and the PCB layout project in order to maximize device and system performance. As power electronics engineers, the only feature that can be controlled in this case is the PCB design parasitics, as the switches are off-the-shelf selected. Figure 5a shows the main internal parasitic components inside a cascode GaN device [54,55]. It can be noticed that the structure

of the cascode device increases the number of internal parasitic inductances and capacitances to be considered in the analysis.

A basic model of a normally-off GaN device is shown in Figure 5b. Some manufacturers provide an extra pin, the so-called Kelvin connection (Figure 5b illustrate this connection). This pad provides the return for the gate driver, minimizing or even eliminating the influence of the parasitic common source inductance in the driver circuit. This pin, however, is not present in all devices. In these circumstances, the source return track of the driver circuit should be placed as close as possible to the gate pin, as shown in Figure 5c, minimizing the influence of the aforementioned inductance in the driver stage and minimizing the gate driver loop. As mentioned previously, a negative voltage is recommended to turn-off cascode-mode and e-mode GaN devices. However, this feature increases the number of components in the driver stage, hence the complexity of the circuit. Increasing the number of components in the driver stage, the minimization of the parasitic inductances in this part of the circuit becomes a challenge during the design stage. In Section 3.1.3, more details regarding this topic will be presented.



Figure 5. Internal parasitics in: (**a**) cascode GaN; (**b**) normally-off GaN; and (**c**) project example of how to connect the return source pin if no Kelvin connection is available.

3.1.3. Signal and Power Loops

The two critical loops that should be carefully projected in order to achieve the best performance of these devices are the signal and power loops, as highlighted in Figure 6a. As previously mentioned, the parasitic inductances and capacitances influence the performance of these devices [56,57], but they are not the only ones. Copper-based planes and tracks interconnect the components on a PCB layout. These connections increase, primarily, the parasitic inductances of the loops, and consequently, these loops should be carefully routed and minimized in order to achieve a better circuit performance.

The signal loop or gate driver loop is the circuit that drives the GaN devices. The transition speed of the device is directly related to the R_{gon} and R_{goff} and the voltage levels applied at the gate/source terminals. The R_{gon} controls the turn-on slew rate $\frac{dv}{dt}$ of the GaN device. If the gate resistor is too small, the $\frac{dv}{dt}$ is high, and ringing between drain-source (overvoltage) and gate-source terminals might occur [58]. This gate-source ringing, if not properly addressed, can cause an inappropriate turn-on if the voltage V_{gs} becomes higher than the threshold voltage V_{th} of the device. A negative voltage to turn-off the GaN component is recommended to minimize this influence, giving more margin between the turn-off voltage plateau and the threshold voltage of the GaN, although this strategy increases the

gate-driver circuitry complexity and the energy consumption of the circuit. R_{goff} is responsible for the pull-down of the device to the off-state.

Gate oscillations are also caused by the power loop parasitics, and this loop should be carefully addressed in order to eliminate unintended device turn-on. The gate oscillations is generated by the common source inductance in the power loop and gate inductances in the signal loop. Both inductances should be minimized during the PCB design stage. The switches need to be placed as close as possible to each other to minimize the common source inductance. Additionally, the output of the driver stage (R_{gon} and R_{goff}) should be placed as close as possible to the gate of the switches to minimize the driver loop and, consequently, the gate parasitic inductance, as illustrated Figure 5c.

As shown in Figure 6b (adapted from [45]), drain-source overvoltages can be observed in the GaN e-mode terminals. All the parasitic capacitances will be charged during the turn-off transient. The overvoltage generated by common source inductances at the power stage level can improperly turn-on the GaN devices since the gate-source signal might present ringing above the threshold voltage level. An experimental verification showing in practice the relatively low threshold level is depicted in Figure 7. It can be noticed that the gate-source voltages from nearby GaN devices were also affected by the ringing. This event happened since the low internal parasitic capacitance values of these devices are not completely immune, and the noise propagates throughout the circuit. Additionally, the components perform an excessive ringing since they are connected to multiple floating points, which brings an extra challenge since the circuit might have multiple topological stages during one switching period, leading to multiple ringing events in one switching cycle.

Snubber circuits [43,59–61] are an alternative to suppress switch overvoltages generated by fast switching transients or bad PCB design. Some snubber circuits are regenerative, which configure an advantage since no energy is dissipated during the commutation period (all energy stored in the snubber is returned to the circuit), although some of these configurations are ratter complex and require more PCB space. On the other hand, some snubber circuits, e.g., RC and RCD snubbers, are passive structures, which reduces the overall efficiency of the circuit by consuming some power, although these are simple structures that do not require a large amount of PCB space.



Figure 6. (a) Critical loops in a power electronics converter design; and (b) drain-source overvoltage and its impact on gate-source voltage level.

From the discussion, some key points can be highlight that should be taken into consideration while developing power converters applying GaN semiconductors:

- PCB design is crucial to achieve the best performance of the GaN devices.
- Power and signal stages should be carefully addressed and routed in order to minimize the parasitic inductances that disrupt the performance of the GaN device. Some devices on the market already integrate GaN devices and their driver circuits in the same package [62–65].

- Although 0 V is sufficient to turn-off the GaN e-mode devices, a negative voltage is preferred in order to increase the noise immunity against ringing at the driver stage, as shown in Figures 6 and 7.
- Gate-resistors are used to control the speed of the device, and its placement during the design stage should be as close as possible to the gate pin of the GaN semiconductor. As mentioned above, monolithic integration of the switch and driver in the same package has been considered for the new generation of GaN power devices. Although this strategy brings the benefits of loops and parasitic minimization, mitigating voltage dips that might collapse the gate of these devices, it also takes away the freedom to control the rise and fall times of the switch by selecting the proper gate resistors. Additionally, these structures can be used to build simple topologies, e.g., buck, boost, buck-boost, and full-bridge. More complex structures still require separate switches and drivers.
- Components that present Kelvin connection internally decouple the common source inductance on the power stage of the device. For components that do not offer this extra pin, the gate return pad should be connected as close as possible to the gate of the GaN device, as shown in Figure 5, minimizing the parasitic inductances at the gate level.



Figure 7. Experimental verification of the capacitive coupling in GaN devices: drain-source overshoot and its influence on the gate-source signal.

3.2. Thermal Management

As previously mentioned, GaN devices cannot achieve their best performance if used in conventional TO packages, although some options are available on the market [46]. Manufacturers are now developing new packages to overcome parasitic problems related to GaN devices, most of them SMD packages. These new packages introduce an extra challenge for power electronics engineers: thermal management. Thermal heat transfer proves to be correlated with the overall performance and reliability of the device [66], and some studies in the field have been realized [67].

Reported in the literature [68–72], GaN components can survive much higher temperatures, in controllable environments, than the Si competitor. For applications in power electronics, a major issue is related in how reliable these devices are to operate in harsh environments, for instance deserts (high ambient temperature) or space (difficult/impossible access to maintenance). Some discussions on this topic are found in the literature [73]. Making these components as reliable as possible is a challenge faced by semiconductor researchers. Studies show that changes in the internal layer distribution/composition [74–76] and gate overdrive protection [77] improve the reliability of these devices. Additionally, the temperature-dependent thermal resistance and reliability of these devices are also an important point, as discussed in [78].

SMD packages are extremely compact, but might introduce thermal problems related in how to extract the heat, generated by conduction and switching losses, from these devices. Research is being conducted to improve the heat dissipation packaging [79] and the thermal management of these devices [80]. Some companies claim that its packages have good thermal transfer capability, in which a heat sink can be directly attached to it. In some cases, a thermal pad is provided on top of the device package [47] to help the heat extraction using passive cooling. In these cases, an SMD or regular heat sink is directly attached to the device, as shown in Figure 8a. Some devices on the market also provide a bottom thermal pad [81] to improve the thermal extraction. This pad needs to be connected directly with the source pin of the device.



Figure 8. Thermal techniques to extract heat from SMD GaN devices.

Most of the devices available on the market do not present thermal pads, nor packages with good thermal transfer capability, which lead to some extra effort to keep the device temperature below its limit. Some of the strategies used are presented in Figure 8b–d. Since these devices transfer the heat through the source pin, some thermal vias are used to connect top and bottom copper layers on the PCB level, and interfaced by a Thermal Interface Material (TIM), a heat sink is attached to spread and cool down the devices (Figure 8b). Another technique is to create a copper region connected to each source of the devices using the top layer of the PCB and attach an SMD heat sink to each device source terminal (Figure 8c). Another option listed herein is to use inner copper layers as heat sinks, increasing the number of layers in the PCB design and using one or more layers, with a large copper plane area, as the heat sink (Figure 8d), helping to extract the heat from these devices. Depending on the project specifications and the chosen technology, the best cooling method among the possible ones can be applied to achieve the maximum component, circuit, and system performance.

4. Comparison between GaN and Si Semiconductors

As previously mentioned, GaN devices are a possible competitor of Si devices currently. Table 1, however, shows just a comparison between different lateral GaN devices/technologies. This comparison is now expanded for Si components with similar voltage and current specifications, similar to Table 2. These devices will be addressed herein with discussions related to their internal characteristics and some important figures-of-merit. These figures-of-merit are important in order to compare the available technologies on the market and show the importance of a good choice for applications in different circuit topologies.

In [82], the author stated that the device parameters should be compared for components with similar current density *J*_{on} and not a similar current level. From the power electronics point-of-view, however, information regarding current density and, more specifically, die or chip area is not provided in datasheets, which leaves no other option than selecting components with a similar current capability for comparison. Therefore, the comparison made herein is between 650/600-V and 100-V GaN and Si devices for similar current levels available on the market. As previously mentioned, one of the main advantages of GaN normally-off devices is the absence of reverse recovery, since no body diode is present in their internal structure. This characteristic is interesting to mitigate part of the switching losses during turn-on of the device since with no body diode, no reverse recovery is observed during the transition between off- and on-states.

FOMs are used to compare materials/technologies and define their theoretical boundaries/ limitations. Some of these FOMs are important in the power electronics field in order to compare fairly devices and have a good indication of their performances [82–87]. These FOMs will be discussed herein, bringing insights for power electronics engineers about which characteristics should be taken into account when selecting active switches for project implementation. Firstly, the FOM shown in (2) compares the on-resistance of the device (R_{ds-on}) and the stored energy across the gate-source terminals (Q_g); hence, conduction and driver loss indicators are obtained for the analyzed device. As highlighted in Figure 9 and Table 2, both 650-V and 100-V GaN devices present better theoretical FOM1 compared with Si technology, and, consequently a better performance is expected in power electronics applications. This figure can be interpreted as follows: the closer the dots and/or regions are to the bottom-left corner, the better will be the performance of the semiconductor, since the device will present both lower conduction losses (related to the R_{ds-on} value) and driver losses (related to the gate charge energy Q_g). The dashed arrow in Figure 9 shows the difference between GaN devices packed in TO-220 [46] and state-of-the-art Si components [88–90]. The continuous line shows the distance between the SMD GaN devices [47,81] available on the market and the Si technology.

Proposed in [83], the FOM presented in (3) gives a good indication about the switching and conduction losses, since the energy stored at the output capacitance C_{oss} is dissipated at the channel of the device in hard-switching applications (modeling switching losses), and the on-resistance R_{ds-on} represents the conduction losses. Analyzing the data in Table 2, GaN devices present a better FOM and are a viable alternative for hard-switching applications with lower switching losses. Finally, the Power-Density-FOM (PDFOM), proposed in [84], is also an important FOM to be discussed, since it considers the package dimensions, together with the thermal and electrical characteristics of the semiconductors. As described in [84] and repeated herein for didactical reasons, Equation (4) brings a figure-of-merit that considers conduction (R_{ds-on}) and switching (Q_{gd}) losses (electrical characteristics), together with thermal resistance R_{thjc} (thermal characteristics) and package dimensions A_{pack} (size of the package). The higher the value returned by this FOM, the higher can be the power density of the converter, since a good compromise between all the aforementioned characteristics is achieved. This figure-of-merit is a good indicator of the fact that, considering the thermal resistance, losses and package dimensions, the size of the heat sink, one of the bulkiest components in a power electronics converter, can be estimated.

$$FOM1 = R_{ds-on} * Q_g \qquad [\Omega nC] \tag{2}$$

$$FOM2 = R_{ds-on} * C_{oss} \qquad [\Omega pF] \tag{3}$$

$$FOM3 = PDFOM = \frac{1}{\sqrt{R_{ds-on}Q_{gd}A_{pack}R_{thjc}}} \qquad \left[\frac{W}{(\Omega nC)^{\frac{1}{2}}(mm^2)K}\right] \tag{4}$$

Tash	Criteria												
iech.	Ref.	V (V)	I (A)	$R_{ds-on}\left(\Omega\right)$	Q_{rr} (nC)	Q_{gd} (nC)	C_{oss} (V)	Package (mm ²)	$R_{thjc}(\tfrac{K}{W})$	Q_g (nC)	FOM1	FOM2 [83]	FOM3 [84]
GaN	[46]	650	20	0.110	54	2.9	56	10.25×8.7	1.3	10	1.1	6.16	0.01527
GaN	[47]	650	22.5	0.067	0	1.3	49	5.55 imes 4.48	0.7	5.8	0.3886	3.283	0.19468
GaN	[81]	650	30	0.050	0	1.8	57	10.05 imes 8.68	0.5	5.8	0.29	2.85	0.07642
GaN	[35]	650	100	0.017	-	-	-	-	-	-	-	-	-
GaN	[48]	650	120	0.012	-	-	-	-	-	25	0.3	-	-
GaN	[91]	600	13	0.140	0	1	28	8 imes 8	1	2.0	0.28	3.92	0.02198
GaN	[92]	600	15	0.055	0	-	72	8 imes 8	1.1	5.8	0.319	3.96	-
GaN	[93]	600	26	0.056	0	2.6	71	8 imes 8	1.3	5.0	0.28	3.976	0.03149
GaN	[92]	600	31	0.055	0	-	72	15.9 imes 11	1	5.8	0.319	3.96	-
Si	[88]	650	20	0.150	8200	15	60	20 imes 15.5	0.74	35	5.25	9	0.0029
Si	[89]	650	20	0.150	5700	15	60	10.2 imes 9.15	0.74	35	5.25	9	0.00965
Si	[90]	650	20	0.124	10,000	18	75	8 imes 8	0.83	41.5	5.146	9.3	0.0126
GaN	[94]	100	45	0.015	0	0.9	140	4.6 imes 4.4	1.1	6.2	0.093	2.1	0.38657
GaN	[95]	100	48	0.004	0	2	800	4.6 imes 1	0.45	512	0.048	3.2	5.40
Si	[96]	100	45	0.0073	74	7.2	595	6.1 imes 5	1	36	0.2628	4.3435	0.143
Si	[97]	100	45	0.0051	150	16	992	10.2 imes 9.15	1	72	0.3672	5.0592	0.03751
Si	[98]	100	45	0.0145	67	12.2	360	10.2 imes 9.15	2.5	25	0.3625	5.22	0.01019

Table 2. Application KPIs for comparison of normally-on GaN, cascode GaN, normally-off GaN, and Si devices.



Figure 9. Comparison between GaN vs. Si components considering conduction and driver losses.

5. Conclusions

This paper summarized the challenges faced by power electronics engineers when it comes to GaN application in power electronics circuits. Important discussions related to the different GaN devices available on the market and their advantages and disadvantages were highlighted in the paper. Comparing the normally-on, cascode, and normally-off lateral devices, from an application point of view, the normally-off devices provide the best cost/benefit, since they present a lower internal parasitic component that enables the application at high frequencies with lower switching and conduction losses, although it is the device with the lowest immunity in the gate-source pins and lowest threshold voltage, which increase the driver and power stage layout complexity. Consequently, a careful power and signal design needs to be considered in order to achieve a noise immunity between the gate-source pins to neither experience shoot-through, nor achieve the breakdown voltage of the devices.

A comparison between GaN and Si technologies was also presented. Gallium nitride devices present better electrical characteristics and FOMs compared with Si-based MOSFETs. The SMD packages of GaN devices raise the thermal design challenge, since a device with a much smaller footprint might present higher temperatures and difficulties to extract the heat. A discussion related to this topic was addressed, showing some possible strategies to cool down the devices. Based on manufacturers' datasheet information, power electronics designers should carefully analyze some essential data provided (Table 2) to know if the package has good thermal transfer capability. Additionally, some FOMs were revised herein, giving the reader some indicators to define which semiconductor offers the best theoretical performance, considering conduction and switching losses, together with thermal transfer capability.

The thermal management and PCB layout should be carefully addressed during the design stage. As pointed out in Section 3.1.3, driver and power stage layouts are extremely important in order to achieve the best performance of GaN-based devices. Minimization of the parasitic inductances in both circuits is important. It was also mentioned that, due to a small margin between 0 V and the threshold voltage of the GaN devices, a negative voltage is recommended to pull-down the component, which increases the complexity of the driver stage and the challenge to minimize the parasitic inductances at the driver circuit.

Figures-of-merit were used to compare different GaN and Si components. These FOMs are important for converter designers to identify possible switches that are candidates to perform correctly within a specific project application. Devices were compared according to the PDFOM, a figure-of-merit that accounts for the electrical properties, thermal properties, and package dimensions. This FOM shows that even cascode GaN devices in TO-220 packages can perform better than SMD Si devices, since this FOM considers all aspects of the device (electrical, thermal, and dimensions).

Author Contributions: Conceptualization, M.D.V.; resources, J.D.; supervision, J.D.; writing, original draft, M.D.V.; writing, review and editing, S.R., G.V.d.B., and J.D.

Funding: G.V.d.B. was funded by a Ph.D. grant of the Research Foundation Flanders (FWO).

Conflicts of Interest: The authors declare no conflict of interest.

References

- Tan, D. Emerging System Applications and Technological Trends in Power Electronics: Power electronics is increasingly cutting across traditional boundaries. *IEEE Power Electron. Mag.* 2015, 2,38–47.10.1109/MPEL.2015.2422051. [CrossRef]
- Dulău, L.I.; Abrudean, M.; Bică, D. Automation of a distributed generation system. In Proceedings of the 2014 49th International Universities Power Engineering Conference (UPEC), Cluj-Napoca, Romania, 2–5 September 2014; pp. 1–5.10.1109/UPEC.2014.6934734. [CrossRef]
- 3. Wang, C.; Nehrir, M.H. Distributed Generation Applications of Fuel Cells. In Proceedings of the 2006 Power Systems Conference: Advanced Metering, Protection, Control, Communication, and Distributed Resources, Clemson, SC, USA, 14–17 March 2006; pp. 244–248.10.1109/PSAMP.2006.285395. [CrossRef]
- Chiradeja, P. Benefit of Distributed Generation: A Line Loss Reduction Analysis. In Proceedings of the 2005 IEEE/PES Transmission Distribution Conference Exposition: Asia and Pacific, Dalian, China, 18 August 2005; pp. 1–5.10.1109/TDC.2005.1546964. [CrossRef]
- Guerrero, J.M.; Berbel, N.; Matas, J.; de Vicuna, L.G.; Miret, J. Decentralized Control for Parallel Operation of Distributed Generation Inverters in Microgrids Using Resistive Output Impedance. In Proceedings of the IECON 2006—32nd Annual Conference on IEEE Industrial Electronics, Paris, France, 6–10 November 2006; pp. 5149–5154.10.1109/IECON.2006.347859. [CrossRef]
- Du, W.; Chen, Z.; Wang, H.F.; Dunn, R. Energy storage systems applied in power system stability control. In Proceedings of the 2007 42nd International Universities Power Engineering Conference, Brighton, UK, 4–6 September 2007; pp. 455–458.10.1109/UPEC.2007.4468989. [CrossRef]
- Ma, Y.; Chen, Y. Storage Systems Management Based on Big Data—Take Three Common Storage Systems as Examples. In Proceedings of the 2018 15th International Conference on Service Systems and Service Management (ICSSSM), Hangzhou, China, 21–22 July 2018; pp. 1–6.10.1109/ICSSSM.2018.8464963. [CrossRef]
- 8. Fei, C.; Lee, F.C.; Li, Q. High-Efficiency High-Power-Density LLC Converter With an Integrated Planar Matrix Transformer for High-Output Current Applications. *IEEE Trans. Ind. Electron.* 2017, 64, 9072–9082.10.1109/TIE.2017.2674599. [CrossRef]
- 9. Huang, Q.; Huang, A.; Yu, R.; Liu, P.; Yu, W. High-Efficiency and High-Density Single-Phase Dual-Mode Cascaded Buck-Boost Multilevel Transformerless PV Inverter with GaN AC Switches. *IEEE Trans. Power Electron.* **2018**, doi:10.1109/TPEL.2018.2878586. [CrossRef]
- 10. Chen, R.; Yu, S. A high-efficiency high-power-density 1 MHz LLC converter with GaN devices and integrated transformer. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 791–796.10.1109/APEC.2018.8341102. [CrossRef]
- Ravyts, S.; Dalla Vecchia, M.; Zwysen, J.; van den Broeck, G.; Driesen, J. Comparison Between an Interleaved Boost Converter Using Si MOSFETs Versus GaN HEMTs. In Proceedings of the PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 5–7 June 2018; pp. 1–8.
- Shamsi, P.; McDonough, M.; Fahimi, B. Wide-Bandgap Semiconductor Technology: Its impact on the electrification of the transportation industry. *IEEE Electrif. Mag.* 2013, *1*, 59–63.10.1109/MELE.2013.2293931. [CrossRef]
- Bindra, A. Wide-Bandgap Power Devices: Adoption Gathers Momentum. *IEEE Power Electron. Mag.* 2018, 5, 22–27.10.1109/MPEL.2017.2782404. [CrossRef]
- 14. Dawon, K. Electric Field Controlled Semiconductor Device. U.S. Patent US3102230A, 27 August 1963.

- Andersen, T.M.; Krismer, F.; Kolar, J.W.; Toifl, T.; Menolfi, C.; Kull, L.; Morf, T.; Kossel, M.; Brändli, M.; Francese, P.A. Modeling and Pareto Optimization of On-Chip Switched Capacitor Converters. *IEEE Trans. Power Electron.* 2017, *32*, 363–377.10.1109/TPEL.2016.2529501. [CrossRef]
- 16. Lefranc, P.; Odic, E.; Kirkpatrick, M.J. Optimisation and characterisation of a planar transformer with a high voltage ratio and high output voltage for plasma reactors. *IET Power Electron.* **2015**, *8*, 929–937.10.1049/iet-pel.2014.0139. [CrossRef]
- Bosshard, R.; Kolar, J.W.; Mühlethaler, J.; Stevanović, I.; Wunsch, B.; Canales, F. Modeling and η-α-Pareto Optimization of Inductive Power Transfer Coils for Electric Vehicles. *IEEE J. Emerg. Sel. Top. Power Electron.* 2015, 3, 50–64.10.1109/JESTPE.2014.2311302. [CrossRef]
- Boillat, D.O.; Krismer, F.; Kolar, J.W. Design Space Analysis and *ρ* η Pareto Optimization of *LCO* utput Filters for Switch-Mode AC Power Sources. *IEEE Trans. Power Electron.* 2015, 30, 6906–6923.10.1109/TPEL.2015.2393151. [CrossRef]
- 19. Baliga, B.J. Semiconductors for high-voltage, vertical channel field-effect transistors. *J. Appl. Phys.* **1982**, 53, 1759–1764.10.1063/1.331646. [CrossRef]
- 20. Baliga, B.J. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Dev. Lett.* **1989**, *10*, 455–457.10.1109/55.43098. [CrossRef]
- 21. Chow, T.P.; Omura, I.; Higashiwaki, M.; Kawarada, H.; Pala, V. Smart Power Devices and ICs Using GaAs and Wide and Extreme Bandgap Semiconductors. *IEEE Trans. Electron Dev.* **2017**, *64*, 856–873.10.1109/TED.2017.2653759. [CrossRef]
- 22. Hudgins, J.L.; Simin, G.S.; Santi, E.; Khan, M.A. An assessment of wide band gap semiconductors for power devices. *IEEE Trans. Power Electron.* 2003, *18*, 907–914.10.1109/TPEL.2003.810840. [CrossRef]
- 23. Shenai, K. Future Prospects of Wideband gap (WBG) Semiconductor Power Switching Devices. *IEEE Trans. Electron Dev.* **2015**, *62*, 248–257.10.1109/TED.2014.2360641. [CrossRef]
- 24. Lidow, A.; Strydom, J.; De Rooij, M.; Reusch, D. *GaN Transistors for Efficient Power Conversion*, 1st ed.; Wiley: Hoboken, NJ, USA, 2015.
- Park, B.; Han, S.; Cha, H. Diode Bridge Embedded AlGaN/GaN Bidirectional Switch. *IEEE Electron Dev. Lett.* 2015, 36, 324–326.10.1109/LED.2015.2398459. [CrossRef]
- Mehrotra, V.; Arias, A.; Neft, C.; Bergman, J.; Urteaga, M.; Brar, B. GaN HEMT-Based> 1-GHz Speed Low-Side Gate Driver and Switch Monolithic Process for 865-MHz Power Conversion Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* 2016, 4, 918–925.10.1109/JESTPE.2016.2564946. [CrossRef]
- Wang, X.; Mazumder, S.K.; Shi, W. A GaN-Based Insulated-Gate Photoconductive Semiconductor Switch for Ultrashort High-Power Electric Pulses. *IEEE Electron Dev. Lett.* 2015, *36*, 493–495.10.1109/LED.2015.2416188. [CrossRef]
- Ren, J.; Liu, C.; Tang, C.W.; Lau, K.M.; Sin, J.K.O. Switching characteristics of monolithically integrated Si-GaN cascoded rectifiers. In Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, Japan, 28 May–1 June 2017; pp. 223–226.10.23919/ISPSD.2017.7988928. [CrossRef]
- Horikiri, F.; Narita, Y.; Yoshida, T.; Kitamura, T.; Ohta, H.; Nakamura, T.; Mishima, T. Wafer-Level Donor Uniformity Improvement by Substrate Off-Angle Control for Vertical GaN-on-GaN Power Switching Devices. *IEEE Trans. Semicond. Manuf.* 2017, 30, 486–493.10.1109/TSM.2017.2745504. [CrossRef]
- Ruzzarin, M.; Meneghini, M.; Bisi, D.; Sun, M.; Palacios, T.; Meneghesso, G.; Zanoni, E. Instability of Dynamic-R_{ON} and Threshold Voltage in GaN-on-GaN Vertical Field-Effect Transistors. *IEEE Trans. Electron Dev.* 2017, 64, 3126–3131.10.1109/TED.2017.2716982. [CrossRef]
- 31. Han, S.; Noh, Y.; Jo, M.; Kim, S.; Oh, J.; Seo, K.; Cha, H. Normally-Off MOS-HFET on AlGaN/GaN-on-Si(110) Grown by NH3MBE. *IEEE Electron Dev. Lett.* **2016**, *37*, 1613–1616.10.1109/LED.2016.2621184. [CrossRef]
- Medjdoub, F.; Hove, M.V.; Cheng, K.; Marcon, D.; Leys, M.; Decoutere, S. Novel E-Mode GaN-on-Si MOSHEMT Using a Selective Thermal Oxidation. *IEEE Electron Dev. Lett.* 2010, 31, 948–950.10.1109/LED.2010.2052014. [CrossRef]
- 33. Cao, L.; Lo, C.; Marchand, H.; Johnson, W.; Fay, P. Low-Loss Coplanar Waveguides on GaN-on-Si Substrates. *IEEE Microw. Wirel. Compon. Lett.* **2018**, *28*, 861–863. [CrossRef]

- Dong, M.; Elmes, J.; Peper, M.; Batarseh, I.; Shen, Z.J. Investigation on inherently safe gate drive techniques for normally-on wide band gap power semiconductor switching devices. In Proceedings of the 2009 IEEE Energy Conversion Congress and Exposition, San Jose, CA, USA, 20–24 September 2009; pp. 120–125.10.1109/ECCE.2009.5316342. [CrossRef]
- Vecchia, M.D.; den Broeck, G.V.; Ravyts, S.; Driesen, J. Application of a 100 A normally-on GaN-based device in a 2 kW/400 V input half-bridge non-isolated DC-DC configuration. In Proceedings of the 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 30 October–1 November 2017; pp. 111–115.10.1109/WiPDA.2017.8170531. [CrossRef]
- Okamoto, M.; Tanaka, T.; Matuzaki, K.; Hashizume, T.; Yamada, H. 13.56-MHz Class-E RF power amplifier using normally-on GaN HEMT. In Proceedings of the IECON 2014—40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014; pp. 982–987.10.1109/IECON.2014.7048621. [CrossRef]
- 37. Jacqmaer, P.; Everts, J.; Gelagaev, R.; Tant, P.; Driesen, J. Fast robust gate-drivers with easily adjustable voltage ranges for driving normally-on wide-band gap power transistors. In Proceedings of the 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010, Ohrid, Macedonia, 6–8 September 2010; pp. T2-44–T2-51.10.1109/EPEPEMC.2010.5606912. [CrossRef]
- 38. Okamoto, M.; Ishibashi, T.; Yamada, H.; Tanaka, T. Resonant Gate Driver for a Normally ON GaN HEMT. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 926–934.10.1109/JESTPE.2016.2587058. [CrossRef]
- Ishibashi, T.; Okamoto, M.; Hiraki, E.; Tanaka, T.; Hashizume, T.; Kikuta, D.; Kachi, T. Experimental validation of newly fabricated normally-on GaN high-electron-mobility transistor. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013; pp. 1584–1591.10.1109/ECCE.2013.6646894. [CrossRef]
- Ishibashi, T.; Okamoto, M.; Hiraki, E.; Tanaka, T.; Hashizume, T.; Kikuta, D.; Kachi, T. Experimental Validation of Normally-On GaN HEMT and Its Gate Drive Circuit. *IEEE Trans. Ind. Appl.* 2015, 51, 2415–2422.10.1109/TIA.2014.2369818. [CrossRef]
- Zhang, W.; Huang, X.; Liu, Z.; Lee, F.C.; She, S.; Du, W.; Li, Q. A New Package of High-Voltage Cascode Gallium Nitride Device for Megahertz Operation. *IEEE Trans. Power Electron.* 2016, 31, 1344–1353.10.1109/TPEL.2015.2418572. [CrossRef]
- 42. Liu, Z.; Huang, X.; Lee, F.C.; Li, Q. Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT. *IEEE Trans. Power Electron.* 2014, 29, 1977–1985.10.1109/TPEL.2013.2264941. [CrossRef]
- Li, H.; Zhang, X.; Wen, L.; Brothers, J.A.; Yao, C.; Han, C.; Liu, L.; Xu, J.; Puukko, J.; Wang, J. Paralleled Operation of High-Voltage Cascode GaN HEMTs. *IEEE J. Emerg. Sel. Top. Power Electron*. 2016, 4, 815–823.10.1109/JESTPE.2016.2557316. [CrossRef]
- 44. Jung, D.Y.; Park, Y.; Lee, H.S.; Jun, C.H.; Jang, H.G.; Park, J.; Kim, M.; Ko, S.C.; Nam, E.S. Design and Evaluation of Cascode GaN FET for Switching Power Conversion Systems. *ETRI J.* **2017**, *39*, 62–68. [CrossRef]
- 45. Chellappan, S. Design Considerations of GaN Devices for Improving Power Converter Efficiency; Texas Instruments Inc.: Dallas, TX, USA, 2017.
- 46. Transphorm GaN Power FET Portfolio. Available online: https://www.transphormusa.com/en/products/ (accessed on 5 December 2018).
- 47. GS66506T. Available online: https://gansystems.com/gan-transistors/gs66506t/ (accessed on 6 November 2018).
- 48. GS-065-120-1-D. Available online: https://gansystems.com/gan-transistors/gs-065-120-1-d/ (accessed on 6 November 2018).
- Mueller, C.R.; Buschhorn, S. Impact of module parasitics on the performance of fastswitching devices. In Proceedings of the PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 20–22 May 2014; pp. 1–8.
- 50. Zhang, Z.; Guo, B.; Wang, F. Evaluation of Switching Loss Contributed by Parasitic Ringing for Fast Switching Wide Band-Gap Devices. *IEEE Trans. Power Electron.* **2018**, doi:10.1109/TPEL.2018.2883454. [CrossRef]
- 51. Reusch, D. Impact of Parasitics on Performance. 2013. p. 5. Avaliable online: https://epc-co.com/epc/ Portals/0/epc/documents/papers/ImpactofParasitcsonPerformance.pdf (accessed on 17 December 2018).

- 52. Lu, J.; Bai, H.; Brown, A.; McAmmond, M.; Chen, D.; Styles, J. Design consideration of gate driver circuits and PCB parasitic parameters of paralleled E-mode GaN HEMTs in zero-voltage-switching applications. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 529–535.10.1109/APEC.2016.7467923. [CrossRef]
- Nayak, P.; Hatua, K. Parasitic Inductance and Capacitance-Assisted Active Gate Driving Technique to Minimize Switching Loss of SiC MOSFET. *IEEE Trans. Ind. Electron.* 2017, 64, 8288–8298.10.1109/TIE.2017.2711512. [CrossRef]
- 54. Huang, X.; Li, Q.; Liu, Z.; Lee, F.C. Analytical loss model of high voltage GaN HEMT in cascode configuration. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013; pp. 3587–3594.10.1109/ECCE.2013.6647173. [CrossRef]
- 55. Huang, X.; Li, Q.; Liu, Z.; Lee, F.C. Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration. *IEEE Trans. Power Electron.* **2014**, *29*, 2208–2219.10.1109/TPEL.2013.2267804. [CrossRef]
- Lidow, A.; Strydom, J.; Strittmatter, R.; Zhou, C. GaN: A Reliable Future in Power Conversion: Dramatic performance improvements at a lower cost. *IEEE Power Electron. Mag.* 2015, 2, 20–26.10.1109/MPEL.2014.2381457. [CrossRef]
- 57. Wang, J.; Chung, H.S.H. Impact of Parasitic Elements on the Spurious Triggering Pulse in Synchronous Buck Converter. *IEEE Trans. Power Electron.* **2014**, *29*, 6672–6685.10.1109/TPEL.2014.2304454. [CrossRef]
- 58. Index of/Application-Notes/AN. Available online: https://www.fairchildsemi.com/application-notes/ AN/ (accessed on 2 January 2019).
- Tibola, G.; Lemmen, E.; Duarte, J.L.; Barbi, I. Passive Regenerative and Dissipative Snubber Cells for Isolated SEPIC Converters: Analysis, Design, and Comparison. *IEEE Trans. Power Electron.* 2017, 32, 9210–9222.10.1109/TPEL.2017.2653940. [CrossRef]
- Finney, S.J.; Williams, B.W.; Green, T.C. RCD snubber revisited. *IEEE Trans. Ind. Appl.* 1996, 32, 155–160.10.1109/28.485827. [CrossRef]
- Yatsugi, K.; Nomura, K.; Hattori, Y. Analytical Technique for Designing an RC Snubber Circuit for Ringing Suppression in a Phase-Leg Configuration. *IEEE Trans. Power Electron.* 2018, 33, 4736–4745.10.1109/TPEL.2017.2731421. [CrossRef]
- Ujita, S.; Kinoshita, Y.; Umeda, H.; Morita, T.; Kaibara, K.; Tamura, S.; Ishida, M.; Ueda, T. A fully integrated GaN-based power IC including gate drivers for high-efficiency DC-DC Converters. In Proceedings of the 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2.10.1109/VLSIC.2016.7573496. [CrossRef]
- Cool-Power ZVS Buck Regulators. Available online: http://www.vicorpower.com/dc-dc-converters-boardmount/cool-power-pi33xx-and-pi34xx (accessed on 17 December 2018).
- 64. LMG3410R070 600-V 70 mΩ GaN With Integrated Driver and Protection | TI.com. Available online: http://www.ti.com/product/LMG3410R070 (accessed on 18 December 2018).
- 65. EPC2115: Dual 150 V, 5 A Integrated Gate Drivers eGaN IC. Available online: https://epc-co.com/epc/ Products/eGaNFETsandICs/EPC2115.aspx (accessed on 17 December 2018).
- 66. Choi, S.; Heller, E.R.; Dorsey, D.; Vetury, R.; Graham, S. The Impact of Bias Conditions on Self-Heating in AlGaN/GaN HEMTs. *IEEE Trans. Electron Dev.* **2013**, *60*, 159–162.10.1109/TED.2012.2224115. [CrossRef]
- 67. Yang, L.; Chen, Z.; Xu, X.; Zhang, J. Study on the Heat Transfer of GaN-Based High Power HEMTs. *IEEE Trans. Semicond. Manuf.* **2017**, *30*, 526–530.10.1109/TSM.2017.2739134. [CrossRef]
- AlOtaibi, B.; Valizadeh, P. Investigation of the High-Temperature Operation of AlGaN/GaN HFETs via Studying the Impact of Temperature Dependency of Drift Transport Characteristics. *IEEE Trans. Dev. Mater. Reliab.* 2012, 12, 547–553.10.1109/TDMR.2012.2187901. [CrossRef]
- Lu, X.; Ma, J.; Yue, C.P.; Lau, K.M. A GaN-Based Lamb-Wave Oscillator on Silicon for High-Temperature Integrated Sensors. *IEEE Microw. Wirel. Compon. Lett.* 2013, 23, 318–320.10.1109/LMWC.2013.2260734. [CrossRef]
- 70. Maier, D.; Alomari, M.; Grandjean, N.; Carlin, J.; Diforte-Poisson, M.; Dua, C.; Chuvilin, A.; Troadec, D.; Gaquiere, C.; Kaiser, U.; et al. Testing the Temperature Limits of GaN-Based HEMT Devices. *IEEE Trans. Dev. Mater. Reliab.* 2010, 10, 427–436.10.1109/TDMR.2010.2072507. [CrossRef]
- Cuerdo, R.; Sillero, E.; Romero, M.F.; Uren, M.J.; di Forte Poisson, M.; Munoz, E.; Calle, F. High-Temperature Microwave Performance of Submicron AlGaN/GaN HEMTs on SiC. *IEEE Electron Dev. Lett.* 2009, 30, 808–810.10.1109/LED.2009.2024964. [CrossRef]

- 72. Roder, C.; Einfeldt, S.; Figge, S.; Hommel, D. Temperature dependence of the thermal expansion of GaN. *Phys. Rev. B* 2005, 72, 085218.10.1103/PhysRevB.72.085218. [CrossRef]
- 73. Bernard, K. Advantages of Using Gallium NitrideFETs in Satellite Applications; Renesas: Tokyo, Japan, 2018.
- 74. Ando, Y.; Ishikura, K.; Murase, Y.; Asano, K.; Takenaka, I.; Takahashi, S.; Takahashi, H.; Sasaoka, C. Impact of Epi-Layer Quality on Reliability of GaN/AlGaN/GaN Heterostructure Field-Effect Transistors on Si Substrate. *IEEE Trans. Electron Dev.* 2013, 60, 4125–4132.10.1109/TED.2013.2284285. [CrossRef]
- 75. Lee, C.; Witkowski, L.; Tserng, H.; Saunier, P.; Birkhahn, R.; Olson, D.; Olson, D.; Munns, G.; Guo, S.; Albert, B. Effects of AlGaN/GaN HEMT structure on RF reliability. *Electron. Lett.* 2005, 41, 155–157.10.1049/el:20057802. [CrossRef]
- Zanoni, E.; Meneghini, M.; Chini, A.; Marcon, D.; Meneghesso, G. AlGaN/GaN-Based HEMTs Failure Physics and Reliability: Mechanisms Affecting Gate Edge and Schottky Junction. *IEEE Trans. Electron Dev.* 2013, 60, 3119–3131.10.1109/TED.2013.2271954. [CrossRef]
- 77. Kwan, A.M.H.; Chen, K.J. A Gate Overdrive Protection Technique for Improved Reliability in AlGaN/GaN Enhancement-Mode HEMTs. *IEEE Electron Dev. Lett.* **2013**, *34*, 30–32.10.1109/LED.2012.2224632. [CrossRef]
- Sun, H.; Pomeroy, J.W.; Simon, R.B.; Francis, D.; Faili, F.; Twitchen, D.J.; Kuball, M. Temperature-Dependent Thermal Resistance of GaN-on-Diamond HEMT Wafers. *IEEE Electron Dev. Lett.* 2016, *37*, 621–624.10.1109/LED.2016.2537835. [CrossRef]
- 79. Chou, H.P.; Ho, C.H.; Cheng, Y.J.; Chou, P.C.; Cheng, S. A new high power device of GaN HEMTs on Si substrate with lateral heat dissipation packaging. In Proceedings of the 2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), Kyoto, Japan, 10–13 June 2012; pp. 1–5.10.1109/COMPEL.2012.6251752. [CrossRef]
- Yu, C.; Labouré; Buttay, C. Thermal management of lateral GaN power devices. In Proceedings of the 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), Chicago, IL, USA, 3–6 May 2015; pp. 40–43.10.1109/IWIPP.2015.7295973. [CrossRef]
- 81. GS66508P. Available online: https://gansystems.com/gan-transistors/gs66508p/ (accessed on 9 November 2018).
- 82. Shenai, K. The Figure of Merit of a Semiconductor Power Electronics Switch. *IEEE Trans. Electron Dev.* **2018**, 65, 4216–4224.10.1109/TED.2018.2866360. [CrossRef]
- Kim, I.J.; Matsumoto, S.; Sakai, T.; Yachi, T. New power device figure of merit for high-frequency applications. In Proceedings of the International Symposium on Power Semiconductor Devices and IC's: ISPSD '95, Yokohama, Japan, 23–25 May 1995; pp. 309–314.10.1109/ISPSD.1995.515055. [CrossRef]
- Wang, H.; Wang, F.; Zhang, J. Power Semiconductor Device Figure of Merit for High-Power-Density Converter Design Applications. *IEEE Trans. Electron Dev.* 2008, 55, 466–470.10.1109/TED.2007.910573. [CrossRef]
- 85. Huang, A.Q. New unipolar switching power device figures of merit. *IEEE Electron Dev. Lett.* 2004, 25, 298–301.10.1109/LED.2004.826533. [CrossRef]
- 86. Keyes, R.W. Figure of merit for semiconductors for high-speed switches. *Proc.* IEEE 1972, 60, 225–225.10.1109/PROC.1972.8593. [CrossRef]
- De Vreede, L.C.N.; de Graaff, H.C.; Hurkx, G.A.M.; Tauritz, J.L.; Baets, R.G.F. A figure of merit for the high-frequency noise behavior of bipolar transistors. *IEEE J. Solid-State Circuits* 1994, 29, 1220–1226.10.1109/4.315206. [CrossRef]
- 88. STW28N65M2 STMicroelectronics | Mouser. Available online: https://www.mouser.be/ProductDetail/511-STW28N65M2 (accessed on 8 November 2018).
- 89. STF28N65M2 STMicroelectronics | Mouser. Available online: https://www.mouser.be/ProductDetail/511-STF28N65M2 (accessed on 8 November 2018).
- 90. STL33N65M2 STMicroelectronics | Mouser. Available online: https://www.mouser.be/ProductDetail/511-STL33N65M2 (accessed on 8 November 2018).
- 91. PGA26E19BA Product Overview. Available online: https://www.mouser.be/datasheet/2/315/pga26e19ba-product-standards-1112740.pdf (accessed on 30 November 2018).
- AG, I.T. Gallium Nitride (GaN)—Infineon Technologies. Available online: https://www.infineon.com/ cms/en/product/power/wide-band-gap-semiconductors-sic-gan/gallium-nitride-gan/ (accessed on 30 November 2018).

- 93. PGA26E07BA Product Overview. Available online: https://www.mouser.be/datasheet/2/315/pga26e07ba-product-standards-1112741.pdf (accessed on 30 November 2018).
- 94. GS61004B. Available online: https://gansystems.com/gan-transistors/gs61004b/ (accessed on 8 November 2018).
- 95. EPC2032. Available online: https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2032.aspx (accessed on 8 November 2018).
- 96. FDMS86152 ON Semiconductor/Fairchild|Mouser. Available online: https://www.mouser.be/ ProductDetail/512-FDMS86152 (accessed on 8 November 2018).
- 97. STF110N10F7 STMicroelectronics | Mouser. Available online: https://www.mouser.be/ProductDetail/511-STF110N10F7 (accessed on 8 November 2018).
- 98. STI45N10F7 STMicroelectronics | Mouser. Available online: https://www.mouser.be/ProductDetail/511-STI45N10F7 (accessed on 8 November 2018).



 \odot 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).