energies

MDPI

Article

Wide Load Range Capacitor Clamped ZVZCS Half Bridge Three-Level DC-DC Converter with Two Unsymmetrical Bi-directional Switches

Yong Shi

School of Electrical and Control Engineering, Shaanxi University of Science and Technology, Xi'an 710021, China; shiyong@sust.edu.cn; Tel.: +86-13891884297

Received: 27 May 2019; Accepted: 17 June 2019; Published: 19 June 2019

Abstract: This paper presents a zero-voltage and zero-current switching (ZVZCS) capacitor-clamped half bridge (HB) three-level dc-dc converter (TLDC), which is well fit for high input voltage dc-dc industrial applications. The maximum voltage stress of the primary switches is limited by the flying capacitor and input capacitors, which is very close to $V_{in}/2$. Two unsymmetrical bidirectional switches are used to replace two of the primary switches in a conventional capacitor-clamped HB TLDC, which ensure ZVZCS of the main switches in wide load range. The reverse direction MOSFETs in the unsymmetrical bidirectional switches have low on-state resistance and are controlled with soft-switching mode irrelevant to the load current. Therefore, the additional power loss can be omitted. The current of the flying capacitor is greatly reduced due to ZVZCS operation, which would result in a smaller volume flying capacitor and high system reliability. Furthermore, the current imbalance problem of the power devices is also well solved. The circuit, basic operation principles and some important technical analyses are discussed in this paper, and experimental results from a 1-kW prototype are provided to evaluate the proposed converter.

Keywords: three-level dc-dc converter; ZVZCS; capacitor clamped; balanced current distribution

1. Introduction

Three-level (TL) dc-dc converters (TLDCs) can be widely used in plenty of existing and upcoming industrial applications, e.g., dc-dc converters for distributed power systems, micro-grids, renewable energy power systems, and electric vehicles [1–4]. The most outstanding attribute of TLDC is reduced voltage stress of the primary switches, and both dynamic and static voltages on the main switches can be confined below $V_{in}/2$ by the clamping devices, such as clamping diodes or capacitors. After diode-clamped TLDC was proposed in 1992, several good studies on this topic have been carried out, which are new topologies, wide load range soft-switching techniques, reduced volume of passive components methods, and new control strategies [5–21]. Several TLDCs were proposed in Reference [5], and most existing TLDCs are invented based on these topologies. A secondary active reset zero-voltage and zero-current switching (ZVZCS) TLDC was reported in Reference [6], wherein an extra capacitor is added to the primary side to realize a phase-shift (PS) switching scheme. In Reference [6], the extra capacitor provides a zero-voltage switching (ZVS) quasi-resonant path for the outer switches and a secondary clamping circuit is adopted to provide zero-current switching (ZCS) for the inner switches. In Reference [7], a passive snubber is series-connected with the primary coil of the transformer to generate reset voltage of the primary current, and two diodes are used to prevent a negative primary current during the free-wheeling stages. Some other new TLDCs were reported in References [8–14], which have different attractive characteristics. To reduce the volume of the passive filter, lots of TLDCs with TL secondary-rectified voltage waveforms were proposed. In Reference [15], a hybrid TLDC

was proposed, which can generate TL secondary waveform before the output filter. A hybrid ZVZCS TLDC was proposed in Reference [16], which can achieve TL secondary rectified waveform as well as a wide soft switching load range. A ZVZCS TLDC with no primary clamping devices was proposed in Reference [17], which has a simpler primary structure. A TLDC with four switches was proposed, which has the minimum primary switches to generate a TL secondary-rectified waveform [18]. Other TLDCs with reduced volume of the output filter were reported in References [19,20]. To improve the reliability of TLDCs, some detailed analyses about current imbalanced problems of the primary components are investigated [21–23]. All mentioned references have made TLDCs more applicable.

Figure 1a shows a capacitor-clamped half bridge (HB)TLDC, and the four switches in Figure 1a are switched in the asymmetrical PWM (APWM) method to achieve balanced voltage on the input and flying capacitors. As depicted in Figure 1a, only one flying capacitor is parallel connected with HB cells, which would minimize the space of the circuit loop among C_{in1}, C_{in2}, and Q_1 to Q_4 in a real product. Hence, the parasitic inductance caused by this circuit loop would be small, which suppresses the voltage spike on the primary switches at turn-off instants. The voltage stress of the main switches is restricted by C_s, and this capacitor would absorb more energy stored in the parasitic inductances of the primary circuit. Therefore, all the primary switches can be well confined in the safe operation area (SOA). In addition, widely-used two-level HB power modules can be adopted in the proposed converter, which makes this topology more convenient for industrial users.

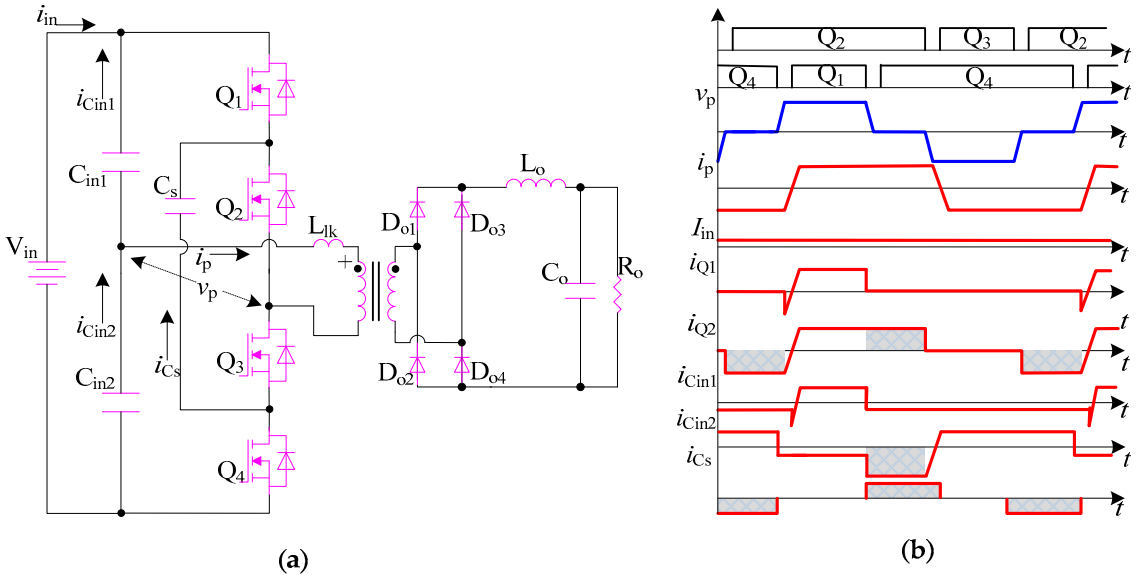

Figure 1. Capacitor-clamped HB TLDC and its key waveforms: (**a**) Circuit; (**b**) Key waveforms.

However, some drawbacks of the converter in Figure 1a should be overcome. First, as illustrated in Figure 1b, i_{Q1} and i_{Q2} are imbalanced due to an asymmetrical switching sequence, which causes some design obstacles for the power devices. Furthermore, with a decrease of the duty ratio, the imbalanced degree of the current distribution among Q_1 to Q_4 is more serious, which would affect the reliability of the converter. Second, the current distribution of C_{in1} and C_{in2} is also imbalanced, and the RMS value of i_{Cin2} is clearly higher than that of i_{Cin1} under a small duty ratio. High current stress leads high operation temperature, and it is well known that the life expectancy of film or an AL electrolytic capacitor is inversely proportional to the operation temperature. Therefore, the reliability of the converter would also be reduced. Third, i_p flows through C_s during the freewheeling stages, which would cause thermal problems of C_s. In addition, a large value capacitance of C_s is required to minimize the voltage ripple on it, which increases the volume of C_s. Finally, Q_1 and Q_3 cannot achieve zero-voltage switching in a wide load range due to less energy reserved in L_{lk}. New capacitor-clamped TLDC without the above-mentioned drawbacks is an interesting problem.

This paper proposes a novel ZVZCS capacitor-clamped HB TLDC, which overcomes all abovementioned shortcomings. In addition, all above features can be achieved with a simple switching sequence. The outline of this paper is concluded as follows. In part 1, the circuit is described, and detailed analysis about the operation principle is presented. Some technique aspects are analyzed in part 2. In part 3, experimental results are provided and analyzed, and some brief conclusions are given in the final part.

2. Circuits and Principle of Operation

Figure 2 shows the proposed ZVZCS HB TLDC, and two unsymmetrical bi-directional switches are replaced by Q_2 and Q_4 in Figure 1a. The unsymmetrical bi-directional switches can conduct a bi-directional current with the same value and sustain different bi-directional voltage. After introducing the unsymmetrical bi-directional switches, the currents of S_2 and S_4 can be controlled as a positive value, negative value or zero freely. Consequently, the converter with APWM switching scheme can also achieve ZVZCS operation. The remaining circuit is identical to that of the converter in Figure 1a, which is not described in detail.

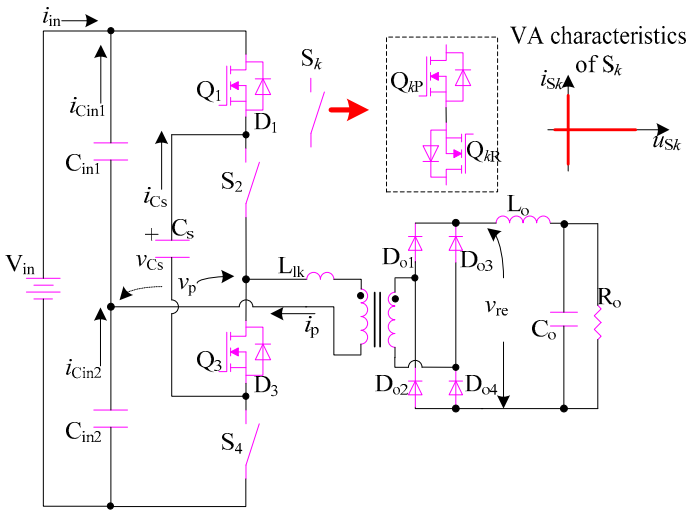

Figure 2. Proposed capacitor-clamped ZVZCS HB TLDC.

Figure 3 shows the waveforms of the proposed converter, and identical circuits over one-half switching period are given in Figure 4. To simplify the analysis, some assumptions are given: all components have ideal characteristics; C_{in1} and C_{in2} are the input capacitors with a certain value, which could reset i_p properly during the operation as well as transfer energy to the load; S_k is replaced by Q_{kP} and Q_{kR} in Figures 3 and 4; $\Delta v_{Cin2} = V_{in}/2 - v_{Cin2}$; the current ripple of L_o is neglected, and i_{Lo} is represented by I_o.

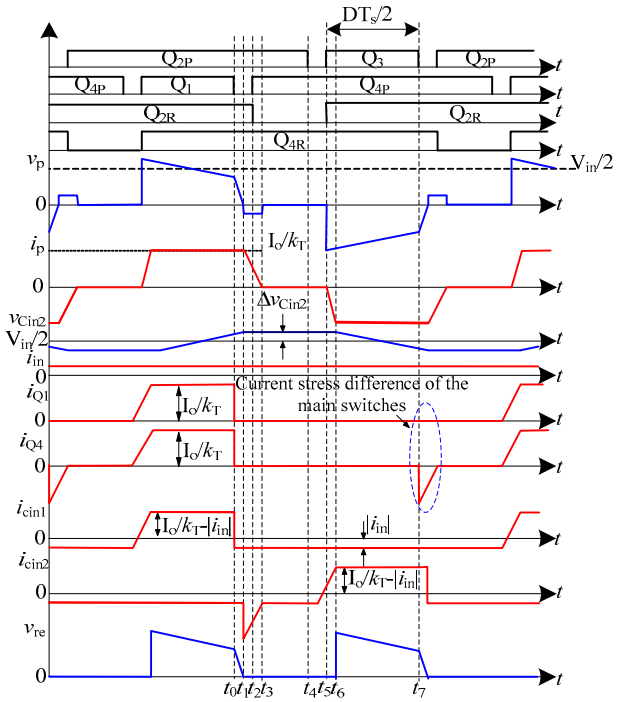

Figure 3. Key waveforms.

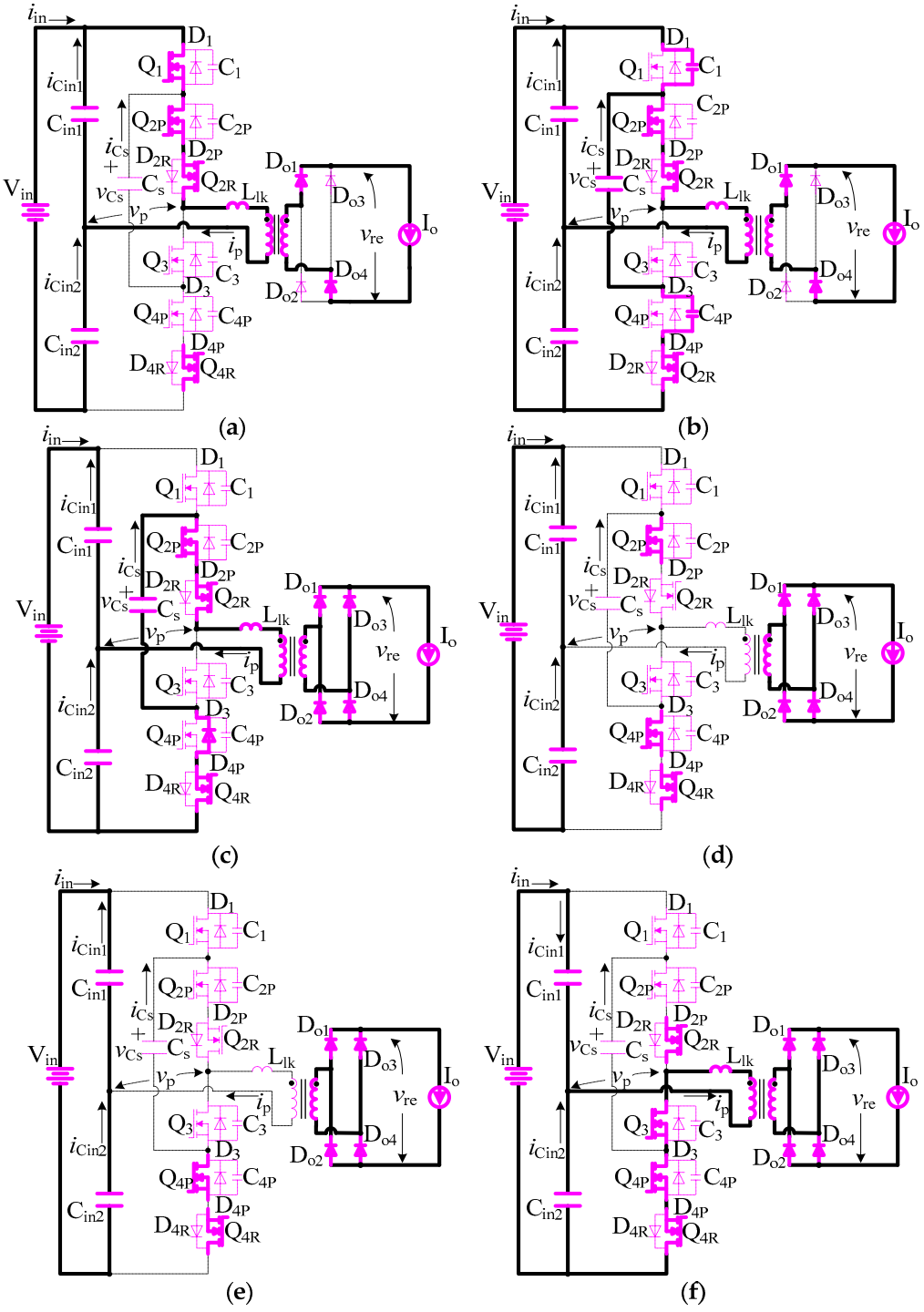

Figure 4. Identical circuits: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; (**f**) Mode 6.

Mode 1 [Figure 4a, before t_0]: Q_1 and Q_{2P} are on; energy is transferred from the primary side to the load; Q_{2R} and Q_{4R} are also on, D_{o1} and D_{o4} are conducted. v_{Cin2} increases with the rate of

$$\frac{dv_{Cin2}}{dt} = \frac{I_o - k_T|i_{in}|}{k_T C_{in1}} - \frac{|i_{in}|}{C_{in2}} \quad (1)$$

During this stage, $v_p = V_{in}/2 - \Delta v_{Cin2}$; $v_{re} = (V_{in} - 2\Delta v_{Cin2})/2k_T$; $i_p = I_o/k_T$; $i_{Cin1} = I_o/k_T - |i_{in}|$, $i_{Cin2} = -|i_{in}|$; $v_{Q3} = v_{Q4P} = V_{in}/2$. Although Q_{4R} is on, i_{Q4R} is zero owing to Q_{4P} is off.

Mode 2 [Figure 4b, t_0–t_1]: At t_0, Q_1 is off, and v_{Q1} cannot change sharply due to C_1; v_{Cin2} increases, and reaches $V_{Cin2max}$ at the end of this mode. $i_p = I_o/k_T$, and charges C_1 and discharges C_{4P} through C_s. This stage continues until $v_{C1} = V_{in}/2$ and $v_{C4P} = 0$. $i_{Cin1} = -|i_{in}|$, $i_{Cin2} = -I_o/k_T - |i_{in}|$. v_{Q3} is v_{Cs}, which is identical to $V_{in}/2$. v_{Q1} and v_{Q4P} are smaller than $V_{in}/2$.

Mode 3 [Figure 4c, t_1–t_3]: At t_1, D_{4P} conducts naturally and I_o is free-wheeled through secondary rectifier diodes. After t_1, Q_{4P} should be triggered on to ensure zero-voltage operation, and as proved in Figure 3, Q_{4P} is on with zero-voltage at t_2. Q_{2R} is also turned off at t_2. As D_{2R} conducts naturally, Q_{2R} can achieve zero-voltage turn-off. v_{Cin2} is $V_{Cin2MAX}$, and $V_{Cin2MAX} - V_{in}/2$ is fully applied to L_{lk} to reset i_p, and i_p is

$$i_p(t) = \frac{I_o}{k_T} - \frac{V_{Cin2MAX} - \frac{V_{in}}{2}}{L_{lk}}(t - t_1) \tag{2}$$

When i_p is zero, this mode is finished, and the time is

$$T_{31} = \frac{I_o L_{lk}}{k_T\left(V_{Cin2MAX} - \frac{V_{in}}{2}\right)} \tag{3}$$

i_{Cin1} is $-|i_{in}|$ and i_{Cin2} is $-I_o/k_T - |i_{in}|$; $v_{Q3} = v_{Q1} = V_{in}/2$.

Mode 4 [Figure 4d, t_3–t_4]: At t_3, i_p is zero, and i_p cannot change the conducting direction because of D_{2R}. After t_3, Q_{2P} can achieve zero-current turned off. During this mode, v_{Cin2} in $V_{Cin2max}$. $i_{Cin1} = i_{Cin2} = -|i_{in}|$; $v_{Q3} = V_{in}/2 + \Delta v_{Cin2}$, and $v_{Q1} = V_{in}/2 - \Delta v_{Cin2}$.

Mode 5 [Figure 4e, t_4–t_5]: At t_5, Q_{2P} is turned off with ZCS. $i_{Cin1} = i_{Cin2} = -|i_{in}|$; $v_{Q1} = v_{Q2} = (V_{in}/2 - |\Delta v_{Cin2}|)/2$, and $v_{Q3} = V_{in}/2 + \Delta v_{Cin2}$.

Mode 6 [Figure 4f, t_5–t_6]: At t_5, Q_3 is on, and Q_3 can achieve ZCS due to the low increasing rate of i_p; Q_{2R} is also turn-on with ZCS owing to Q_{2P} is off. Q_{4P} has been turned on at t_2; i_p increases linearly at the rate of

$$i_p(t) = -\frac{V_{CBLMAX}}{L_{lk}}(t - t_5) \tag{4}$$

At the end of this interval, i_p is $-I_o/k_T$, and the interval is

$$T_{56} = \frac{L_{lk} I_o}{k_T V_{CBLMAX}} \tag{5}$$

At t_6, i_p is $-I_o/k_T$. The proposed converter goes into the second half switching cycle and primarily powers the load. $v_p = -V_{in}/2 + \Delta v_{Cin2}$; $v_{re} = -(V_{in} - 2\Delta v_{Cin2})/2k_T$; $i_p = -I_o/k_T$; $i_{Cin1} = -|i_{in}|$, $i_{Cin2} = I_o/k_T - |i_{in}|$.

3. Technical Analysis

3.1. Soft Switching of Q_{2P} and Q_{4P}

3.1.1. Turn-on Instants

Q_{2P} and Q_{4P} can achieve zero-voltage turn-on easily because large equivalent primary inductor can provide enough energy to discharge or charge the parasitic output capacitances of Q_1, Q_3, Q_{2P} and Q_{4P}. For example, to ensure ZVS of Q_{4P}, the energy stored in the output inductor and the leakage inductor of the transformer should be

$$\frac{1}{2}L_r\left(\frac{I_o}{k_T}\right)^2 \geq \frac{1}{2}(C_1 + C_{4P})\left(\frac{V_{in}}{2}\right)^2 \tag{6}$$

where L_r is the equivalent primary inductor at this instant, and the minimum load current to achieve ZVS is

$$I_{o,min} \geq \frac{V_{in}}{2k_T}\sqrt{\frac{(C_1 + C_{4P})}{L_r}} \tag{7}$$

3.1.2. Turn-off Instants

Q_{2P} and Q_{4P} are triggered off after i_p is reduced to zero. Hence, Q_{2P} and Q_{4P} can ensure ZCS in a wide load range. The reset time of i_p is determined by (3), and T_{reset} is the minimum time delay of the driving signals of Q_{2P} and Q_{4P}. Therefore, to keep a safe zero-current turn-off, T_{reset} should be larger than the reset time of i_p, and C_{in2} should be designed with following equation [17]

$$C_{in2} \leq \frac{(T_s - 2T_{reset})T_{reset}}{4L_{lk}} \tag{8}$$

Reduced C_{in2} could cause a large value of reset voltage of i_p, which can ensure safe ZCS operation. However, it may cause high OFF voltage on D_{o1} to D_{o4}, Q_{2R}, Q_{4R}, and Q_3. Hence, there should be a trade-off between the ZCS condition and the OFF voltages on D_{o1} to D_{o4}, Q_{2R}, Q_{4R}, and Q_3.

3.2. Soft Switching of Q_1 and Q_3

3.2.1. Turn-on Instants

When Q_1 and Q_3 are on, i_p is still zero, and i_p cannot vary sharply due to the fact that L_{lk} limits the increasing rate. Consequently, Q_1 and Q_3 can obtain quasi ZCS turn-on. To reduce the switching-on loss further, low driving resistors are preferred for Q_1 and Q_3.

3.2.2. Turn-off Instants

When Q_1 and Q_3 are off, v_{Q1} and v_{Q3} varies with low slope because C_1 and C_3. Consequently, Q_1 and Q_3 can obtain quasi ZVS operation. To minimize the power loss further, extra output capacitors of Q_1 and Q_3 could be added.

3.3. Soft Switching of Q_{2R} and Q_{4R}

The identical circuit of Q_{2R} during the turn-off interval is shown in Figure 4c. As illustrated in Figure 3, D_{2R} is already conducted before t_2, and Q_{2R} is gated off at t_2. Hence, Q_{2R} can be switched off with zero-voltage properly. The identical circuit of Q_{2R} during the turn-on period is shown in Figure 4e. As depicted in Figure 3, Q_{2P} is already off before t_5 and Q_{2R} is gated on at t_5. Therefore, the turn-on power loss of Q_{2R} is zero. The soft switching condition of Q_{4R} is similar to that of Q_{2R}, and detailed analysis is not presented in this paper.

3.4. Voltage Balance of the Primary Capacitors

3.4.1. Input Capacitors

With identical capacitance and symmetrical circuit structure, the initial voltage of C_{in1} and C_{in2} is $V_{in}/2$. v_{Cin1} and v_{Cin2} can be stable, owing to the fact that charging and discharging currents of these capacitors are balanced over one switching period. Corresponding waveforms are given in Figure 3, and identical circuits can be referenced in Figure 4. As the positive and negative pulses of the currents flowing through C_{in1} and C_{in2} are balanced over one switching period, the mid-point voltage of C_{in1} and C_{in2} can be stable over one switching period.

3.4.2. Flying Capacitors

The initial voltage of C_s is also $V_{in}/2$ due to symmetrical circuit structure, and v_{Cs} can be stable owing to the fact that charging and discharging currents of C_s are balanced over one switching period. Corresponding waveforms are given in Figure 3, and identical circuits can be referenced in Figure 4. The positive and negative pulses of the current flowing through C_s are balanced over one switching period. Hence, C_s can achieve stable voltage over one switching cycle.

3.5. Current Stress of the Primary Component

3.5.1. S_2 and S_4

The average value of i_{S2} and i_{S4} is

$$I_{AVG\_S_{2,4}} = \frac{I_o}{k_T}\left(\frac{D}{2} - \frac{1}{2}\frac{T_{31}}{T_s}\right) \tag{9}$$

The RMS value of i_{S2} and i_{S4} is

$$I_{RMS\_S_{2,4}} \approx \sqrt{\frac{1}{T_s}\int_0^{D\frac{T_s}{2}}\left(\frac{I_o}{k_T}\right)^2 dt + \frac{1}{T_s}\int_0^{T_{31}}\left(\frac{I_o}{T_{31}k_T}\right)^2 t^2 dt} = \frac{I_o}{k_T}\sqrt{\frac{D}{2} + \frac{T_{31}}{3T_s}} \tag{10}$$

3.5.2. Q_1 and Q_3

The average value of i_{Q1} and i_{Q3} is

$$I_{AVG\_Q_{1,3}} \approx \frac{I_o}{k_T}\frac{D}{2} \tag{11}$$

The RMS value of i_{Q1} and i_{Q3} is

$$I_{RMS\_Q_{1,3}} \approx \sqrt{\frac{1}{T_s}\int_0^{D\frac{T_s}{2}}\left(\frac{I_o}{k_T}\right)^2 dt} = \frac{I_o}{k_T}\sqrt{\frac{D}{2}} \tag{12}$$

3.5.3. C_{in1}

The average current of i_{Cin1} is zero. The time integral of the positive pulse of i_{Cin1} is

$$I_{pos\_C_{in1}} = \int_0^{\frac{DT_s}{2}}\left(\frac{I_o}{k_T} - |i_{in}|\right)dt = \left(\frac{I_o}{k_T} - |i_{in}|\right)\frac{DT_s}{2} \tag{13}$$

The time integral of the negative pulse of i_{Cin1} is

$$I_{neg\_C_{in1}} = \int_{\frac{DT_s}{2}}^{T_s}|i_{in}|dt = |i_{in}|(2-D)\frac{T_s}{2} \tag{14}$$

To keep charge balance over one switching cycle, the average current of i_{Cin1} is zero. Hence, $|i_{in}|$ can be computed as

$$|i_{in}| = \frac{I_o}{k_T}\frac{D}{2} \tag{15}$$

The RMS value of i_{Cin1} is

$$I_{RMS\_C_{in1}} \approx \sqrt{\frac{1}{T_s}\int_0^{\frac{DT_s}{2}}\left(\frac{I_o}{k_T}\right)^2\left(1-\frac{D}{2}\right)^2 dt + \frac{1}{T_s}\int_{\frac{DT_s}{2}}^{T_s}\left(\frac{I_o}{k_T}\right)^2\left(\frac{D}{2}\right)^2 dt} = \frac{I_o}{k_T}\sqrt{\frac{D}{2} - \frac{D^2}{4}} \tag{16}$$

3.5.4. C_{in2}

The average current of i_{Cin2} is zero. The RMS value of i_{Cin2} can be computed according to Figure 3

$$I_{RMS\_C_{in2}} \approx \frac{I_o}{k_T}\sqrt{\frac{D}{2} - \frac{D^2}{4} + \frac{2T_{31}}{3T_s}} \tag{17}$$

3.5.5. C_s

The average current of i_{Cs} is zero. The RMS value of i_{Cs} can be computed according to Figure 3

$$I_{RMS\_C_s} \approx \frac{I_o}{k_T}\sqrt{\frac{2T_{31}}{3T_s}} \tag{18}$$

3.6. Comparison with the Conventional Capacitor Clamped TL dc-dc Converter

3.6.1. Main Switches

As illustrated in Figure 5a, the current difference between Q_1 and Q_2 of the converter in Figure 1a is inversely proportional to the duty ratio D, and when D = 0.3, the current of Q_2 would be twice that of Q_1. Hence, the current distribution of the main switches of the converter in Figure 1a is imbalanced. Consequently, the current rating of Q_2 and Q_4 is much higher than that of Q_1 and Q_2. However, in the proposed converter, the primary switches have balanced and reduced current. As shown in Figure 5c, the current difference between i_{Q1} and i_{Q2P} is around 0.01 per unit, which is mainly caused by the negative current pulse of i_{Q2P}. However, the RMS value of the negative pulse can be neglected due to the fact that the time of this pulse is very short. As the primary free-wheeling current is reset to zero, the current stress on the main switches in the proposed converter is also reduced. The maximum value of the off-voltage stress on Q_3 is $V_{in}/2 + \Delta v_{Cin2}$, which is slightly higher than that of the converter in Figure 1a. However, as Δv_{Cin2} is usually small, which is not exceed 30 V. Hence, the increasing voltage stress on Q_3 can still be accepted.

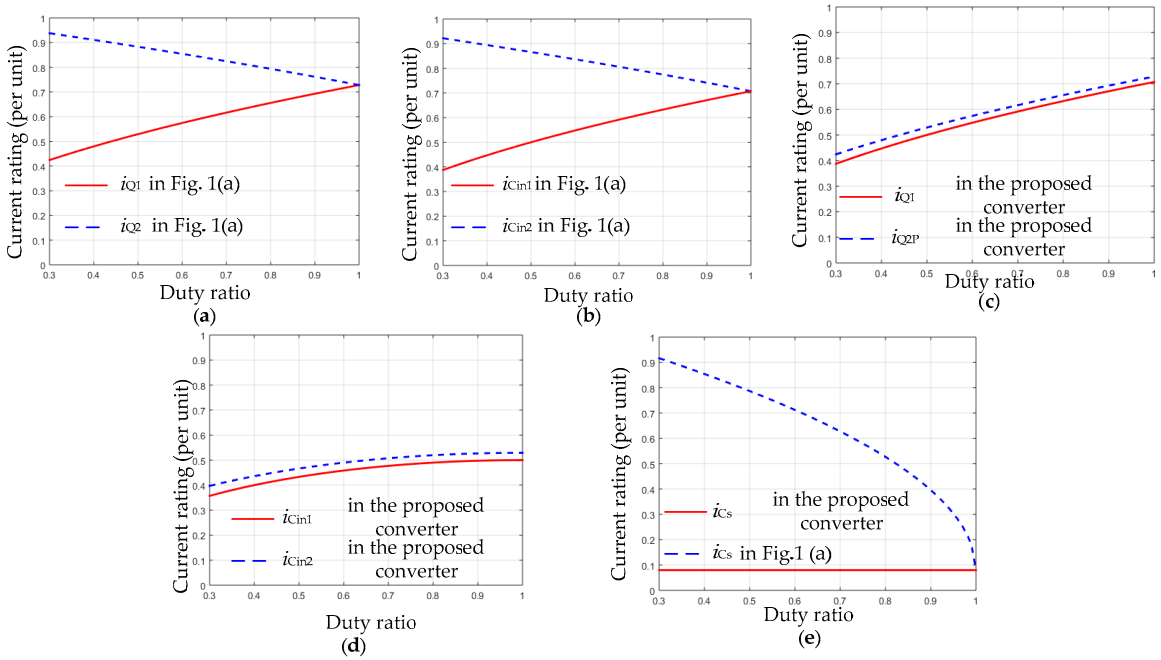

Figure 5. Current of the primary switches: (**a**) i_{Q1} and i_{Q2} in Figure 1a; (**b**) i_{Cin1} and i_{Cin2} in Figure 1a; (**c**) i_{Q1} and i_{Q2P} in the proposed converter; (**d**) i_{Cin1} and i_{Cin2} in the proposed converter; (**e**) i_{Cs}.

3.6.2. Primary Capacitors

As illustrated in Figure 5b, the current difference between C_{in1} and C_{in2} of the converter in Figure 1a is varied with the duty ratio D, and when D = 0.3, the current of C_{in2} would be twice that of C_{in1}. Hence, the current distribution of the input capacitors of the converter in Figure 1a is imbalanced. Furthermore, the current rating of C_{in2} is much higher than that of C_{in1}. However, in the proposed converter, the input capacitors have balanced and reduced current. As shown in Figure 5d, the current difference between i_{Cin1} and i_{Cin2} is around 0.01 per unit, which is mainly caused by the current pulses

during switching instants. However, the RMS value of these pulses can also be neglected due to fact that the times are very short. As i_p during the free-wheeling stages is zero, the RMS value of i_{Cin1} and i_{Cin2} in the proposed converter is also reduced. The current comparison of C_s is provided in Figure 5e, and the RMS value of i_{Cs} in the proposed converter is obviously lower than C_s in Figure 1. Hence, the required value of C_s in the proposed converter is much lower than C_s in Figure 1, which results in reduced volume of this capacitor.

3.6.3. Soft Switching Load Range

As proven in Table 1, the ZVS load range of Q_1 and Q_3 in Figure 1a is narrow owing to the fact that only low energy kept in L_{lk} can be used to discharge or charge C_1, C_3, C_{2p}, and C_{4p}, which would lead to poor efficiency under light load condition. Hence, C_1, C_3, C_{2p}, and C_{4p} in Figure 1a should be small to ensure ZVS operation of Q_1 and Q_3. However, a large value of C_1, C_3, C_{2p}, and C_{4p} is better for minimizing turn-off power loss of Q_1 and Q_3. Hence, the switching-off power loss of Q_1 to Q_3 in Figure 1a cannot be optimized.

Table 1. Soft switching of the main switches.

Item	Q_1	Q_2	Q_3	Q_4
Proposed	ZCZVS, easy	ZVZCS, easy	ZCZVS, easy	ZVZCS, easy
Figure 1a	ZVS, hard	ZVS, easy	ZVS, hard	ZVS, easy

As depicted in Figures 2–4, Q_{2P} and Q_{4P} in the proposed converter are turned-on with zero-voltage and off with zero-current; while, Q_1 and Q_3 are on with quasi-ZCS mode and off with quasi-ZVS mode. Hence, the soft-switching conditions of the primary switches in the proposed converter are not interconnected, and the switching-off power loss of Q_1 and Q_3 can be reduced without increasing the switching-on power loss.

3.7. Brief Comparison with Other Typical HB TLDCs

To evaluate the proposed converter further, some brief comparison is carried out in this part. The components comparison is shown in Table 2. Compared with classical HB TLDCs, the power devices with high voltage rating of the proposed converter are less than other converters. As allowed voltage ripple on the input capacitors is large, C_{in1} and C_{in2} in the proposed converter are small, which means reduced system volume and BOM cost. In Reference [7], an extra capacitor is required to generate the reset voltage of i_p, and the number of capacitors of the converter in Reference [7] is highest.

Table 2. Components comparison.

Converter	Power Devices High Voltage	Power Devices Low Voltage	Capacitors Large Value	Capacitors Small Value
Proposed	4	2	0	3
[1]	6	0	2	0
[6]	6	1	2	1
[7]	6	2	2	2

The performance comparison is depicted in Table 3. As two of the primary switches cannot ensure safe ZVS operation under light output current, the converter in Reference [1] has the worst soft-switching characteristics. As the switching-on power loss and switching-off power loss can be optimized at the same time, the proposed converter has the best soft switching characteristics among the four converters. The extra power devices in Reference [6] are operated in hard switching mode, which will reduce the efficiency. As i_p is reduced to zero in the free-wheeling stages, the proposed converter and the converters in References [6,7] have small duty ratio loss. In addition, the current

stress of the primary components is large and uneven in the converter [1], owing to similar reasons as the converter in Figure 1a.

Table 3. Performance comparison.

Converter	Soft Switching Primary Switches	Soft Switching Extra Power Devices	Current Stress Primary Components	Duty Ratio Loss
Proposed	Good	Good	Small (even)	Small
[1]	Worse	NA	Large (uneven)	Large
[6]	Medium	Worse	Small (even)	Small
[7]	Medium	Good	Small (even)	Small

4. Experimental Results

The operation principle and characteristics of the proposed converter are proved by a 1–kW experimental equipment, and some specifications of the experimental equipment are listed in Table 4. Figures 6–12 show the experimental results.

Figure 6 gives the primary voltage of the transformer, and v_p changes with the same rate with v_{Cin1} and v_{Cin2} during the power-transferring stages. At the beginning of the free-wheeling stages, v_p provides enough and constant reset voltage of i_p. As provided in Figure 7, i_p remains as zero during the free-wheeling stages, which ensures zero-current turn-off of Q_{2p} and Q_{4P}. In addition, the primary circulating current is nearly zero, which reduces the conduction loss. As proved in Figure 8, C_{in2} is charged or discharged by i_p during power-transfer stages, hence, v_{Cin2} varies within the boundary of Δv_{Cin2} linearly with time. During free-wheeling stages, v_{Cin2} is unchanged, owing to i_p remaining as zero. As shown in Figure 9, v_{Do1} is also changed with the slope of v_p/k_T, and the voltage stress of v_{Do1} is increased.

Table 4. Specifications of the experimental equipment.

Item	Parameter
V_{in}	400 V–600 V
Rated V_o	200 V
Rated I_o	5 A
f_s	100 kHz
Q_1, Q_3, Q_{2p} and Q_{4p}	20 A/600 V
Q_{2R}, Q_{4R}	20 A/25 V
D_{o1} to D_{o4}	20 A/600 V
k_T	1:1.15
C_{in1}, C_{in2}	200 μF
C_s	1.5 μF
L_o	20 μH/5 A
C_o	200 μF

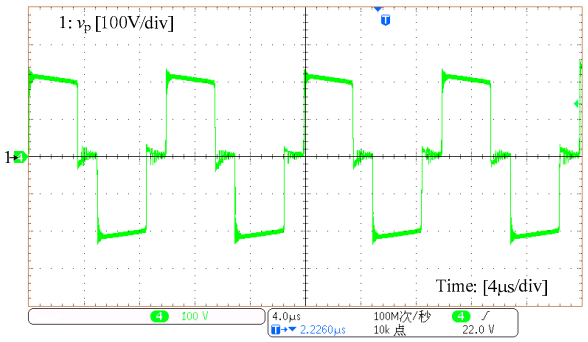

Figure 6. Waveform of v_p.

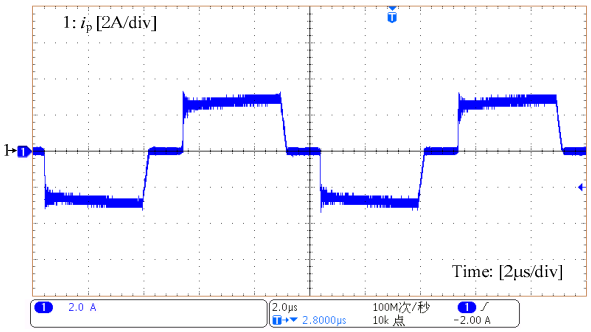

Figure 7. Waveform of i_p.

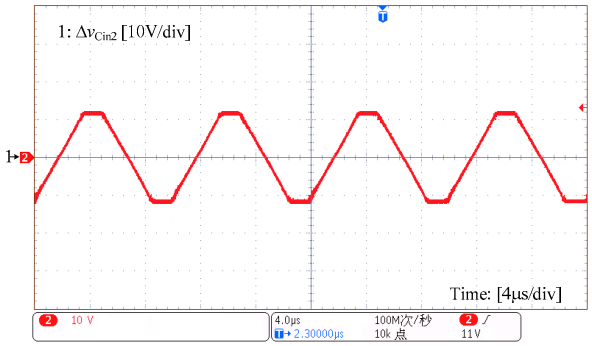

Figure 8. Waveform of Δv_{Cin2}.

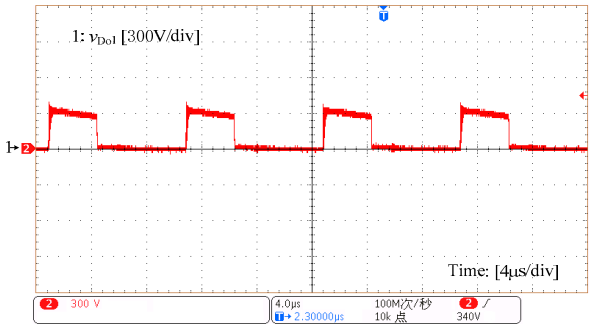

Figure 9. Waveform of v_{Do1}.

The soft-switching characteristic of Q_{2P} is proved in Figure 10, and it is clear that Q_{2P} can achieve ZVZCS. Before the switch-on instant, i_{Q2P} conducts in the reverse direction owing to the fact that D_{2P} is already on, hence, Q_{2p} is switched on with zero-voltage. Before the switching-off signal of Q_{2P} is coming, i_{2P} reduces to zero. Therefore, Q_{2P} can achieve ZCS turn-off properly.

v_{Q3}, i_{Q3} and v_{GSQ3} are depicted in Figure 11, which proves Q_3 is operated in ZCZVS. At the time of switching-on, i_{Q3} cannot change sharply owing to the fact that L_{lk} limits the changing rate of i_p, thus, Q_3 is switched with quasi-ZCS mode. At the time of switching-off, v_{Q3} cannot change sharply owing to the fact that C_3 limits the changing rate; therefore, the switching-off power loss of Q_3 is also small. It should be pointed out that a large value of C_3 would not take great effect on ZVS turn-on of Q_3, which means both the turn-on and turn-off switching loss of Q_{2P} and Q_3 can be optimum. As proved in Figures 10 and 11, the voltage stress of Q_3 and Q_{2P} is confined close to $V_{in}/2$.

The efficiency comparison results are illustrated in Figure 12. In Figure 12a, the proposed converter has high efficiency under low output current condition owing to reduced switching power loss of the primary switches. Under high output current conditions, the efficiency of the proposed converter is also better due to the fact that switching-off power loss can be further reduced. In Figure 12b, when I_o is constant, the efficiency of both converters is changed inversely proportional to V_{in}. In addition, the

efficiency of the proposed converter is decreased slowly owing to the fact that V_{in} has a small effect on the soft switching condition of the primary switches.

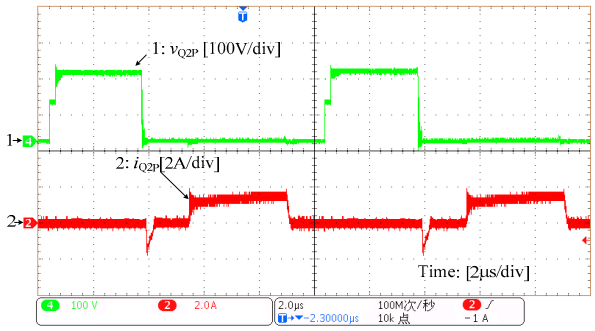

Figure 10. Waveform of v_{Q2P} and i_{Q2P}.

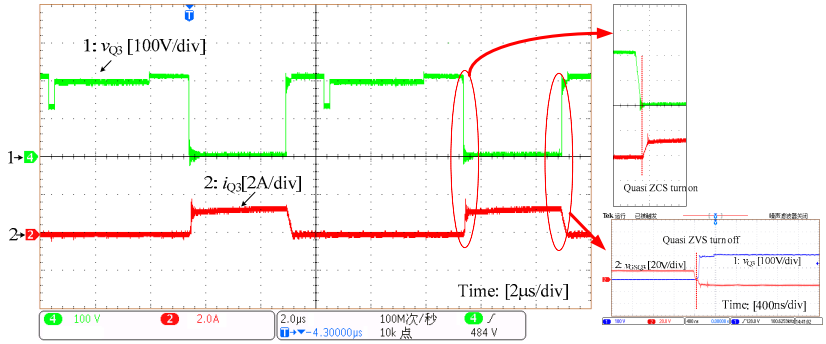

Figure 11. Waveform of v_{Q3}, i_{Q3} and v_{GSQ3}.

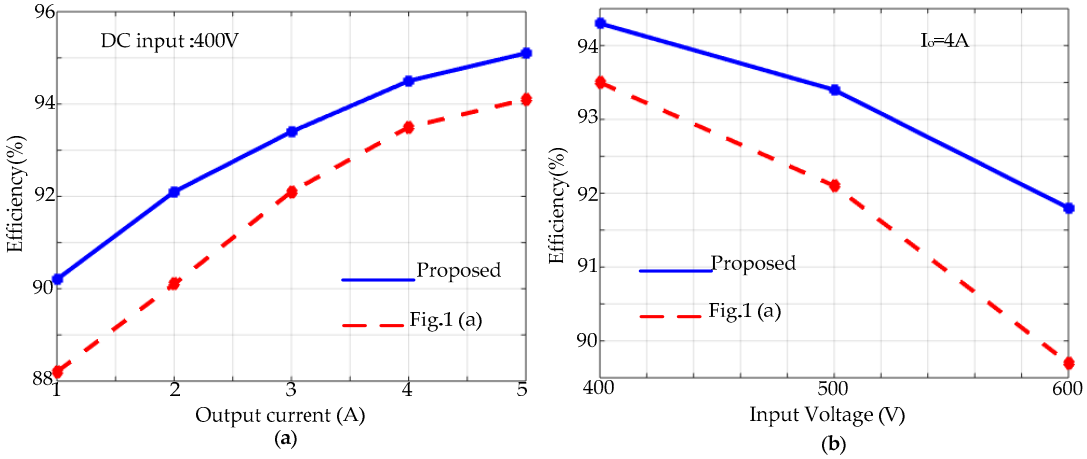

Figure 12. Efficiency curves: (**a**) V_{in} = 400 V, I_o is varied; (**b**) I_o = 4 A, V_{in} is varied.

5. Conclusions

A new ZVZCS capacitor-clamped HB TLDC with two unsymmetrical bidirectional switches is proposed and analyzed, and the experimental results can well support the theoretical analysis. After discussion, some obvious advantages of the proposed converter can be concluded, e.g., balanced and reduced current stress of the primary components, small and reduced volume of the clamping capacitor, wide load range soft-switching operation for both turn-on and turn-off instants and a simple switching scheme. The only drawback of the proposed converter is the off voltage of Q_3 is slightly higher than $V_{in}/2$.

Funding: This research was funded by [Natural Science Foundation of Shaanxi University of Science and Technology] grant number [2016XSGG08].

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Pinheiro, J.R.; Barbi, I. The three-level ZVS PWM converter—A new concept in high-voltage DC-to-DC conversion. In Proceedings of the IEEE IECON, San Diego, CA, USA, 13 November 1992; pp. 173–178.
2. Barbosa, P.M.; Lee, F.C. Design aspects of parallel three-phase DCM boost rectifiers. In Proceedings of the IEEE PESC, Charleston, SC, USA, 1 July 1999; pp. 331–336.
3. Blaabjerg, F.; Chen, Z.; Kjaer, S.B. Power electronics as efficient interface in dispersed power generation systems. *IEEE Trans. Power Electron.* **2004**, *19*, 1184–1194. [CrossRef]
4. Mohsenian, H.; Davoudi, A. Towards building an optimal demand response framework for DC distribution network. *IEEE Trans. Smart Grid* **2014**, *5*, 2626–2634. [CrossRef]
5. Deschamps, E.; Barbi, I. A comparison among three-level ZVS-PWM isolated DC-to-DC converters. In Proceedings of the IEEE IECON, Aachen, Germany, 31 August–4 September 1998; pp. 1024–1029.
6. Canales, F.; Barbosa, P.M.; Lee, F.C. A zero-voltage and zero current-switching three level DC/DC converter. *IEEE Trans. Power Electron.* **2002**, *17*, 898–904. [CrossRef]
7. Ruan, X.; Zhou, L.; Yan, Y. Soft-switching PWM three-level converters. *IEEE Trans. Power Electron.* **2001**, *16*, 612–622. [CrossRef]
8. Lin, B. Hybrid DC/DC converter based on dual three-level circuit and half-bridge circuit. *IET Power Electron.* **2016**, *9*, 817–824. [CrossRef]
9. Lin, B.; Zhang, S. Analysis and implementation of a three-level hybrid dc–dc converter with the balanced capacitor voltages. *IET Power Electron.* **2016**, *9*, 457–465. [CrossRef]
10. Lu, S.; Mu, M.; Jiao, Y.; Lee, F.C.; Zhao, Z. Coupled inductors in interleaved multiphase three-level DC–DC converter for high-power applications. *IEEE Trans. Power Electron.* **2016**, *31*, 120–134. [CrossRef]
11. Zhang, Y.; Shi, J.; Zhou, L. Wide input-voltage range boost three-level DC–DC converter with quasi-Z source for fuel cell vehicles. *IEEE Trans. Power Electron.* **2017**, *32*, 6728–6738. [CrossRef]
12. Jin, L.; Duan, S. Comparative analysis of three-level dual active bridge DC–DC converter between reflux-power-optimised and current-stress-optimised phase shift control. *IET Power Electron.* **2018**, *11*, 1681–1688. [CrossRef]
13. Hong, F.; Li, L.; Wu, Y.; Ji, B.; Zhou, Y. 1500 V three-level forward converter with phase-shifted control. *IET Power Electron.* **2018**, *11*, 1547–1555. [CrossRef]
14. Manoranjan, S.; Sivakumar, K. Fault tolerant three-level boost inverter with reduced source and LC count. *IET Power Electron.* **2018**, *11*, 399–405.
15. Ruan, X.; Chen, Z.; Chen, W. Zero-voltage-switching PWM hybrid full-bridge three-level converter. *IEEE Trans. Power Electron.* **2005**, *20*, 395–404. [CrossRef]
16. Ruan, X.; Li, B. Zero-voltage and zero-current-switching PWM hybrid full-bridge three-level converter. *IEEE Trans. Ind. Electron.* **2005**, *52*, 213–220. [CrossRef]
17. Shi, Y.; Wang, X.; Xi, J.; Gui, X.W.; Yang, X. Wide load range ZVZCS three-level DC-DC converter with compact structure. *IEEE Trans. Power Electron.* **2019**, *34*, 5032–5037. [CrossRef]
18. Kim, D.-Y.; Kim, J.-K.; Moon, G.-W. A three-level converter with reduced filter size using two transformers and flying capacitors. *IEEE Trans. Power Electron.* **2013**, *28*, 46–53. [CrossRef]
19. Shi, Y.; Yang, X. Soft switching PWM cascaded three-level combined DC–DC converters with reduced filter size and wide ZVS load range. *IEEE Trans. Power Electron.* **2015**, *30*, 6604–6616. [CrossRef]
20. Shi, Y. Full ZVS load range diode clamped three-level DC–DC converter with secondary modulation. *J. Power Electron.* **2016**, *16*, 93–101. [CrossRef]
21. Liu, D.; Deng, F.; Zhang, Q.; Chen, Z. Zero-voltage switching PWM strategy based capacitor current-balancing control for half-bridge three-level DC/DC converter. *IEEE Trans. Power Electron.* **2018**, *33*, 357–369. [CrossRef]

22. Liu, D.; Deng, F.; Gong, Z.; Chen, Z. Input-parallel output-parallel three-level DC/DC converters with interleaving control strategy for minimizing and balancing capacitor ripple currents. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 1122–1132. [CrossRef]
23. Liu, W.; Jin, H.; Yao, W.; Lu, Z. An interleaved PWM method with better voltage-balancing ability for half-bridge three-level DC/DC converter. *IEEE Trans. Power Electron.* **2018**, *33*, 4594–4598. [CrossRef]