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Derivative-Free Direct Search Optimization Method for Enhancing Performance of Analytical Design Approach-Based Digital Controller for Switching Regulator

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Abstract: Although an analytical design approach-based digital controller—which is essentially a deadbeat controller—shows zero steady-state error and no intersampling oscillations, it takes a finite number of sampling periods to settle down to a steady-state value. This paper describes the application of a derivative-free Nelder–Mead (N–M) simplex method to the digital controller for retuning of its coefficients intelligently to ensure improved settling and rise times without disturbing the deadbeat controller characteristics (i.e., no ripples between the sampling periods and no steady-state error). A switching-mode buck regulator working at 1 MHz in continuous conduction mode (CCM) is considered as a plant. Numerical simulation results depict that the N–M algorithm-based optimized digital controller not only shows improved steady-state and transient performance but also guarantees rigorous robustness against model uncertainty and disturbance as compared to its traditional counterpart, as well as the other optimized digital controller fine-tuned through other derivative-free metaheuristic optimization techniques, such as the genetic algorithm (GA). A system generator-based hardware software co-simulation is also performed to validate the simulation results.

Keywords: Nelder–Mead simplex method; analytical design approach based digital controller; engineering optimization; switching regulator

1. Introduction

Tightly regulated DC-to-DC switching regulators are a requirement of modern low-power high-frequency (for enhancing the integration of devices and passive components) digital devices. Perturbations in input voltage or load current may keep the output voltage unregulated, thus reducing the devices life. There is a need to introduce a controller into the loop to keep the output voltage regulated, regardless of the changes in load current and input voltage. A direct discrete-time controller

designed on the basis of an analytical design approach (synthesis rather than analysis approach) offers somewhat nominal performance. This paper proposes that better transient response and steady-state error characteristics can be achieved by retuning the digital controller coefficients using the Nelder–Mead local search algorithm.

Both emulation and direct digital design approaches are extensively used for constructing digital controllers for a wide variety of engineering applications. Reference [1] suggested a new discrete-time PID controller with a filter, combining the pole-zero cancellation (PZC) and inversion formulae-based analytical design control methodologies, for the buck regulator to ensure sufficiently large stability margins and superior performance. The method, however, involves heavy computations. Abbas et al. in Reference [2] successfully designed the phase lead-lag control theory-based digital controllers for the buck regulator, with consideration of all the control loop parameters. Reference [3] suggested a digital gain scheduling controller designed on the basis of lead-lag control theory for the modeled DC-DC series resonant converter for DC wind turbines, operating in continuous conduction mode (CCM). In Reference [4], for the sake of surmounting the difficulties in estimating discrete buck converter power stage parameters from noise, a new self-tuned Kalman filter (KF)-based parametric system identification technique was proposed. A direct digital design technique based PID controller was then applied to the identified buck converter to improve the tracking performance. The paper, however, lacks the detail of designing the PID controller. A unified nonlinear robust current observer for robust sensorless controllers of switching regulators was proposed in Reference [5]. Although the observer speeds up the tuning process, it requires a memory cheaper code. In Reference [6], based on the switched Lyapunov theory, a novel sampled-data control approach (essentially a digital control strategy) was developed for the buck converter working in CCM and DCM modes with variable switching frequency operation to ensure set-point tracking and stability. However, to realize the controller, a sampled data switched model for the converter has to be developed. In Reference [7], a sampled data controller was designed for a buck converter to realize the concept of sensorless control, with the help of direct digital control theory; it was targeted to minimize the output voltage fluctuations because of load variations.

Deadbeat control theory is also employed for the design of digital controllers for various engineering applications. In Reference [8], a discrete gain variable controller was designed on the basis of classical deadbeat control methodology, while the gain of nonlinear coupled equations was determined by using evolutionary techniques, such as the genetic algorithm along with the Newton Raphson method. The simple optimized deadbeat-controlled system shows comparable results with that of the finite control step method. In Reference [9] a single-input, single-output sampled data system was considered as a plant. Deadbeat control methodology was applied to minimize the cumulative time-weighted functions of tracking error in the frequency domain. The application of deadbeat control quickly reduces the error sequence. Two examples of sample data system were presented to show the performance of deadbeat control techniques. In Reference [10] polynomial-based control was applied for a double-boost converter. The controller was tested against the changes in source voltage and load resistance. It was found that, although the deadbeat controller had a great ability to track the error signal, it was more sensitive to parametric changes. Similarly, deadbeat control theory was employed to design a digital controller for an inverter of distributed generators. The current controlled deadbeat controller was designed in such a way to position the closed loop poles at the origin with a minimum disturbance input gain [11]. In all the above-mentioned references, the digital control laws are tuned using the traditional control theory for ensuring a nominal performance, which can be further improved using optimization techniques.

Numerous examples in the literature are reported where the digital control laws are optimized using the various advanced calculus-based or metaheuristic-based optimization techniques. For example, in Reference [12], the Levenberg–Marquardt (LM) algorithm-based nonlinear least squares optimization method was applied to PZC-based digital controllers for the buck regulator. The numerical results show tremendous improvement for the optimized controllers. Reference [13] suggested the dynamic

PSO (dPSO)-based optimization of digital fractional order PID (FO-PID) controller applied to the buck converter fed DC motor for optimal speed control. Similarly, optimization techniques such as PSO was employed for optimizing the parameters of the fuzzy controller applied to the Quasi-Z Source converter [14] and for fine-tuning digital PID controller parameters [15]; the magnitude optimum criterion for developing explicit analytical tuning rules for digital PID controllers [16]; the genetic optimization scheme for improving a single-input fuzzy PID controller for the buck regulator [17]; the election campaign optimization algorithm for tuning digital PID controllers for the discrete-time system [18]; the gradient descent method for refining the digital control law for ac-to-dc converters to achieve unity power factor [19]. Similarly, in Reference [20], different swarm intelligence-based optimization techniques (i.e., an artificial bee colony, cuckoo search, etc.) were employed to get the enhanced speed and efficient maximum power point tracking algorithm for a photovoltaic system. Even promising derivative-free metaheuristic techniques are also subjected to limitations: The PSO suffers from the premature convergence problem like other stochastic algorithms; the GA requires coding the data to be in categorical form.

Well-recognized traditional control theory-based digital controllers, if optimized in an efficient way even with local search optimization methods, may offer excellent transient response and steady-state error characteristics. Motivated by this concept, this paper proposes the analytical design approach-based optimized digital controller. In this research, it was observed that the digital controller was optimized more efficiently with substantially fewer objective function evaluations by a simpler and derivative-free N–M method, as compared to other the derivative-free GA metaheuristic method. There are various factors responsible for the success of the N–M method over the other methods. It is simple in structure and performs deterministic transformations. The algorithm employs operations, namely, reflection, expansion, contraction and shrinkage while finding new lower points in the search space easily without using the information of derivatives. Ridges in the objective surface are easily traversed by the algorithm, while exploring the new lower points. This characteristic prevents the algorithm from converging too early. This justifies the applicability of the N–M method for optimizing the discrete-time controllers for switching converters. In addition, according to the best knowledge of the authors, the analytical design method has not been optimized by the N–M method.

The paper commences with the modeling of the buck switching converter to be controlled in Section 2. The complete design procedure of the analytical design approach-based digital controller is highlighted in Section 3. The suggested Nelder–Mead algorithm for optimizing digital controller is treated in Section 4. Comprehensive numerical simulation results with discussion are presented in Section 5. A cycle-accurate hardware-software co-simulation for fast prototyping is performed in Section 6. The findings of the paper are concluded in Section 7.

2. Buck Converter Modeling

A highly unregulated DC input voltage V_{in} got converted into a lowly regulated output voltage V_{out} using a buck converter, whose circuit diagram is shown in Figure 1. The circuit includes the unavoidable parasitic elements, like inductor DCR and capacitor ESR. DCR is the direct current resistance of inductor while ESR is the equivalent series resistance of the capacitor, denoted by R_L and R_C (in our case), respectively. An additional zero is introduced in the buck converter's transfer function because of the ESR of the capacitor [21]. For the lossless buck converter, the input voltage V_{in}, the output voltage V_{out} and the switch duty ratio D are interrelated, over a period of steady-state operation, as:

$$\begin{aligned} \overline{P}_{L,in} &= \frac{1}{T}\int_{0}^{DT}(V_{in}-V_{out})I_L dt = \frac{1}{T}\int_{DT}^{T} V_{out}I_L dt = \overline{P}_{L,out} \\ \Rightarrow \frac{1}{T}(V_{in}-V_{out})I_L DT &= \frac{1}{T}V_{out}I_L(T-DT) \Rightarrow V_{out} = D\cdot V_{in} \end{aligned} \quad (1)$$

The specifications of the buck converter to be considered throughout the paper are as the following: V_{in} = 3.6 V, V_{out} = 2.0 V, L = 6.8 µH, C = 6.8 µF, r_{L} = 505 mΩ, r_{C} = 50 mΩ, f_{s} = 1 MHz, and $T_s = 1/f_{\mathrm{s}}$ =

1 µs. The detailed block diagram (also including the buck converter circuit diagram) of the closed-loop digital control system is shown in Figure 1.

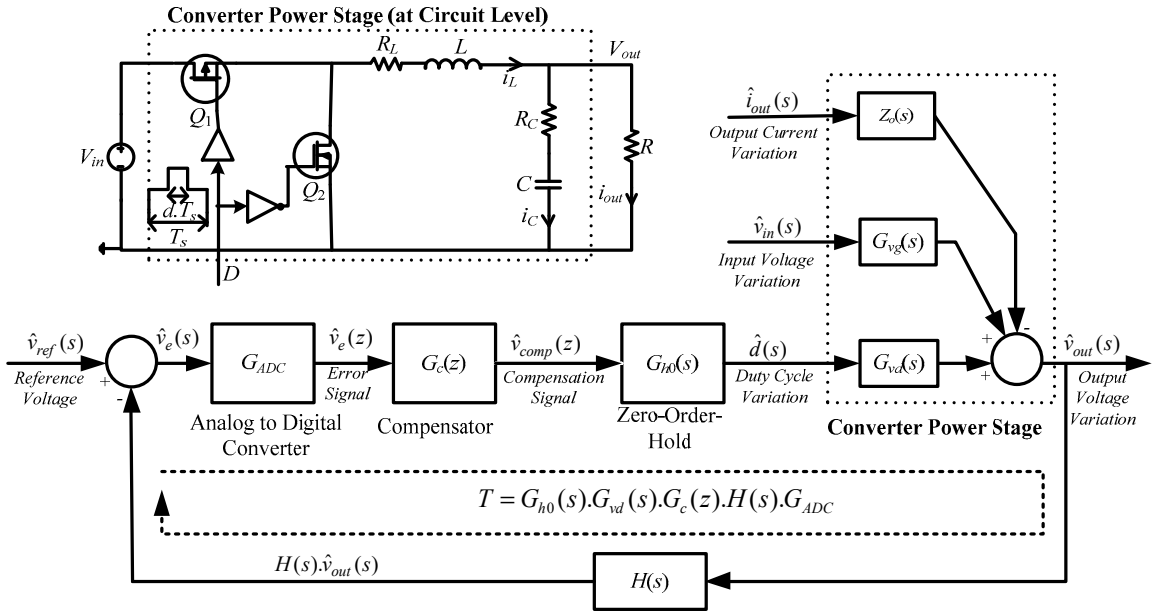

Figure 1. Closed-loop digital control system block diagram (also including the circuit diagram).

As can be observed from Figure 1, the output voltage variation $\hat{v}_{out}(s)$ is a linear combination of the input voltage variation $\hat{v}_{in}(s)$, the load current variation $\hat{i}_{out}(s)$ and the small-signal duty cycle perturbation $\hat{d}(s)$, propagated through the transfer functions, namely the line-to-output transfer function $G_{vg}(s)$, the converter output impedance of the loaded power converter $Z_o(s)$ and the control-to-output transfer function $G_{vd}(s)$, respectively. That is to say:

$$\hat{v}_{out}(s) = G_{vd}(s) \cdot \hat{d}(s) + G_{vg}(s) \cdot \hat{v}_{in}(s) - Z_o(s) \cdot \hat{i}_{out}(s) \tag{2}$$

The three transfer functions $G_{vd}(s)$, $G_{vg}(s)$, and $Z_o(s)$, derived using the state-space averaging technique [22,23], are expressed by:

$$\begin{aligned} G_{vd}(s) = \left.\frac{\hat{v}_{out}(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_{out}(s)=0}} &= V_{in}(s)\left[\frac{\left(\frac{R}{R+R_L}\right)(R_C C s+1)}{LC\left(\frac{R+R_C}{R+R_L}\right)s^2+\left(\frac{L}{R+R_L}+C(R\|R_L)+R_C C\right)s+1}\right] \\ &= V_{in}\left(\frac{R}{R+R_L}\right)\left(\frac{\frac{s}{\omega_{ZERO}}+1}{\frac{s^2}{{\omega_0}^2}+\frac{s}{Q\omega_0}+1}\right) \end{aligned} \tag{3}$$

$$\begin{aligned} G_{vg}(s) = \left.\frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)}\right|_{\substack{\hat{d}(s)=0 \\ \hat{i}_{out}(s)=0}} &= D\left[\frac{\left(\frac{R}{R+R_L}\right)(R_C C s+1)}{LC\left(\frac{R+R_C}{R+R_L}\right)s^2+\left(\frac{L}{R+R_L}+C(R\parallel R_L)+R_C C\right)s+1}\right] \\ &= D\left(\frac{R}{R+R_L}\right)\left(\frac{\frac{s}{\omega_{ZERO}}+1}{\frac{s^2}{{\omega_0}^2}+\frac{s}{Q\omega_0}+1}\right) \end{aligned} \tag{4}$$

$$Z_o(s) = -\left.\frac{\hat{v}_{out}(s)}{\hat{i}_{out}(s)}\right|_{\substack{\hat{d}(s)=0 \\ \hat{v}_{in}(s)=0}} = R_L\left[\frac{\left(\frac{R}{R+R_L}\right)(1+Ls/R_L)(R_CCs+1)}{LC\left(\frac{R+R_C}{R+R_L}\right)s^2+\left(\frac{L}{R+R_L}+C(R \parallel R_L)+R_CC\right)s+1}\right]$$
$$= R_L\left(\frac{R}{R+R_L}\right)\frac{\left(\frac{s}{R_L/L}+1\right)\left(\frac{s}{\omega_{ZERO}}+1\right)}{\left(\frac{s^2}{{\omega_0}^2}+\frac{s}{Q\omega_0}+1\right)} \quad (5)$$

With:

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC\frac{R+R_C}{R+R_L}}} \approx \frac{1}{\sqrt{LC}} \quad if\ R_C << R,\ R_L << R; \quad (6)$$

$$\omega_{ZERO} = 2\pi f_{ZERO} = \frac{1}{R_CC} \quad (7)$$

$$Q = \frac{1}{2\zeta} = \frac{1}{\omega_0\left(\frac{L}{R+R_L}+\frac{RR_LC}{R+R_L}+R_CC\right)} \approx \frac{1}{\omega_0\left(\frac{L}{R}+R_LC+R_CC\right)} \quad (8)$$

By the introduction of a feedback loop, the effect of $\hat{v}_{in}(s)$ and $\hat{i}_{out}(s)$ on $\hat{v}_{out}(s)$ can be diminished. The $\hat{v}_{out}(s)$, with the feedback loop, takes the following form:

$$\hat{v}_{out}(s) = \hat{v}_{ref}(s)\cdot\frac{1}{H(s)}\cdot\frac{T}{1+T} + \hat{v}_{in}(s)\cdot\frac{G_{vg}(s)}{1+T} - \hat{i}_{out}(s)\cdot\frac{Z_o(s)}{1+T} \quad (9)$$

where the product of all the gains in the loop designated as loop gain T is given by:

$$T = G_{h0}(s)\cdot G_{vd}(s)\cdot G_c(z)\cdot H(s)\cdot G_{ADC} \quad (10)$$

Here, G_{ADC} and the sensor gain $H(s)$ are considered in unity for the sake of simplicity. For a sufficiently large magnitude in loop gain T, the last two terms of Equation (2) can be ignored, as they are reduced by a factor of $1/(1+T)$. However, the first term suggests that, for the known DC reference V_{ref} and DC sensor gain $H(0)$, $\hat{v}_{out}(s)$ may precisely track $V_{ref}(s)$ provided that $\hat{v}_{ref} = 0$ and $\|T(0)\| \gg 1$. The first term, therefore, is responsible for the output voltage regulation and stability of the converter. Correspondingly, the control-to-output transfer function $G_{vd}(s)$ is considered as a plant for the digital controller design.

In order to design the direct digital design approach-based digital controller, the second-order analog buck converter $G_p(s)$ needs to be discretized. The $G_{vd}(s)$ (which is actually $G_p(s)$) preceded by the zero-order-hold (ZOH), for the component values mentioned above with a sampling period of 1 µs, can be discretized as:

$$G_p(z) = Z\left\{\frac{1-e^{-sT_s}}{s}\cdot G_p(s)\right\} = \left(1-z^{-1}\right)\cdot Z\left\{\frac{G_p(s)}{s}\right\}$$
$$= \frac{0.061653z^{-1}\left(1+0.1781z^{-1}\right)}{\left(1-1.87z^{-1}+0.8924z^{-2}\right)} \quad (11)$$

3. Analytical Design Approach-Based Digital Controller

The analytically designed discrete deadbeat controller enforces the error sequence of a closed-loop control system to become zero on the application of the specific time-domain input signal. The output response of the feedback system exhibits minimum settling time, no inter-sampling ripples and zero steady-state error. The controller achieves the reference voltage in a quick and efficient manner. The analytical design approach-based digital controller algorithm [8,10,24] is explained by the following steps:

1. The analog transfer function of plant $G_p(s)$ is firstly discretized by using one of the transformation techniques like ZOH (in our case), with the sampling period T_s, as follows:

$$G_p(z) = Z\left\{\frac{1-e^{-Ts}}{s}G_p(s)\right\} = \left(1-z^{-1}\right)Z\left(\frac{G_p(s)}{s}\right) = \frac{0.061653z^{-1}\left(1+0.1718z^{-1}\right)}{\left(1-1.87z^{-1}+0.8924z^{-2}\right)} \tag{12}$$

2. In order to have minimum settling time with zero steady-state error, the closed-loop transfer function described by Equation (13):

$$T(z) = \frac{Y(z)}{R(z)} = \frac{G_c(z)G_p(z)}{1+G_c(z)G_p(z)} \tag{13}$$

should have finite impulse response as:

$$T(z) = \sum_{q=1}^{N} a_q.z^{-q} = a_0 + a_1z^{-1} + a_2z^{-2} + \cdots + a_Nz^{-N} \tag{14}$$

where N is the order of the overall system and is equal to or greater than the order of plant n, and a_1 to a_N are the coefficients of the impulse response of the closed-loop control system. From Equation (14), two deadbeat control criteria can be explored as follows:

- The sum of the coefficients of polynomial $\sum_{q=1}^{N} a_q$ should be equal to 1, i.e., $\sum_{q=1}^{N} a_q = 1$. This is actually the DC gain of the system.
- For the controller to exhibit the deadbeat response, all closed-loop poles should be forced at origin. This can be mathematically written as $T(z) = z^{-q}$ where $q \geq 1$ is termed as the control system delay and is the integral multiple of T_s with the minimum values of 1. It should be clear that $T(z)$ should not contain any value with a positive term of z; otherwise the system responds before the input is applied, which is against the physical realization of the controller.

As the transfer function of the buck converter is of second order (n = 2) and the series expansion of $G_p(z)$ starts with z^{-1}, the closed-loop pulse transfer function should be of the following form:

$$T(z) = a_1z^{-1} + a_2z^{-2} \tag{15}$$

3. The controller pulse transfer function can be derived by rearranging Equation (13) as:

$$G_c(z) = \frac{T(z)}{G_p(z)\cdot[1-T(z)]} \tag{16}$$

4. In order to achieve the steady-state value with the limited number of sampling periods, the error sequence is described as the difference of the reference signal and the output signal:

$$E(z) = R(z) - Y(z) = R(z)[1-T(z)] \tag{17}$$

should be minimized in a quicker way. By substituting the discrete-time step input signal, Equation (17) can be written as:

$$E(z) = \frac{(1-T(z))}{(1-z^{-1})} \tag{18}$$

In order to achieve the steady-state value with a finite number of sampling periods, $1 - T(z)$ must be of the following form:

$$1 - T(z) = \left(1 - z^{-1}\right) \cdot N(z) \tag{19}$$

where $N(z)$ is a polynomial with finite terms in negative power of z. By rearranging Equation (19), $N(z)$ can be written as:

$$N(z) = \frac{1 - T(z)}{1 - z^{-1}} = \frac{1 - a_1 z^{-1} - a_2 z^{-2}}{1 - z^{-1}} \tag{20}$$

The solution of Equation (20) gives the quotient $N_Q(z)$ and the remainder $N_R(z)$ as:

$$N_Q(z) = 1 + (1 - a_1) z^{-1} \tag{21}$$

$$N_R(z) = (1 - a_1 - a_2) z^{-2} \tag{22}$$

5. In order to avoid the inter-sampling oscillations after the steady-state is reached, $D(z)$ must be of the following form:

$$D(z) = b_0 + b_1 z^{-1} \tag{23}$$

From Figure 1, $D(z)$ can be written as:

$$D(z) = T(z) \cdot \frac{R(z)}{G_p(z)} \tag{24}$$

By substituting the unit step input and digitized plant in Equation (24), and for $D(z)$ to be similar as in Equation (23), $T(z)$ must be of the following form:

$$\begin{aligned} T(z) &= \left(0.61653 + 0.010981 z^{-1}\right) T_1 \\ \Rightarrow T_1 &= \tfrac{a_1 z^{-1} + a_2 z^{-2}}{0.61653 + 0.010981 z^{-1}} \end{aligned} \tag{25}$$

The solution of Equation (25) gives quotient T_{1Q} and remainder T_{1R} equations as:

$$T_{1Q} = 1.622 a_1 z^{-1} \tag{26}$$

$$T_{1R} = (a_2 - 0.17811 a_1) z^{-2} \tag{27}$$

6. As the controller forces the error sequence to zero with minimum sampling period and no inter-sampling oscillations as the steady-state is reached, both the remainder terms defined in Equations (22) and (27) must be equal to zero. And by solving simultaneously both the equations, the coefficient of $T(z)$ can be calculated.

7. Thus, by substituting the coefficients of $T(z)$, the discrete time controller comes out to be:

$$G_c(z) = \frac{13.77 z^2 - 25.75 z + 12.29}{z^2 - 0.8488 z - 0.1512} \tag{28}$$

This completes the design procedure of the controller.

4. Derivative-Free Nelder–Mead Simplex Algorithm

One of the direct search methods (DRMs), named the Nelder–Mead (N–M) simplex method is employed for fine-tuning of the digital compensator, designed on the basis of an analytical design approach. The method optimizes the compensator by minimizing the voltage error signal in a quicker way without considering the information of derivatives. The objective function, in a multidimensional

space, considered for minimizing the cost (error signal) is the integral of the squared error (ISE) and is given by:

$$\text{ISE} : J = \int_0^\infty e^2(t)dt, e(t) = V_{out}(t) - V_{ref}(t), \tag{29}$$

The N–M algorithm adopted here is proposed by Lagarias et al. [25] and does not use numerical or analytic gradients. Since no bounds (lower and upper) on decision variables are imposed, the optimization problem is essentially the unconstrained one. There is no guarantee of convergence of the algorithm to a local optimum.

The $n + 1$ points of n-dimensional simplex actually represent the solutions of the problem. Regarding the construction of a simplex around initial guess x_0, each component $x_0(i)$ of x_0 adds 5%. In addition to x_0, n vectors constitute the elements of n-dimensional simplex. The algorithm employs four operations, namely, reflection, expansion, contraction and shrinkage during each of the iterations. At each iteration of the algorithm, the simplex modifies itself repeatedly according to the following way:

1. **Vertices Representation:** First of all, all $n + 1$ points (vertices) in the current simplex are denoted by x_i, $i = 1, \ldots, n + 1$.
2. **Order:** The vertices in the simplex are ordered such that $f(x_1) \leq f(x_2) \leq \cdots \leq f(x_{n+1})$. This implies that, $f(x_1)$ refers to the best point whereas $f(x_{n+1})$ represents the worst point. At each step in the iteration, the current worst point x_{n+1} is discarded and replaced by another point, which becomes part of the simplex.
3. **Reflection:** The reflection point x_r is generated by:

$$x_r = 2x_m - x_{n+1}$$

where x_m represents the centroid of the n best vertices except x_{n+1} and is calculated by:

$$x_m = \sum_{i=1}^{n} x_i/n$$

Correspondingly, $f(x_r)$ is then calculated. If $f(x_1) \leq f(x_r) < f(x_n)$, x_r gets accepted and replaces x_{n+1} and the iteration is terminated.

4. **Expansion:** If $f(x_r) \leq f(x_1)$, the expansion point x_e is evaluated by:

$$x_e = x_m + 2(x_m - x_{n+1})$$

Eventually, $f(x_e)$ is then calculated. If $f(x_e) < f(x_r)$, x_e is accepted and the iteration is terminated. Otherwise (if $f(x_e) \geq f(x_r)$), x_r is accepted and the iteration is terminated.

5. **Contraction:** If $f(x_r) \geq f(x_n)$, a contraction between x_m and the better of x_{n+1} and x_r, is carried out.

    a. **Outside:** If $f(x_n) \leq f(x_r) < f(x_{n+1})$, an outside contraction is performed. x_{oc} is calculated by:

$$x_{oc} = x_m + (x_r - x_m)/2$$

Correspondingly, $f(x_{oc})$ is calculated. If $f(x_{oc}) \leq f(x_r)$, x_{oc} is accepted and the iteration is terminated. Otherwise, a shrinkage is performed (step 6)).

b. **Inside:** If $f(x_r) \geq f(x_{n+1})$, an inside contraction is performed. x_{ic} is calculated by:

$$x_{ic} = x_m + (x_{n+1} - x_m)/2$$

Correspondingly, $f(x_{ic})$ is calculated. If $f(x_{ic}) \leq f(x_{n+1})$, x_{ic} is accepted and the iteration is terminated. Otherwise, a shrinkage is performed (step 6)).

6. **Shrinkage:** The n (new) points are generated by:

$$v_i = x_1 + (x_i - x_1)/2\,, \quad i = 2, \ldots, n+1, \tag{30}$$

$f(v_i)$ is calculated. Thus, at the next iteration, $x_1, v_2, \ldots, v_{n+1}$ constitute the vertices of the simplex.

The points that the algorithm might calculate in the procedure, along with each new possible form of simplex, are depicted in Figure 2. A bold outline represents the original simplex. The algorithm stops as the stopping criteria meet.

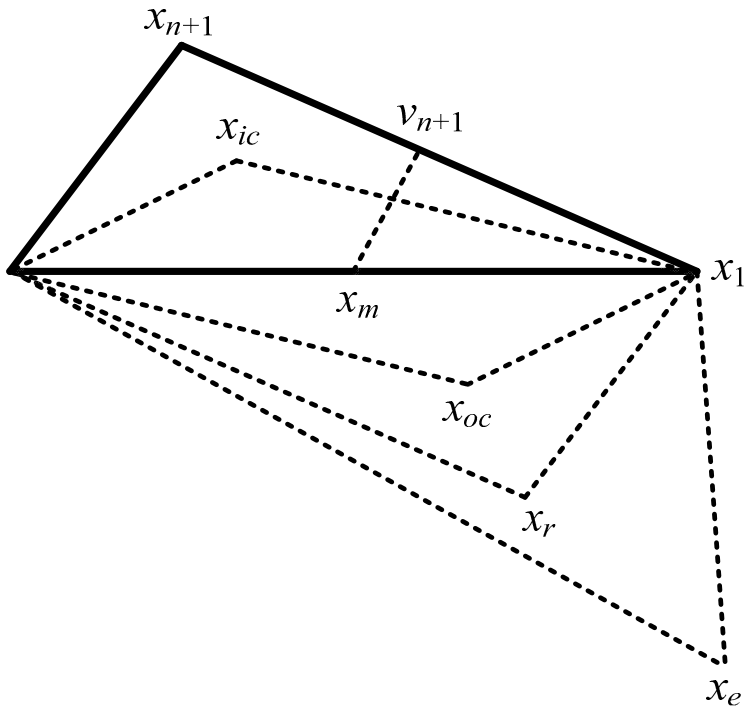

Figure 2. Pictorial description of Nelder–Mead (N–M) simplex method.

The application of the N–M optimization method to the conventional deadbeat controller results in an optimized controller. By taking the initial point as a real vector or real array of the coefficients of the digital controller computed through analytical design approach, the algorithm starts minimizing the cost function (the integral of the squared error (ISE)) at each iteration and ultimately comes up with the updated coefficients of the digital controller. The first few iterations, in the same run, as they display during the progression of the algorithm, are highlighted in Figure 3. Inspection of the results of the optimization reveals a reduction of the cost function monotonically with each iteration, thus ensuring better set-point tracking. Unoptimized and optimized digital controllers are described in Table 1.

Iteration	Func-count	min f(x)	Procedure
0	1	5.1579e-07	
1	7	5.1579e-07	initial simplex
2	9	5.1579e-07	contract outside
3	11	5.1579e-07	contract inside
4	12	5.1579e-07	reflect
5	14	5.1579e-07	contract inside
6	16	5.1579e-07	contract inside
7	18	5.1579e-07	contract inside
8	20	5.1579e-07	contract inside
9	22	5.1579e-07	contract inside
10	24	5.1579e-07	contract inside
11	25	5.1579e-07	reflect
12	27	5.1579e-07	contract inside
13	29	5.1579e-07	contract inside
14	30	5.1579e-07	reflect
15	31	5.1579e-07	reflect
16	33	5.1579e-07	contract inside
17	35	5.1579e-07	contract inside
18	36	5.1579e-07	reflect
19	38	5.1579e-07	contract inside
20	40	5.15373e-07	contract inside
21	42	5.15373e-07	contract inside
22	44	5.15373e-07	contract inside
23	46	5.14314e-07	reflect
24	48	5.1424e-07	reflect
25	50	5.1424e-07	contract inside
26	52	5.12348e-07	expand
27	54	5.12348e-07	contract inside
28	56	5.10885e-07	expand
29	57	5.10885e-07	reflect
30	59	5.07822e-07	expand

Figure 3. First few iterations performed by the algorithm.

Table 1. Unoptimized and optimized digital controllers transfer functions.

Unoptimized Digital Controller	Optimized Digital Controller
$\frac{13.77z^2-25.75z+12.29}{z^2-0.8488z-0.1512}$	$\frac{13.7941z^2-25.7944z+12.3097}{0.8504z^2-0.7046z-0.1459} = \frac{16.2207z^2-30.3321z+14.4752}{z^2-0.8286z-0.1716}$

It should be noted that with the increase of problem dimension, the performance of the N–M method, however, deteriorates. This is because it has to count the objective function to be minimized a lot of the time, thus taking longer computational time.

5. Simulation Results and Discussion

In order to investigate the performance of the Nelder–Mead simplex algorithm-based optimized digital compensators and to show its supremacy over its unoptimized counterpart and the one optimized by other derivative-free metaheuristic techniques, such as the GA, numerical simulation

results computed through MATLAB/Simulink environment are presented. A fixed-type solver is used for simulation purposes.

5.1. Nominal Performance

The optimized digital controller offered a much-improved output voltage response with a reduced rise, peak and settling times and overshoot than that of the conventional digital controller (see Figure 4). There is always a trade-off between the transient response characteristics and steady-state error characteristics. Improving one type of characteristics deteriorates the other type of characteristics. The Nelder–Mead algorithm, however, intelligently retuned the compensator coefficients without disturbing the deadbeat characteristics associated with V_{out}. The performance parameters offered by the optimized and unoptimized controllers are tabulated in Table 2.

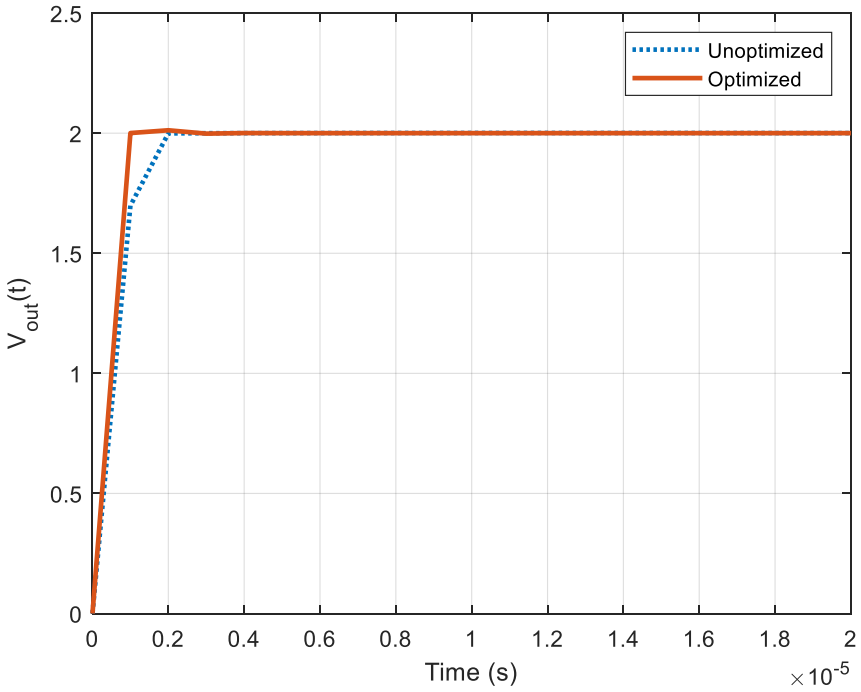

Figure 4. Output voltage response offered by digital compensators.

Table 2. Comparison of performance parameters.

Case No.	Digital Controller	Performance Parameters		
		Rise Time (s)	**Peak Time (s)**	**Settling Time (s)**
1	Unoptimized	1.2203×10^{-6}	1.1000×10^{-5}	1.8701×10^{-6}
	Optimized	7.9977×10^{-7}	2.0000×10^{-6}	9.7972×10^{-7}

In Figure 5, the control signal to the plant is also presented for the unoptimized and optimized compensated systems. As can be observed, a little bit more control effort was required, for the optimized case, to decrease the regulation times.

Just for the sake of comparison and to investigate how other derivative-free metaheuristic techniques behave while fine-tuning the controller coefficients, another derivative-free metaheuristic technique, the GA, was employed to retune the controller coefficients. It is traditionally a well-known algorithm and becomes most effective (by evolving population) especially when very little information is available about the search. One can easily understand the concept of bio-inspired operators such as selection, crossover and mutation used by it. Further, it comes with the advantages of parallel search and random excursions. This is the reason for the selection of this algorithm for the comparison

purpose. Of course, other metaheuristic algorithms could also be selected. The GA parameters used for the simulation purposes are tabulated in Table 3.

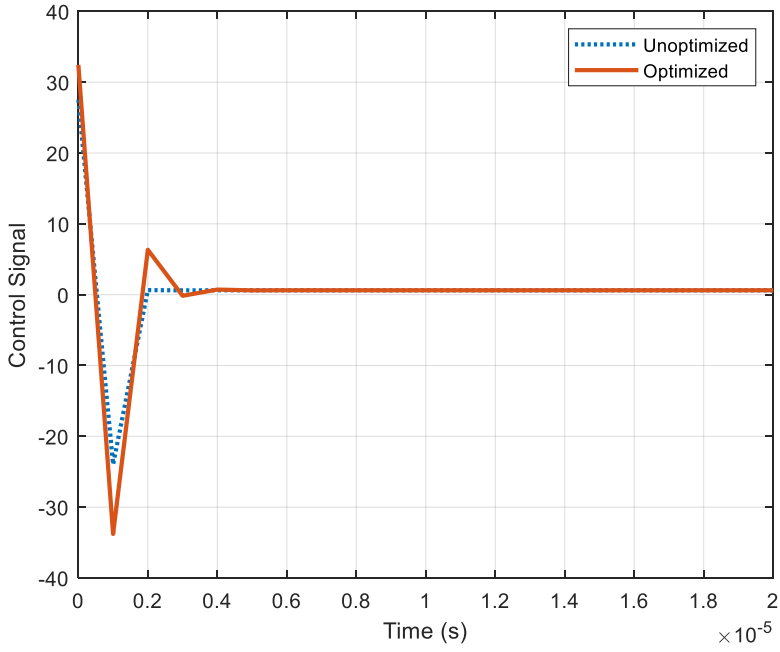

Figure 5. Control signal to the plant.

Table 3. The genetic algorithm (GA) parameter values.

GA Parameters	Value
Maximum Number of Generations/Iterations (Termination Criteria)	50
Initial Population Size/Number of Chromosomes (Genomes)	200
Number of Genes in Each Chromosome	6
Selection Strategy	Stochastic Uniform
Crossover Rate or Probability	0.65
Mutation Function	Adaptive Feasible
Fitness Function (to be Minimized) Type	ISE
Function Tolerance	1×10^{-6}

From Figure 6, it can be inferred that the GA could not perform better than the N–M method. It offered a relatively longer rise time and peak time of 1.1395×10^{-6} s and 4×10^{-6} s, respectively, with a larger overshoot of 23.8728%. In addition, as the deadbeat characteristics lost their nature, the controller optimized by the GA was no longer a deadbeat controller.

The findings depict that the N–M method minimizes the unconstrained multivariable objective function (ISE in our case) more rigorously, compared to the GA metaheuristic approach. The successful optimized control solution suggests that the scorned DSMs deserve more attention from the optimization community.

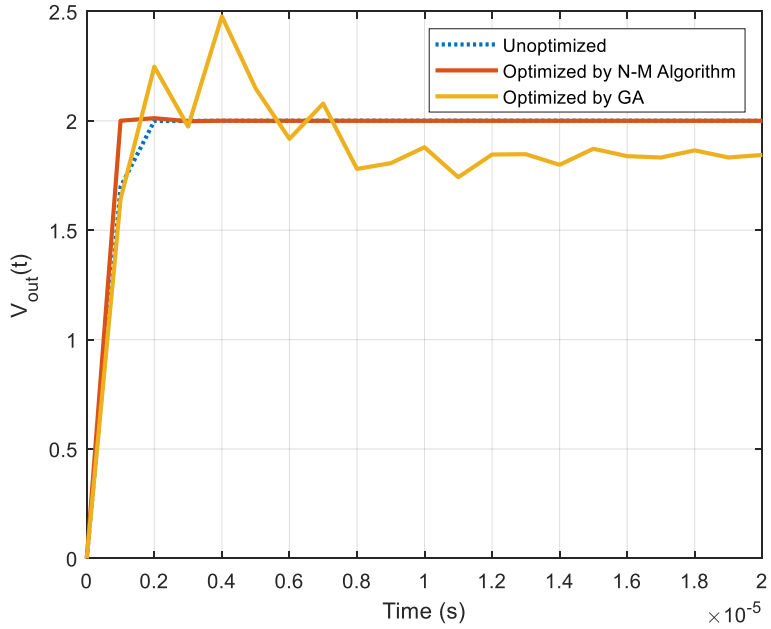

Figure 6. Output voltage response offered by digital compensators.

5.2. Load Transient Response

The optimized controller (tuned by the N–M method) not only exhibited better nominal characteristics but also an excellent load transient response. For a change in load resistance from 4.5 Ω (i_{out} = 444.44 mA) to 9.0 Ω (i_{out} = 222.22 mA) and then from 9.0 Ω to 4.5 Ω, the optimized controller recovered more rapidly to its steady-state value with a peak to peak voltage spike of 63 mV, compared to the unoptimized controller, which offered 68 mV for the peak to peak voltage spike (see Figure 7). The optimized controller, therefore, showed more robustness against the variations in load current to maintain the output voltage at the desired level.

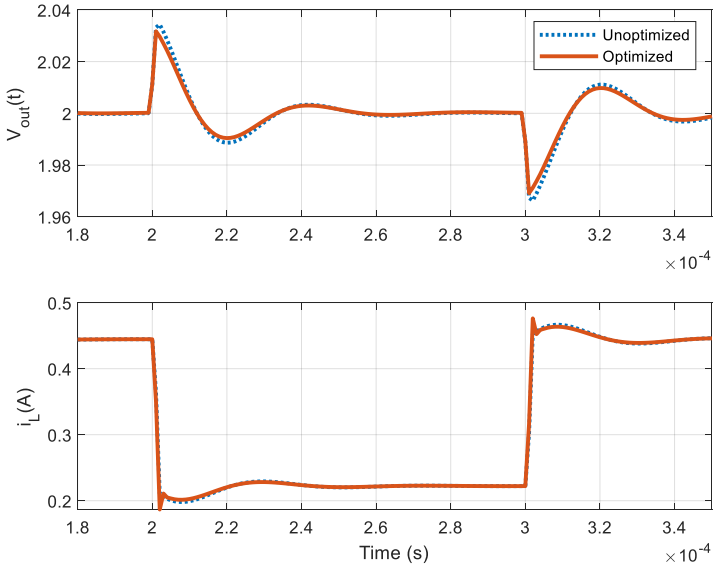

Figure 7. Load transient response offered by digital compensators.

5.3. Disturbance Rejection

The variations in converter power stage parameters can be modeled by disturbance. For a step disturbance occurring at the plant input, the optimized controller rejected the disturbance quickly,

without an increase of the overshoot, as compared to the unoptimized controller (see Figure 8). The optimized controller thus exhibited a good disturbance rejection capability.

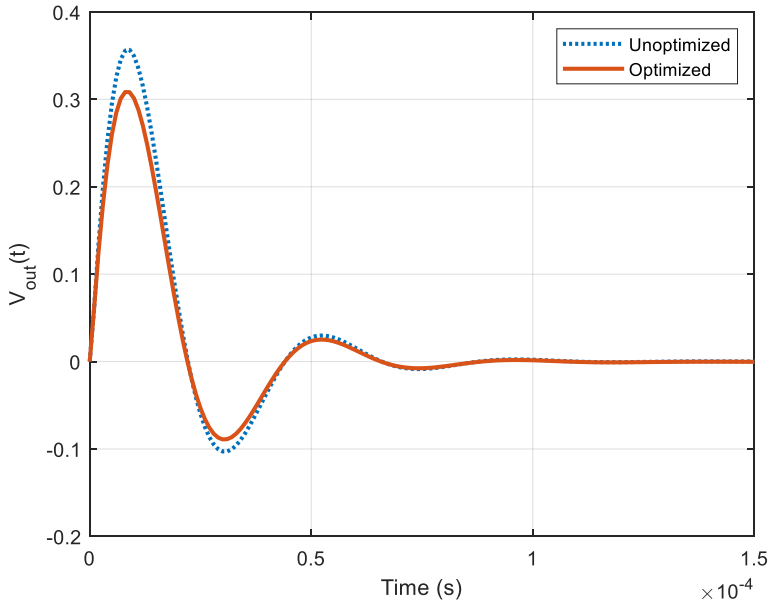

Figure 8. Disturbance rejection performance offered by digital compensators.

5.4. Set-Point Tracking

The closed-loop set-point tracking demands that $e(t) = V_{ref}(t) - V_{out}(t) \rightarrow 0$ as $t \rightarrow \infty$. As can be observed from Figure 9, variations in the reference voltage from 2 V to 3 V and then from 3 V to 2 V was rapidly followed by the optimized digital compensator, with regard to its unoptimized counterpart, thus validating its significance.

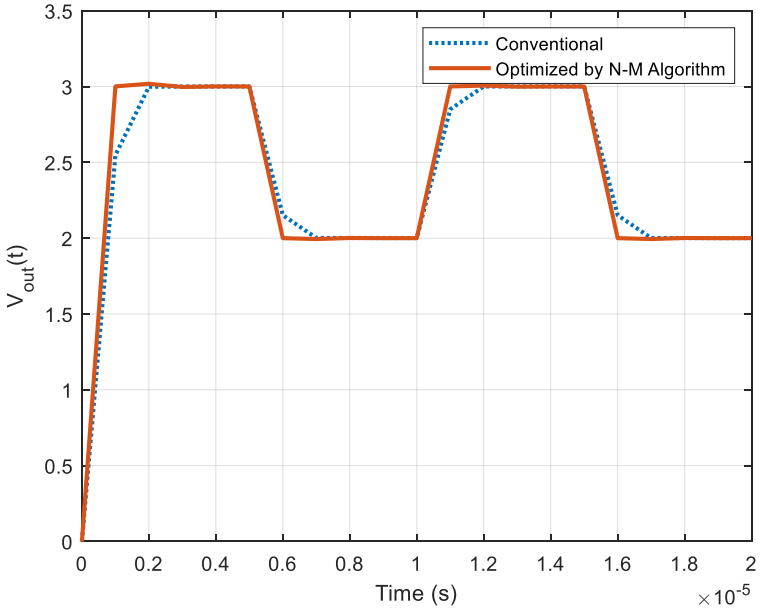

Figure 9. Set-point tracking performance offered by digital compensators.

6. Hardware-Software Co-Simulation

The proposed optimized controller was also validated through hardware/software co-simulation using the Xilinx Artix-7 FPGA board (XC7A35T-1CPG236C) from Xilinx, Inc. (an American technology

company), which was connected to a PC using a JTAG interface. To this end, a controller implementable model was developed using the Xilinx System Generator (XSG) toolset [26] in the MATLAB/Simulink environment. To test the XSG hardware controller, the error signal generated by the difference of reference signal and output signal, after digitization through ADC, in the Simulink environment, was made available to the controller using the "Gateway In" block. Similarly, the "Gateway Out" block was used to connect the controller output to the plant. These blocks performed the necessary data type conversions. This implies that some information may be lost during these conversions. However, the resolution of controller coefficients was of high significance, which may degrade the performance of the controller. Therefore, the controller coefficients were coded using single-precision floating-point data type, having a word length of 32 bits. With the successful model development, the executable bitstream was generated by the compiler, which was then downloaded into the FPGA board through the JTAG interface. Note that no VHDL code was required to be developed for testing the controller. Thus, the XSG-based hardware implementation shortens the development time drastically.

The steps in performing hardware/software co-simulation are as follows:

1. The optimized controller (described in Table 1) is re-written in the following form:

$$\begin{aligned} G_c(z) &= \frac{D(z)}{E(z)} \\ &= \frac{16.2207z^2 - 30.3321z + 14.4752}{z^2 - 0.8286z - 0.1716} \\ &= \frac{16.2207 - 30.3321z^{-1} + 14.4752z^{-2}}{1 - 0.8286z^{-1} - 0.1716z^{-2}} \end{aligned} \tag{31}$$

2. The above re-organized controller is converted into a difference equation as:

$$\begin{aligned} d(k) &= 16.2207e(k) - 30.3321e(k-1) + 14.4752e(k-2) + 0.8286d(k-1) \\ &+ 0.1716d(k-2) \end{aligned} \tag{32}$$

3. The controller described in Equation (30) or (31) is realized using adders/subtractors, multipliers, and delay elements from the XSG library as shown in Figure 10.

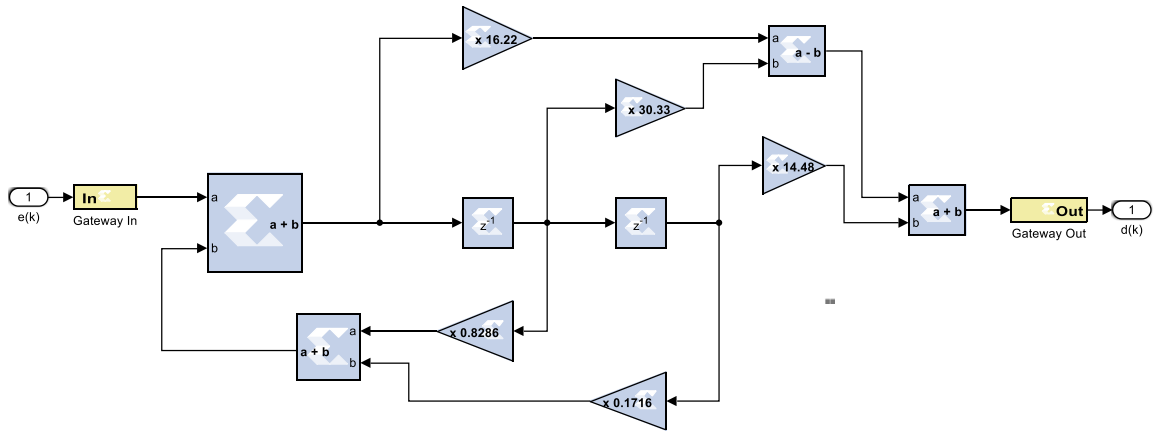

Figure 10. Digital controller realization using the Xilinx System Generator (XSG) library elements.

For realization of controller, standard programming was adopted, which uses n delay elements as compared to direct programming, which uses $n + m$, where n ($n = 2$) and m ($m = 2$ in our case) represent the number of poles and zeros respectively, such that $n \geq m$ [27].

4. The controller was inserted inside the control loop of the buck converter and the resulting model is shown in Figure 11.

5. The overall model was compiled and the corresponding bitstream generated after the synthesis of VHDL code was downloaded into the FPGA. The situation of programming the FPGA is depicted in Figure 12.
6. Now, the output regulation of the controlled buck converter in a hardware/software co-simulation setting was analyzed. The regulation performance is depicted in Figure 13. It can be seen that the XSG-based controller exhibited a performance comparable to what was obtained during the simulations.

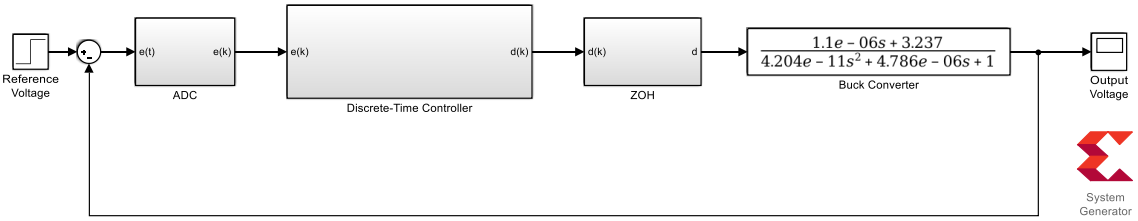

Figure 11. Closed loop representing hardware/software co-simulation.

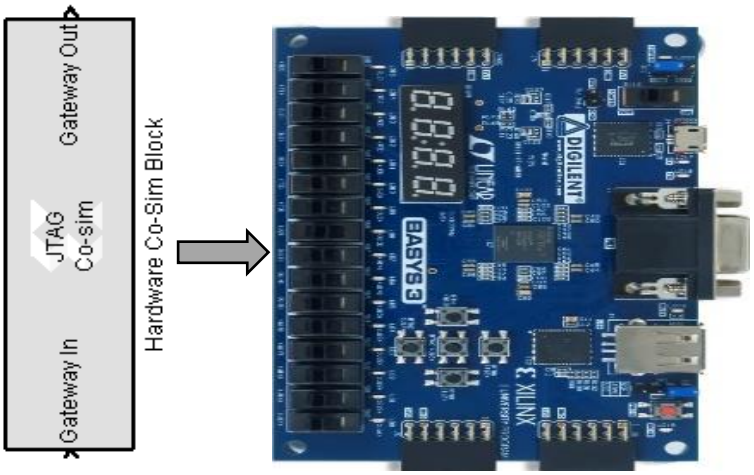

Figure 12. Bitstream to program the Xilinx Artix-7 FPGA board.

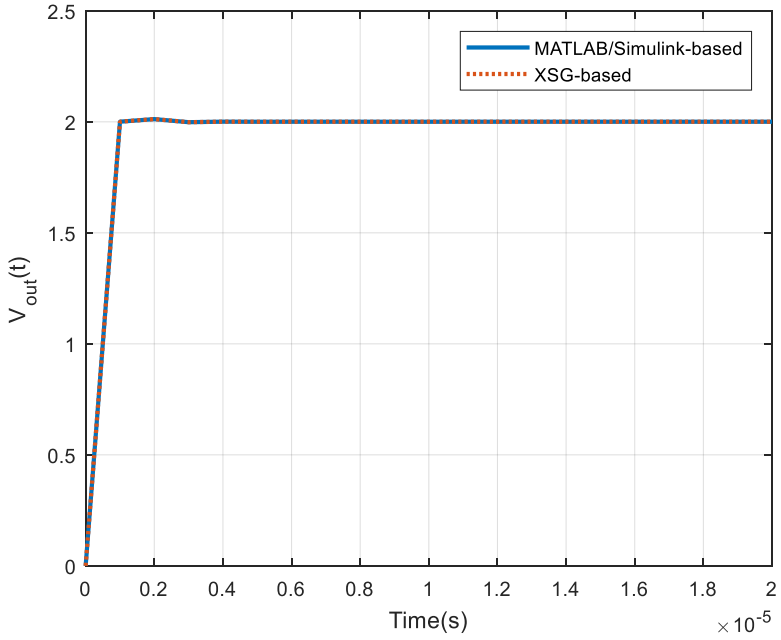

Figure 13. Response shown by the Simulink and XSG-based compensated system.

7. Conclusions

The paper suggests the application of the derivative-free Nelder–Mead simplex algorithm to the deadbeat control theory-based digital controller to ameliorate the performance. The nominally computed digital controller parameters were readjusted through the N–M algorithm. The optimized digital controller offered a superior load transient response, disturbance rejection, setpoint tracking and so on, compared to its unoptimized counterpart. While optimizing the controller, the deadbeat characteristics remained the same, but presented improved time-domain characteristics. Usually, an improvement in response times introduces overshoots, but this was not the case here. Like the GA, the N–M method does not involve operators like selection, crossover and mutation and thus was found to exhibit rigorous convergence characteristics. MATLAB/Simulink-based numerical results showed the superiority of the N–M method over the other derivative-free algorithms, like the GA. A system generator-based hardware into the loop implementation was performed to validate the simulation results. Variants of N–M method can be introduced, in the future, for further improvement in performance.

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