

Article

# Assessment of Efficiency and Reliability of Wide Band-Gap Based H8 Inverter in Electric Vehicle Applications

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**Abstract:** This paper analyzes the performance of a three-phase converter architecture with a reduced common mode voltage to be used in electric motor drives. Starting from the classical three-phase bridge architecture, two additional switches are inserted in the DC link, in order to decouple the source from the load during the freewheeling intervals. Ad-hoc modulation strategies are introduced and evaluated against the classical three-phase space vector modulation. Three main parameters are analyzed: common mode voltage, efficiency and reliability. Experimental measurements on a converter prototype are used to evaluate the common mode performance. The efficiency in the case of Si-IGBT and SiC-MOSFETs is experimentally evaluated. Reliability analysis performed with a Coffin-Mason model showed that the higher efficiency offered by the SiC devices allows for a marked extension of the lifetime.

**Keywords:** pulse width modulated inverter; motor drive; electric vehicle; pulse-width modulation; space vector; common-mode voltage; leakage current

## 1. Introduction

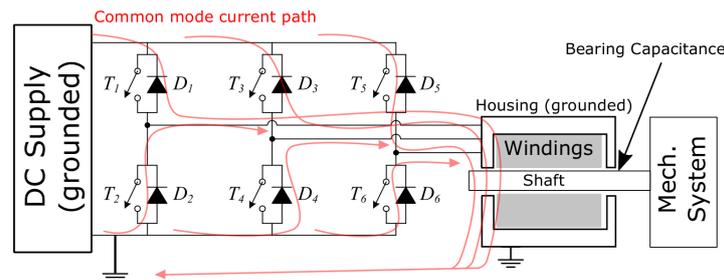
Transformerless three-phase, two-level architectures are widely used for power converters due to their good harmonic characteristics; however, they exhibit poor common-mode performance.

The problem of common-mode currents (CMCs) is a very sensitive issue in electric drives. Rapidly varying PWM-frequency common-mode voltages (CMVs) at the output of an inverter cause common-mode currents to flow through the usually capacitive common-mode paths that exist between the inverter and the ground. This may lead to partial discharges, faults, and electromagnetic interference (EMI) that in turn can cause the inverter control to trip [1,2].

One of the most common paths for CMCs in electric motor drives is through the shaft bearings, because of the parasitic capacitance between stator and rotor [3]. CMCs can damage the bearings causing premature motor failure. This problem has been thoroughly studied and modeled [4,5], and

many solutions have been proposed to reduce or compensate for its effects, including common-mode transformers [6] and active filters [7,8].

In automotive traction drives, CMCs are the source of EMI and possible resonance phenomena [9]. Possible return current paths include the braided shield of the motor cable, the metallic vehicle body and parasitic capacitance among the vehicle components [10], as shown in Figure 1, where the common mode current path is highlighted for a three-phase full-bridge electrical drive. These problems can be mitigated by suitable mechanical packaging and cable routing [11] and by shielding and isolating the traction system from the vehicle chassis, although this will not protect the motor bearings from suffering the effects of CMCs [12].



**Figure 1.** Common-mode current path in an electrical drive system.

For the above reasons, researchers have been active in finding new solutions to reduce this undesired current, and reducing the common mode voltage variation is one of the most investigated solutions. In fact, the leakage current is proportional to the voltage derivative over the parasitic capacitance in the common-mode circuit.

Wide-bandgap devices and the consequent increase of the operating frequency of converters is increasing performance [13] and reliability [14], but it is also making CMV reduction even more necessary [15].

This paper explores the performance of a three-phase converter named H8 [16,17] with the focus on motor drive application. Different semiconductors and modulation strategies are evaluated having the three-phase full-bridge (H6) architecture as a benchmark.

## 2. Modulations for Common-Mode Voltage Mitigation

Figure 2 shows the general layout of an electric motor drive. The type of the motor is not specified, as the scheme has a general validity. The “Current control trajectory” block is customized depending on the kind of the machine: Surface Permanent Magnet machines (SPM) would normally feature a zero direct current, whereas Internal Permanent Magnet (IPM) as well as Synchronous Reluctance machines (SRM) would have an optimized current reference generation. Induction machines would also have an additional control loop for the control of the flux.

The energy flow between source and mechanical output is normally controlled by the combination of a power electronic converter, where the control of the energy flow actually occurs, and an electromechanical converter, i.e., an electrical machine, that acts as drive mechanism. Basically, the utility input is rectified by means of either a controlled or an uncontrolled rectifier and then converted again into AC to supply the motor with a three-phase voltage adjusted in magnitude and frequency using a modulation technique. A battery can be used instead of the utility grid to provide the DC link. The direct connection of the battery to the metallic chassis of the car and the machine bearing and parasitic capacitance to the housing would constitute the common-mode path.

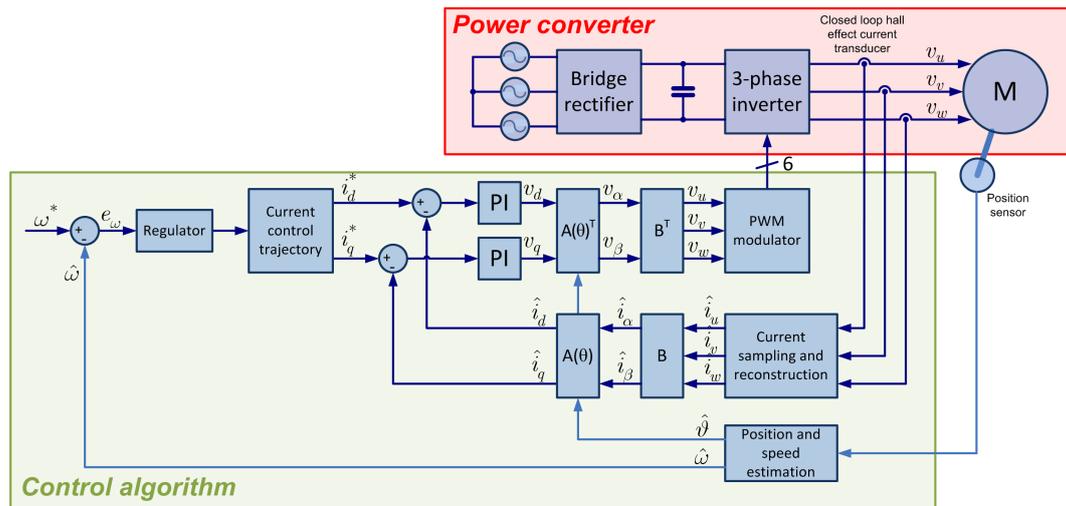


Figure 2. Block scheme of the control for a three-phase motor drive inverter.

Space vector PWM (SVPWM) is the most common kind of modulation for coping with this problem. A constant CMV is not difficult to obtain in principle: it suffices to only use states having the same CMV. Nevertheless, this approach has its own drawbacks, that in some cases prevent its use. Many authors have pursued a reduction of the CMV employing variations of the basic SVPWM [18–20]. In principle, each technique has its own drawbacks, like distortion, partial elimination of the CMV [19], or increased current ripple. This section reports a brief survey of existing reduced CMV PWMs (RCMV-PWM).

Unlike SVPWM, which uses of all the possible space vectors, RCMV-PWM methods employ only subsets of the active ones [19]. These methods are briefly described in the following, while vector patterns for each are listed in Table 1 considering the operating regions defined in Figure 3.

- Active Zero-State (AZSPWM): two opposite active vectors are used in place of the zero-voltage vectors  $V_0$  and  $V_7$ . Three variations on this idea (AZSPWM1-3) can be found in literature; they differ in the adoption of different combinations of opposite vectors.
- Remote States (RSPWM): this method uses three active vectors  $120^\circ$  apart. Two groups are determined ( $V_2$ - $V_4$ - $V_6$  and  $V_1$ - $V_3$ - $V_5$ ) and, within each group, different vector sequences can be chosen. Four variations can be found in literature for this type of modulation, referred to as RSPWM1, RSPWM2A, RSPWM2B, and RSPWM3.
- Near States (NSPWM): given a reference, the closest voltage vector and its two neighbors are used. They are sequenced to minimize the number of switching events. Within each sampling interval there is one of the bridge legs undergoing zero switching events.
- Discontinuous (DPWM): differs from regular SVPWM for using only one of the two zero states; therefore, CMV undergoes one less step of variation.

Each RCMV-PWM technique yields different frequency and polarity of CMV. RSPWM1 and RSPWM2 have theoretically no CMV variation, which is the most favorable condition. In RSPWM3, CMV is constant for each  $60^\circ$  interval. With AZSPWM2 and AZSPWM3, the CMV has the same frequency as the PWM, but with smaller steps relative to SVPWM. All the other techniques have higher CMV frequency and/or step size, therefore they are less attractive. SVPWM, AZSPWM1, DPWM1, and NSPWM result in inverter legs switching one at a time, while all the other RCMV-PWMs techniques determine simultaneous switching of two legs. This causes large (sometimes intolerably so) output ripple due to line-to-line output voltage reversals.

In conclusion, only NSPWM and AZSPWM1 are practical methods for reducing the CMV in two-level three-phase motor drives.

Figure 4 shows the output voltage generation of the different modulation strategies, highlighting the eligible voltage vectors. A reference voltage in the first sextant is considered and the length of the used vectors is proportional to the time they are applied.



Figure 3. Definition of A- and B-regions on the space vector (SV) diagram.

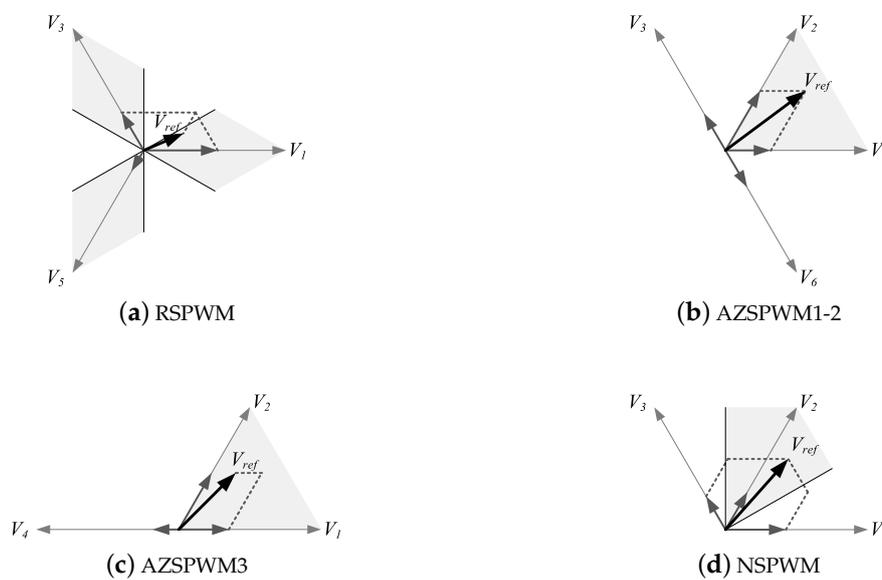


Figure 4. Reference voltage formation for the RCMV-PWM. Shaded areas indicate the regions where the depicted sets of vectors are employed.

Table 1. Vector patterns for various space-vector methods.

| SV Method | A1      | A2      | A3      | A4      | A5      | A6      |       |       |       |       |       |       |    |
|-----------|---------|---------|---------|---------|---------|---------|-------|-------|-------|-------|-------|-------|----|
| SVPWM     | 7210127 | 7230327 | 7430347 | 7450547 | 7650567 | 7610167 |       |       |       |       |       |       |    |
| AZSPWM1   | 3216123 | 4321234 | 5432345 | 6543456 | 1654561 | 2165612 |       |       |       |       |       |       |    |
| AZSPWM2   | 6213126 | 1324231 | 2435342 | 3546453 | 4651564 | 5162615 |       |       |       |       |       |       |    |
| AZSPWM3   | 12421   | 23532   | 34643   | 45154   | 56265   | 61316   |       |       |       |       |       |       |    |
| RSPWM1    | 31513   | 31513   | 31513   | 31513   | 31513   | 31513   |       |       |       |       |       |       |    |
| RSPWM2A   | 31513   | 13531   | 13531   | 15351   | 15351   | 31513   |       |       |       |       |       |       |    |
| RSPWM2B   | 42624   | 42624   | 24642   | 24642   | 26462   | 26462   |       |       |       |       |       |       |    |
|           | B1      | B2      | B3      | B4      | B5      | B6      |       |       |       |       |       |       |    |
| RSPWM3    | 31513   | 42624   | 13531   | 24642   | 15351   | 26462   |       |       |       |       |       |       |    |
| NSPWM     | 21612   | 32123   | 43234   | 54345   | 65456   | 16561   |       |       |       |       |       |       |    |
|           | B1      | A1      | B2      | A2      | B3      | A3      | B4    | A4    | B5    | A5    | B6    | A6    | B1 |
| DPWM1     | 72127   |         | 23032   |         | 74347   |         | 45054 |       | 76567 |       | 61016 |       |    |
|           |         | 21012   |         | 72327   |         | 43034   |       | 74547 |       | 65056 |       | 76167 |    |
| DPWM2     | 72127   |         | 23732   |         | 74347   |         | 45754 |       | 76567 |       | 61716 |       |    |
|           |         | 21712   |         | 72327   |         | 43734   |       | 74547 |       | 65756 |       | 76167 |    |

### 3. Modulations for the H8 Architecture

The main idea behind the proposed H8 inverter is the reduction of the CMV by decoupling the AC and DC sides with power switches [16]; this strategy has already been proven effective for single-phase photovoltaic inverters. A dedicated PWM technique was developed for CMV reduction alongside the proposed H8 architecture, exploiting the SVM degrees of freedom.

#### 3.1. Architecture of the Converter

Figure 5 shows the H8 inverter architecture. Deriving from the traditional three-phase bridge structure (H6) with the addition of two switches, it was named “H8”. In addition to the two additional active devices, at the DC side, there is a network composed of a three-level voltage divider and two clamping diodes. The following subsections offer a detailed description of the added parts.

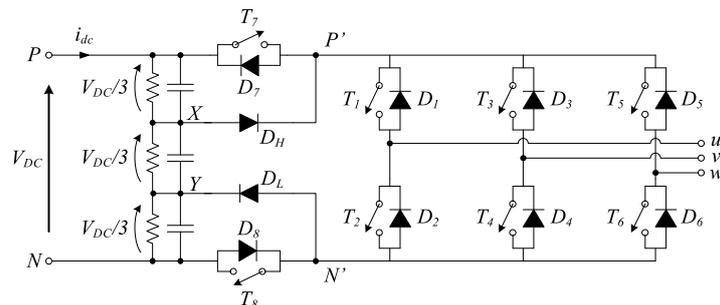


Figure 5. H8 inverter.

#### 3.1.1. Voltage Divider

Three series capacitance form the DC Link, (Figure 6a) with the purpose of obtaining intermediate voltage levels:

$$V_{YN} = \frac{1}{3} V_{DC}, V_{XN} = \frac{2}{3} V_{DC} \tag{1}$$

These two levels are useful to match the CMV values respectively during the odd ( $V_1, V_3, V_5$ ) and even ( $V_2, V_4, V_6$ ) active states, as will be further explained in Section 3.2. In order to ensure a good partition of the voltage across the capacitors (i.e., not determined by their ESRs), three resistors were added in parallel to them and their value has to be as small as possible compatibly with their power losses.

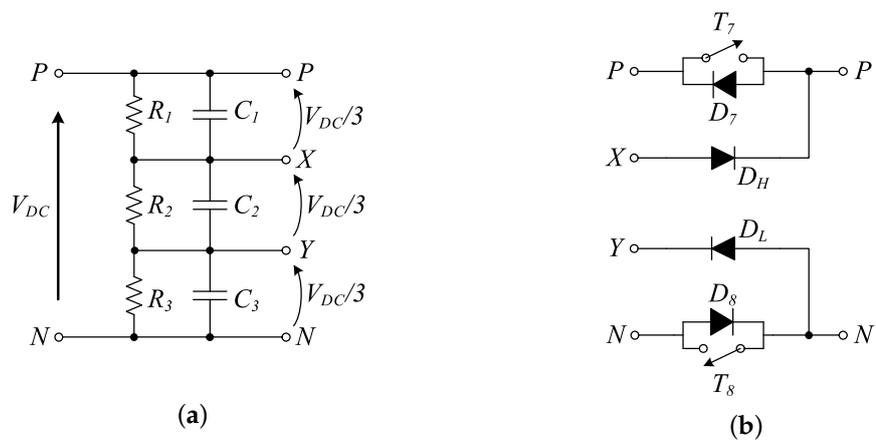


Figure 6. DC side of the H8 inverter: voltage divider (a) and decoupling network (b).

### 3.1.2. DC Decoupling and Voltage Clamping

As shown in Figure 6b, H8 includes two switching devices referred to as  $T_7$  and  $T_8$  which decouple the AC and DC path during the diode free-wheeling. On the contrary, during active states they are kept on, so to ensure the usual conduction path from the DC source to the inverter legs. In this condition they inevitably introduce on-state losses that detriment the overall efficiency of the converter. However, if they are chosen accurately, this drawback can still have an acceptable impact. As a matter of fact, the six H6 devices in the bridge must withstand the entire supply voltage, whereas across  $T_7$  and  $T_8$  only one third of it appears, so they can be chosen with a smaller breakdown voltage, which usually goes with smaller on-state resistance. It is also worth mentioning that, on the other hand, their current rating must be the same as the other six devices.

Moving to the diodes named  $D_H$  and  $D_L$ , the first is placed between the intermediate point of the divider  $X$  and the top bridge rail, labelled as  $P'$ ; reciprocally, the latter is placed between the negative bridge rail ( $N'$ ) and the intermediate point of the divider  $Y$ . The diodes have the function of fixing the floating bridge voltage during the freewheeling phases. Actually, they happen to be off for most of the time, since they are only forced on for a short period, when the inverter enters a zero state. The actual duration of this period depends on the time necessary for the charge redistribution to occur and this, given a certain supply voltage, is ultimately up to physical parameters of the components, such as stray capacitances and resistances. This process is more deeply explained in the following section dedicated to the reduction of the CMV. As a conventional three-phase full bridge, the H8 inverter must introduce a dead-time during the transition between two active vectors. In the usual operation, the decoupling devices are commutated at the same time as the full-bridge ones, making the dead-time compensation the same as the H6 converter. Since  $T_7$  and  $T_8$  are connected in series, there is the possibility to choose different switching instants for the decoupling devices and the full-bridge devices. For example, by switching off the decoupling device before the corresponding full-bridge one during a state transition, one of the  $D_H$  or  $D_L$  diodes would be forced to carry the current, increasing the speed of the  $V_{CM}$  transient. During this intermediate state, the effective output voltage would be the same as the corresponding resistive divider. The drawbacks of this operation mode are the possibility to unbalance the capacitive divider, to increase the current rating of the diodes, and to make the dead-time compensation a more challenging task.

Although it would be theoretically possible to choose any voltage subdivision, choosing to divide the DC voltage into three equal parts allows to match the intrinsic  $V_{CM}$  configuration of the H6 modulation, as shown in Table 2.

### 3.2. Common-Mode Voltage Variations Reduction

Together with the H8 architecture, this paper proposes a particular SVM aimed at reducing CMV variations, called constant common-mode voltage SVM (CCMV SVM) [16]. CCMV SVM uses a subset of the possible voltage vectors, alternating between using the odd and the even numbered states only and simultaneously commanding the decoupling switches  $T_7$  and  $T_8$  with a definite pattern. This yields a constant CMV of  $V_{DC}/3$  or  $2V_{DC}/3$  (Table 2, rightmost column). The main drawback is that this technique can be used only for modulation indexes up to 0.5 [16].

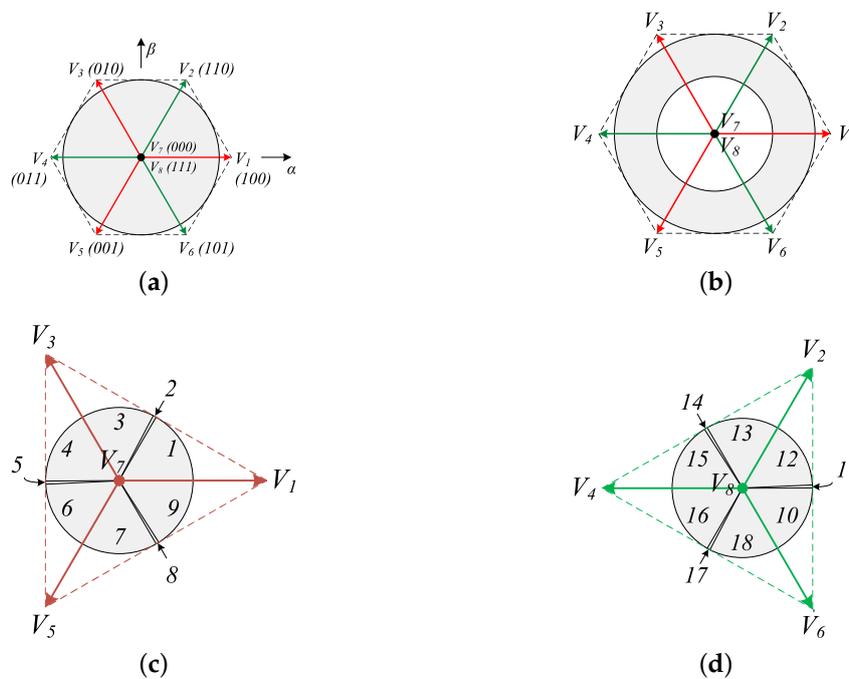
Table 2 shows the inverter output common mode voltage values both for a conventional H6 three-phase inverter and for the H8 inverter with the CCMV SVM. With H6, the CMV varies from 0 to  $V_{DC}$ , undergoing a  $V_{DC}/3$  step at each commutation. The H8 converter, on the other hand, presents two values of CMV:  $2V_{DC}/3$  for the even states, and  $V_{DC}/3$  for the odd ones, thanks to the decoupling devices  $T_7$  and  $T_8$  on the DC side and to the clamping diodes  $D_L$  and  $D_H$ .

**Table 2.** Common-mode voltage ( $V_{CM}$ ) values.

| Vector | $\frac{V_{uN}}{V_{DC}}$ | $\frac{V_{vN}}{V_{DC}}$ | $\frac{V_{wN}}{V_{DC}}$ | $\frac{V_{CM}}{V_{DC}}$ |     |
|--------|-------------------------|-------------------------|-------------------------|-------------------------|-----|
|        |                         |                         |                         | H6                      | H8  |
| $V_1$  | 1                       | 0                       | 0                       | 1/3                     | 1/3 |
| $V_2$  | 1                       | 1                       | 0                       | 2/3                     | 2/3 |
| $V_3$  | 0                       | 1                       | 0                       | 1/3                     | 1/3 |
| $V_4$  | 0                       | 1                       | 1                       | 2/3                     | 2/3 |
| $V_5$  | 0                       | 0                       | 1                       | 1/3                     | 1/3 |
| $V_6$  | 1                       | 0                       | 1                       | 2/3                     | 2/3 |
| H6     | $V_7$                   | 0                       | 0                       | 0                       |     |
|        | $V_8$                   | 1                       | 1                       | 1                       | 1   |
| H8     | $V_7$                   | 1/3                     | 1/3                     | 1/3                     | 1/3 |
|        | $V_8$                   | 2/3                     | 2/3                     | 2/3                     | 2/3 |

### 3.3. Space Vector Modulation

The CCMV SVM adopted for driving the H8 inverter aims to make CMV vary as little as possible. As another mandatory feature, the converter must ensure single-leg commutations, in order for the modulation to be actually feasible. Figure 7a shows the space vector representation with the corresponding full-bridge configuration in the  $\alpha\beta$  plane that will be used in the following analysis. As stated above, the main drawback of this modulation technique is that it applies only to modulation indexes less than 0.5 (shaded areas in Figure 7c,d). Therefore, a different PWM scheme must be used whenever higher modulation indexes are needed. Traditional SVPWM with DC side decoupling during the inactive states can be adopted in such cases, extending the modulation index range up to  $\sqrt{3}/2$  (shaded area in Figure 7b). SVPWM performs worse than CCMV SVM in terms of CMV; nevertheless, it performs better with the H8 topology than it would if it was used with a conventional three-phase inverter. The two following subsections give a detailed description of the two modulation strategies.



**Figure 7.**  $\alpha\beta$  plane space vector diagrams. Odd vectors (red), even vectors (green). (a) SV vectors. (b) Modulation index region where SVPWM is used ( $0.5 \leq m < \sqrt{3}/2$ ). (c) Feasibility region ( $m < 0.5$ ) and modulation zone numbers for odd CCMV SVM. (d) Feasibility region ( $m < 0.5$ ) and modulation zone numbers for even CCMV SVM.

### 3.3.1. Constant Common-Mode Voltage Space Vector Modulation (CCMV SVM)

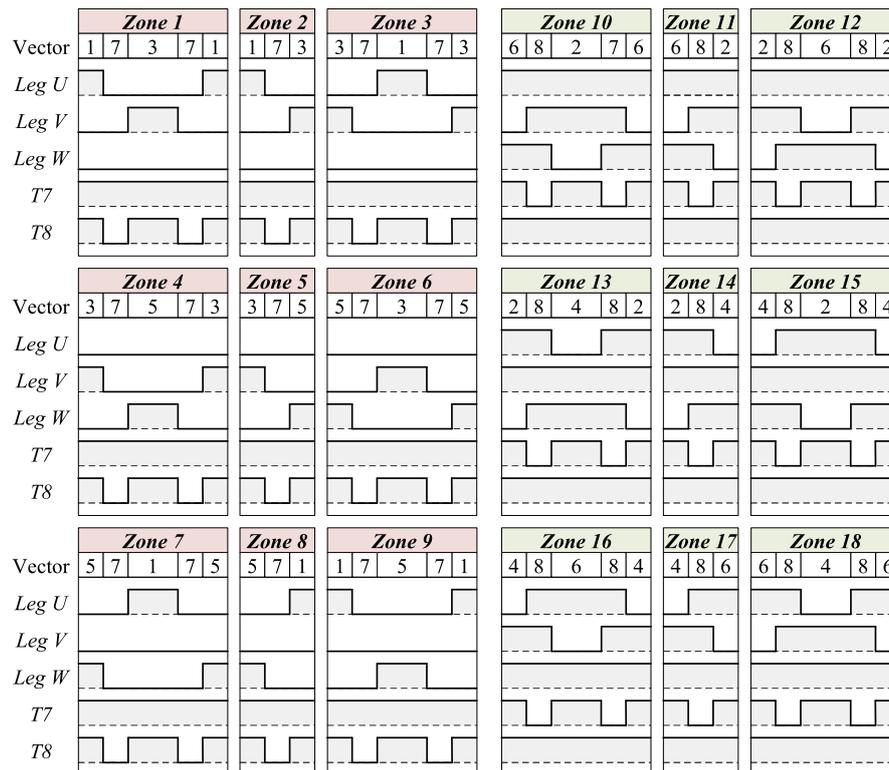
CCMV SVM maintains a constant output CMV, using only vectors with the same  $V_{CM}$ . Table 2 shows the  $V_{CM}/V_{DC}$  ratio for the eight SVM states. It is easy to calculate that even active vectors ( $V_2, V_4$  and  $V_6$ ) have  $V_{CM} = 2V_{DC}/3$ , while odd active vectors ( $V_1, V_3$  and  $V_5$ ) have  $V_{CM} = V_{DC}/3$ . This is true also for the H6, as documented by the thriving literature of optimized modulations that achieve constant common mode voltage [18]. One drawback is that those modulations do not use any inactive vectors ( $V_7, V_8$ ), resulting in more than one bridge leg commutating simultaneously. If the H8 architecture is adopted, thanks to DC decoupling,  $V_{CM}$  values for the inactive vectors are equal to those of the active states, so that it is possible to maintain the CMV constant using all the odd vectors, active and inactive ( $V_1, V_3, V_5$  and  $V_7$ ), or using the even ones ( $V_2, V_4, V_6$  and  $V_8$ ). As already mentioned, on each transition from an active vector to an inactive one, the CMV equals  $4V_{DC}/9$  or  $5V_{DC}/9$ , causing a  $\pm 2V_{DC}/9$  variation of the CMV.

The reference vector is synthesized in the  $\alpha\beta$  plane switching between the two nearest odd or even vectors with the addition of the proper (odd or even) inactive state. The vectors that can be reached using this modulation technique are inside two equilateral triangles with vertices on the used active vectors (Figure 7c,d). The highest modulation index that can be maintained throughout the full circle is 0.5. SVPWM is used for higher modulation indexes, as described in Section 3.3.2.

The  $\alpha\beta$  plane can be divided into several zones. Considering the odd vectors (Figure 7c), there are six  $60^\circ$ -wide zones (nr. 1, 3, 4, 6, 7 and 9), plus 3 very narrow slices (zones 2, 5 and 8). The narrow zones are for representing space vector states used for just a single PWM period, and are necessary for having a smooth transition between the two adjacent zones. An equivalent zone partition can be adopted if even vectors are used. Table 3 reports the vectors used in all the zones for both even and odd vectors CCMV SVM. In order to obtain symmetrical switching periods, one of the two active states in the  $60^\circ$ -wide zones is equally divided in two time slots placed at the beginning and end of each sequence. Figure 8 shows the output pulse pattern obtained during a switching period for each  $\alpha\beta$  plane zone, for even and odd vectors. For the narrow slices (zones 2, 5, 8, 11, 14 and 17), no symmetry is necessary. Moreover, the position of these zones in the  $\alpha\beta$  plane means that the modulation values for the two active states will be approximately the same. Since they have only three states instead of five, these intermediate states last half as long as the others, to limit the output current ripple.

**Table 3.** Vectors used in the CCMV SVM strategy.

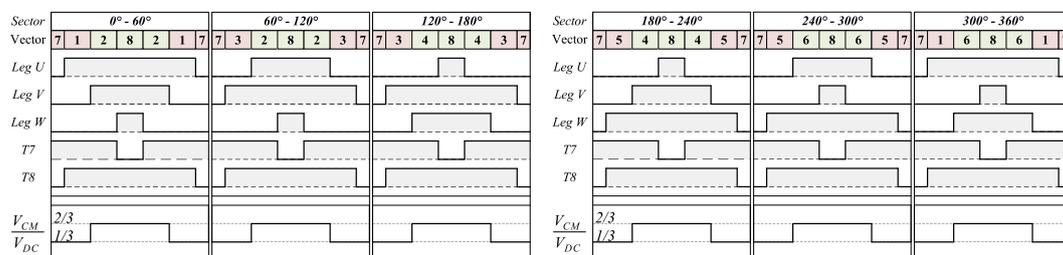
| Angles                    | Odd Vectors     | Even Vectors    |
|---------------------------|-----------------|-----------------|
| $0^\circ$ – $60^\circ$    |                 | $V_2, V_6, V_8$ |
| $60^\circ$ – $120^\circ$  | $V_1, V_3, V_7$ | $V_2, V_4, V_8$ |
| $120^\circ$ – $180^\circ$ |                 | $V_2, V_4, V_8$ |
| $180^\circ$ – $240^\circ$ | $V_3, V_5, V_7$ |                 |
| $240^\circ$ – $300^\circ$ |                 | $V_4, V_6, V_8$ |
| $300^\circ$ – $360^\circ$ | $V_5, V_1, V_7$ | $V_2, V_6, V_8$ |



**Figure 8.** State sequences for CCMV SVM in H8 converter. Zones from 1 to 9 employ odd vectors, zones from 10 to 18 even ones.

### 3.3.2. Space-Vector Modulation

Considering the voltage limit of the CCMV SVM, when the modulation index exceeds 0.5, an automatic switch to the SVPWM is performed. The duration of inactive vectors during each PWM period is equally divided between  $V_7$  and  $V_8$ ; therefore, each sequence has a central symmetry and active states are placed to minimize the switching events with respect to the adjacent inactive states. The DC decoupling switches T7 and T8 are turned off during the zero states. The resulting pulse pattern is shown in Figure 9, along with the evolution of CMV. It is worth mentioning that this modulation applied to a traditional three-phase converter would exhibit CMV varying from zero to  $V_{DC}$  within each PWM period, whereas the H8 architecture limits the  $V_{CM}$  excursion to  $V_{DC}/3 \div 2V_{DC}/3$ . In comparison to CCMV SVM, more common-mode voltage is present, but still the H8 structure helps to keep its excursion limited.



**Figure 9.** Vectors usage and switch pulse pattern throughout the rotational period for the SVPWM. Only one PWM period is presented. Red represents the odd vectors, whereas green the even ones.

## 4. Experimental Results

A prototype of the proposed H8 converter architecture was designed, fabricated and deeply tested. The prototype can be easily converted to H6 topology by disabling T7 and T8 gate drivers

and short-circuiting the associated switching devices. In this way H6 SVPWM, H8 SVPWM and H8 CCMV SVM solutions can be implemented and tested using the same prototype, allowing an easy comparison between the three solutions in terms of power quality and efficiency, while a comparison between silicon IGBTs and wide band-gap (SiC) power MOSFETs can be done, simply replacing the switching devices.

The load of the converter was a three phase RL configuration, using a star connection ( $10 \Omega + 2$  mH for each phase); while the bus voltage was fixed at 250 V. The prototype uses a PWM frequency of 10 kHz, and produces, at the output, a fundamental frequency of 50 Hz. Although the impedance of the RL load is different from that of an electrical machine, which would have a small resistance and a back electromotive force, this experimental setup can still be used to evaluate the efficiency and common mode voltage performance, since they do not depend on the load but only on the power converter.

#### 4.1. H6 versus H8: Power Quality and Efficiency

According to [16], CMV reduction is a key element for both electric drives and photovoltaic applications. As it can be seen from Figures 10 and 11, H8 CCMV SVM excels for the  $v_{cm}$  harmonic content. Using the H8 topology and the proposed CCMV SVM, all the harmonics in the spectrum are lower, as summarized in Table 4.

Regarding the line to line output voltage ( $v_{out}$  in the following), H6 SVPWM, H8 SVPWM perform in a very similar way as depicted in Figure 12, while H8 CCMV SVM shows a similar behavior for all the harmonics components except for the 10 kHz harmonic, that is about 15 dB higher, and a lower spectral components around 250 kHz (as highlighted in the box in Figure 12).

**Table 4.** Harmonic content comparison between H8 CCMV SVM and H6 SVPWM.

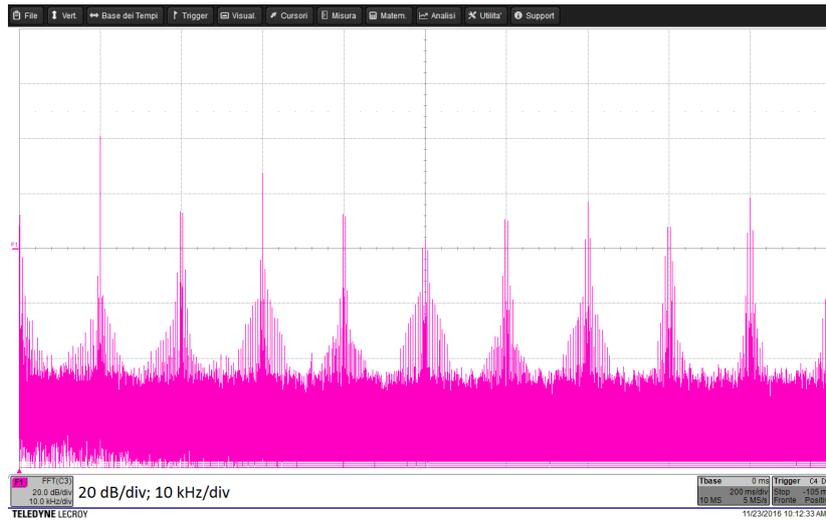
| Harmonic | Reduction H8 CCMV SVM vs. H6 SVPWM [dB] |
|----------|---|
| 1st      | −28                                     |
| 2nd      | 0                                       |
| 3rd      | −28                                     |
| 4th      | −4                                      |
| 5th      | −8                                      |
| 6th      | −16                                     |
| 7th      | −16                                     |

After this comparison in terms of spectral quality, the behavior in terms of efficiency was investigated comparing traditional silicon IGBTs and SiC power MOSFETs. At first the prototype was tested using Infineon IKW50N650H5 IGBTs as switching devices. Efficiency tests were made using H6 SVPWM, H8 SVPWM and H8 CCMV SVM configurations. As expected, Figure 13 confirms that H6 SVPWM performs better than the other two configurations regardless of the value of the modulation index  $m$ .

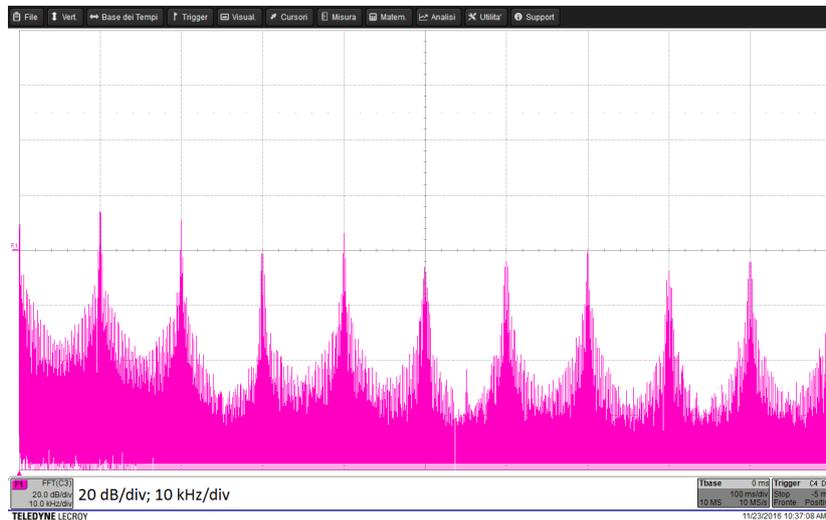
H8 CCMV SVM, on the other hand, can work with modulation indexes up to ( $m = 0.45$ ), and in this condition it features an efficiency only 0.5% lower than the best in class H6 SVPWM. The losses are 31.2 W for H8 CCMV SVM versus 26.4 W for H6 SVPWM (+18%), as summarized in Table 5.

**Table 5.** Comparison between H6 SVPWM, H8 SVPWM and H8 CCMV SVM with Silicon IGBT.

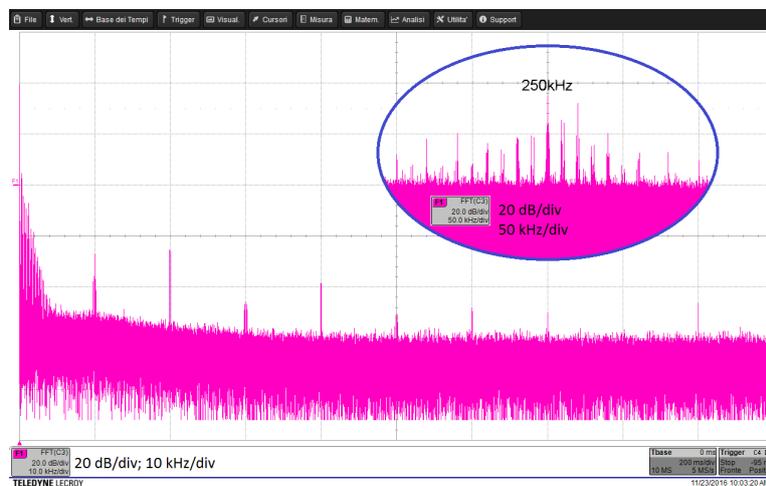
| Architecture | $m = 0.45$ |                | $m = 0.85$ |                |
|--------------|------------|----------------|------------|----------------|
|              | $\eta$ (%) | $P_{loss}$ (W) | $\eta$ (%) | $P_{loss}$ (W) |
| H6 SVPWM     | 96.8       | 26.4           | 98.1       | 55             |
| H8 SVPWM     | 95.1       | 39.7           | 95.5       | 102            |
| H8 CCMV SVM  | 96.3       | 31.2           | n.a.       | n.a.           |



**Figure 10.** CMV spectrum; H6 architecture and SVPWM. Modulation index  $m = 0.4$ . Frequency range of 0–100 kHz.



**Figure 11.** CMV spectrum; H8 architecture and CMMV SVM. Modulation index  $m = 0.4$ . Frequency range of 0–100 kHz.



**Figure 12.** Spectral analysis of the voltage output of H6 converter. Frequency range of 0–100 kHz in the main figure, 200–300 kHz in the small round box [17].

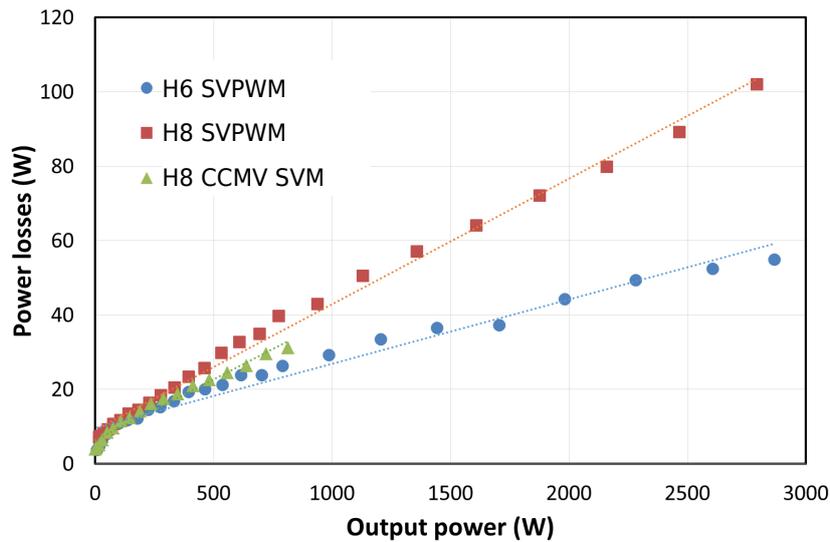


Figure 13. Power losses of silicon IGBTs versus output power [17].

Rohm SCT2120AF SiC power MOSFETs, (650 V, 29 A) are then used for the next batch of tests. With a modulation index up to  $m = 0.45$  it is possible to compare the three solutions, Figure 14 shows the results, while Table 6 reports some analytical data. Using SiC power MOSFETs, H6 results better than H8.

Table 6. Efficiency and total power loss comparison among H6 SVPWM, H8 SVPWM and H8 CCMV SVM. SiC power MOSFETs switching devices [17].

| Architecture | $m = 0.45$ |                | $m = 0.85$ |                |
|--------------|------------|----------------|------------|----------------|
|              | $\eta$ (%) | $P_{loss}$ (W) | $\eta$ (%) | $P_{loss}$ (W) |
| H6 SVPWM     | 97.7       | 19.2           | 98.9       | 32.6           |
| H8 SVPWM     | 96.9       | 25.5           | 97.1       | 85.6           |
| H8 CCMV SVM  | 97.1       | 24.3           | n.a.       | n.a.           |

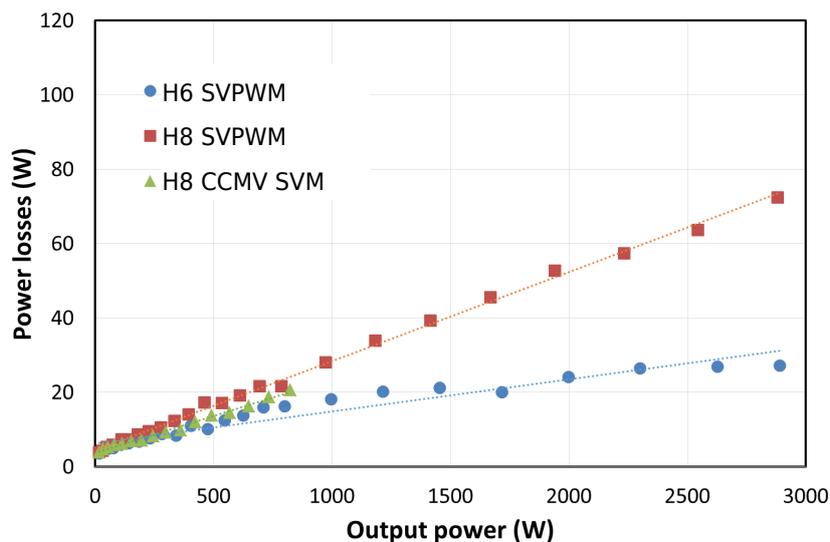


Figure 14. Power losses of SiC power MOSFETs versus output power [17].

#### 4.2. Performance Comparison

The comparison between Si and SiC two production technologies is a hot research topic. The experiments compare H6 SVPWM, H8 SVPWM and H8 CCMV SVM architectures (Figures 15 and 16).

SiC devices perform better than the traditional silicon ones for all modulation indexes and for all the proposed architectures. Using H6 SVPWM configuration at high modulation index, the SiC devices efficiency is 0.82% better than using silicon IGBTs, and total power losses are 40% smaller. Having lower losses would allow for a reduced heatsink with a thermal resistance 67% higher. Close to the maximum modulation index for the CCMV SVM ( $m = 0.45$ ), a higher efficiency (+0.83%) is achieved by SiC devices.

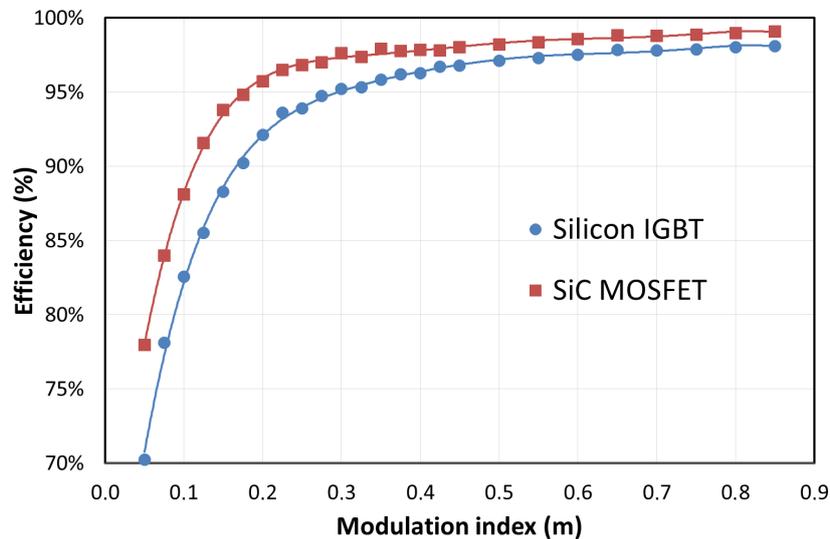


Figure 15. Efficiency comparison with different semiconductors: H6 SVPWM architecture [17].

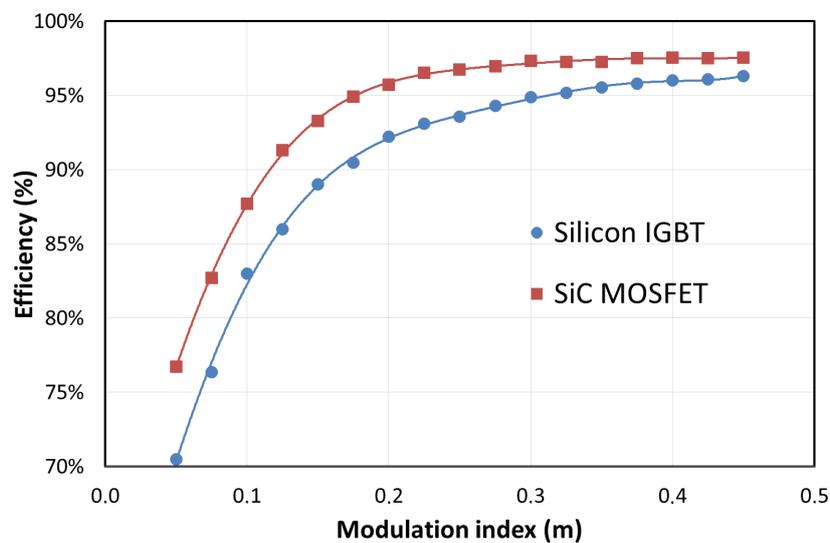


Figure 16. Efficiency comparison with different semiconductors: H8 CCMV SVM architecture [17].

## 5. Reliability Study

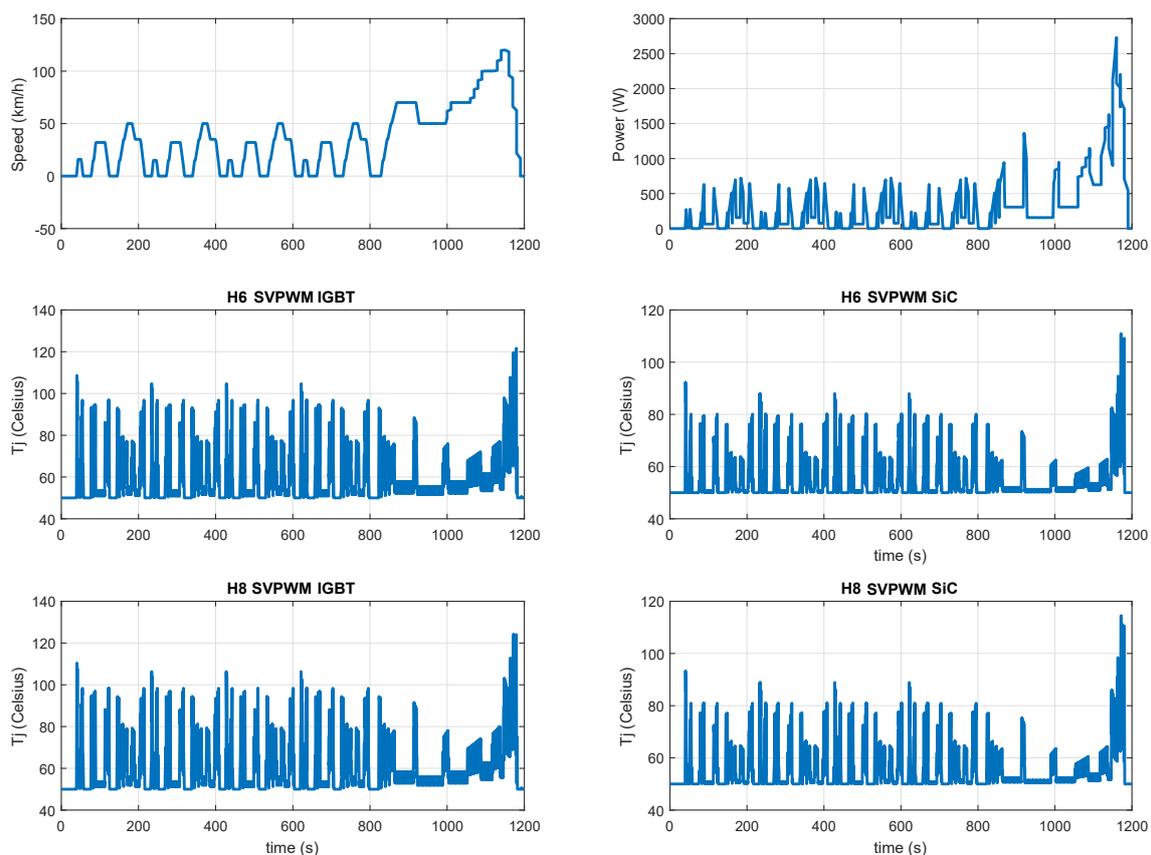
The efficiency and the power quality of a power electronics converter are only one aspect of the whole system. Although the use of SiC devices does not allow for an improvement in the common-mode voltage generation, the efficiency improvement is unmistakable. However, the SiC semiconductor results in additional cost and efficiency alone is normally not enough to motivate it. An increased efficiency can result in a reduced volume of the heatsink or in the possibility to increase the frequency to reduce the weight of the magnetic components. In the following a different analysis is performed, aiming at quantifying the benefits in terms of lifetime extension of a SiC converter with the

same thermal design of an Si one. This question is of industrial interest, because of the possibility to re-use existing thermal designs and the possibility to decrease the maintenance of the products [21,22].

The Coffin-Manson-Arrhenius formula is a well-known model to estimate the module's lifetime given its mission profile [23] (2). The number of cycles until failure  $N_f$  is calculated depending on the average operating temperature  $T_{jm}$  and on the amplitude of the thermal cycles  $\Delta T_j$ .  $k_B$  is the Boltzmann constant, while coefficients  $a$ ,  $\alpha$ , and  $E_a$  are usually chosen to fit the equation upon the results of multiple reliability experiments [24].

$$N_f = a \cdot \Delta T^{-\alpha} \cdot e^{\frac{E_a}{k_B T_{jm}}} \quad (2)$$

As an application example, referring to a motor drive for an electric vehicle, the New European Driving Cycle (NEDC) was chosen as a reference; it refers to a specific speed profile as shown at the top of Figure 17. Several assumptions have been made to match this profile with the devices chosen for this analysis. Considering a maximum electrical frequency of 100 Hz and a peak current amplitude of 15 A, the second plot of Figure 17 shows the converter's output power. It is possible, by taking as a reference the datasheet values and an identical thermal design (considering devices packaged in the same power module), to estimate the losses and, consequently, to calculate the resulting junction temperature, as shown for the T1 device at the bottom of Figure 17 for different semiconductor technologies and modulation. The full-bridge devices experience the most severe losses, because they are always carrying the current, differently from the DC devices.



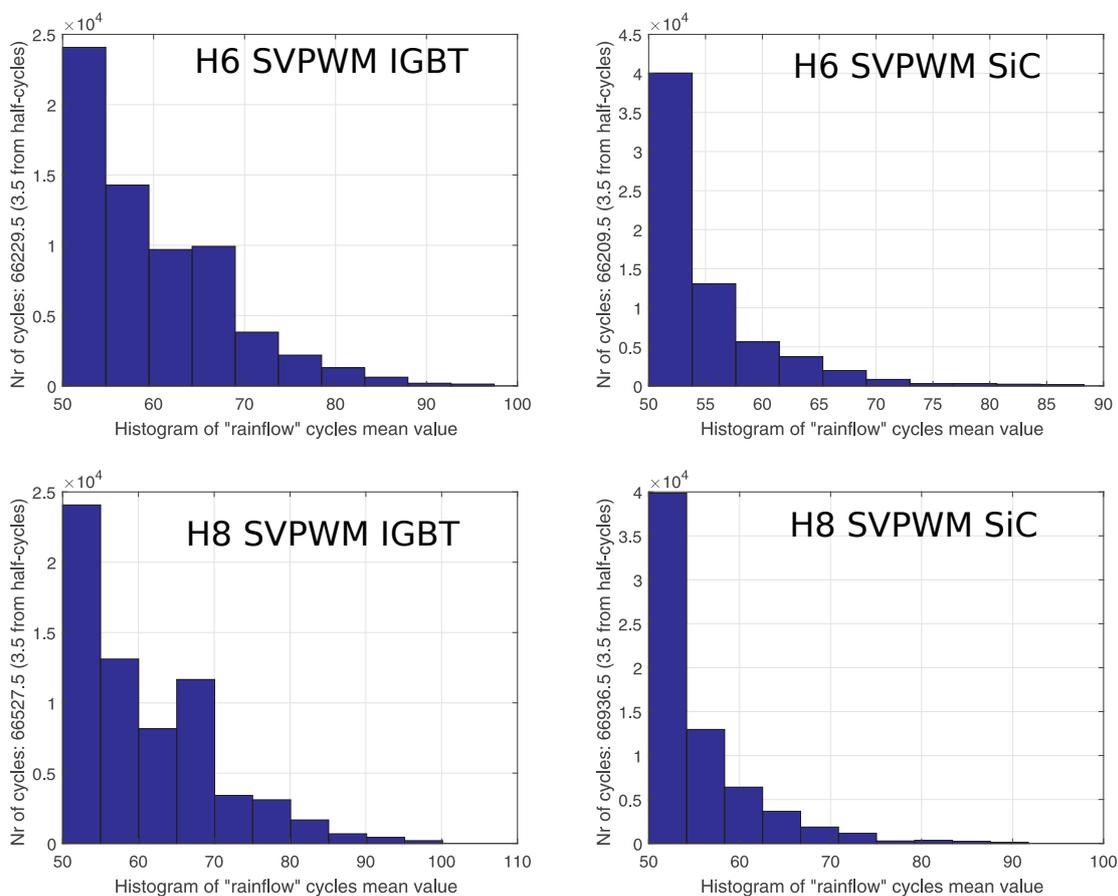
**Figure 17.** Junction temperature evaluation with silicon IGBTs and SiC power MOSFETs according to the New European Driving Cycle.

A Rainflow cycle counting procedure is then applied to these profiles, obtaining the graphs of Figure 18. Considering one hour of average usage per day of the electric car, it is possible to calculate the overall lifetime of the converter by dividing the length of the cycle by the accumulated damage.

The results are shown in Table 7. As can be seen, the lower efficiency of the H8 converter is paid in terms of a reduced lifetime. The reduction is not excessive, because the losses are spread over a greater number of devices, so the lifetime decrease is due to an increase of the case temperature. What is interesting, is that the higher efficiency of SiC devices can reduce the damage due to thermal stress by a factor 4 on average.

**Table 7.** Expected lifetime forecast through rainflow analysis.

| Case Study    | Lifetime (Years) |
|---------------|------------------|
| H6 SVPWM IGBT | 16.6             |
| H6 SVPWM SiC  | 67.7             |
| H8 SVPWM IGBT | 13.2             |
| H8 SVPWM SiC  | 54.9             |



**Figure 18.** Accumulated damage at different average junction temperatures.

Although different failure modes may occur reducing a module lifetime, the above analysis shows that the use of SiC devices, despite higher initial costs, can strongly reduce damage accumulation. The benefits of increased lifetime expectation may justify the additional costs.

## 6. Conclusions

This paper analyzes the H8 converter applied to the power train of an electrical vehicle. The H8 converter is a modified three-phase bridge with two additional series devices, that decouple the AC load from the power supply during the free-wheeling phase. The main objective is to reduce the common mode voltage, that is a source of electromagnetic interference and decreases the lifetime of

the bearings of the electrical machine. Experiments show a marked reduction in the common mode voltage compared to the standard three-phase bridge. A comparison in terms of efficiency and lifetime between SiC and Si transistors is carried out, showing how the SiC solution allows for a marked increase of efficiency and almost four times the lifetime for the same thermal design. This lifetime extension can compensate for the additional cost of the SiC devices compared to the Si ones.

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