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# A Novel Fault-Tolerant Control of Modular Multilevel Converter under Sub-Module Faults Based on Phase Disposition PWM

**Jingyuan Yin [1,*], Wen Wu [2], Tongzhen Wei [1], Xuezhi Wu [2] and Qunhai Huo [1]**

[1] Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing 100044, China; tzwei@mail.iee.ac.cn (T.W.); huoqunhai@mail.iee.ac.cn (Q.H.)
[2] National Active Distribution Network Technology Research Center, Beijing Jiaotong University, Beijing 100044, China; 17117417@bjtu.edu.cn (W.W.); xzhwu@bjtu.edu.cn (X.W.)
* Correspondence: yinjingyuan@mail.iee.ac.cn; Tel.: +86-138-1151-8632

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**Abstract:** Each arm of modular multilevel converter (MMC) consists of a large number of sub-module (SM) units. However, it also increases the probability of SM failure during the long-term system operation. Focusing on the fault-tolerant operation issue for the MMC under SM faults, the traditional zero-sequence voltage injection fault-tolerant control algorithm is analyzed detailed and its disadvantages are concluded. Based on this, a novel fault-tolerant control strategy based on phase disposition pulse-width modulation (PD-PWM) is proposed in this paper, which has three main benefits: (i) it has carrier and modulation wave dual correction mechanism, which control ability is more higher and flexible; (ii) it only needs to inject zero-sequence voltage in half a cycle of the modulation wave, which simplifies the complexity of traditional zero-sequence voltage injection control algorithms and much easier for implement; (iii) furthermore, the zero-sequence voltage can even be avoided injecting under the symmetrical fault conditions. Finally, the effectiveness of the proposed control strategy is verified with the simulation and experiment studies under different fault conditions.

**Keywords:** modular multilevel converter (MMC); Sub-module (SM) fault; fault-tolerant control; Phase Disposition PWM

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## 1. Introduction

Compared with the traditional two-level converter, modular multilevel converter (MMC) enjoys the advantage of modular design [1,2], which allows MMC good scalability and facilitates the improvement of voltage level, as well as other advantages as many output levels and good harmonic characteristics. Therefore, in recent years, MMC topology converters have been widely studied and applied in high-voltage direct current transmission (HVDC), staticsynchronous compensator (STATCOM), and medium-voltage motor drive [3–6].

In actual transmission projects, in order to adapt to higher transmission voltage level, a large number of sub-modules (SMs) are often cascaded. For example, Trans Bay Cable Project is reported to have 216 SMs per arm [7], and the Zhou Shan multi-terminal flexible HVDC transmission project completed in 2014 in China is larger cascaded reach 250 SMs per arm [8].

As the number of cascaded SMs increasing, the security risks of MMC converters become larger, where the SM faults are prone to occur. When a SM fault occurs and is not processed in time, it may cause system shutdown and even endanger the security of the power grid [9,10]. Therefore, fault-tolerant control approach under SM faults is a problem that needs to be studied.

Generally, the common fault-tolerant control strategies are often designed based on equipping redundant SMs [8]. According to the operation state of the redundant SMs, two main schemes are developed, which are cold-reserve mode and hot-reserve mode, respectively. For the cold-reserve scheme [11,12], it means that the redundant SMs are all in bypassed state when the system operating normally and will replace the same number of faulty SMs when SMs malfunction. For the hot-reserve scheme [13–15], it means that the redundant SMs are all operating identically as the rated SMs. However, there are two further detailed modes under this scheme. We call it hot-reserve mode-a, b, respectively, where hot-reserve mode-a means that simultaneously bypass the same number of faulty SMs in each arm to keep the system strictly symmetrical [13]; and hot-reserve mode-b means that only bypass the faulty SMs [14,15]. Compared to the mode-a, the hot-reserve mode-b scheme can ensure full utilizing of all SMs during normal operation period and can avoid the long changing time for redundant SM capacitors to rated values. Furthermore, some extra healthy SMs may need be bypassed in hot-reserve mode-a, which might induce a greater transient impact on the system when large number of SMs are simultaneously bypassed. Therefore, hot-reserve mode-b is a more preferable redundant option for the MMC since its economic and reliability. However, this scheme also has a potential problem, where the system may operate asymmetric under asymmetrical faults. For ensuring the subsequent stable operation, the corresponding fault-tolerant control approach should be further considered, and this is also what this paper deals with.

Based on the background of hot-reserve mode-b, an energy-balancing-based fault-tolerant control strategy is proposed in [16]. Its main control idea is to increase the SM capacitor voltages on the faulty arms to ensure the energy equalization of each arm, thereby achieving the subsequent balance operation of the system. However, the reference command of the SM capacitor voltage needs to be calculated, and the increased value of SM capacitor voltage will become larger as the number of malfunction SMs increases. The neutral-point shift control method has been applied in the H-bridge cascaded multilevel converter system, which can well solve the problems caused by the module faults [17–20]. Inspired by this idea, the corresponding neutral-point shift control approaches suitable for the MMC system are researched in [15,21]. With injecting the zero-sequence voltage to modify the modulation waves, the converter line-voltages in the grid side are ensured balanced to maintain the system stable operation under SM faults. The advantage of these methods in [15,21] is that they do not need to adjust the SM capacitor voltages in fault arms. Similar to the methods in [15,21], an improved zero-sequence voltage injection fault-tolerant control strategy is proposed in [22]. It simplifies the calculation process of the required zero-sequence voltage. However, the common shortcoming in [15–22] is that they main only consider one arm occurs SM faults. When the upper and lower arm occur SM faults simultaneously, multiple zero-sequence voltages need to be calculated, which increase the complexity of the control method. It should be further improved.

Aiming at this problem and for better deal with the multiple SM fault conditions, also under the background of the redundant SMs equipped with hot reserve scheme and only bypassing the faulty SMs when SMs malfunction, a novel fault-tolerant control strategy is proposed in this paper. Compared to the current approaches, it has three main benefits: (i) it has carrier and modulation wave dual correction mechanism, which control ability is more higher and flexible; (ii) it only needs to inject zero-sequence voltage in half a cycle of the modulation wave, which simplifies the complexity of traditional zero-sequence voltage injection control algorithms and more easier for implement; (iii) furthermore, the zero-sequence voltage can even be avoided injecting under the symmetrical fault conditions. Finally, the effectiveness of the proposed control strategy is verified with the simulation and experiment studies under different fault conditions.

## 2. Basics Principles of MMC

### *2.1. MMC Topology*

A typical three-phase MMC topology is shown in Figure 1. It consists of six symmetrical arms, which can be divided into three units: phase, arm, and SM. $N$ identical SM units and one arm inductance for suppressing the circulating current and the fault current rising rate are connected in series on each arm, and the AC output terminal is taken out from the midpoint of the upper and lower arm inductances connected to each other. In order to enhance the reliability of the system, there are a certain number of redundant SMs.

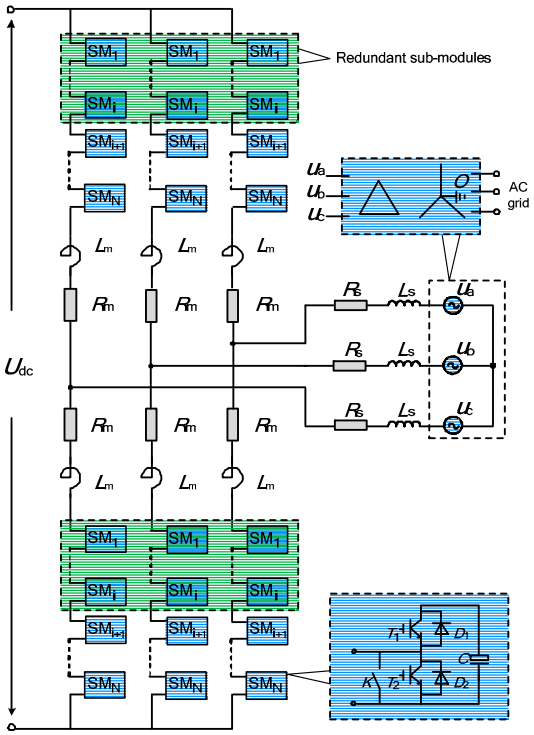


**Figure 1.** Topology structure of three-phase modular multilevel converter (MMC).

Among them, the internal structure of the SM unit has various forms [23–25], and the more common half-bridge SM structure is selected as the research object. Specifically, it is composed of an insulated gate bipolar transistor (IGBT) half bridge, a DC capacitor $C$, and a bypass switch $K$. In the normal working state of the system, the SM capacitor voltage $U_{SM}$ has two levels of output states of 0 and DC capacitor voltage $U_C$. When $T_1$ is turned on and $T_2$ is off, the SM is inserted and outputs $U_C$. When $T_1$ is turned off and $T_2$ is on, the SM is bypassed and output zero. Thus, the AC side multi-level output of the MMC converter can be realized by properly controlling the on-off state of the SM.

### *2.2. Phase Disposition PWM and Voltage Balancing Strategy*

Currently, MMC's commonly used modulation methods include carrier phase shift modulation, phase disposition modulation, and nearest level modulation. Because the phase disposition modulation (PD-PWM) method has better harmonic characteristics and is easier to implement [26,27], in this paper, PD-PWM is selected as the basic modulation strategy in subsequent analysis and experiment.

In addition, in order to reduce the fluctuation of SM capacitor voltage, this paper selects the more common capacitor voltage balancing control based on the sorting algorithm [16,28]. The schematic diagram of the relevant control method is shown in Figure 2. Where $v_j^*$ is the sampled phase voltage of phase j after standard (j = a, b, c). $i_{jp}$ and $i_{jl}$ are the arm current of the upper and lower arm of phase j, respectively. $N_{jsum}$ is the rated total number of the inserted SMs of phase j (i.e., as shown in Figure 1,

it is equal to $N$ if no SM faults occur). $n_{jp}$ is the number of the SMs need to be inserted in the upper arm of phase j, which is obtained from the PD-PWM modulation. $n_{jl}$ is the number of the SMs need to be inserted in the lower arm of phase j, which can be obtained directly by calculating $N_{jsum} - n_{jp}$.

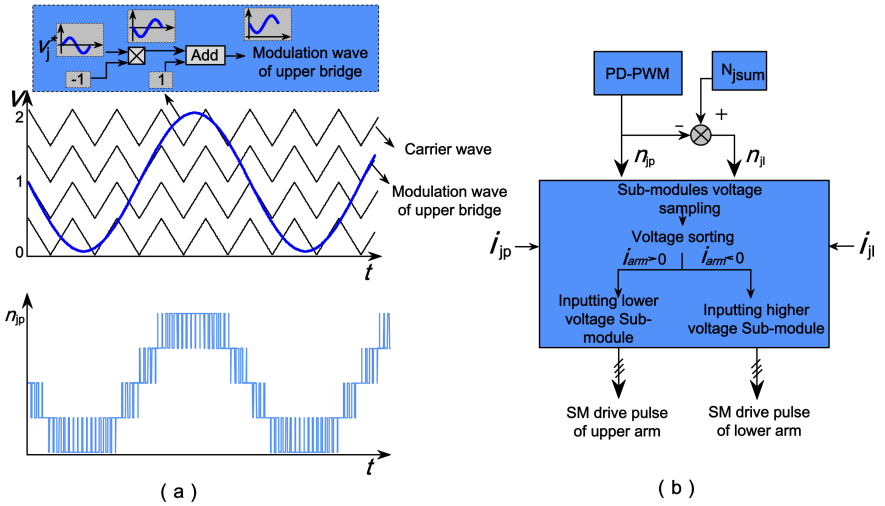


**Figure 2.** Schematic diagram basic control: (**a**) Diagram of the pulse-width modulation (PD-PWM); (**b**) Diagram of the capacitor voltage sorting algorithm.

When the system is operating, the numbers of the SMs need to be inserted in the upper arm $n_{jp}$ and the lower arm $n_{jl}$ are obtained according to the PD-PWM modulation firstly, and then the voltage of each SM in the arm is sorted by the capacitor voltage sorting algorithm. According to the direction of the arm current, the SM with lower capacitor voltage is preferentially charged, and the SM with higher capacitor voltage is preferentially bypassed and discharged, thereby ensuring a relatively balanced voltage of each module during the whole dynamic operation.

## 3. Analysis of the Traditional Zero-Sequence Voltage Injection Control Method

After the SM occur faults, it is easy to know that the phase voltage output ability of the fault phase will be changed, and the neutral-point of the phase voltage in the ac side will be offset accordingly. In order to ensure that the MMC converter can continue stable operation with connected to the grid, the zero-sequence voltages can be injected to ensure the line voltage of the MMC converter remains unchanged before and after the SM faults, thereby realizing the fault-crossing of the SM [22]. The basic modulation diagram of the zero-sequence voltage injection control method is shown in Figure 3. Where Figure 3a depicts the schematic diagram of three-phase modulation waves when only the upper arm of phase occur faults, Figure 3b depicts the schematic diagram of three-phase modulation waves when the upper and lower arms of phase j simultaneously occur faults.

With comparing the Figure 3a,b, it can be observed that if the SM faults only occur only in the upper arm, on the basis of bypassing the faulty SMs, the fault-crossing can be realized by only adding one corresponding zero-sequence voltage component on the modulation wave of each phase. It is easy to achieve. However, if the SM simultaneously occur faults in the upper and lower arms, two injected zero-sequence voltages and the four corresponding correction times $t_1$, $t_1$, $t_1$, and $t_4$ are need to be calculated. In addition, if the numbers of the faulty SMs in the upper and lower arms are not identical, the two required zero-sequence voltages are needed to be calculated respectively. This will increase the complexity of the fault-tolerant control algorithm.

Considering that the location and the time of occurring SM faults are random, the MMC might with (i) the signal faulty arm; (ii) the upper and lower symmetrical faulty arms; and (iii) the upper and lower asymmetrical faulty arms after SMs malfunction. Furthermore, the faulty arms state may be re-changed between the mentioned three states when the SMs fault again. Therefore, in order to ensure

the stable operation of MMC system and flexibly deal with the multiple possible arms faulty states after SMs malfunction, this paper improves the traditional zero-sequence voltage injection control method, and proposes a new fault-tolerant control strategy based on PD-PWM.

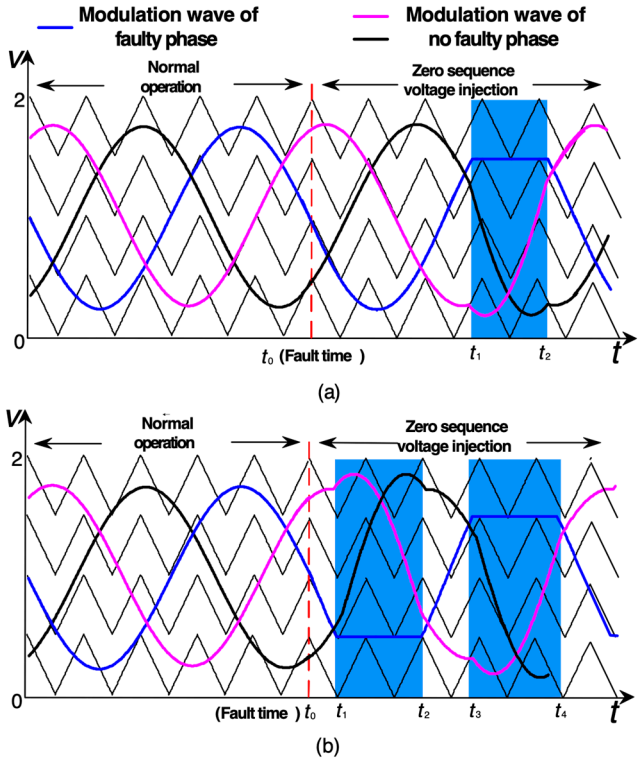


**Figure 3.** Diagram of zero sequence voltage injection modulation: (**a**) Schematic diagram of fault modulation wave of upper arm; (**b**) Schematic diagram of fault modulation wave of upper arm and lower arm.

## 4. Novel Fault-Tolerant Control Strategy

### *4.1. Overall Control Process of the Proposed Fault-Tolerant Control Strategy*

In order to facilitate the later analysis, we define the faulty SM numbers in the upper and lower arms of phase j are $n_{\mathrm{jp\_fau}}$ and $n_{\mathrm{jl\_fau}}$, respectively. At the same time, we assume the modulation ratio of the system is $m$ under the normal operation. When the number of the faulty SMs in the arm satisfies Equation (1), the fault will not affect the normal operation of the system because of itself modulation margin of the system. While when the Equation (1) is not valid, the fault-tolerant control strategy must be inserted to ensure the subsequent stable operation of the MMC converter.

$$\begin{cases} m \leq 1 - \frac{2n_{\mathrm{jp\_fau}}}{\mathrm{N}} \\ m \leq 1 - \frac{2n_{\mathrm{jl\_fau}}}{\mathrm{N}} \end{cases} \tag{1}$$

Figure 4 shows the overall control flow chart of the fault-tolerant control strategy proposed in this paper. It can be divided into three main parts in the process of implementation:

1. Sub module fault handling. Its main task is to block the trigger pulse of the faulty SMs and isolate the faulty SMs through closing the bypass switch.
2. Correction of the modulation state. The main task of this part is that with combining the faulty SM numbers of the fault phase, achieving the correction of the original carrier and modulation waves by adopting the proposed correction algorithm (where its specific implementation method will be discussed in detail in Section 4.2, thereby obtaining the SM numbers that need to be inserted in

each arms after SMs malfunction. In addition, it should be note that this step is the also core part of the fault-tolerant control strategy. In the traditional zero-sequence voltage injection control method, it only with correcting the modulation waves to help achieve the SM fault-crossing. Compared to it, we add the correction algorithm of the carrier waves on the basis of the correction algorithm of the modulation waves, and realized their combination. This effectively simplifies the complexity of traditional control algorithm when deal with multiple arms occurring SM faults.

3. Generation of the SM drive pulses. In this part, with combining the SM numbers that need to be inserted in each arms obtained from the step (2), the drive pulses of the remained healthy SMs are generated by using SM voltage sorting control algorithm, and finally completes the fault-tolerant control.

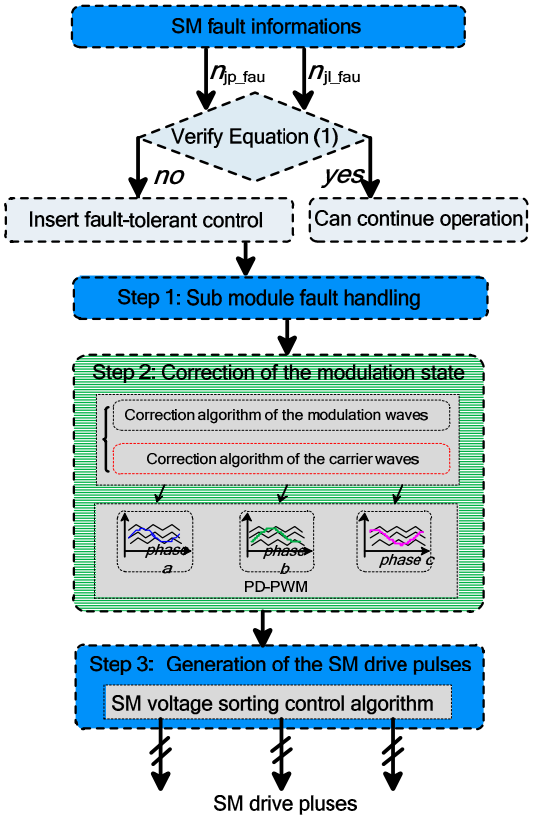


**Figure 4.** Overall flow chart of the proposed fault-tolerant control strategy.

### *4.2. Specific Implementation Method of the Correction of the Carrier and Modulation Waves*

When the system is operation under the normal state, we can depict the modulation diagram of one phase as Figure 5.

As shown in Figure 5, when the MMC system is operating normally, the carrier waves of the $N$ SMs in the upper arm equally distributed in the interval [0, 2] according to the ratio of $\gamma$, where it is easy to know:

$$\gamma = \frac{2}{\mathrm{N}} \tag{2}$$

However, if the SMs occurring faults, the number of SMs that can normally be switched in the faulty phase will be change as the faulty SMs are bypassed. Therefore, the original modulation link must be revised and divided into two parts: 'Correction algorithm of the carrier waves' and 'Correction algorithm of the modulation waves'. We will describe the implementation method detailed in Sections 4.2.1 and 4.2.2, respectively.

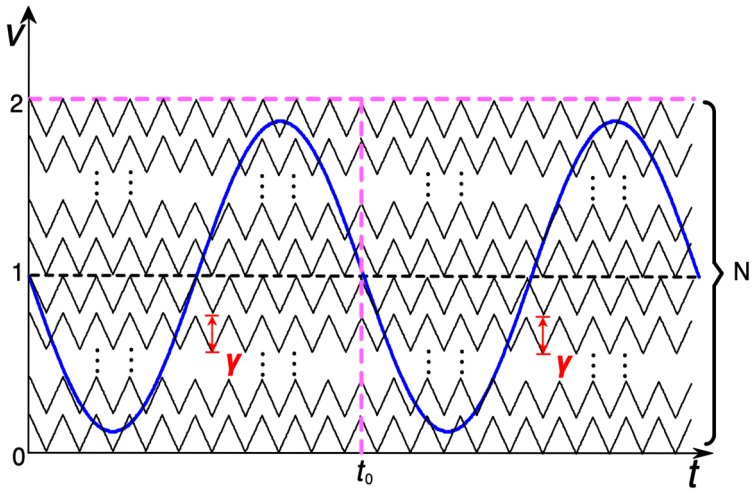


**Figure 5.** Modulation diagram of one phase under the normal operation.

4.2.1. Correction Algorithm of the Carrier Waves

Assuming the SMs occurring faults at $t_0$, and to ensure the generality of the analysis process, supposing the SMs fault in both the upper and lower arms of phase j. Firstly, with comparing the upper arm faulty SM numbers $n_{\mathrm{jp\_fau}}$ and the lower arm faulty SM numbers of $n_{\mathrm{jl\_fau}}$ of phase j, we define the smaller of the two is $\chi_{\mathrm{j}}$, and the larger of the two is $\tau_{\mathrm{j}}$. Thereby we obtain:

$$\chi_{\mathrm{j}} = \min\left[n_{\mathrm{jp\_fau}}\ ,\ n_{\mathrm{jl\_fau}}\right] \tag{3}$$

$$\tau_{\mathrm{j}} = \max\left[n_{\mathrm{jp\_fau}}\ ,\ n_{\mathrm{jl\_fau}}\right] \tag{4}$$

In order to ensure the maximum utilization of the remained healthy SMs, the number of SMs that need to participate in switching operation in the two arms of the fault phase should respectively be:

$$N_{\mathrm{j}\chi} = N - \chi_{\mathrm{j}} \tag{5}$$

$$N_{\mathrm{j}\tau} = N - \tau_{\mathrm{j}} \tag{6}$$

Then, for correcting carrier wave conveniently, the correction coefficient $K_{\mathrm{jc}}$ ($K_{\mathrm{jc}} \geq 1$) about the amplitude of the carrier waves is introduced. Simultaneously, combing the smaller faulty SM number $\chi_{\mathrm{j}}$, we establish a relationship between them, where:

$$K_{\mathrm{jc}} \cdot \gamma = \frac{2}{N - \chi_{\mathrm{j}}} \tag{7}$$

Further, we can obtain:

$$K_{\mathrm{jc}} = \frac{2}{\gamma(N - \chi_{\mathrm{j}})} = \frac{N}{N - \chi_{\mathrm{j}}} \tag{8}$$

Based on the Equation (8), enlarging the amplitude of the carrier waves with the coefficient $K_{\mathrm{jc}}$, we can obtain the initially corrected modulation diagram of the faulty phase as shown in Figure 6. It can be observed that the carrier waves in the interval [0, 2] are re-distributed equally according to the ratio of $K_{\mathrm{jc}}{}^{*}\gamma$ at this time.

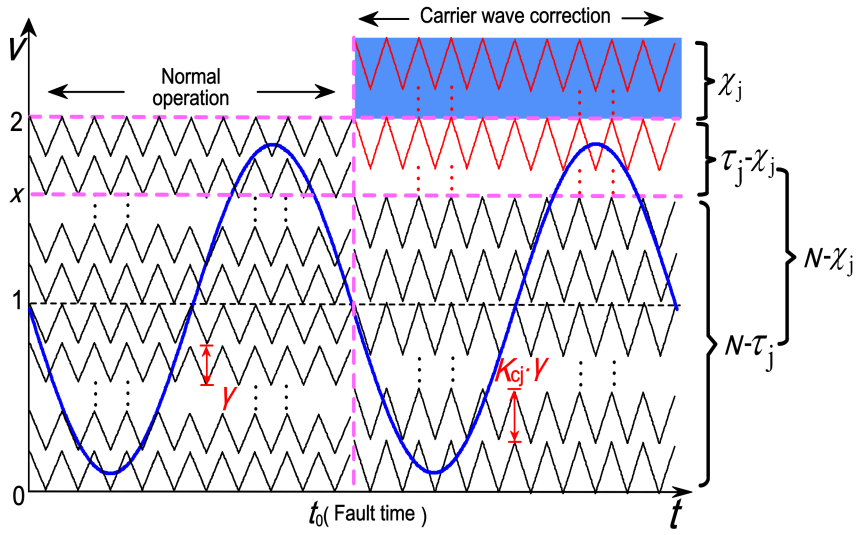


**Figure 6.** Modulation diagram of the faulty phase under carrier wave correction.

Therefore, through the correction algorithm of the carrier waves, we firstly guarantee the SMs on the smaller faulty SM numbers arm can all normally participate in the switching operation. In other words, we can equivalently consider that the MMC is under the 'signal arm fault' state, and its rated SM number is $N_{j\chi} = N - \chi_j$; its faulty SM number is $\tau_j - \chi_j$. Especially, we can found that when the $\tau_j - \chi_j = 0$ (e.g., the faulty SM numbers in the upper and the lower arm are equal), the SM fault-crossing can be achieved only with the carrier wave correction algorithm.

In addition, if the influence of the different faulty SM numbers $\tau_j - \chi_j$ is not considered at present, it can be considered that the fault phase will operate normally according to the newly rated total number of the inserted SMs of phase $N_{jsum} = N_{j\chi}$. Under the control of sorting algorithm, the SM capacitor voltage of the fault phase will automatically be average raised and operating stable [16,28].

4.2.2. Correction Algorithm of the Modulation Waves

As analyzed in the previous section, the faulty phase can be equivalently converted to 'signal arm fault' state with the carrier wave correction algorithm. For further eliminating the effects of the different faulty SM numbers $\tau_j - \chi_j$, we establish the modulation wave correction algorithm, where it is achieved by the zero-sequence voltage injection control method.

Firstly, according to the Figure 6, we can calculate:

$$x = K_{jc} \cdot \gamma \cdot (N - \tau_j) = 2 \cdot \frac{N - \tau_j}{N - \chi_j} \tag{9}$$

Then, according the traditional zero-sequence voltage injection control method [23], the zero sequence voltage that needed to be injected into the initial modulation wave $v_j^*$ of each phase can be obtained by (9):

$$k_{jm}(t) = -v_j^* + (x - 1) \tag{10}$$

Substituting Equations (3), (4) and (9) to (10), we can obtain:

$$k_{jm}(t) = -v_j^* + (2 \cdot \frac{N - \tau_j}{N - \chi_j} - 1) = -v_j^* + (2 \cdot \frac{N - \max\left[n_{jp\_fau}\,,\, n_{jl\_fau}\right]}{N - \min\left[n_{jp\_fau}\,,\, n_{jl\_fau}\right]} - 1) \tag{11}$$

Based on the Figure 6, injecting the zero-sequence voltage $k_{jm}(t)$ in the interval $[t_1, t_2]$, we can obtain the final corrected modulation diagram of the faulty phase as shown in Figure 7.

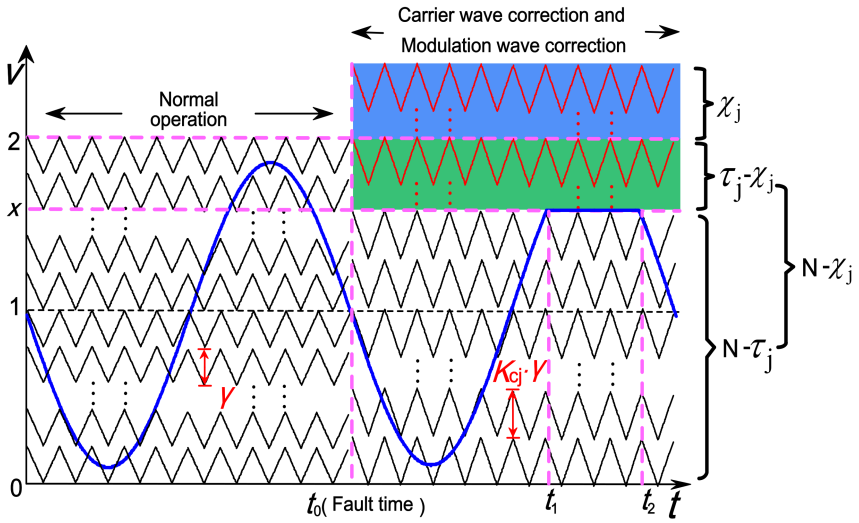


**Figure 7.** Final modulation diagram of the faulty phase under fault-tolerant control.

In addition, assuming the sampled phase voltage of phase j after the standard is:

$$v_j{}^* = m\sin(\omega t + \varphi_j) \tag{12}$$

where, $\varphi_j$ denotes the initial phase angle of the phase voltage. Combining Equations (9) and (11), the corresponding times $t_1$ and $t_2$ in one modulation period can be calculated respectively:

$$\begin{cases} t_1 = \dfrac{\arcsin[(1-2\cdot\frac{N-\tau_j}{N-\chi_j})/m]-\varphi_j}{\omega} \\ t_2 = \pi - \dfrac{\arcsin[(1-2\cdot\frac{N-\tau_j}{N-\chi_j})/m]-\varphi_j}{\omega} \end{cases} \tag{13}$$

Based on the above analysis, the overall implementation block diagram of the fault-tolerant control strategy in the MMC system can be obtained as shown in Figure 8.

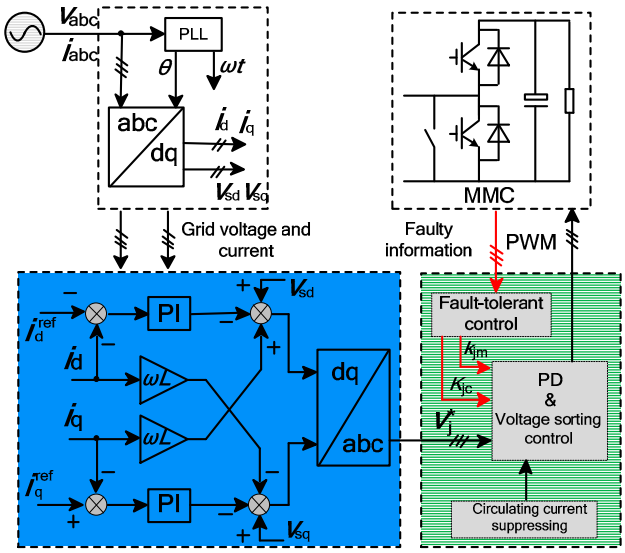


**Figure 8.** Schematic diagram of control system.

### *4.3. Maximum Control Range of the Proposed Control Strategy*

Restricting condition 1: meet the voltage pressure requirements. Because when the faulty arm is asymmetric, the carrier wave of each SM will be revised through the increasing carrier wave amplitude control link. At this time, the steady-state operating voltage of the SM will be raised. In order to ensure that the working voltage of the SM is less than the withstand voltage of the SM, it is necessary to satisfy the following requirements:

$$\frac{U_{\mathrm{dc}}}{\mathrm{N}-\chi_{\mathrm{j}}} < U_{\mathrm{m}} \tag{14}$$

With

$$\min\left[n_{\mathrm{jp\_fau}}\ ,\ n_{\mathrm{jl\_fau}}\right] < N(1-\frac{U_{\mathrm{dc}}}{U_{\mathrm{m}}}) \tag{15}$$

Restricting condition 2: ensure that the system does not appear over modulation. According to the analysis of the previous section, combining the Equations (9)–(13), the set of the modulation amplitudes in the upper arm of each phase in the limiting modulation wave range [t1, t2] can be calculated as follows:

$$U_{\mathrm{j}}{}^{*} = \left\{ 2\cdot\frac{N-\tau_{\mathrm{j}}}{N-\chi_{\mathrm{j}}}, 1-m,\ 1+m, (1-\sqrt{3}m-2\frac{\tau_{\mathrm{j}}-\chi_{\mathrm{j}}}{N-\chi_{\mathrm{j}}}) \right\} \tag{16}$$

As the system works normally, there must be:

$$\begin{cases} 0 \le m \le 1 \\ 0 \le \chi_{\mathrm{j}} < \tau_{\mathrm{j}} \le N \end{cases} \tag{17}$$

Therefore, to ensure that the system does not appear over modulation after the SM fault, it is necessary to ensure that:

$$0 \le 1-\sqrt{3}m-2\cdot\frac{\tau_{\mathrm{j}}-\chi_{\mathrm{j}}}{N-\chi_{\mathrm{j}}} \le 2 \tag{18}$$

with

$$\max\left[n_{\mathrm{jp\_fau}}\ ,\ n_{\mathrm{jl\_fau}}\right] \le \frac{1-\sqrt{3}m}{2}N - \frac{1+\sqrt{3}m}{2}\chi_{\mathrm{j}} \tag{19}$$

## 5. Simulation Studies

A three-phase MMC simulation model is built in MATLAB/Simulink simulation software as shown in Figure 1. The main parameters of the simulation system are shown in Table 1. In the simulation process, the circulating current suppression strategy is always put into operation when the grid is connected [29].

**Table 1.** Main parameters of the simulation system.

| Parameters | Value |
|---|---|
| Ac system nominal voltage | 10 kV |
| Ac System inductance $L_s$ | 5 mH |
| Fundamental frequency | 50 Hz |
| Ac system power losses $R_s$ | 0.03 Ω |
| Arm inductance $L_m$ | 5 mH |
| Series arm resistance $R_m$ | 0.01 Ω |
| Dc bus voltage $U_{dc}$ | 20 kV |
| Number of SMs per arm N | 20 |
| Number of redundant SMs per arm | 5 |
| Sub-module capacitor $C$ | 2000 μF |
| Transformer ratio | 1:1 (Y/Δ) |

### *5.1. Case 1*

Fault condition 1: Single arm fault to symmetrical arm fault. When the system operates to t = 0.4 s, five SMs in the upper arm of phase a occur fault; at t = 0.5 s, the fault-tolerant control strategy is enabled; at t = 0.9 s, five SMs in the lower arm of phase a are failed again. Figure 9 is the related simulation results.

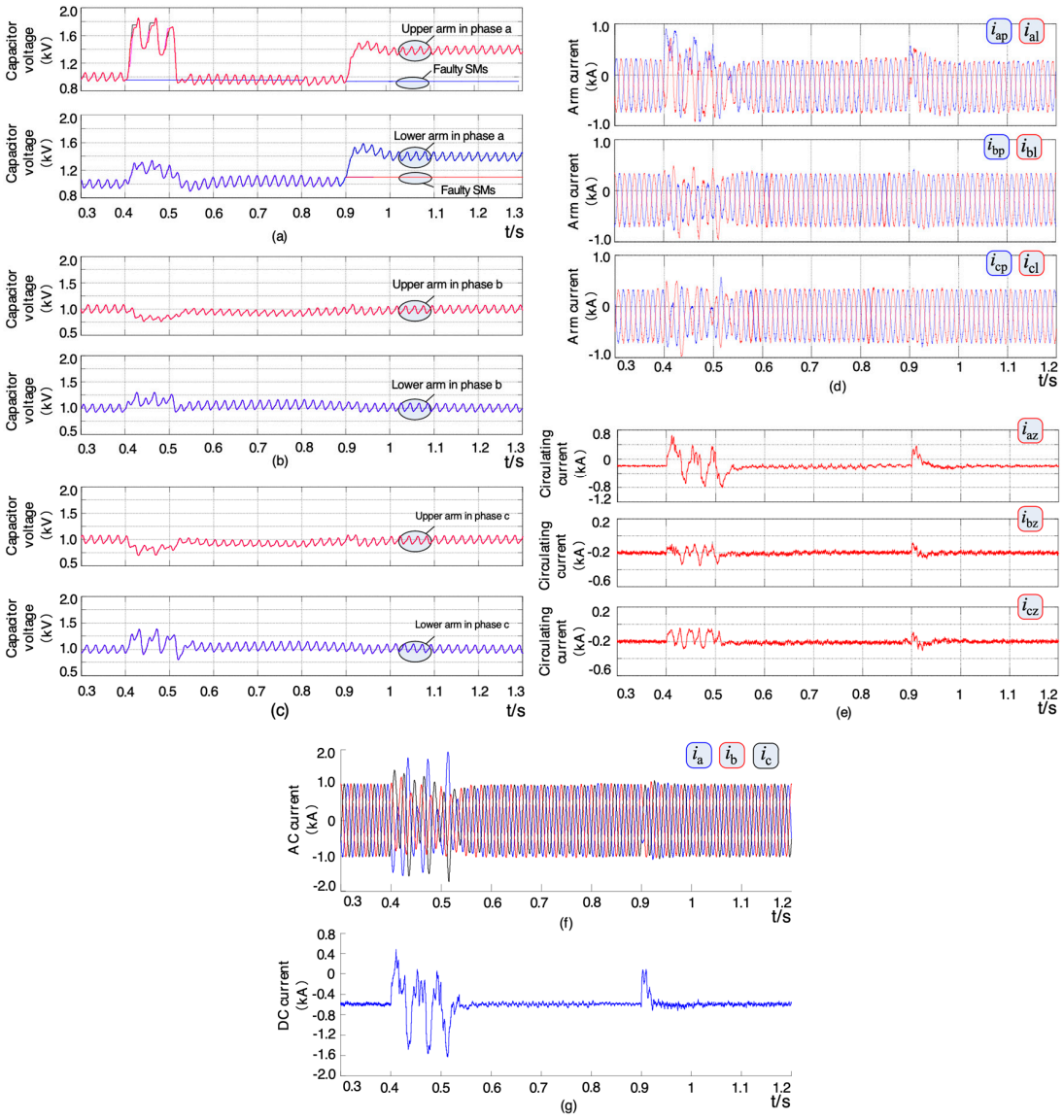


**Figure 9.** Simulation results of fault condition 1: (**a**) Capacitor voltage of phase a; (**b**) Capacitor voltage of phase b; (**c**) Capacitor voltage of phase c; (**d**) Arm current of phase j (j = a,b,c); (**e**) Circulating current of phase j (j = a,b,c); (**f**) AC current; (**g**) DC-link current.

From Figure 9a–g, it can be seen that: (1) When the system is in normal operation, the voltage and current of the system are stable. (2) When the SMs fail at t = 0.4 s, the SM capacitor voltage of each phase begins to oscillate irregularly, the arm current and AC grid-connected current show an asymmetric state, and the DC current and circulating current of the system also appear relatively fluctuant. (3) When fault-tolerant control strategy is enabled at t = 0.5 s, the system SM voltage immediately starts to return to normal value, the fluctuation of circulating current and DC current is obviously suppressed, and the arm current and AC grid-connected current are quickly restored to symmetry and stable operation. (4) When the SMs occur fault again at t = 0.9 s, through the control of

the increasing carrier wave amplitude, the SM voltage of fault phase is in the boost operation (up to about 1.3 kV) and the SM voltage of the non-fault phase continues to maintain the stable operation of the original rated value (1.0 kV), and all the current can continue to maintain stable operation through rapid transient regulation.

The above results show that the proposed fault-tolerant control strategy can quickly realize fault-tolerant operation after the SM fault, and can respond quickly when the single arm SM fault transforms to symmetrical fault.

### *5.2. Case 2*

Fault condition 2: Single arm fault to arm asymmetric fault. When the system operates to t = 0.4 s, five SMs in the upper arm of phase a occur fault; at t = 0.5 s, the fault-tolerant control strategy is enabled; at t = 0.9 s, three SMs in the lower arm of phase a are failed again. Figures 10 and A1 are the related simulation results.

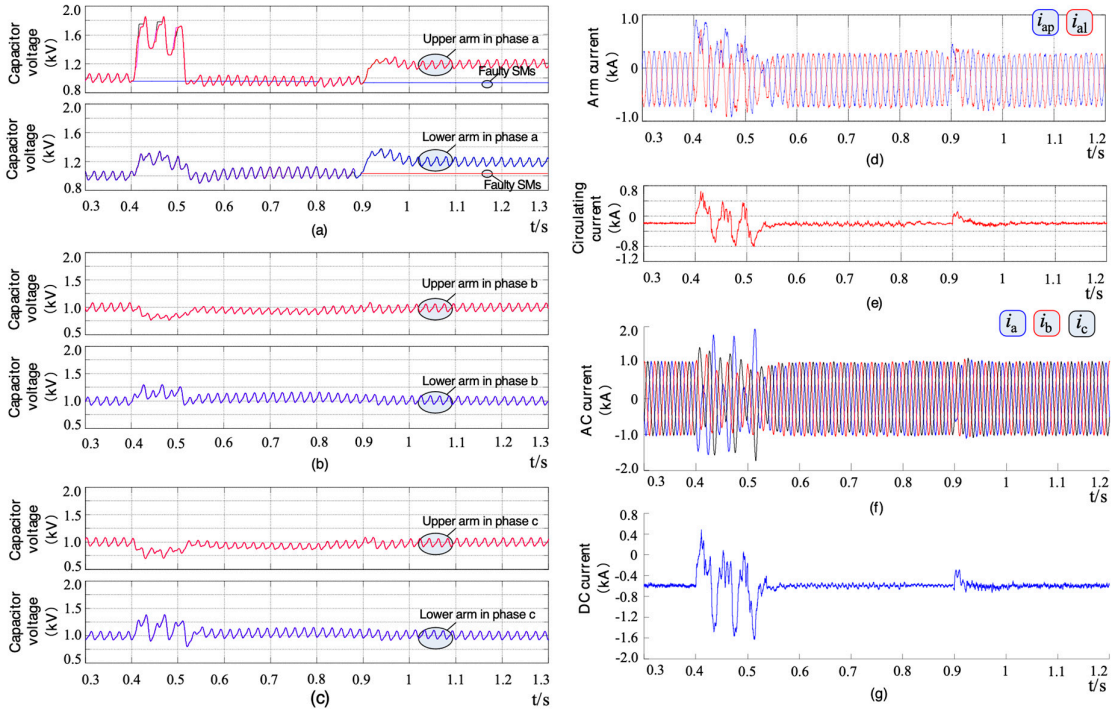


**Figure 10.** Simulation results of fault condition 2: (**a**) Capacitor voltage of phase a; (**b**) Capacitor voltage of phase b; (**c**) Capacitor voltage of phase c; (**d**) Arm current of phase a; (**e**) Circulating current of phase a; (**f**) AC current; (**g**) DC-link current.

It can be seen that: (1) Since the operation conditions of the system before t = 0.9 s are the same as the fault condition 1, the simulation of the system in 0~0.9 s is basically the same as the fault condition 1. (2) When the SMs occur fault again at t = 0.9 s, the system is operating asymmetrically in the upper and lower arms. The SM voltage of the fault phase is increased to about 1.2 kV by increasing carrier wave amplitude, while the SM voltage of the non-fault phase keeps the stable operation with the original rated value, and all the current can continue to maintain stable operation through rapid transient regulation.

Because the $\chi_a$ (the smaller number of faulty SMs of phase a) is smaller than the fault condition 1, the boosting amplitude of SM voltage of the fault phase is smaller than the fault condition 1, and the impact of the AC and DC current of the system is relatively small at t = 0.9 s. The above results also show that the proposed fault-tolerant control strategy can effectively achieve fault-tolerant operation after the SM fault, and can also respond quickly when the single arm fault transforms to the asymmetric arm fault.

### *5.3. Case 3*

Fault condition 3: Arm symmetrical fault to arm asymmetric fault. When the system operates to t = 0.4 s, three SMs in the upper arm and lower arm of phase occur fault simultaneously; at t = 0.5 s, the fault-tolerant control strategy is enabled; at t = 0.9 s, two SMs in the upper arm of phase a are failed again. Figures 11 and A2 are the related simulation results.

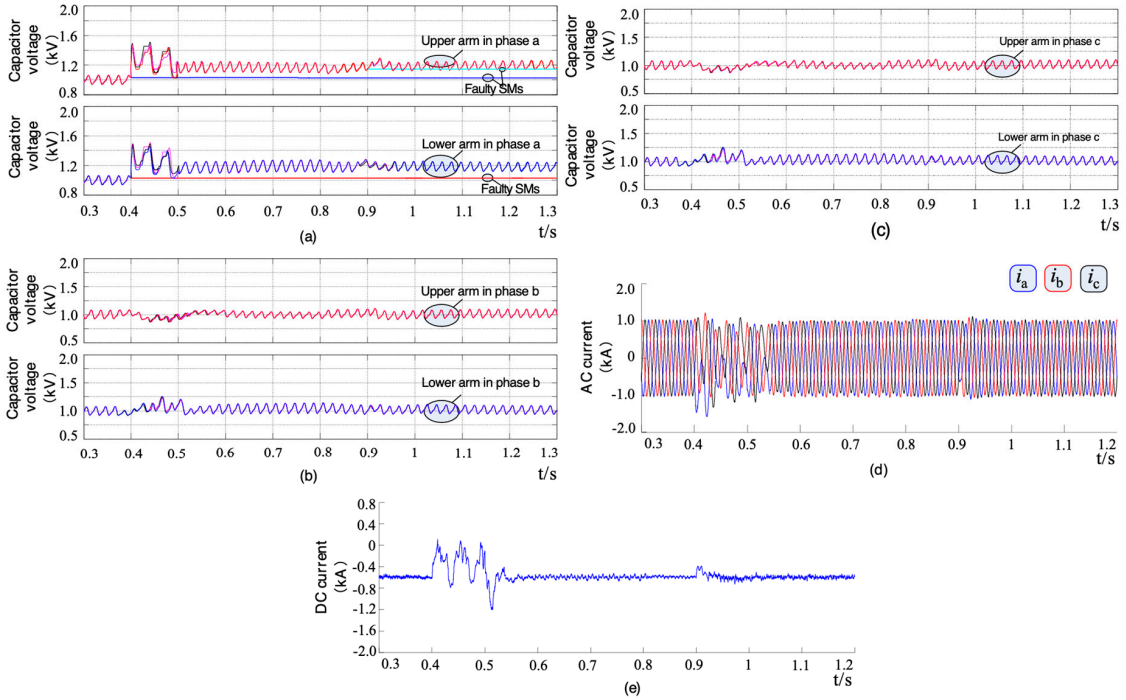


**Figure 11.** Simulation results of fault condition 3: (**a**) Capacitor voltage of phase a; (**b**) Capacitor voltage of phase b; (**c**) Capacitor voltage of phase c; (**d**) AC current; (**e**) DC-link current.

It can be seen that: (1) When the system is in normal operation, the voltage and current of the system are stable. (2) When the SMs fail at t = 0.4 s, the capacitor voltage of each phase SM begins to oscillate irregularly, the arm current and AC grid-connected current show an asymmetric state. But at this time, the arm structure is still in symmetrical state and the number of faulty SMs is smaller than fault conditions 1 and 2, so the oscillation amplitude of voltage and current is slight compared with the fault conditions 1 and 2. (3) When fault-tolerant control strategy is enabled at t = 0.5 s, the SM voltage of the fault phase is increased to about 1.2 kV, while the SM voltage of the non-fault phase keeps the stable operation with the original rated value, and all the current can continue to maintain stable operation rapidly. (4) When the SMs occur fault again at t = 0.9 s, through the control of the limiting modulation wave amplitude, the system can continue to operate stably.

Based on the simulation results of fault conditions 1–3, it can be seen that the fault-tolerant control strategy of the SM proposed in this paper can effectively realize the fault-tolerant operation control of the system after the SM fault, and can respond flexibly to different fault conditions of the arm, and can respond quickly when the fault state of the arm changes.

## 6. Experimental Studies

In order to verify the fault-tolerant control strategy, a 2-terminal MMC-based experimental platform is built in the laboratory. The experimental platform is shown in Figure 12. Among them, MMC1 is the DC voltage source and MMC2 is to verify the control strategy. The basic parameters of MMC prototype are shown in Table 2.

In the course of the experiment, the SM1 in the upper arm of phase a occurs fault at t1, fault-tolerant control strategy is enabled at t2 and the SM4 in the lower arm of phase a occurs fault again at t3. Figure 13 shows the relevant experimental waveform.

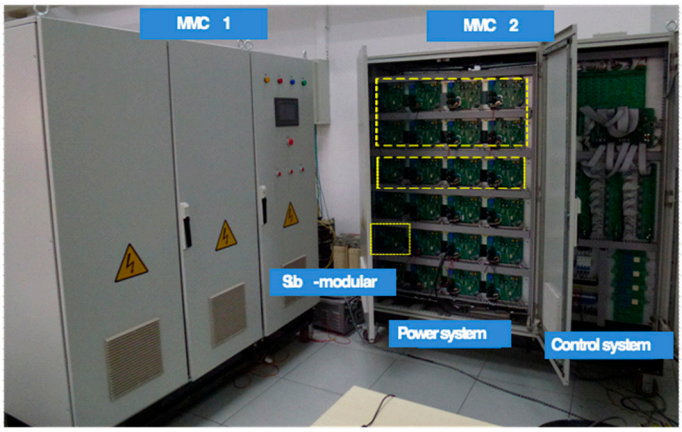


**Figure 12.** The photograph of MMC experiment prototype.

**Table 2.** Experimental parameters of the MMC prototype.

| Parameters | Value |
|---|---|
| AC System inductance $L_s$ | 5 mH |
| Arm inductance $L_m$ | 5 mH |
| DC bus voltage $U_{dc}$ | 20 kV |
| Number of SMs per arm N | 4 |
| Number of redundant SMs per arm | 1 |
| Sub-module capacitor $C$ | 2000 μF |
| Transformer ratio | 380 V/380 V (Y/Δ) |

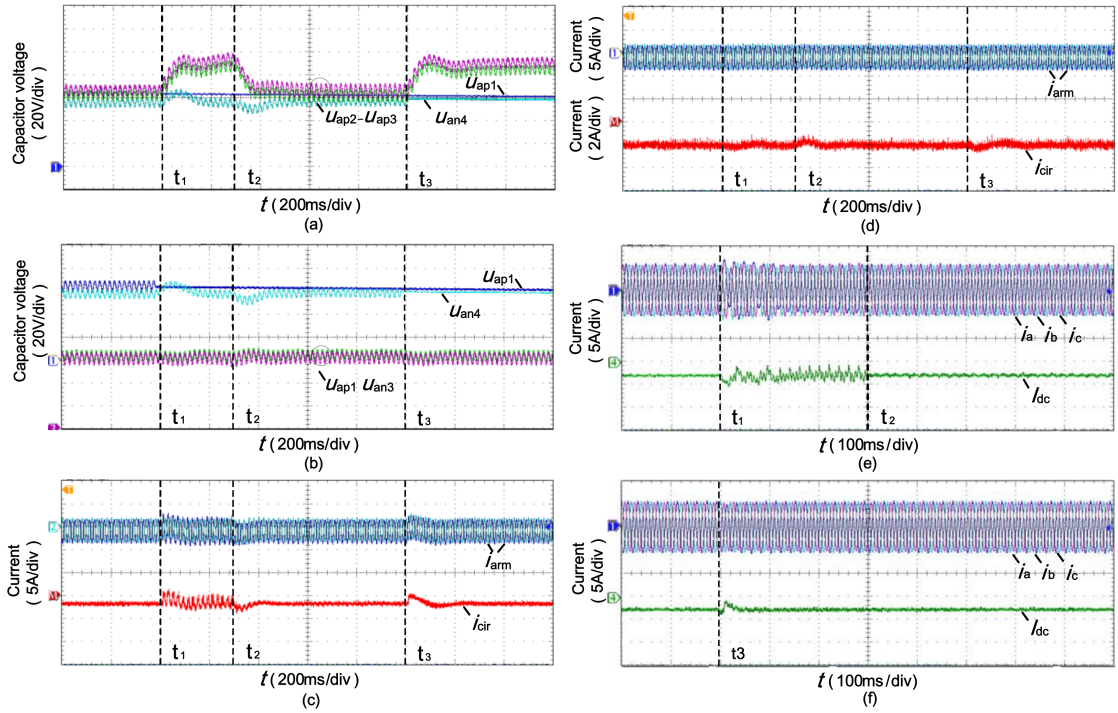


**Figure 13.** Waveforms of experiment: (**a**) Capacitor voltage of phase a; (**b**) Capacitor voltage of phase b; (**c**) Circulating current of phase a; (**d**) Circulating current of phase b; (**e**) AC current and DC current from t1 to t3; (**f**) AC current and DC current after t3.

It can be seen from Figure 13 that: (1) Before the fault, the system operates steadily. When the SM1 fails at t1, the capacitor voltage of SM1 begins to oscillate irregularly, the arm current and AC grid-connected current show an asymmetric state, and the DC current and circulating current of the system also appear relatively fluctuant. (2) When the fault-tolerant control strategy is put into operation at t2, SM1 voltage starts to return to normal value and the arm current and AC grid-connected current are restored to symmetry and stable operation. (3) When the SM4 occurs fault again at t3, the SM4 voltage of the fault phase is increased to 80 V, while the SM voltage of the non-fault phase keeps the stable operation with the original rated value (60 V). There is no major impact on the system in the process, and the system current is still in a stable state.

Limited by the number of SMs of the experimental platform, the experiment only validates the fault condition 1, but the experimental results are basically consistent with the simulation. The results of simulation and experiment show that the design of fault-tolerant control strategy proposed in this paper is reasonable and effective, and it is helpful to realize fault-crossing of SMs under different operating conditions.

## 7. Conclusions

The fault-tolerant operation issue of MMC under SM faults is studied in this paper. The main works and contributions can be summarized as:

(1) The traditional zero-sequence voltage injection fault-tolerant control algorithm is analyzed detailed. It reveals that the traditional method is easy to implement under the signal arm faulty state. However, if the SM simultaneously occurring faults in the upper and lower arms or appearing multiple arm failures, the required zero-sequence voltages will be calculated difficult. The SM fault-crossing is complicated to realize.

(2) A novel fault-tolerant control strategy based on PD-PWM is proposed, which has three main benefits: (i) it has carrier and modulation wave dual correction mechanism, which control ability is more higher and flexible; (ii) it only needs to inject zero-sequence voltage in half a cycle of the modulation wave, which simplifies the complexity of traditional zero-sequence voltage injection control algorithms and much easier for implement; (iii) furthermore, the zero-sequence voltage can even be avoided injecting under the symmetrical fault conditions.

(3) The simulations in the MATLAB/SIMULINK and experiments with 2-terminal a MMC-based prototype are all studied with the proposed control strategy under different fault conditions. The results confirm the efficiency of the control strategy.

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**Conflicts of Interest:** The authors declare no conflict of interest.

## Appendix A

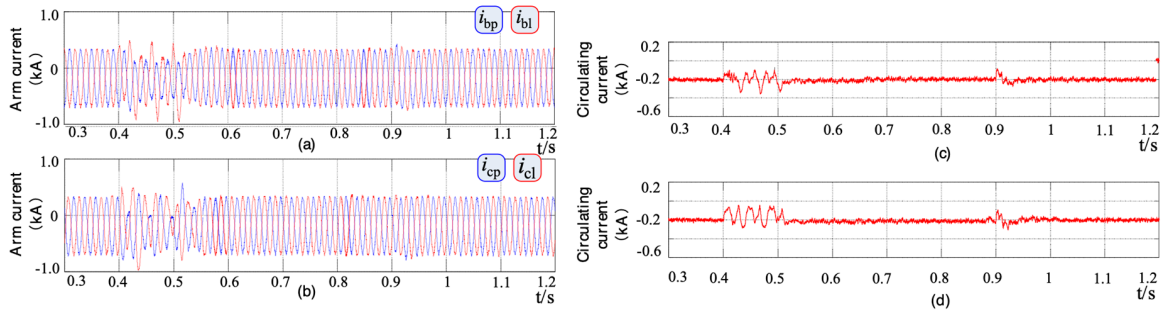


**Figure A1.** Simulation results of fault condition 2: (**a**) Arm current of phase b; (**b**) Arm current of phase c; (**c**) Circulating current of phase b; (**d**) Circulating current of phase c.

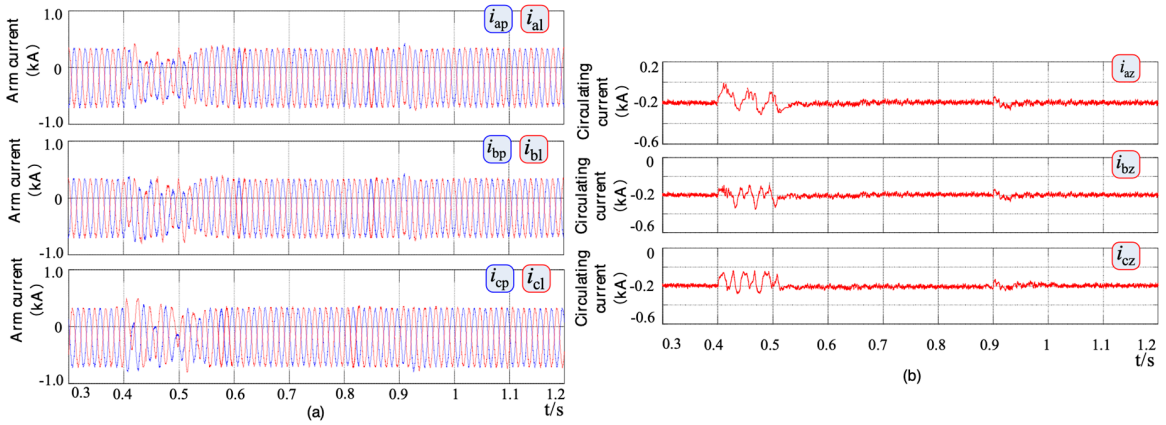


**Figure A2.** Simulation results of fault condition 3: (**a**) Arm current of phase j (j = a,b,c); (**b**) Circulating current of phase j (j = a,b,c).

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