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Analysis to Input Current Zero Crossing Distortion of Bridgeless Rectifier Operating under Different Power Factors

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Abstract: The principles and operating characteristics of bridgeless rectifiers under different power factors are discussed with emphasis on analyzing the input current distortion. Firstly, two driving modes are analyzed and compared. Based on the results of comparison it is concluded that the complementary drive mode is a better choice in terms of reducing the current distortion when bridgeless rectifier operates on non-unity power factor. Then, the mechanism causing input current zero-crossing distortion is analyzed. The input current during the distortion is expressed by the piecewise function when a bridgeless rectifier operates under complementary drive mode. Based on the piecewise function, the harmonic analysis is performed. Besides, the relationships between the input current Total Harmonic Distortion (THD) and the filtering inductance, the input current amplitude and the power factor angle are also investigated, which is useful when designing bridgeless rectifiers and selecting the corresponding parameters. Finally, the accuracy of the theoretical analysis is verified through the simulation and experiment.

Keywords: bridgeless rectifier; non-unity power factor; current distortion; piecewise function; parameter selection

1. Introduction

Devices based on full-control Pulse Width Modulation (PWM) converter technology have been widely used to solve power quality problems, such as harmonic and reactive power contamination, which is caused by certain power electronic devices. Among them, the static var generator (SVG), static synchronous compensator (STATCOM), and active power filter (APF) are most popularly used in this area [1–3]. However, adding these devices into the grid undoubtedly increases the use of physical devices and extra power loss [4]. Therefore, increasing attention is being paid to the incorporation of reactive power compensation and other power quality functionality into fully controlled bidirectional converters used in renewable energy-based generation systems or Vehicle-to-grid (V2G) systems [5–7].

However, in many practical applications, including speed regulation with fan type loads, wind power integration, and plug-in electrical vehicle applications, only unidirectional power flow is required. In these situations, some fully controlled switches can be eliminated or replaced to simplify the system, which greatly reduces the complexity of system, saves costs, and improves the system reliability [8,9]. Taking these considerations into account, many researchers have investigated the possibility of incorporating reactive power compensation (RPC) and harmonic current compensation (HCC) functionalities into general unidirectional power converters [10,11].

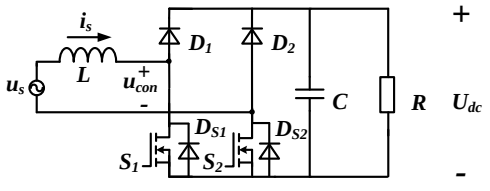
Bridgeless rectifiers, as a kind of unidirectional converter, have a simpler structure and lower power losses [12–14]. Especially when multilevel medium- or high-voltage converters are formed by cascading bridgeless rectifiers, the advantages of fewer massive fully control switching devices, lower costs, and improved reliability become more significant. In [15], a cascaded bridgeless rectifier typology was proposed and a mechanism causing current zero-crossing distortion was discussed. However, a detailed theoretical analysis of the current distortion was not carried out, and the ability of bridgeless rectifiers operating under leading or lagging power factors was not mentioned. The input current distortion of bridgeless rectifiers under a unity power factor was analyzed theoretically in [16] and a control strategy based on specific lagging power factor was proposed, but there was no analysis of the input current distortion under leading or lagging power factor. In [17], some reactive power compensation functionality was integrated in bridgeless rectifiers, and the input current distortion characteristics given different power factors was analyzed to determine the reactive power compensation ability of bridgeless rectifiers. However, all analyses provided by [17] are based on the assumption that bridgeless rectifiers operate under synchronous driving mode. It will be seen from the later discussion that compared with synchronous driving mode, complementary driving mode induces fewer harmonics in the input current of bridgeless rectifiers, and therefore is a more suitable driving mode for bridgeless rectifiers under different power factors.

As mentioned above, the research of bridgeless rectifiers in most literature was performed based on the unity power factor. Only a few studies discuss the characteristics of bridgeless rectifiers operating under non-unity power factors. However, no studies have reported the effect of different driving modes on input current distortion when bridgeless rectifiers operate under non-unit power factors. In order to more effectively integrate RPC and HCC capabilities into a bridgeless rectifier, the harmonic characteristics of bridgeless rectifiers under different power factors in complementary driving mode are discussed in this paper. We concluded that the complementary drive mode is a better choice in terms of reducing the current distortion when bridgeless rectifiers operate under non-unity power factors. Meanwhile, this analysis is helpful for the design of bridgeless rectifiers and the selection of the corresponding parameters under non-unity power factors. Two driving modes for switches are discussed on the basis of the principle of bridgeless rectifiers in Section 2. Then, the characteristics of current zero-crossing distortion under different power factors are analyzed in Section 3. The limitation of filter inductance, input current amplitude, and the value of the power factor angle in the allowable range of the total harmonic distortion (THD) of the current are analyzed in Section 4. Finally, the accuracy of the proposed theoretical analysis is verified through simulation and experiment.

2. Operating Principle and Driving Modes of Switches

2.1. Effective Operation Mode and Mathematical Model

The circuit topology of a bridgeless rectifier is shown in Figure 1a, where u_{con} is the alternating current (AC) side voltage of bridgeless rectifier and i_s is the input current. The polarity of u_{con} and i_s shown in Figure 1a is defined as positive polarity. L is the AC side filter inductance, C is the direct current (DC) side of the filter capacitor, U_{dc} is the DC side output voltage, and R is the equivalent load of bridgeless rectifier.



(**a**)

Figure 1. *Cont.*

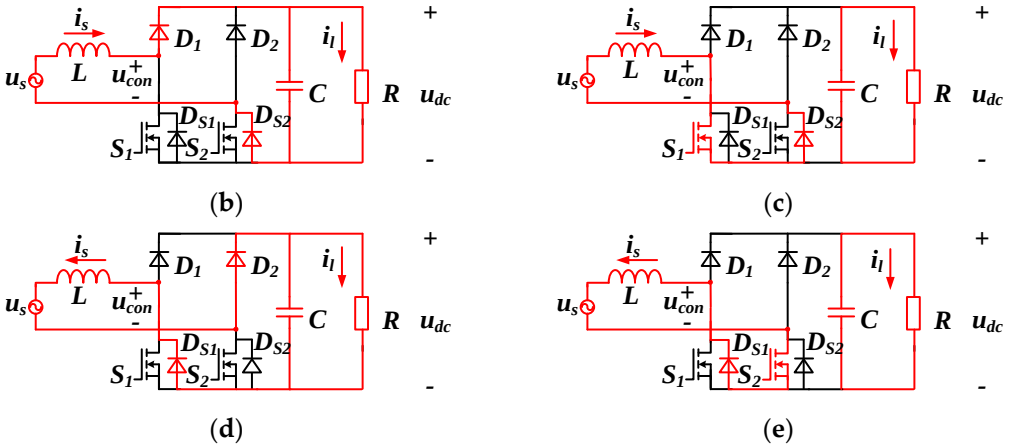


Figure 1. Main topology of the bridgeless rectifier and its four operation modes: (**a**) Main topology of the bridgeless rectifier; (**b**) Mode I; (**c**) Mode II; (**d**) Mode III; (**e**) Mode IV.

Due to the unidirectional conduction property of the fast recovery diodes, the value of the AC side voltage u_{con} of the bridgeless rectifier depends on the switching state and the polarity of the input current. Thus, there are only four effective operation modes for bridgeless rectifiers as shown in Figure 1b–e, which are summarized in Table 1.

Table 1. Four operation modes of bridgeless rectifiers.

Mode I	Mode II	Mode III	Mode IV
$i_s > 0$		$i_s < 0$	
$u_{con} = U_{dc}$	$u_{con} = 0$	$u_{con} = -U_{dc}$	$u_{con} = 0$
D_1, D_{S2} conductivity	S_1, D_{S2} conductivity	D_2, D_{S1} conductivity	S_2, D_{S1} conductivity

From Table 1, the expression of AC side voltage is obtained as:

$$u_{con} = \mathrm{sgn}(i_s) \cdot S \cdot U_{dc} \tag{1}$$

where S ($S = 0, 1$) refers to the switch function of bridgeless rectifier and $\mathrm{sgn}(i_s)$ is the sign function. If $i_s \geq 0$, $\mathrm{sgn}(i_s) = 1$. If $i_s < 0$, $\mathrm{sgn}(i_s) = -1$.

Applying the Kirchhoff's voltage law (KVL) and Kirchhoff's circuit laws (KCL) to the topology shown in Figure 1, the steady-state mathematical model of the system can be obtained by ignoring AC-side power loss:

$$\begin{cases} L\frac{di_s}{dt} = u_s - \mathrm{sgn}(i_s) \cdot S \cdot U_{dc} \\ C\frac{dU_{dc}}{dt} = \mathrm{sgn}(i_s) \cdot S \cdot i_s - \frac{U_{dc}}{R} \end{cases} \tag{2}$$

2.2. Driving Mode of Two Switches

Since only one switch affects the commutation process during each half cycle of the input current and the two switches have the same source (or emitter) voltage, synchronous and complementary driving modes can be applied.

Figure 2 depicts a block diagram for complementary drive. The output of voltage regulator is shifted to satisfy the required power factor and then given as the input current. Complementary signal g_{S1}, g_{S2} is generated in modulation as driving signals of switches S_1, S_2, respectively.

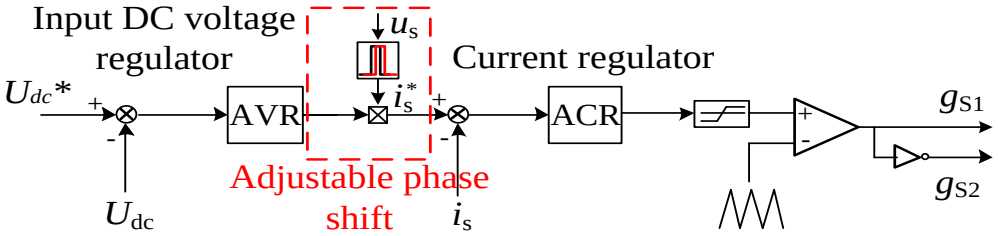


Figure 2. Block diagram of the complementary drive.

The block diagram for a synchronous drive is shown in Figure 3, where S_1 and S_2 are driven by the same control signal. However, it is necessary to take the absolute value of the grid voltage and the input current, otherwise the current will be discontinuous in the negative half cycle. The corresponding waveform is shown in Figure 4. Its relevant parameters were selected as U_{sm} = 311 V, f = 50 Hz, U_{dc} = 400 V, R = 0.09 Ω, and L = 3 mH. When the polarity of i_s reverses from positive to negative, u_s also reverses its polarity. At this moment, if S_1 and S_2 are turned on, i_s runs through S_2 and D_{S1} and increases, while its polarity is negative. When S_1 and S_2 are turned off, $u_{con} = -u_{dc}$, based on the boost characteristics of the rectifier, the voltage of the inductance drops, $u_L = u_s - u_{con} > 0$. Thus, the polarity of i_s is negative and the amplitude decreases, which causes $i_s^* - i_s$ to become smaller. The duty ratio d_{S1} of S_1 and d_{S2} of S_2 decreases as well. This control leads i_s in the cut-off state at the negative half cycle.

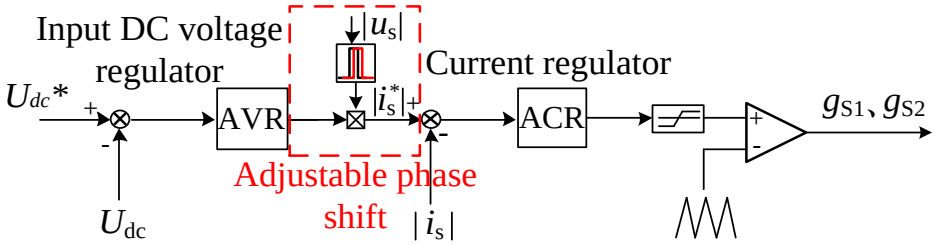


Figure 3. Block diagram for a synchronous drive.

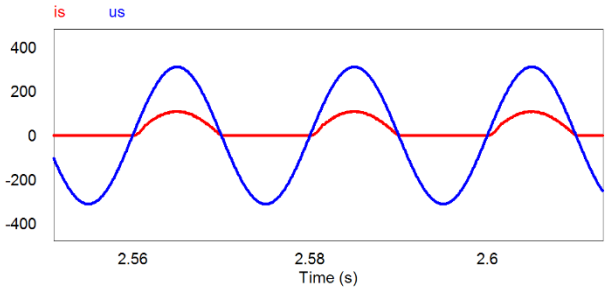


Figure 4. Simulation current waveform on the alternating current (AC) side based on a synchronous drive without an absolute value module.

Synchronous driving mode significantly simplifies the implementation of the control circuit of the bridgeless rectifier and is more popularly used than complementary driving mode in practical applications. When a bridgeless rectifier operates under a unity power factor, there is no difference in the current distortion under the two different driving modes. However, when incorporating the reactive power compensation (RPC) and harmonic current compensation (HCC) functionalities into the bridgeless rectifier, the bridgeless rectifier is required to operate under non-unity power factors. In this situation, the two driving modes have different effects on the input current waveform. It will be seen that complementary driving mode is a better choice in terms of reducing the current distortion compared with synchronous driving, which is discussed in detail in Section 3.

3. Analysis of Input Current Zero-Crossing Distortion

3.1. Theory for Input Current Zero-Crossing Distortion

Due to the unidirectional power flow for the bridgeless rectifier, whenever the polarities of the current and voltage on the AC side of the rectifier switch, an input current distortion appears. The steady state AC side phasor diagram is shown in Figure 5, where U^*_{con} and I^*_s are the reference voltage and reference current on the AC side of the rectifier, respectively. When the rectifier is operating under a unity power factor, the input current I_s is in phase with the source voltage U_s, and the voltage across the input inductor U_L is orthogonal to I_s. According to the triangle law of vector addition, U_{con} lags I_s by θ, as shown in Figure 5. This lagging angle θ indicates that, during the period of θ after the current crosses zero, the input current i_s and the AC-side voltage u_{con} are required to have opposite polarities. However, due to the unidirectional power flow, the AC-side voltage and current of the bridgeless rectifier must have the same polarity. Hence, during this period, AC-side voltage u_{con} can only be kept at zero, which makes the input current uncontrollable [18,19]. Note that the heavier the loads, the more serious the input current zero-crossing distortion.

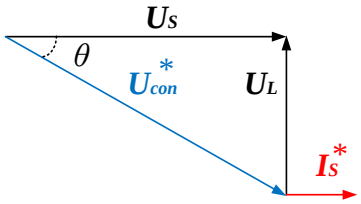


Figure 5. Phasor diagram on the AC side under unity power factor.

From the above analysis, the current zero-crossing distortion is generated under leading, lagging, and unity power factor. As the leading or lagging angle increases, the current distortion becomes more severe. Notably, the distortion of the input current under a leading power factor is more severe than the distortion of the input current under a lagging power factor. Sections 3.2–3.4 discuss the input current distortion under unity power factor, leading power factor, and lagging power factor in detail, respectively, and describe the input current distortion by piecewise function in each part.

3.2. Distortion Characteristics of Input Current under Unity Power Factor

Figure 6 displays an AC-side phasor diagram under a unity power factor. Considering the symmetry, only the half-cycle waveform is analyzed.

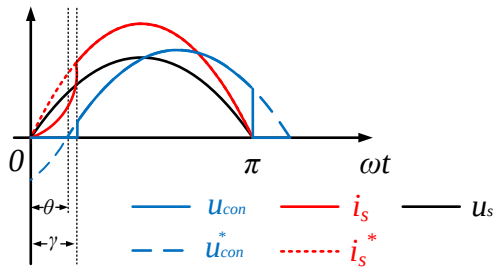


Figure 6. Expected waveforms and actual waveforms of the AC-side fundamental voltage and current of bridgeless rectifier under a unity power factor.

The grid voltage u_s, reference input current i^*_s, and reference voltage on the AC side of the rectifier u^*_{con} under a unity power factor can be expressed as follows:

$$u_s = U_{sm} \sin \omega t \tag{3}$$

$$i^*_s = I_{sm} \sin \omega t \tag{4}$$

$$u_{con}^{*} = U_{conm}\sin(\omega t - \theta) \tag{5}$$

If $i_s^{*} > 0$ and $u_{con}^{*} < 0$ within the range of 0–θ, the u_{con} cannot follow u_{con}^{*}. In this period, u_{con} is clamped to zero, and $u_s = u_L$. Accordingly, i_s is expressed as:

$$i_s(t) = \frac{U_{sm}}{L}\int_0^t \sin(\omega\tau)d\tau = \frac{U_{sm}}{\omega L}(1-\cos(\omega t)) \tag{6}$$

When $\omega t = \theta$, the polarity of u_{con}^{*} is reversed from negative to positive, and u_{con} has the ability to follow u_{con}^{*}, theoretically. However, as $i_s^{*} > i_s$, in order to make i_s follow i_s^{*}, u_{con} is still maintained at zero until $i_s = i_s^{*}$ over a period of $\omega t > \theta$. Let $i_s = i_s^{*}$ when $\omega t = \gamma$, as:

$$\frac{U_{sm}}{\omega L}(1-\cos(\omega t_k)) = I_{sm}\sin(\omega t_k) \tag{7}$$

$$\gamma = 2\arctan\left(\frac{\omega L I_{sm}}{U_{sm}}\right) \tag{8}$$

Therefore, the piecewise function of the input current in a power frequency cycle is expressed as

$$i_s(t) = \begin{cases} \frac{U_{sm}}{\omega L}(1-\cos(\omega t)), & 0 < \omega t \le \gamma \\ I_{sm}\sin\omega t, & \gamma < \omega t \le \pi \\ \frac{U_{sm}}{\omega L}(-1-\cos(\omega t)), & \pi < \omega t \le \pi+\gamma \\ I_{sm}\sin\omega t, & \pi+\gamma < \omega t \le 2\pi \end{cases} \tag{9}$$

The RMS value of fundamental component of input current is

$$I_{sm1RMS} = \sqrt{\frac{a^2+b^2}{2}} \tag{10}$$

where:

$$a = \frac{2U_{sm}}{\pi\omega L}(\sin\gamma - \frac{1}{2}\gamma - \frac{1}{4}\sin 2\gamma) + \frac{I_{sm}}{2\pi}(\cos 2\gamma - 1) \tag{11}$$

$$b = \frac{2U_{sm}}{\pi\omega L}(-\cos\gamma + \frac{1}{4}\cos 2\gamma + \frac{3}{4}) + \frac{I_{sm}}{\pi}(\frac{1}{2}\sin 2\gamma - \gamma + \pi) \tag{12}$$

The Root Mean Square (RMS) value of input current is:

$$I_{smRMS} = \sqrt{\frac{\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} {i_s}^2(t)dt} = \sqrt{(\frac{U_{sm}^2}{4\pi\omega^2L^2} + \frac{I_{sm}^2}{4\pi})\sin 2\gamma - \frac{2U_{sm}^2}{\pi\omega^2L^2}\sin\gamma + (\frac{3U_{sm}^2}{2\pi\omega^2L^2} - \frac{I_{sm}^2}{2\pi})\gamma + \frac{I_{sm}^2}{2}} \tag{13}$$

where I_{sm} can be obtained based on conservation of power, as:

$$I_{sm} = \frac{2}{U_{sm}}\cdot\frac{U_{dc}^2}{R} \tag{14}$$

THD of input current can be deduced as:

$$THD = \frac{\sqrt{I_{smRMS}^2 - I_{sm1RMS}^2}}{I_{sm1RMS}} \tag{15}$$

Note that the above analytical methods can be applied to both driving modes.

3.3. Distortion Characteristics of Input Current under Leading Power Factor

Figure 7 shows the AC-side fundamental waveform of a system with a synchronous drive. When $\omega t = 0$, the polarity of i_s^{*} is reversed from negative to positive, u_{con} is zero, and the polarity of u_s is negative, which leads to the negative increase in u_s. The rate of increase of $|i_s^{*}|$ is larger than that of

$|i_s|$ in the heavy load. In order to make $|i_s|$ follow $|i_s^*|$, u_{con} is clamped to zero until $i_s = i_s^*$ when $\omega t = \gamma$. The amplitude of i_s^* is smaller in the underloading. $i_s = -i_s^*$ can be achieved within a certain period after reversing the polarity of i_s. When u_s approaches 0, the growth rate of $|i_s|$ decreases. The change rate of i_s is 0 when $\omega t = \theta$, $|i_s| < |i_s^*|$. Then u_s reverses its polarity. To make $|i_s|$ follow $|i_s^*|$, u_{con} is clamped to zero until $i_s = i_s^*$. The current distortion process will end at this point.

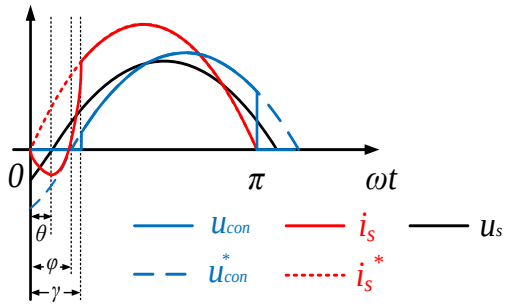


Figure 7. Expected waveforms and actual waveforms of the AC-side fundamental voltage and current with synchronous drive under a leading power factor.

Figure 8 shows the AC-side fundamental waveforms with complementary drive. When $\omega t = 0$, the polarity of i_s^* is reversed from negative to positive, u_{con} is zero, and the polarity of u_s is negative, which leads to the negative increase in u_s. At this moment, the polarity of i_s is negative. As $i_s^* - i_s > 0$, the current control loop causes the duty ratio d_{S1} of S_1 to increase and the duty ratio d_{S2} of S_2 to decrease. Based on the negative polarity of u_s, $|i_s|$ decreases with the decrease in d_{S2}. Once the polarity of i_s has reversed its polarity from negative to positive, the polarity of i_s reverses to negative again due to $u_{con} = 0$. This control places i_s in a discontinuous state when $0 < \omega t < \theta$. When $\theta < \omega t < \gamma$ and $u_s > 0$, in order to make i_s follow i_s^*, u_{con} is clamped to zero until $i_s = i_s^*$ when $\omega t = \gamma$. The current distortion process will end at this point.

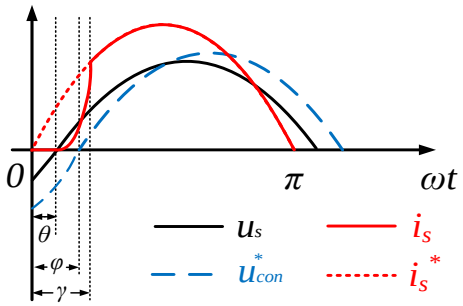


Figure 8. Expected waveforms and actual waveforms of AC side fundamental voltage and current with complementary drive under leading power factor.

The piecewise function expression of the input current is:

$$i_s(t) = \begin{cases} 0, & 0 < \omega t \le \theta \\ \frac{U_{sm}}{\omega L}(1 - \cos(\omega t - \theta)), & \theta < \omega t \le \gamma \\ I_{sm} \sin \omega t, & \gamma < \omega t \le \pi \\ 0, & \pi < \omega t \le \pi + \theta \\ \frac{U_{sm}}{\omega L}(-1 - \cos(\omega t - \theta)), & \pi + \theta < \omega t \le \pi + \gamma \\ I_{sm} \sin \omega t, & \pi + \gamma \le \omega t < 2\pi \end{cases} \tag{16}$$

Let $i_s = i_s^*$ at $\omega t_k = \gamma$. γ can be expressed as:

$$\gamma = \arctan\left(\frac{U_{sm} \sin\theta + \omega L I_{sm}}{U_{sm} \cos\theta}\right) + \arctan\left(\frac{\sqrt{\omega^2 L^2 I_{sm}^2 + 2\omega L U_{sm} I_{sm} \sin\theta}}{U_{sm}}\right) \tag{17}$$

The comparison shows that the current distortion becomes more severe under synchronous driving. Therefore, the complementary drive is a more appropriate choice under a leading power factor.

3.4. Distortion Characteristics of Input Current under Lagging Power Factor

When the angle of the lagging power factor is θ under a complementary drive, there are two phase relations between the AC-side voltage and the input current according to the value of $|u_L|$ and $|u_s \sin\theta|$. In Figure 9, i_s goes ahead of u_{con}. Based on the above analysis, the piecewise function expression of i_s is:

$$i_s(t) = \begin{cases} I_{sm}\sin(\omega t - \theta), & 0 < \omega t \le \theta \\ \frac{U_{sm}}{\omega L}(\cos\theta - \cos(\omega t)), & \theta < \omega t \le \gamma \\ I_{sm}\sin(\omega t - \theta), & \gamma < \omega t \le \pi + \theta \\ \frac{U_{sm}}{\omega L}(-\cos\theta - \cos(\omega t)), & \pi + \theta < \omega t \le \pi + \gamma \\ I_{sm}\sin(\omega t - \theta), & \pi + \gamma < \omega t \le 2\pi \end{cases} \tag{18}$$

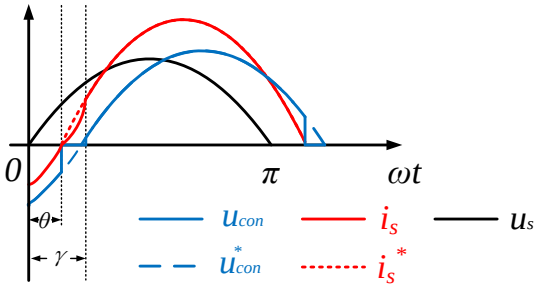


Figure 9. Expected waveforms and actual waveforms of AC-side fundamental voltage and current under a lagging power factor ($U_L > |U_s \sin\theta|$).

Let $i_s = i_s^*$ at $\omega t_k = \gamma$. γ can be expressed as:

$$\gamma = \arctan\left(\frac{\omega L I_{sm}\cos\theta}{U_{sm} - \omega L I_{sm}\sin\theta}\right) + \arctan\left(\frac{\sqrt{(U_{sm}\sin\theta - \omega L I_{sm})^2}}{U_{sm}\cos\theta}\right) \tag{19}$$

i_s lags u_{con} as shown in Figure 10, and its piecewise function expression is:

$$i_s(t) = \begin{cases} I_{sm}\sin(\omega t - \theta), & 0 < \omega t \le \varphi \\ I_{sm}\sin(\varphi - \theta) + \frac{U_{sm}}{\omega L}(\cos\varphi - \cos\omega t), & \varphi < \omega t \le \gamma \\ 0, & \gamma < \omega t \le \theta \\ I_{sm}\sin(\omega t - \theta), & \theta < \omega t \le \pi + \varphi \\ -I_{sm}\sin(\varphi - \theta) - \frac{U_{sm}}{\omega L}(\cos\varphi + \cos\omega t), & \pi + \varphi < \omega t \le \pi + \gamma \\ 0, & \pi + \gamma < \omega t \le \pi + \theta \\ I_{sm}\sin(\omega t - \theta), & \pi + \theta < \omega t \le 2\pi \end{cases} \tag{20}$$

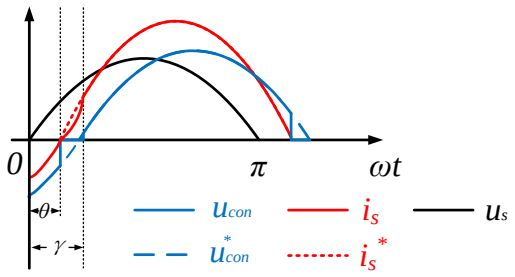


Figure 10. Expected waveforms and actual waveforms of AC side fundamental voltage and current under lagging power factor ($U_L < |U_s \sin\theta|$).

Based on cosine law, the angle φ of u_{con} that lags u_s can be deduced:

$$\varphi = \arccos\left(\frac{U_{sm} - \omega L I_{sm}\sin\theta}{\sqrt{U_{sm}^2 + \omega^2 L^2 I_{sm}^2 - 2\omega L I_{sm} U_{sm}\sin\theta}}\right) \tag{21}$$

Let $i_s = 0$ when $\omega t_k = \gamma$, yielding:

$$\gamma = \arccos\left(\frac{\omega L I_{sm}}{U_{sm}} \cdot \sin(\varphi - \theta) + \cos\varphi\right) \tag{22}$$

4. Constrain of Input Current on Filter Inductance, Input Current Amplitude, and Power Factor Angel Based on THD

Based on the above analysis, the input current zero-crossing distortion is affected by filter inductance L, input current amplitude I_{sm}, and power factor angle θ. Therefore, the allowable range of THD restricts the value of L, I_{sm}, and θ.

At first, the limitation of THD on L and I_{sm} was investigated. Taking $\theta = 0°$ as an example, Figure 11 shows the relation between current THD and L and I_{sm} when U_{sm} = 311 V, f = 50 Hz, and U_{dc} = 400 V. When L was chosen from 1–6 mH, and I_{sm} was changed from 10 to 60 A, the degree of input current distortion was aggravated with the increase in L and I_{sm}, and the maximum THD reached 6.96%. Figure 12 shows the contour line of THD with current and inductance when U_{sm} = 311 V, f = 50 Hz, and U_{dc} = 400 V. The values of L and I_{sm} can be determined based on the allowable range. For example, the shaded area in Figure 12 is the limitation on L and I_{sm} when THD < 1.4%. It is assumed that I_{sm} = 40 A, so 2.5 mH inductance can be selected when the THD of the current requirements are satisfied. In this case, THD was about 1.25%. In practical applications, if the THD of the equipment current is above 5%, the equipment will not be allowed to connect to the grid. Hence, the contour line of current 5% THD should be drawn and the RPC and HCC functionalities of bridgeless rectifiers should be limited in practical applications.

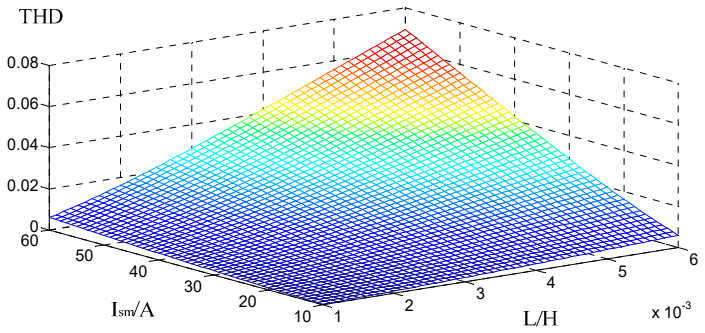


Figure 11. Three-dimensional (3D) diagram of current total harmonic distortion (THD) under a unity power factor.

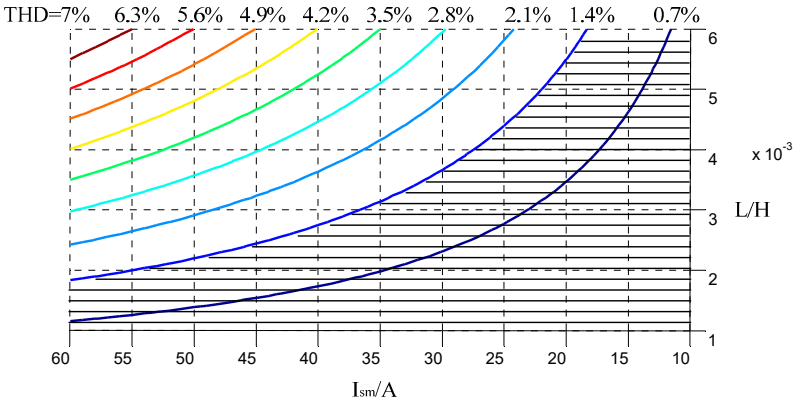


Figure 12. Contour line of current THD under a unity power factor.

If the value of L and I_{sm} are determined in the design, the range of power factor angle θ can be determined based on the allowable range of THD. This also demonstrates the relation between THD and θ. Under the conditions where I_{sm} = 92 A, U_{sm} = 311 V, and L = 3 mH (θ less than zero refers to input current phase leading grid voltage phase), Figure 13 can be obtained. When the current phase leads the grid voltage phase, THD increases rapidly with the leading angle. When the current lags grid voltage by about 16°, the theorical value of THD is closer to zero because the AC-side voltage and input current are in the same phase position at this moment, and no polarity opposite exists in this period, thus avoiding current zero-crossing distortion. When the current lags grid voltage more than 16°, THD increases with the lagging angle, but the degree is less than that when the current leads the grid voltage. The range of the power factor angle can be determined from Figure 13 to ensure THD falls within the allowable range, which actually determines the reactive compensation capacity of the bridgeless rectifier. In conclusion, the mathematical analysis of the current distortion can be used to select filter inductance, input current amplitude, and power factor angle.

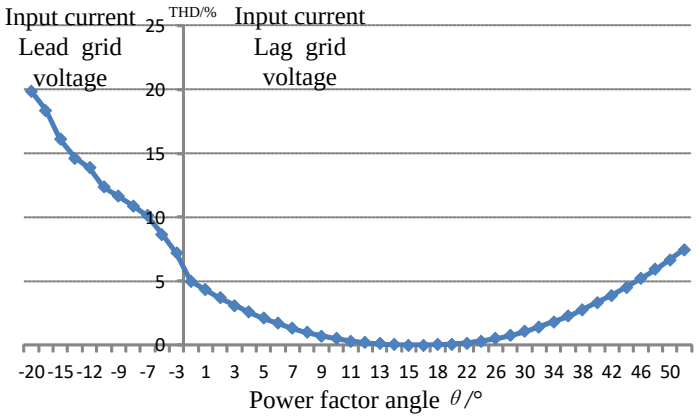


Figure 13. Relations between THD and power factor angle θ.

5. Simulation and Experimental Results

A simulation model of a bridgeless rectifier was set up based on MATLAB/Simulink (9.3.0.713579 (R2017b), MathWorks, Natick, MA, USA). The simulation main parameters are shown in Table 2.

Table 2. Main parameters of the simulation.

Parameters	Value
Input voltage (RMS)	220 V
Source voltage frequency	50 Hz
Input current (RMS)	65 A
Input inductance	3 mH
Switching frequency	5 kHz
Load side capacitance	4700 uF
DC-link resistance	0.09 Ω
DC-link voltage	400 V

In order to reduce the current distortion, the complementary drive was adopted for the simulation. Figure 14 depicts the simulation waveforms of the grid voltage and input current under a unity power factor. Voltage and current are in phase, and the current is obviously distorted at the point. The distortion angle is 0.523 radians. The current THD shown in Figure 15 is 5.11%. The theoretical value of distortion angle is 0.5438 radians, and THD theoretical value was 5.01%. Therefore, the theoretical value is basically the same as the simulation result.

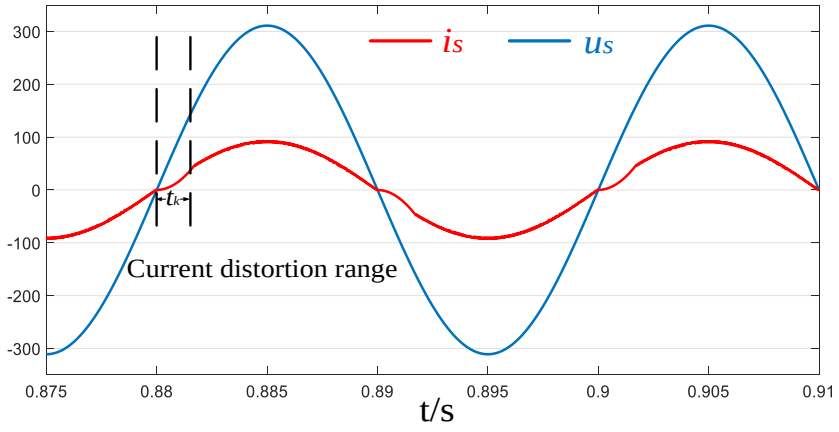


Figure 14. Simulation waveforms of grid voltage and input current under unity power factor.

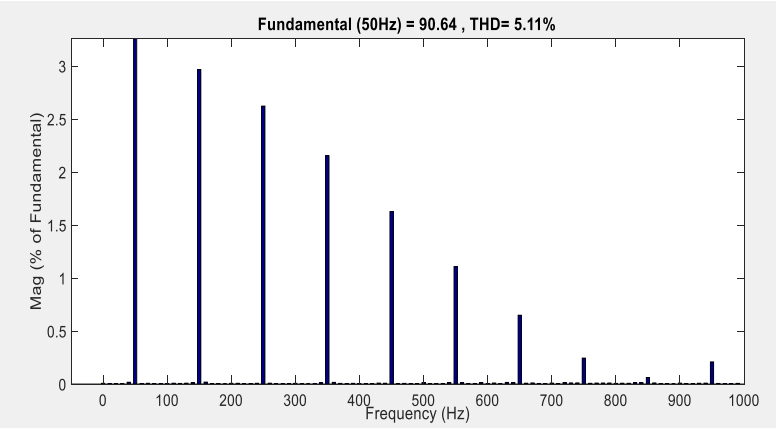


Figure 15. THD analysis of input current under unity power factor.

Figure 16 shows the theoretical value of THD and the simulation value of THD under different I_{sm}. They are basically identical through comparison. Figure 17 depicts the simulation waveforms of the grid voltage and input current when the input current led the grid voltage by 20°. $U_L > |U_s \sin\theta|$ when the angle that the input current lagged grid voltage was 5°, and the simulation waveforms of grid voltage and input current are shown in Figure 18. $U_L < |U_s \sin\theta|$ when the input current lagged the grid voltage by 45°. The simulation waveforms of the grid voltage and input current are shown in Figure 19. The above simulation waveforms basically conform to the theoretical analysis.

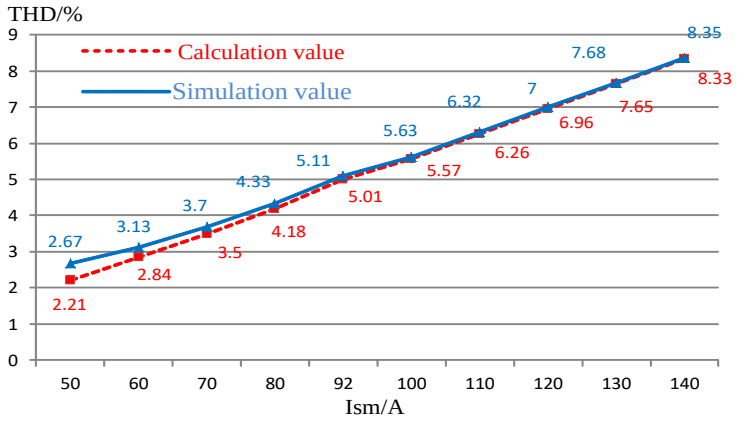


Figure 16. Theoretical and simulation THD under a unity power factor.

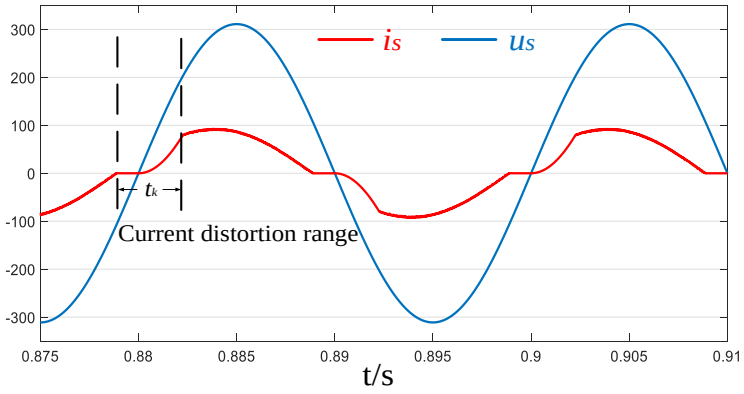


Figure 17. Simulation waveforms of grid voltage and input current under leading power factor.

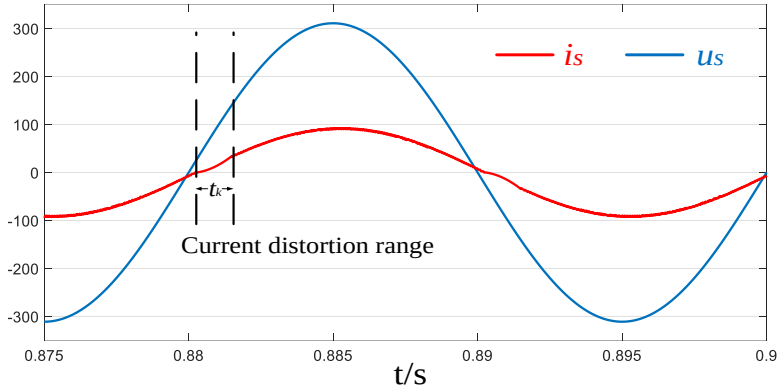


Figure 18. Simulation waveforms of grid voltage and input current when i_s lags u_s by 5°.

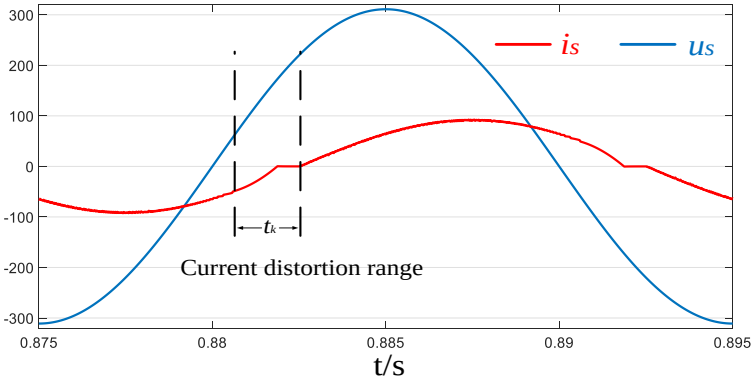


Figure 19. Simulation waveforms of grid voltage and input current when i_s lags u_s by 45°.

Figure 20 shows the relation between theoretical value of THD and simulation value of THD with θ under the conditions of I_{sm} = 92 A, U_{sm} = 311 V, and L = 3 mH. The theoretical value is basically the same as the simulation result. It should be noted that the switching frequency and the higher harmonic of its multiple were ignored when the THD was calculated. However, the smaller the THD, the larger the proportion of higher harmonic in current distortion. Therefore, when THD is closer to zero, its theoretical value is slightly less than the simulation value.

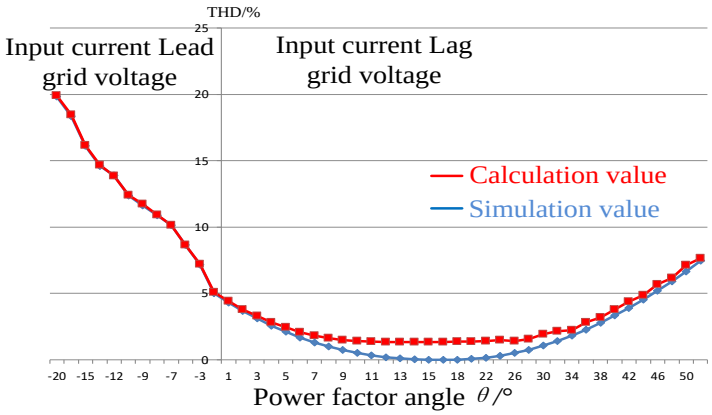


Figure 20. Relationship between theoretical THD and simulation THD with power factor angle θ.

The down-scale prototype of a bridgeless rectifier was set up with TMS320F28335 as a core controller. The parameters of this prototype are provided in Table 3. IXFH46N65X2 46-A 650-V MOSFETs, and IDW15E65D2 30-A 650-V power silicon diodes were employed throughout. Aluminum electrolyte capacitors and input inductor with a Toroidal Ferrite Core and 117 turns of 0.1 × 200 Litzy wire were also adopted in this experiment, on DC side AC side, respectively.

Table 3. The main parameters of the experiments.

Parameter	Value
Input voltage (RMS)	24 V
Source voltage frequency	50 Hz
Input current (RMS)	1.37 A
Input inductance	5 mH
Switching frequency	5 kHz
Load side capacitance	2200 uF
DC-link resistance	50 Ω
DC-link voltage	40 V

Complementary drive mode as adopted. The downscaled prototype is shown in Figure 21.

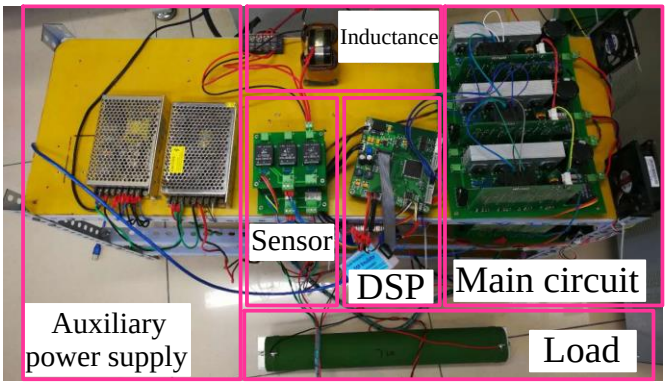


Figure 21. Down-scale experimental prototype.

Figure 22 shows the waveform of u_s and i_s under a unity power factor. The zero-crossing points of i_s coincided with u_s, and i_s distorted based approximately on the cosine law in the period after crossing the zero point. Figure 23 shows the zoomed-in waveforms of driving signals g_{S1} and i_s of u_s and S_1. $u_s > 0$ during the distortion period of i_s, whereas S_1 remains in conduction in order to make u_{con} approximate zero. All the above experiment results satisfy the theoretical analysis.

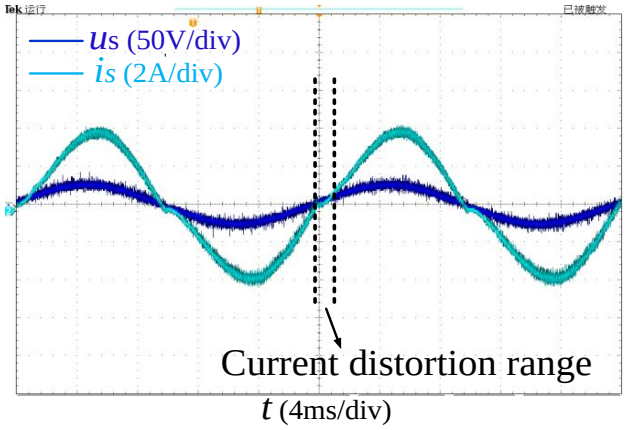


Figure 22. Experiment waveforms of grid voltage and input current under unity power factor.

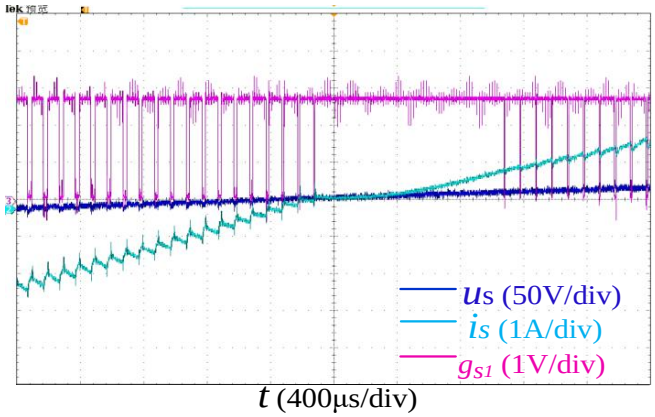


Figure 23. Zoomed-in experiment waveforms of grid voltage and input current under unity power factor.

Figure 24 shows the experiment waveforms of u_s and i_s under a leading power factor. i_s stays near zero within a period after crossing zero. u_s gradually turns to sine waveform after crossing zero, which satisfies the proposed theoretical analysis. Figures 25 and 26 show the experiment waveforms of u_s and i_s when the angles i_s lag u_s by 8°and 40°, respectively. When the lagging angle is 8°, $U_L > |U_s \sin\theta|$. When it is 40°, $U_L < |U_s \sin\theta|$. These experimental waveforms basically conform to the theoretical analysis and simulation waveforms.

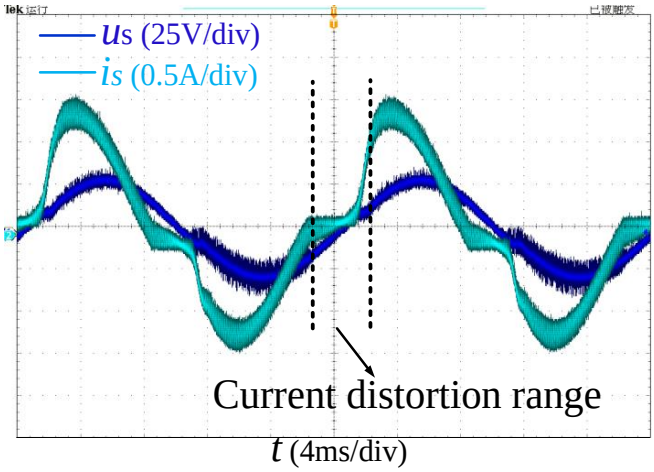


Figure 24. Experiment waveforms of grid voltage and input current under leading power factor.

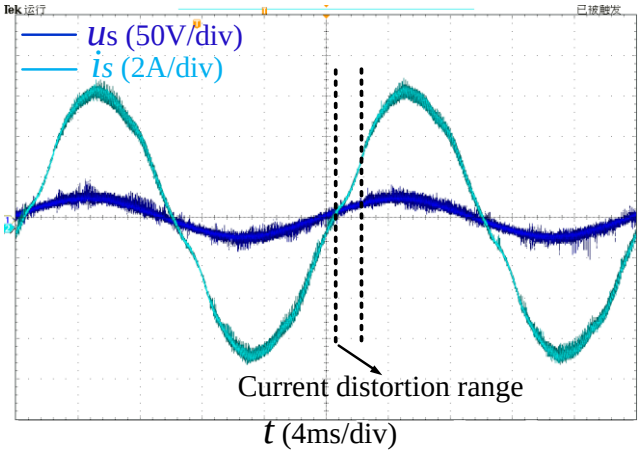


Figure 25. Experiment waveforms of grid voltage and input current when is lags us by 8°.

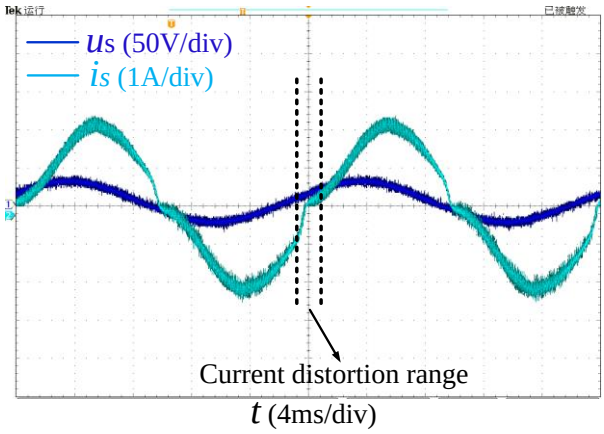


Figure 26. Experiment waveforms of grid voltage and input current when i_s lags u_s by 40°.

6. Conclusions

In order to more effectively integrate the RPC and HCC capabilities into the bridgeless rectifier, the input current harmonic characteristic of bridgeless rectifier under different power factors in two driving modes is discussed in this paper. Firstly, two driving modes are analyzed. Based on the above analysis, it is concluded that the complementary drive mode is a better choice in terms of reducing the current distortion when bridgeless rectifier operates under non-unity power factor. And then, the mechanism of input current zero-crossing distortion is analyzed. Furthermore, the input current during the distortion is expressed by the piecewise function when a bridgeless rectifier operates under complementary driving mode. Based on the piecewise function, the harmonic analysis is performed. Besides, when bridgeless rectifier operates under non-unity power factor, the above analysis makes the criteria of selecting parameters including the filter inductance, input current amplitude and power factor angle be further improved. Finally, the correctness and effectiveness of proposed theory is verified through the simulation and the experiment.

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Conflicts of Interest: The authors declare no conflict of interest.

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