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PLL-Less Three-Phase Four-Wire SAPF with STF-*dq*0 Technique for Harmonics Mitigation under Distorted Supply Voltage and Unbalanced Load Conditions

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Abstract: This paper presents a non-iterative technique that generates reference current to manage operation of a three-phase four-wire shunt active power filter which employs a three-leg split capacitor voltage source inverter (VSI) topology. The proposed technique integrates together a self-tuning-filter (STF) and direct-quadrature-zero (*dq*0) principle (referred here as STF-*dq*0), allowing the controlled shunt active power filter (SAPF) to perform effectively under distorted source voltages and unbalanced load conditions. Unlike the previous technique developed based on the standard *dq*0 principle, the proposed technique does not require any service from a phase-locked loop (PLL) where two STFs are applied to separate harmonic and fundamental elements for the purpose of generating synchronization phases and reference current, respectively. Simulation work which includes connection of the SAPF circuits, design of control techniques and all the necessary assessments are conducted in MATLAB-Simulink platform. Performance achieved by the SAPF while utilizing the proposed technique is thoroughly investigated and benchmarked with that demonstrated by the SAPF while using the standard *dq*0 technique, to evaluate the inherent advantages. Exhaustive simulation results are provided and thoroughly discussed to support design concept, effectiveness, and benefits of the proposed technique.

Keywords: *dq*0 principle; harmonics filtering; voltage source inverter; neutral current; reference current generation; synchronization phase; unbalanced load

1. Introduction

Ensuring good quality of power supply is often a challenging task due to ever-increasing usage of power electronics products. These products, which are more commonly known as nonlinear loads, draw non-sinusoidal currents and reactive power from the connected power system, and cause high harmonic distortion (indicated by total harmonic distortion (THD) values) in the source current and deteriorate overall power system efficiency (indicated by power factor). Moreover, in three-phase four-wire system, connection of single-phase loads and unequal loads distribution across the three phases causes excessive neutral currents. These power quality issues can partially be solved by applying passive filter. The viable solution is by using active power filter (APF) connected in parallel to the polluted power system. APFs that are applied in this manner are called the shunt-typed. The good thing about shunt active power filters (SAPFs) is that they are able to deal with unbalanced issues in the source current along with mitigating harmonic current and compensating reactive power.

For application in three-phase four-wire system, SAPFs are available in two basic topologies. First, three-leg split capacitor topology where the middle-point of its dc-link is connected to the neutral

wire of the power system [1]. Second, four-leg topology which is a more complex topology due to higher number of semiconductor switches employed and an additional control input [2]. In this work, the split capacitor topology is preferred for its less complicated structure. Its connection path to the neutral wire allows the excessive neutral currents to flow towards the two dc-link capacitors where they will be absorbed and eventually be removed from the neutral wire [3]. Nevertheless, this is only possible when the controller is designed with such ability. However, as a result of using the two dc-link capacitors, the controller design is undoubtedly becoming more challenging as the controller needs to cope with voltage imbalance problem now. Overall, other than the common mitigation issues encountered in a typical three-phase three-wire system, the SAPF is demanded to cope with additional issues of neutral current and dc-link voltage unbalance when it is applied in a three-phase four-wire system.

According to *dq*0 principle, ability to extract fundamental element from the load current and synchronization phases from the source voltage is the key factor that determines quality of the generated reference current. In *dq*0-frames, the load current comprises of fundamental (appear as dc signal) and harmonic (appear as ripples) elements. A high ripple level tends to degrade capability of the technique and quality of the generated reference current. However, high-pass filter (HPF) which is commonly applied to isolate the fundamental and harmonic elements may not be effective even though a good agreement between filter's order and its cutoff frequency has been met. Moreover, many issues exist in matching the filter's order and cutoff frequency as it is performed in iterative manner. In other words, there is a need to test various combinations of the filter's order and cutting frequency to find out the best combination. As a result, large amount of time will be spent just for the tuning purposes, and thus not worthwhile to be implemented.

Another inherent weakness of the standard *dq*0 technique is that it requires the service of an additional phase-locked loop (PLL) circuit to perform *dq*0-frames transformation and subsequently synchronize reference current with that of the operating power system. The additional PLL circuit not only complicates its control structure, but also fails to perform satisfactorily especially when the source voltage is subjected to distortion [9,10]. An alternative to solve phase tracking error of a standard PLL is by improving its tracking capability, and this has led to the development of self-tuning-filter (STF) PLL [10] and decoupled double PLL [9]. However, the incorporation of STF and decoupling network in PLL structure further increases complexity of an already complex PLL structure.

In this study, a technique to generate reference current (named as STF-*dq*0) for a three-phase four-wire SAPF without needing any service from a PLL is proposed. The proposed technique is developed and evaluated in MATLAB-Simulink platform (R2012a, The MathWorks, Inc., Natick, MA, USA). To confirm theoretical development of the proposed technique, it is thoroughly tested and evaluated under various scenarios of source voltages (including distorted and unbalanced conditions) and unbalanced loads. Moreover, to show benefits of the proposed technique, the standard *dq*0 technique is implemented too, and both techniques are evaluated in a comparative manner under similar test scenarios. The next section presents power circuit arrangement of SAPF and control techniques applied in this work. In Section 3, working principle of the standard *dq*0 technique is described. Next, with reference to the standard *dq*0 technique, the proposed STF-*dq*0 technique is presented in Section 4, focusing on the implemented enhancements. All simulation findings are

presented and thoroughly discussed in Section 5. Finally, a brief conclusion is provided to highlight contributions of this work.

2. Three-Phase Three-Leg Four-Wire Shunt Active Power Filter: Arrangement of Power Circuits and Control Strategies

Figure 1 shows power circuit arrangement and control structure of a three-phase three-leg four-wire SAPF. A standard two-level inverter with two split dc-link capacitors (serving as the SAPF) is connected to the operating power system at point of common coupling (PCC) between the power supply and nonlinear loads. Note that there is an output filter interfacing between the SAPF and the connected power system. Its main purpose is to minimize switching ripples generated by SAPF so that mitigating opposition current (referred here as injection current i_{inj}) can effectively be injected into any polluted power system to cancel out harmonic current. Furthermore, the middle-point of the two dc-link capacitors is connected to the return neutral wire N to minimize neutral current. In addition, while performing mitigation function, a certain amount of current (referred here as dc-link charging current i_{dc}) is also drawn by the SAPF to regulate voltage across its dc-link capacitors. In a three-phase four-wire power system, the connected nonlinear loads can be of single-phase balanced/unbalanced and three-phase balanced loads. When the SAPF is installed and functioning properly, harmonic current and excessive neutral current in the polluted power system will slowly be removed and eventually the source current will be balanced and regain its sinusoidal appearance with fundamental frequency, and neutral current will be maintained at zero.
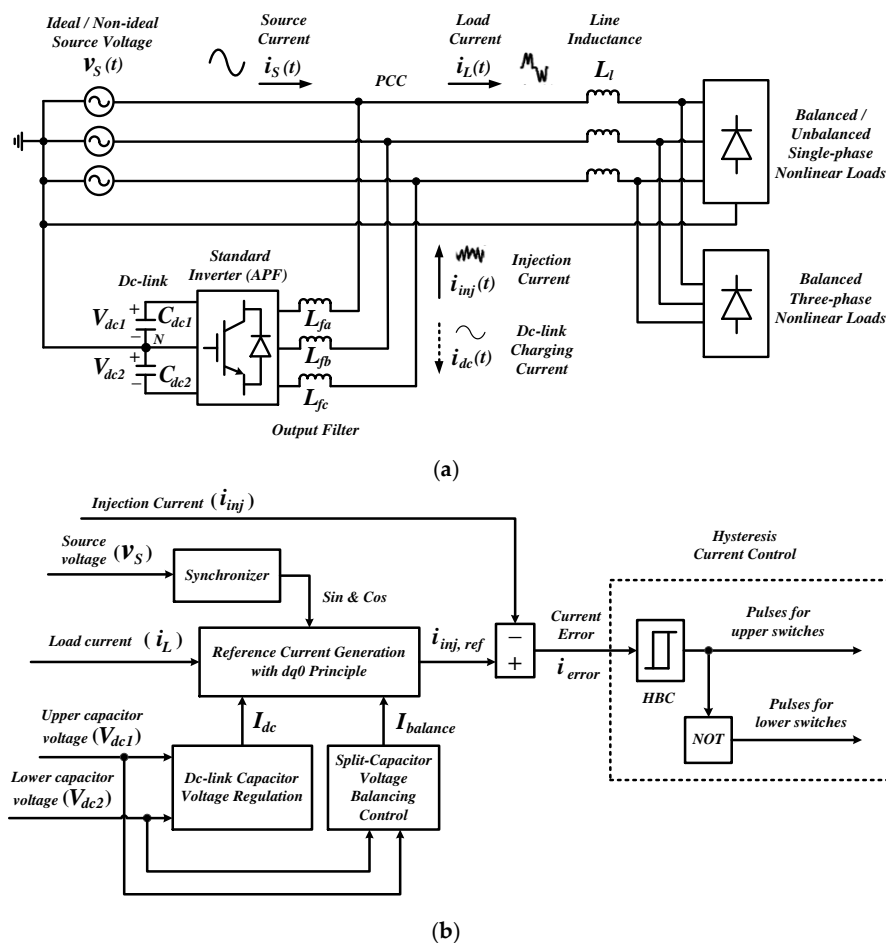

(a)

(b)

Figure 1. Three-phase three-leg four-wire shunt active power filter (SAPF) with two split dc-link capacitors: (**a**) power circuit arrangement, and (**b**) overall control structure.

To effectively manage operation of SAPF in a three-phase four-wire system, its control system needs to perform few control procedures which include extraction of synchronization phases (sin & cos) from source voltage v_S, extraction of harmonic current from load current i_L, estimation of I_{dc} (magnitude of the dc-link charging current i_{dc}) and $I_{balance}$ (balancing current) from split dc-link capacitor voltages (V_{dc1} and V_{dc2}), derivation of reference current $i_{inj,\,ref}$ by using all the signals obtained in the previous procedures, and generation of switching pulses based on the generated reference current $i_{inj,\,ref}$. It is important to note that operation of a typical SAPF is fully based on characteristic of the generated reference current. In this work, other than mitigation of harmonic current, the SAPF is also needed to regulate its dc-link voltage and ensure voltage balance across its split dc-link capacitors. Hence, the generated reference current must contain details on system's harmonics, compatible phases to ensure synchronized operation, amount of dc-link charging current to maintain constant dc-link voltage and balancing current to manage voltage balance of the two split dc-link capacitors.

This manuscript emphasizes on the control procedure of generating reference current where it is performed according to *dq*0 principle. Further details are presented in Sections 3 and 4. Meanwhile, to regulate dc-link voltage and maintain voltage balance of the split dc-link capacitor, the conventional proportional-integral (PI) technique is adopted due to its straightforward feature [1,11]. Lastly, to generate switching pulses, a standard hysteresis band current control (HBC) technique is applied as it offers the benefits of structure simplicity and quick current controllability [1,2,6].

3. Working Principle of the Standard *dq*0 Technique

Figure 2 shows control structure of a standard *dq*0 technique which is commonly applied for the purpose of generating reference current. According to *dq*0 principle, extraction of harmonic current from load current is performed on *dq*0-frames where the load current i_{Labc} (in *abc*-domain) is first transformed into $\alpha\beta$0-domain by using Clarke-matrix expressed as Equation (1) and then into *dq*0-frames by using Park-matrix expressed as Equation (2).

$$T_{\alpha\beta0}^{abc} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{1}$$

$$T_{dq}^{\alpha\beta} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ -\cos(\omega t) & \sin(\omega t) \end{bmatrix} \tag{2}$$

Note that $\sin(\omega t)$ and $\cos(\omega t)$ denote synchronization reference phases which are particularly delivered by a PLL.

Let the three-phase load current expressed in matrix form be $i_{Labc} = [i_{La}\ i_{Lb}\ i_{Lc}]^{\mathrm{T}}$. Hence, by using Equation (1), the corresponding representation in $\alpha\beta$0-domain can be expressed as:

$$\begin{bmatrix} i_{L\alpha} & i_{L\beta} & i_{L0} \end{bmatrix}^{\mathrm{T}} = T_{\alpha\beta0}^{abc} \begin{bmatrix} i_{La} & i_{Lb} & i_{Lc} \end{bmatrix}^{\mathrm{T}}. \tag{3}$$

Subsequently, load current $i_{L\alpha\beta}$ in $\alpha\beta$-domain is further transformed into *dq*-frames according to Equation (4). Note that 0-domain of $\alpha\beta$0-domain is not required in the transformation process, and it is directly applied as 0-frame of *dq*0-frames. In other words, 0-domain is equivalent to 0-frame.

$$\begin{bmatrix} i_{Ld} & i_{Lq} \end{bmatrix}^{\mathrm{T}} = T_{dq}^{\alpha\beta} \begin{bmatrix} i_{L\alpha} & i_{L\beta} \end{bmatrix}^{\mathrm{T}} \tag{4}$$
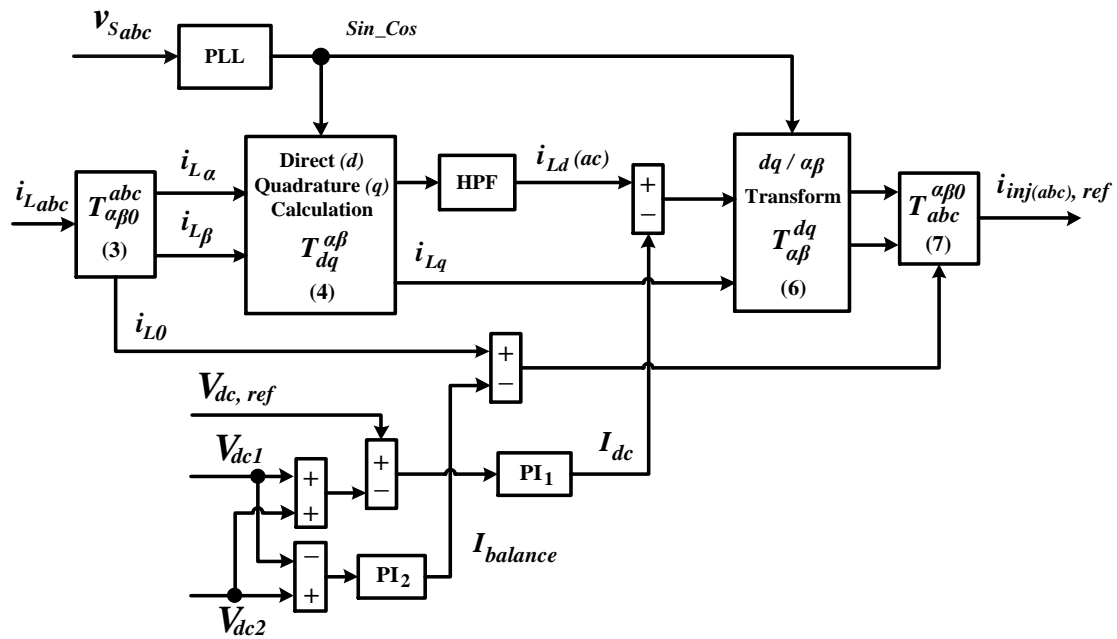
Figure 2. Block diagram showing control structure of standard *dq*0 technique [1].

In *dq*-frames, as a consequence of harmonic contamination, the load current signal contains both fundamental (stationary dc) and harmonic (oscillating ac) elements. Hence, the following relationship can be formed:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} i_{Ld(dc)} + i_{Ld(ac)} \\ i_{Lq(dc)} + i_{Lq(ac)} \end{bmatrix} \tag{5}$$

where $i_{Ld\,(dc)}$ and $i_{Ld\,(ac)}$, respectively, denote the dc and ac elements of the load current in *d*-frame. The same representation applies to the elements of load current in *q*-frame. Note that the stationary dc element of *d*-frame represents the magnitude of fundamental load current whereas the oscillating ac element represents the magnitude of harmonic current. On the other hand, *q*-frame contains phase information of the load current. Not to forget, 0-frame of *dq*0-frames which is directly taken from that of $\alpha\beta$0-domain is needed to maintain dc-link voltage balance. In other words, the ac element of *d*-frame load current $i_{Ld(ac)}$, *q*-frame load current i_{Lq} and 0-frame load current i_{L0} are three distinct unwanted parts of load currents that represent harmonic, reactive and unbalanced currents, respectively.

Hence, in order to remove those unwanted signals, to maintain constant dc-link voltage and to maintain voltage balance across the two split dc-link capacitors, the reference current $i_{inj(abc),\,ref}$ is derived by considering all those factors according to the following approach:

$$\begin{bmatrix} i_{L\alpha,\,ref} & i_{L\beta,ref} \end{bmatrix}^{\mathrm{T}} = T_{\alpha\beta}^{dq} \begin{bmatrix} \left(i_{Ld(ac)} - I_{dc}\right) & i_{Lq} \end{bmatrix}^{\mathrm{T}} \tag{6}$$

$$\begin{bmatrix} i_{inja,ref} & i_{injb,ref} & i_{injc,ref} \end{bmatrix}^{\mathrm{T}} = T_{abc}^{\alpha\beta0} \begin{bmatrix} i_{L\alpha,ref} & i_{L\beta,ref} & \left(i_{L0} - I_{balance}\right) \end{bmatrix}^{\mathrm{T}} \tag{7}$$

where inverse Park-matrix $T_{\alpha\beta}^{dq}$ and inverse Clarke-matrix $T_{abc}^{\alpha\beta0}$ are given as follows:

$$T_{\alpha\beta}^{dq} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) \\ \cos(\omega t) & \sin(\omega t) \end{bmatrix} \tag{8}$$

$$T_{abc}^{\alpha\beta0} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}. \tag{9}$$

Meanwhile, I_{dc} symbolizes the amount of dc-link charging current i_{dc} needed to maintain constant dc-link voltage at desired level (denoted as $V_{dc,\,ref}$) and compensate losses associated with switching operation of SAPF, and $I_{balance}$ symbolizes the amount of balancing current needed to maintain the voltage balance.

The oscillating ac element of *d*-frame load current $i_{Ld(ac)}$ applied in Equation (6) can be obtained by filtering directly the *d*-frame load current with a high-pass filter (HPF) [1,6,12]. It is worth noting that in some *dq*0 techniques, the oscillating ac element is also obtained indirectly by using low-pass filter (LPF) associated with a simple calculation, in which the LPF is first applied to obtain the stationary dc element $i_{Ld(dc)}$ and is then subtracted from the actual *d*-frame load current i_{Ld} [13–15]. Next, I_{dc} is estimated by minimizing the error $e_1(t)$ resulted between reference dc-link voltage $V_{dc,\,ref}$ and the total instantaneous dc-link voltage ($V_{dc}(t) = V_{dc1}(t) + V_{dc2}(t)$) with a PI controller. Mathematically, the approach can be expressed as:

$$I_{dc} = k_{p1}e_1(t) + k_{i1}\int_0^t e_1(t)dt \tag{10}$$

$$e_1(t) = V_{dc,\,ref} - (V_{dc1}(t) + V_{dc2}(t)) \tag{11}$$

where k_{p1} and k_{i1} are the two constant values that respectively symbolize proportional and integral gains of PI_1 (first PI) controller. In this work, the values are set to be 0.3 and 2, respectively. Similarly, a PI controller is applied to estimate $I_{balance}$ by minimizing the error $e_2(t)$ resulted between the two split dc-link capacitors. Mathematically, the approach can be expressed as:

$$I_{balance} = k_{p2}e_2(t) + k_{i2}\int_0^t e_2(t)dt \tag{12}$$

$$e_2(t) = V_{dc2}(t) - V_{dc1}(t) \tag{13}$$

where k_{p2} and k_{i2} are the two constant values that respectively symbolize proportional and integral gains of PI_2 (second PI) controller. The values are set to be 0.02 and 0.1, respectively.

4. Working Principle the Proposed STF-*dq*0 Technique

Figure 3 presents a block diagram that illustrates control structure and particulars of the proposed STF-*dq*0 technique. Basically, the proposed STF-*dq*0 technique generates reference current in a similar manner to that of a standard *dq*0 technique where both techniques perform according to the consecutive transformation sequences of "*abc-αβ0-dq0-αβ0-abc*". However, in the proposed technique, two modifications are made to further enhance capability of SAPF in performing its intended functions. First, the conventional PLL circuit is removed and replaced with a straightforward synchronization technique. Second, instead of applying HPF to perform direct extraction of harmonic element on *dq*0-frames, a self-tuning-filter (STF) is employed to extract the harmonic element indirectly on *αβ*0-domain (an earlier transformation stage before entering the *dq*0-frames).
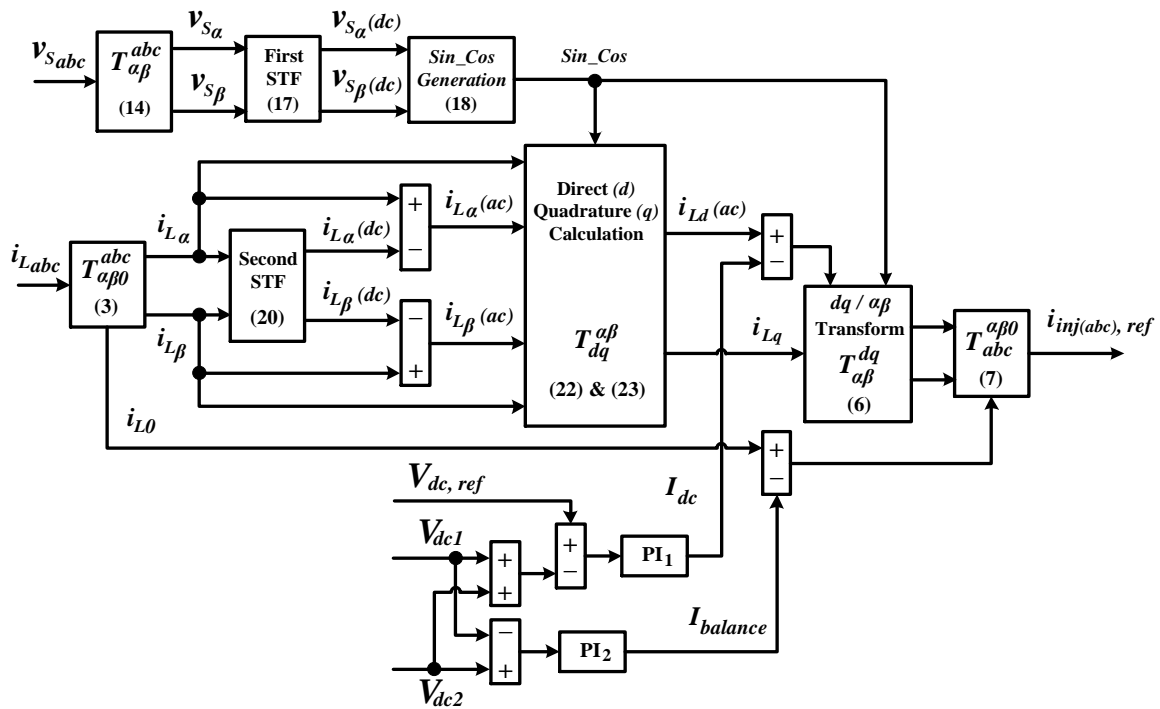
Figure 3. Block diagram showing control structure of the proposed self-tuning-filter (STF)-*dq*0 technique.

In the proposed STF-*dq*0 technique, the process of extracting synchronization phases from the source voltage is rather straightforward and non-iterative. Let the three-phase source voltage expressed in matrix form be $v_{Sabc} = [v_{Sa}\ v_{Sb}\ v_{Sc}]^{\mathrm{T}}$, and by using Clarke-transform matrix (considers only two phases $\alpha\beta$-domain), the source voltage signals (in *abc*-domain) can be transformed into $\alpha\beta$-domain according to:

$$\begin{bmatrix} v_{S\alpha} & v_{S\beta} \end{bmatrix}^{\mathrm{T}} = \boldsymbol{T}_{\alpha\beta}^{abc} \begin{bmatrix} v_{Sa} & v_{Sb} & v_{Sc} \end{bmatrix}^{\mathrm{T}} \tag{14}$$

where

$$\boldsymbol{T}_{\alpha\beta}^{abc} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{15}$$

In $\alpha\beta$-domain, under influence of distortions, the voltage signals can respectively be decomposed into fundamental and harmonic elements. Hence, the following relationship can be formed:

$$\begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = \begin{bmatrix} v_{S\alpha(dc)} + v_{S\alpha(ac)} \\ v_{S\beta(dc)} + v_{S\beta(ac)} \end{bmatrix} \tag{16}$$

where $v_{S\alpha(dc)}$ and $v_{S\alpha(ac)}$ denote the fundamental (dc) and harmonic (ac) elements of source voltage in α-domain, respectively. The same representation applies to element of source voltages in β-domain. To generate synchronization phases, the dc elements in both $\alpha\beta$-domain are required. A self-tuning filtering approach [16] is applied to extract the dc elements. The applied STF is capable of suppressing all the harmonic elements existed in the distorted voltage signals and thus improving quality of the extracted synchronization phases. As revealed in [16–18], the transfer function (after performing Laplace transformation) of a typical STF can be expressed as follow:

$$\begin{bmatrix} v_{S\alpha(dc)}(s) \\ v_{S\beta(dc)}(s) \end{bmatrix} = \frac{K_1}{s} \begin{bmatrix} v_{S\alpha}(s) - v_{S\alpha(dc)}(s) \\ v_{S\beta}(s) - v_{S\beta(dc)}(s) \end{bmatrix} + \frac{2\pi f_{c1}}{s} \begin{bmatrix} -v_{S\beta(dc)}(s) \\ v_{S\alpha(dc)}(s) \end{bmatrix} \tag{17}$$

where K_1 is a constant gain parameter and f_{c1} is the cutoff frequency of STF$_1$ (first STF). In this work, the values are set to be 20 and 50 Hz, respectively. With availability of $v_{S\alpha(dc)}$ and $v_{S\beta(dc)}$, the synchronization phases, $\sin(\omega t)$ and $\cos(\omega t)$ can be obtained according to following approach:

$$\begin{bmatrix} \sin(\omega t) \\ \cos(\omega t) \end{bmatrix} = \frac{1}{\sqrt{v_{S\alpha(dc)}{}^2 + v_{S\beta(dc)}{}^2}} \begin{bmatrix} v_{S\alpha(dc)} \\ v_{S\beta(dc)} \end{bmatrix}. \tag{18}$$

By using Equation (18), the service from conventional PLL can be neglected and the synchronization phases can now effectively be generated regardless of any distortions in the source voltage.

On the other hand, for harmonic extraction, a STF is also employed to perform indirect extraction of harmonic elements from the load current on $\alpha\beta$-domain. By using Equation (3), the three-phase load current in abc-domain is first transformed into $\alpha\beta$-domain. Focusing only on $\alpha\beta$-domain (0-domain does not involve in harmonic extraction), due to harmonic contamination, the load current signals $i_{L\alpha\beta}$ can respectively be decomposed into fundamental and harmonic elements. Hence, the following relationship can be formed:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_{L\alpha(dc)} + i_{L\alpha(ac)} \\ i_{L\beta(dc)} + i_{L\beta(ac)} \end{bmatrix} \tag{19}$$

where $i_{L\alpha(dc)}$ and $i_{L\alpha(ac)}$ denote the fundamental (dc) and harmonic (ac) elements of load current in α-domain, respectively. The same representation applies to elements of load current in β-domain.

The transfer function (after performing Laplace transformation) of STF applied to extract the dc elements ($i_{L\alpha(dc)}$ and $i_{L\beta(dc)}$) of load current in $\alpha\beta$-domain is given as follows:

$$\begin{bmatrix} i_{L\alpha(dc)}(s) \\ i_{L\beta(dc)}(s) \end{bmatrix} = \frac{K_2}{s} \begin{bmatrix} i_{L\alpha}(s) - i_{L\alpha(dc)}(s) \\ i_{L\beta}(s) - i_{L\beta(dc)}(s) \end{bmatrix} + \frac{2\pi f_{c2}}{s} \begin{bmatrix} -i_{L\beta(dc)}(s) \\ i_{L\alpha(dc)}(s) \end{bmatrix}. \tag{20}$$

where K_2 is a constant gain parameter and f_{c2} is the cutoff frequency of STF$_2$ (second STF). In this work, the values are set to be 20 and 50 Hz, respectively. With availability of dc elements ($i_{L\alpha(dc)}$ and $i_{L\beta(dc)}$), the ac elements ($i_{L\alpha(ac)}$ and $i_{L\beta(ac)}$) can be obtained by using simple calculation expressed as:

$$\begin{bmatrix} i_{L\alpha(ac)} \\ i_{L\beta(ac)} \end{bmatrix} = \begin{bmatrix} i_{L\alpha} - i_{L\alpha(dc)} \\ i_{L\beta} - i_{L\beta(dc)} \end{bmatrix}. \tag{21}$$

From Equation (21), it can be seen that according to this STF approach, the ac elements are obtained by subtracting the dc elements (extracted in advance using the STF) from the actual load current signal in $\alpha\beta$-domain $i_{L\alpha\beta}$. Therefore, in this manner, the harmonic or ac elements are said to be extracted indirectly.

Next, the ac elements obtained from Equation (21) and synchronization phases obtained from Equation (18) are applied to perform transformation of $\alpha\beta$-domain into d-frame (contains only ac elements) according to the following approach:

$$i_{Ld(ac)} = i_{L\alpha(ac)} \sin(\omega t) + i_{L\beta(ac)} \cos(\omega t) \tag{22}$$

and meanwhile, the original load current signal in $\alpha\beta$-domain $i_{L\alpha\beta}$ and the similar synchronization phases are applied to perform transformation of $\alpha\beta$-domain into q-frame according to the following approach:

$$i_{Lq} = -i_{L\alpha} \cos(\omega t) + i_{L\beta} \sin(\omega t). \tag{23}$$

Note that 0-domain of $\alpha\beta$0-domain does not need to be transformed, and it is directly applied as 0-frame of dq0-frames. Finally, together with I_{dc} (obtained from Equation (10)) and $I_{balance}$ (obtain from Equation (12)), Equations (6) and (7) are applied to generate the reference current $i_{inj(abc), ref}$.

5. Results and Discussion

Simulation work which includes connection of SAPF circuits, design of its control system, and performance assessment of the proposed STF-*dq*0 technique is performed in MATLAB-Simulink platform (R2012a). Figure 4 shows the simulation model developed for this work. It is constructed using simple Simulink-blocks, and is executed in discrete environment. A standard two-level inverter with split dc-link capacitors of 3300 μF (each) is employed as the SAPF. Its output is connected to a simple 5 mH *L*-typed filter to minimize switching ripples. The line inductance is set to be 1 mH. For this work, the reference dc-link voltage is set to be 880 V (440 V for each split capacitor). The procedures applied for designing and determining parameter specifications of the SAPF are reported in [19–21]. Meanwhile, for the sources of harmonics, two types of nonlinear loads are considered. The first nonlinear load comprises of three single-phase nonlinear loads distributed unequally (in unbalanced manner) across the three phases of the connected power system (referred here as Load 1). The second nonlinear load comprises of three unbalanced single-phase nonlinear loads connected in parallel with a balanced three-phase nonlinear load (referred here as Load 2). Particulars of Loads 1 and 2 are summarized in Table 1.

Table 1. Nonlinear load configuration for simulation work.

Nonlinear Load		Load Descriptions
Load 1: Unbalanced single-phase load	Phase *a*	Uncontrolled single-phase rectifier feeding a parallel connected 80 Ω resistor and 1500 μF capacitor
	Phase *b*	Uncontrolled single-phase rectifier feeding a series connected 20 Ω resistor and 50 mH inductor
	Phase *c*	Uncontrolled single-phase rectifier feeding a parallel connected 60 Ω resistor and 1000 μF capacitor
Load 2: Unbalanced single-phase load and balanced three-phase load connected in parallel (refer Figure 4a)	Phase *a*	Uncontrolled single-phase rectifier feeding a series connected 30 Ω resistor and 30 mH inductor
	Phase *b*	Uncontrolled single-phase rectifier feeding a parallel connected 80 Ω resistor and 1500 μF capacitor
	Phase *c*	Uncontrolled single-phase rectifier feeding a series connected 20 Ω resistor and 50 mH inductor
		Uncontrolled three-phase rectifier feeding a series connected 50 Ω resistor and 100 mH inductor

Analysis is performed in a comparative manner, i.e., by benchmarking performance demonstrated by SAPF while applying the proposed STF-*dq*0 technique, with the one using the standard *dq*0 technique. Steady-state simulation studies are conducted, considering four scenarios of source voltages, i.e., in scenario A, a sinusoidal-balanced source voltage, in scenario B, non-sinusoidal-balanced source voltage, in scenario C, sinusoidal-unbalanced source voltage, and in scenario D, non-sinusoidal-unbalanced source voltage. For these four scenarios, particulars of the source voltages applied are given as follows:
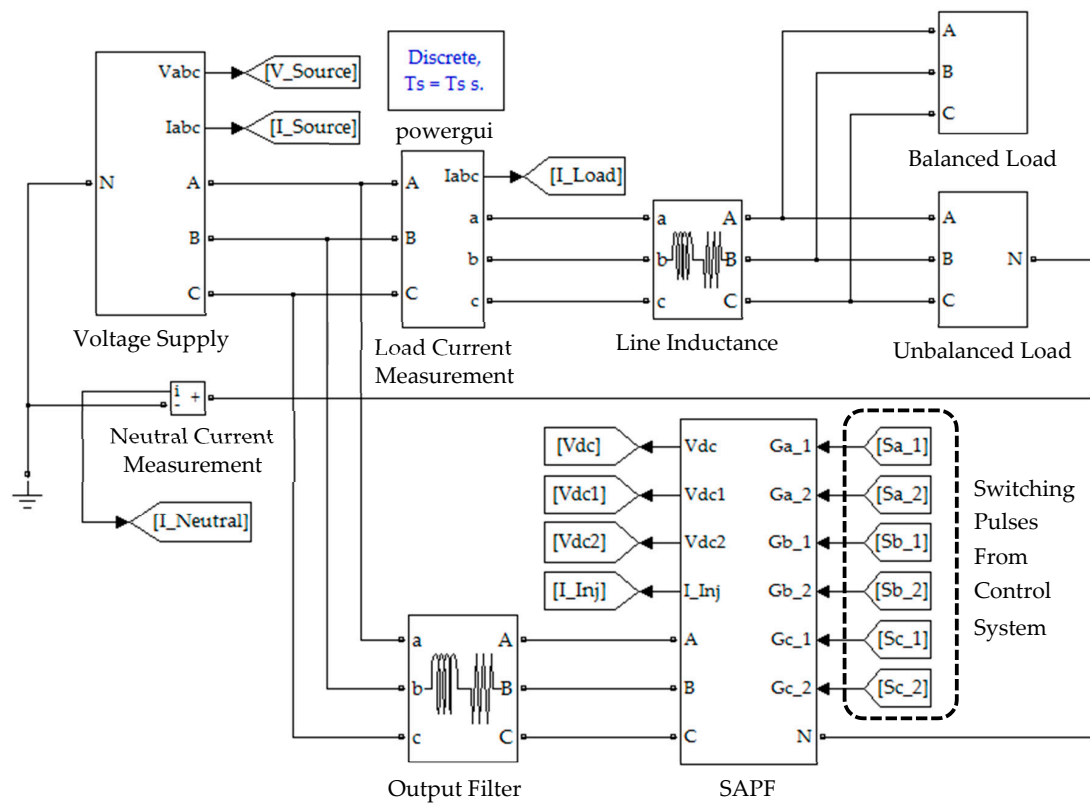
(**a**)
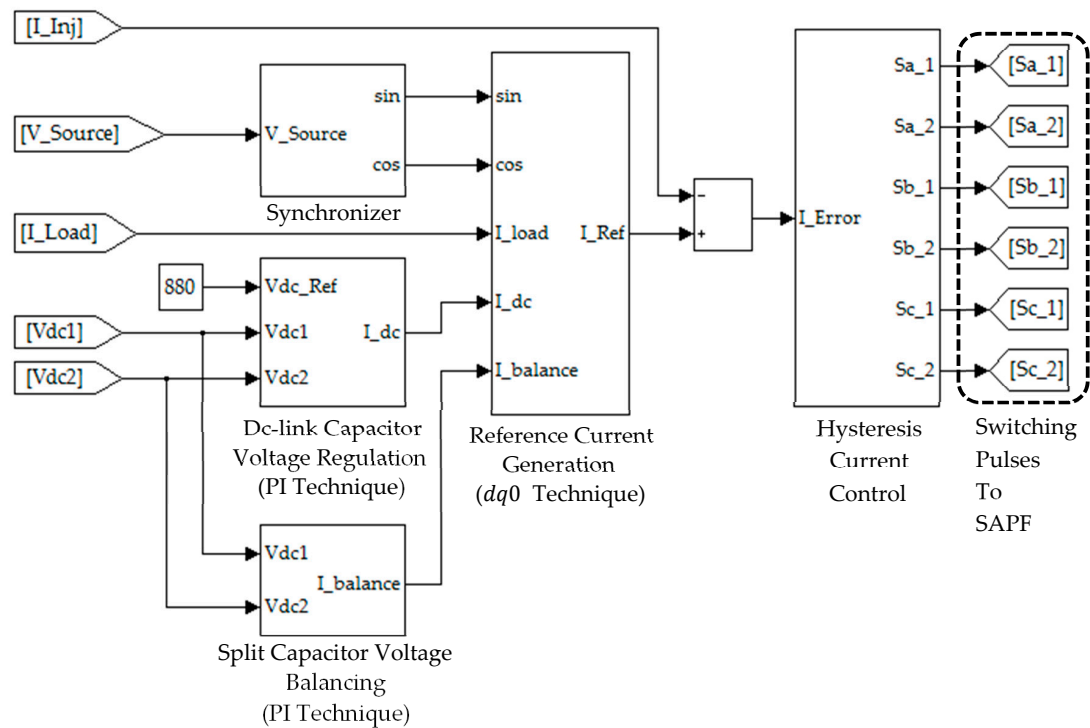
(**b**)

Figure 4. Simulation model of three-phase three-leg four-wire SAPF developed in MATLAB-Simulink platform: (**a**) power circuit arrangement, and (**b**) control system.

Scenario A: Sinusoidal-balanced source voltage:

$$(THDa = THDb = THDc = 0.00\%)$$

$$v_{Sa} = 326\sin(\omega t) \tag{24}$$

$$v_{Sb} = 326\sin\left(\omega t + 240^\circ\right) \tag{25}$$

$$v_{Sc} = 326\sin\left(\omega t + 120^\circ\right). \tag{26}$$

Scenario B: Non-sinusoidal-balanced source voltage:

$$(THDa = THDb = THDc = 20.80\%)$$

$$v_{Sa} = 326\sin(\omega t) + 50\sin(3\omega t) + 40\sin(5\omega t) + 20\sin(7\omega t) + 10\sin(9\omega t) \tag{27}$$

$$\begin{aligned} v_{Sb} = {}& 326\sin\left(\omega t + 240^\circ\right) + 50\sin\left(3\left(\omega t + 240^\circ\right)\right) + 40\sin\left(5\left(\omega t + 240^\circ\right)\right) \\ & +20\sin\left(7\left(\omega t + 240^\circ\right)\right) + 10\sin\left(9\left(\omega t + 240^\circ\right)\right) \end{aligned} \tag{28}$$

$$\begin{aligned} v_{Sc} = {}& 326\sin\left(\omega t + 120^\circ\right) + 50\sin\left(3\left(\omega t + 120^\circ\right)\right) + 40\sin\left(5\left(\omega t + 120^\circ\right)\right) \\ & +20\sin\left(7\left(\omega t + 120^\circ\right)\right) + 10\sin\left(9\left(\omega t + 120^\circ\right)\right). \end{aligned} \tag{29}$$

Scenario C: Sinusoidal-unbalanced source voltage:

$$(THDa = THDb = THDc = 0.00\%)$$

$$v_{Sa} = 326\sin(\omega t) \tag{30}$$

$$v_{Sb} = 246\sin\left(\omega t + 240^\circ\right) \tag{31}$$

$$v_{Sc} = 286\sin\left(\omega t + 120^\circ\right). \tag{32}$$

Scenario D: Non-sinusoidal-unbalanced source voltage

$$(THDa = 16.80\%, THDb = 15.74\% \text{ and } THDc = 6.99\%)$$

$$v_{Sa} = 326\sin(\omega t) + 40\sin(3\omega t) + 30\sin(5\omega t) + 20\sin(7\omega t) + 10\sin(9\omega t) \tag{33}$$

$$\begin{aligned} v_{Sb} = {}& 246\sin\left(\omega t + 240^\circ\right) + 30\sin\left(3\left(\omega t + 240^\circ\right)\right) + 20\sin\left(5\left(\omega t + 240^\circ\right)\right) \\ & +10\sin\left(7\left(\omega t + 240^\circ\right)\right) + 10\sin\left(9\left(\omega t + 240^\circ\right)\right) \end{aligned} \tag{34}$$

$$\begin{aligned} v_{Sc} = {}& 286\sin\left(\omega t + 120^\circ\right) + 10\sin\left(3\left(\omega t + 120^\circ\right)\right) + 10\sin\left(5\left(\omega t + 120^\circ\right)\right) \\ & +10\sin\left(7\left(\omega t + 120^\circ\right)\right) + 10\sin\left(9\left(\omega t + 120^\circ\right)\right). \end{aligned} \tag{35}$$

5.1. Sinusoidal-Balanced Source Voltage (Scenario A)

In Scenario A, an ideal situation of sinusoidal-balanced source voltage is considered. All the simulation waveforms obtained under this scenario are shown in Figures 5–9. Meanwhile, Table 2 summarizes the findings in comparative manner. Referring to Figure 5, it can clearly be observed that both the proposed STF-*dq*0 and standard *dq*0 techniques are able to accurately detect synchronization phase value ωt (appear in the form of sawtooth wave-shape) from a sinusoidal-balanced source voltage. Next, from Figure 6, both techniques are revealed to have effectively directed their respective SAPF in mitigating harmonic currents generated by Loads 1, where the source currents are found to have regained sinusoidal shape with THD values (as tabulated in Table 2) well-maintained below the 5% harmonic limit set by IEEE standard 519 [22]. Note that no significant differences can be

observed between the THD values resulted by the proposed STF-*dq*0 and standard *dq*0 techniques. In addition, it also can be seen that high neutral currents caused by connection of single-phase loads has effectively been reduced by both SAPFs, proving the ability of both techniques in removing excessive neutral currents.

Furthermore, as indicated in Table 2, large phase differences that resulted between the source current and voltage have been minimized by both SAPFs. In other words, it proves that both techniques are able to effectively synchronize operation of SAPF with the operating power system. This is basically due to the accurate synchronization phase value ωt detected by both techniques (as indicated in Figure 5). As a result, the source current seems to work in phase with the source voltage and thus it leads to almost unity power factor of 0.999. Similar findings can be observed for Load 2, as indicated in Figure 8 and Table 2. Therefore, as an overall, both techniques show almost similar performances when operating under sinusoidal-balanced source voltage scenario.

Table 2. Comparative analysis of the proposed STF-*dq*0 and the standard *dq*0 techniques under Scenario A.

| Performance Parameter	Load 1			Load 2		
	Phase *a*	**Phase *b***	**Phase *c***	**Phase *a***	**Phase *b***	**Phase *c***
Before connecting SAPF						
THD value (%)	118.27	25.99	114.73	13.46	45.53	14.73
Phase difference (°)	9.80	15.60	7.50	8.50	6.80	10.90
Power factor	0.636	0.932	0.651	0.980	0.903	0.971
After connecting SAPF with the proposed STF-*dq*0 technique						
THD value (%)	2.97	2.81	2.81	0.98	0.96	1.03
Phase difference (°)	0.70	0.30	0.40	0.00	0.20	0.20
Power factor	0.999	0.999	0.999	0.999	0.999	0.999
After connecting SAPF with the standard *dq*0 technique						
THD value (%)	2.93	2.78	2.92	1.02	0.97	1.01
Phase difference (°)	0.80	0.10	0.60	0.00	0.10	0.20
Power factor	0.999	0.999	0.999	0.999	0.999	0.999
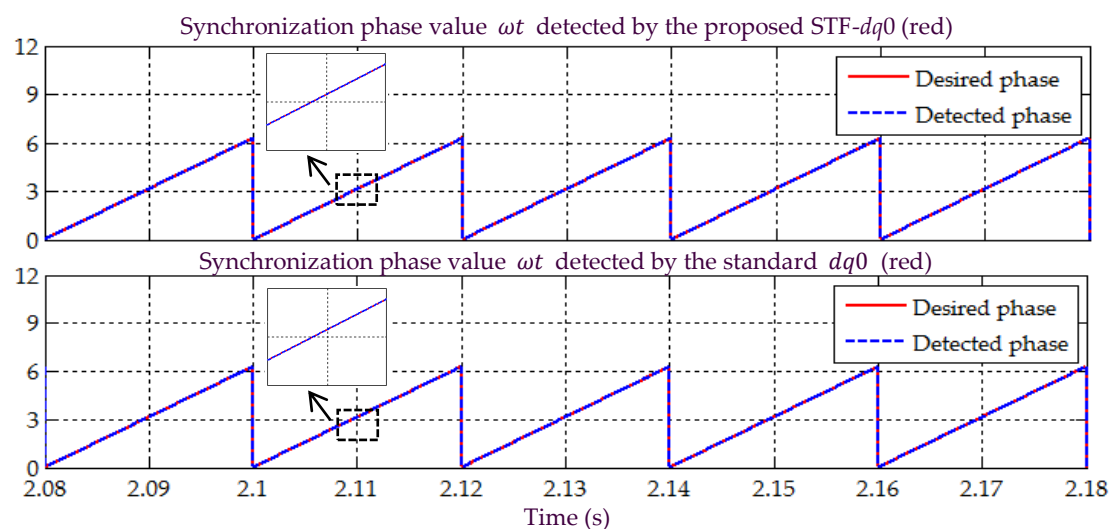
Figure 5. Simulation result showing the detected synchronization reference phase value ωt under Scenario A.

Other than effective harmonic mitigation, ability to regulate dc-link voltage is also an important feature of SAPF, thus must thoroughly be assessed. Figures 7 and 9 provide the related results. From the findings, while applying the proposed STF-*dq*0 technique, the SAPF is found to have effectively regulated and maintained its dc-link voltage at the desired level of 880 V, for both Loads 1 and 2. Similarly, it is also clear from the findings that voltages across the two split dc-link capacitors (V_{dc1} and V_{dc2}) are evenly regulated at half the value of overall dc-link voltage V_{dc}, i.e., 440 V. This implies that the two PI techniques applied respectively for regulating the dc-link voltage and ensuring voltage balance of the two split dc-link capacitors have performed effectively and are compatible with the proposed STF-*dq*0 technique.
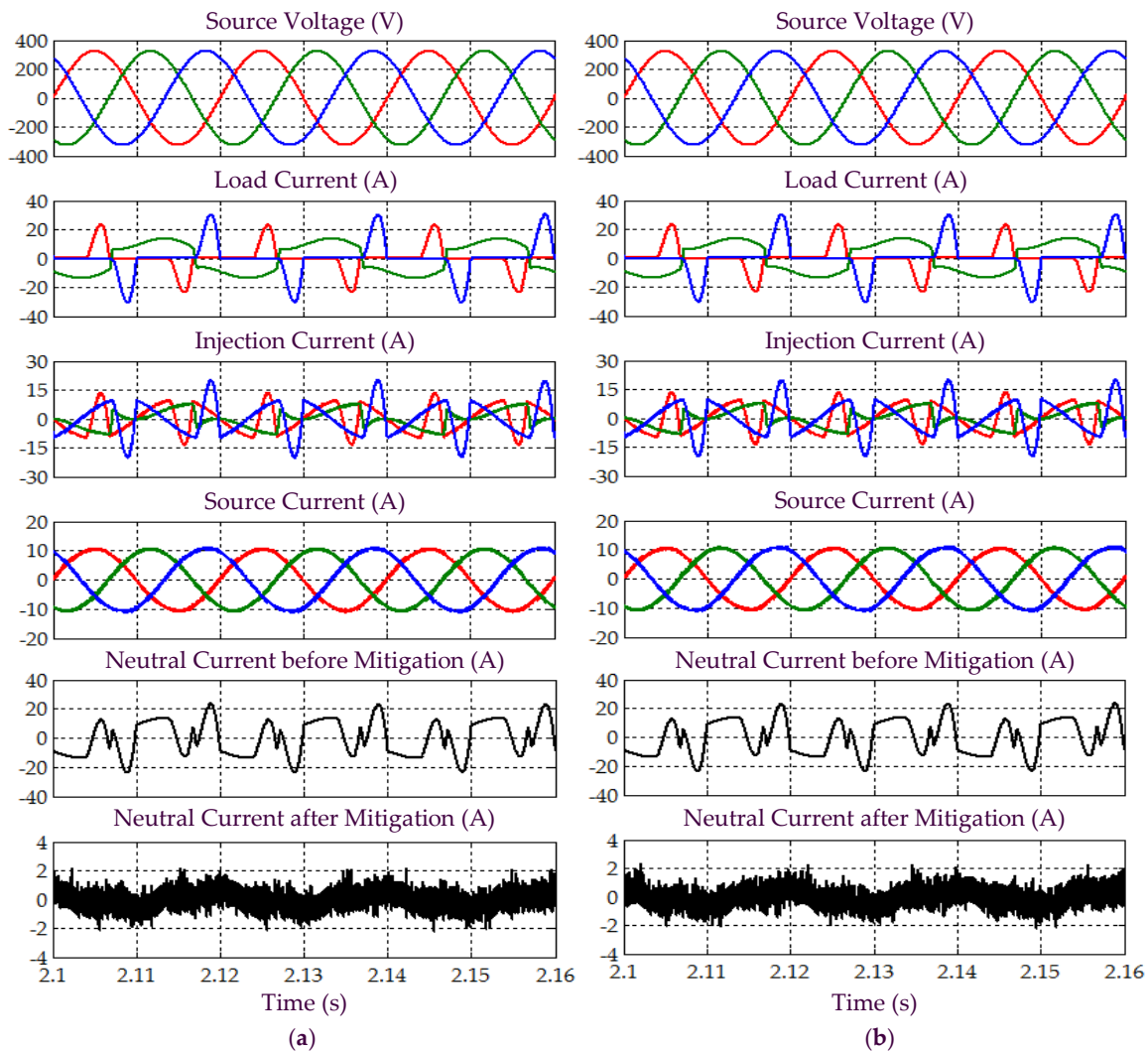
Figure 6. Simulation results obtained under Scenario A for Load 1, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-*dq*0 and (**b**) standard *dq*0 techniques.
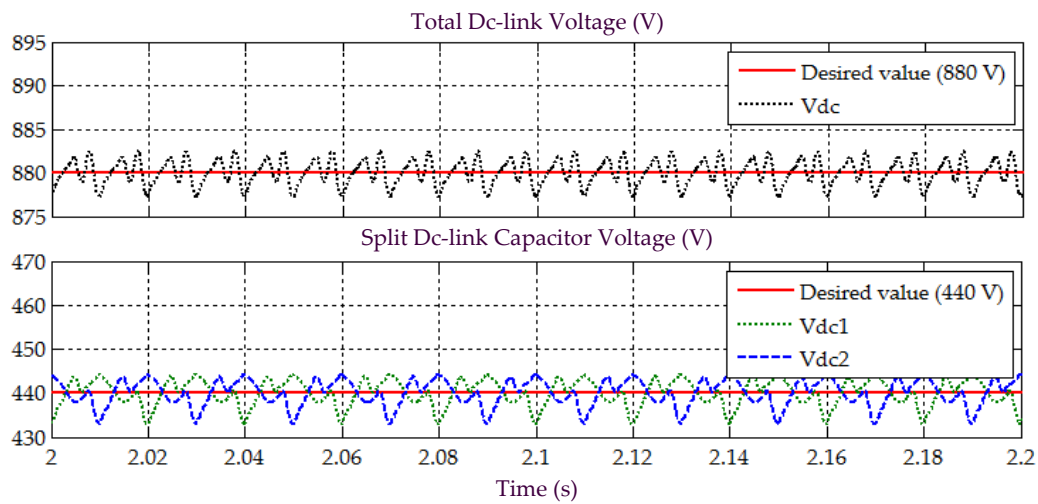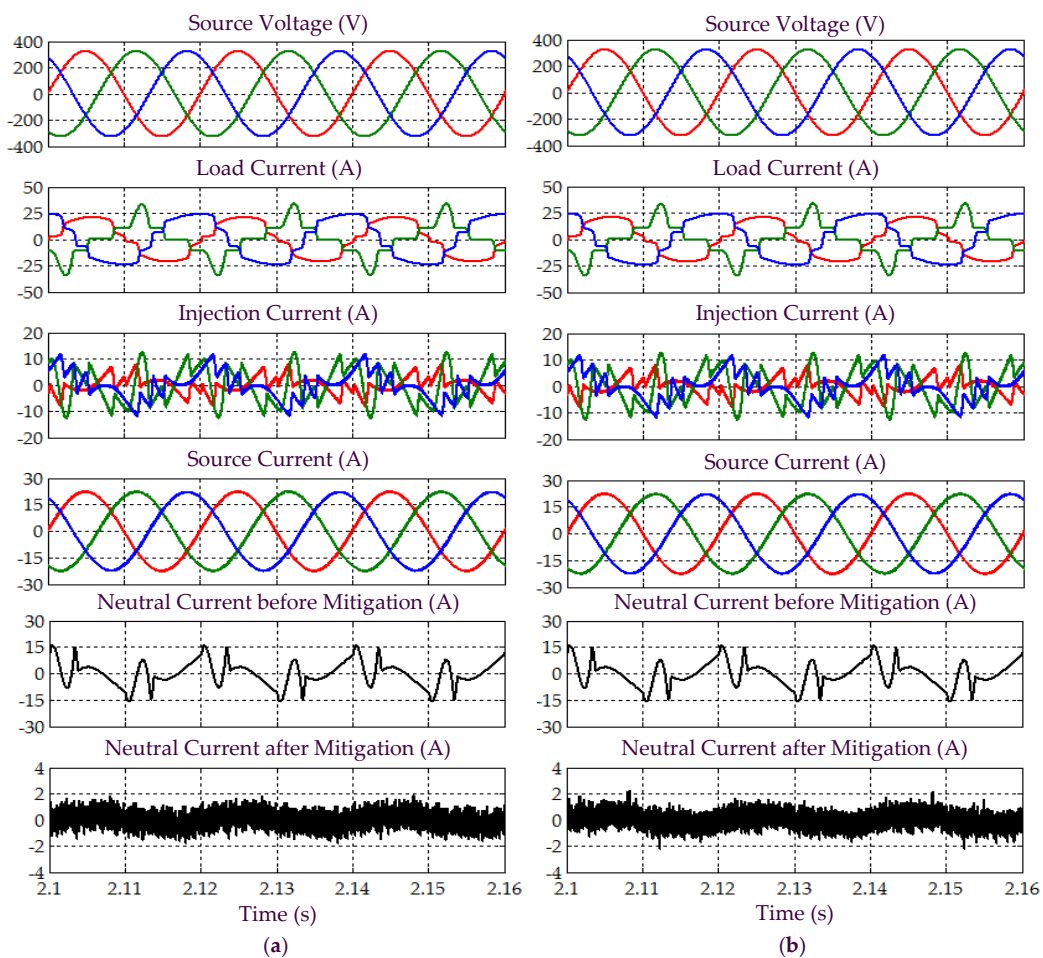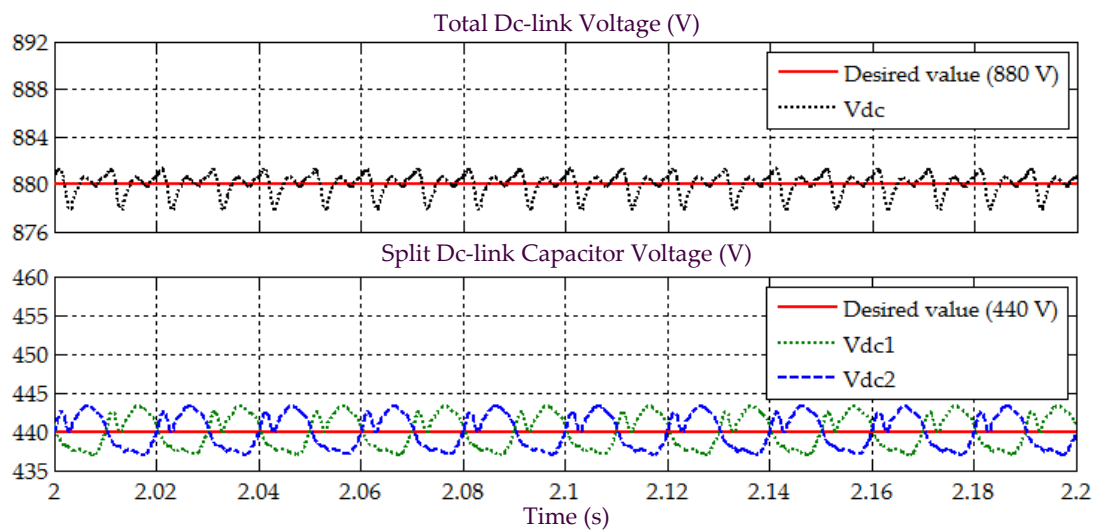
Figure 7. Simulation result obtained under Scenario A for Load 1, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-*dq*0 technique.

Figure 8. Simulation results obtained under Scenario A for Load 2, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-*dq*0 and (**b**) standard *dq*0 techniques.

Figure 9. Simulation result obtained under Scenario A for Load 2, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-dq0 technique.

5.2. Non-Sinusoidal-Balanced Source Voltage (Scenario B)

In Scenario B, a non-sinusoidal-balanced (harmonic distorted) source voltage is considered. All the simulation waveforms obtained under this scenario are shown in Figures 10–14. Meanwhile, Table 3 summarizes the findings in comparative manner. Referring to Figure 10, it can clearly be observed that the proposed STF-dq0 technique effectively detects synchronization phase value ωt (appear in the form of sawtooth wave-shape) from a non-sinusoidal-balanced source voltage, where the detected phase value is found to accurately match the desired phase value. In contrast, for the standard dq0 technique, discrepancies existed between the detected and desired phase value, where the resulted sawtooth waveform of the detected phase value is observed to be oscillating along the desired phase value. This implies that the standard dq0 technique cannot work as desired when the source voltage suffers from distortion.
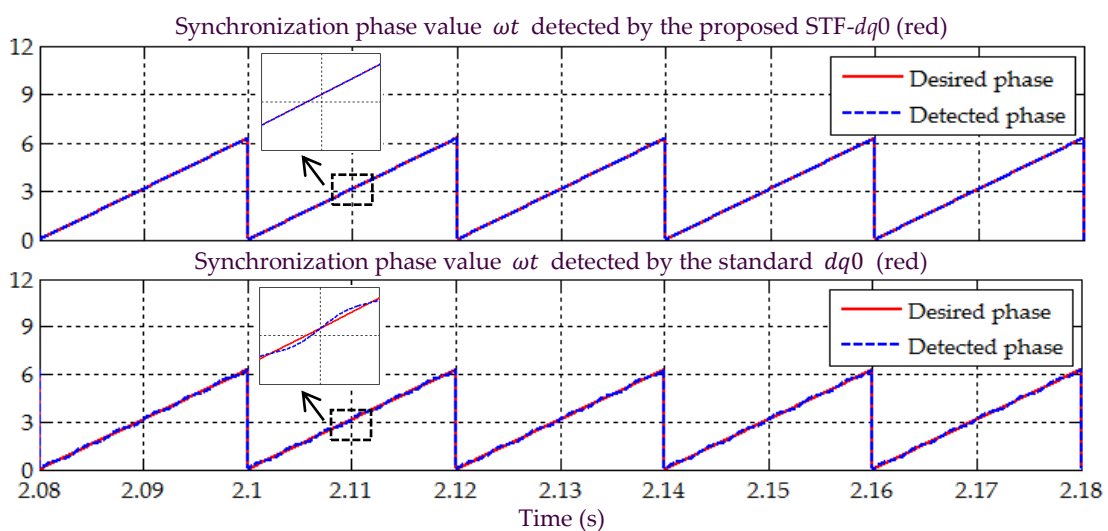

Figure 10. Simulation result showing the detected synchronization reference phase value ωt under Scenario B.

Table 3. Comparative analysis of the proposed STF-*dq*0 and the standard *dq*0 techniques under Scenario B.

Performance Parameter	Load 1			Load 2		
	Phase *a*	Phase *b*	Phase *c*	Phase *a*	Phase *b*	Phase *c*
Before connecting SAPF						
THD value (%)	123.98	35.29	120.11	15.63	46.21	20.71
Phase difference (°)	10.10	10.40	8.20	11.10	12.10	11.80
Power factor	0.618	0.927	0.633	0.969	0.887	0.958
After connecting SAPF with the proposed STF-*dq*0 technique						
THD value (%)	2.91	2.90	2.73	0.92	0.95	0.98
Phase difference (°)	0.80	0.20	0.30	0.10	0.20	0.20
Power factor	0.999	0.999	0.999	0.999	0.999	0.999
After connecting SAPF with the standard *dq*0 technique						
THD value (%)	8.56	8.08	7.41	6.75	6.92	7.33
Phase difference (°)	0.80	0.10	0.50	0.10	0.20	0.10
Power factor	0.996	0.997	0.997	0.997	0.997	0.997
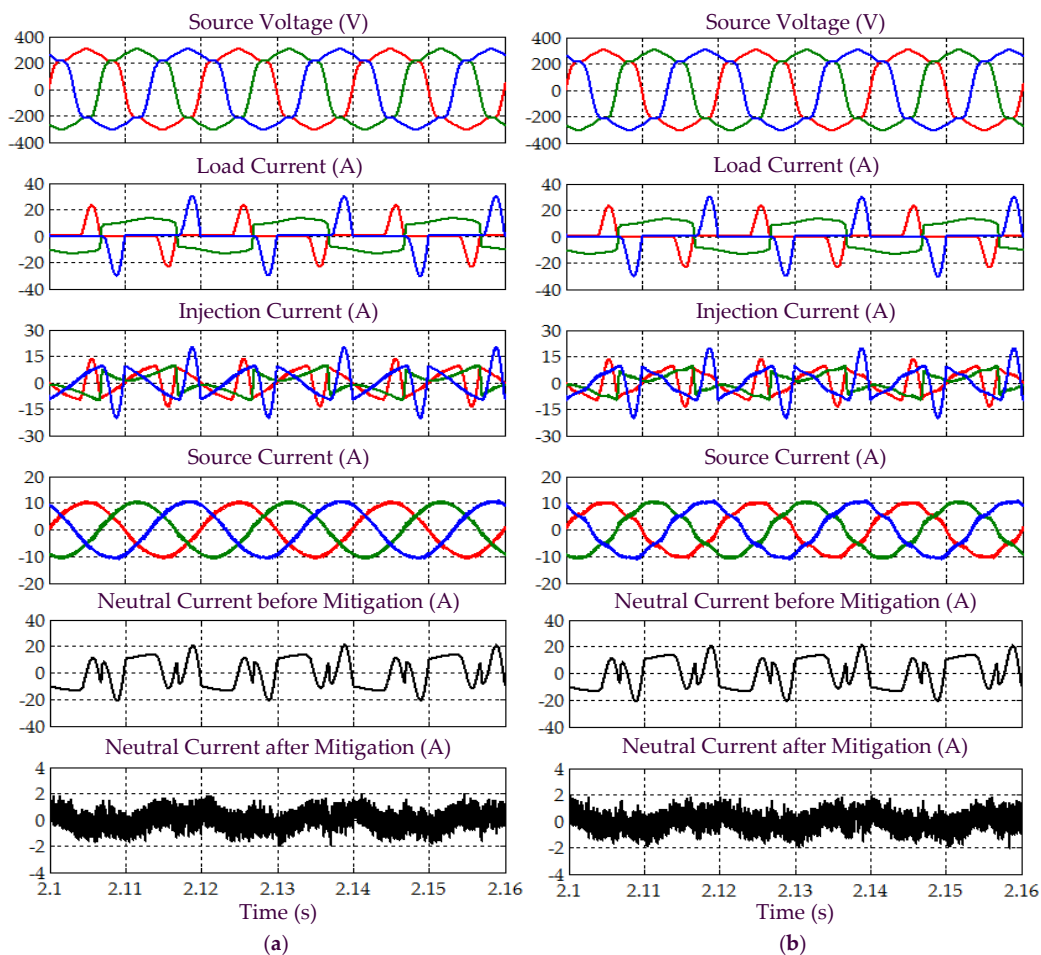
Figure 11. Simulation results obtained under Scenario B for Load 1, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-*dq*0 and (**b**) standard *dq*0 techniques.
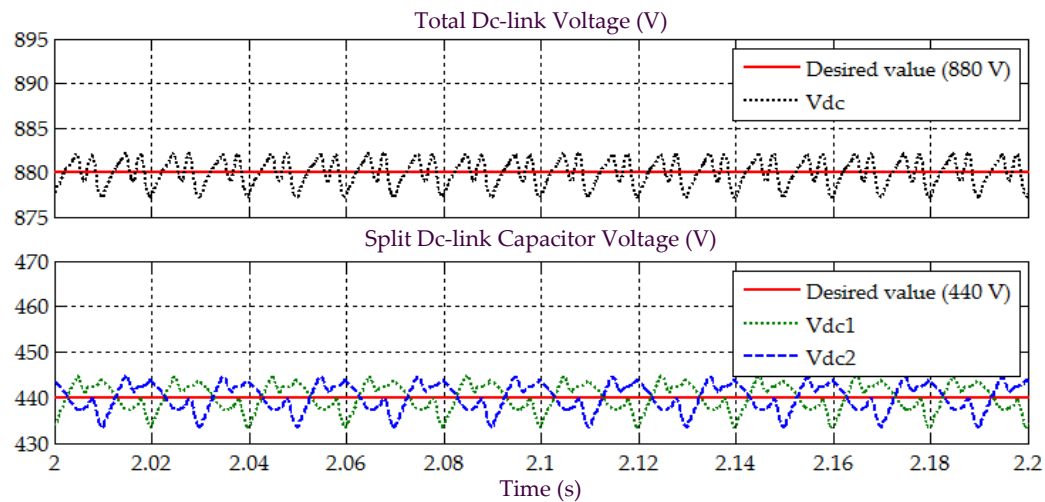
Figure 12. Simulation result obtained under Scenario B for Load 1, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-$dq0$ technique.
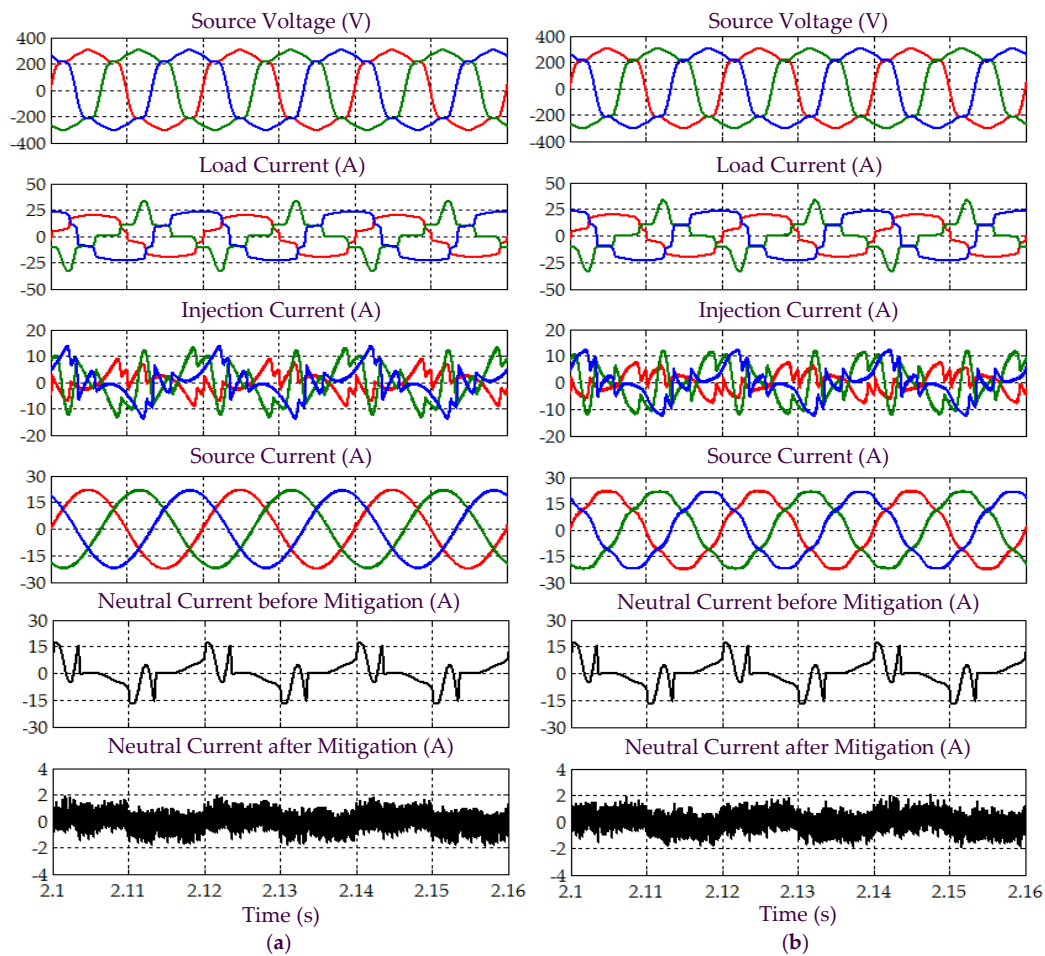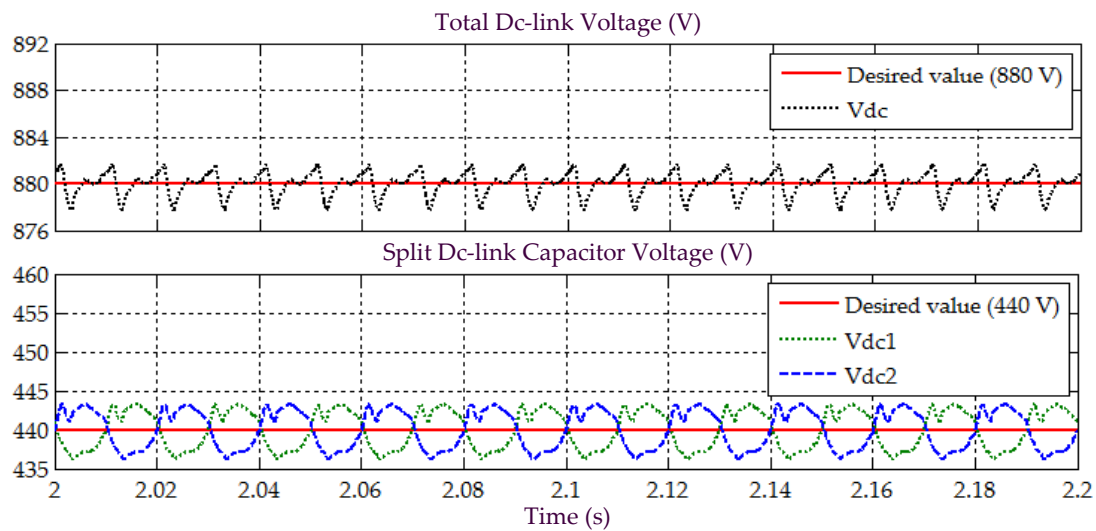

Figure 13. Simulation results obtained under Scenario B for Load 2, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-$dq0$ and (**b**) standard $dq0$ techniques.

Figure 14. Simulation result obtained under Scenario B for Load 2, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-*dq*0 technique.

Next, referring to Figure 11, it can be seen that while using the proposed STF-*dq*0 technique, SAPF is observed to have successfully mitigated harmonic currents generated by Load 1, where the source currents have regained sinusoidal shape with THD values (as tabulated in Table 3) complying with the 5% harmonic limit. In contrast, SAPF that applies the standard *dq*0 technique is only capable of reducing distortion level suffered by the source currents but it fails to provide mitigation performance that complies with IEEE standard 519. In this case, the mitigated source currents fail to recover the desired sinusoidal shape and the recorded THD values are far beyond 5%. Nevertheless, both techniques are able to remove excessive neutral currents caused by connection of single-phase loads.

Furthermore, as indicated in Table 3, both techniques are able to direct their respective SAPF in minimizing the large phase differences that resulted between the source current and voltage. With minimum phase differences, an almost unity power factor of 0.999 can be achieved when the proposed STF-*dq*0 technique is applied. In contrast, due to high-level of distortion retained in the mitigated source current, the standard *dq*0 technique can only provide a power factor up to 0.997 even though the phase differences have been minimized. Similar findings can be observed for Load 2, where the proposed STF-*dq*0 technique is revealed to outperform the standard *dq*0 technique when operating under non-sinusoidal-balanced source voltage scenario (as indicated in Figure 13 and Table 3).

Moreover, the assessment on behavior of dc-link voltage is also conducted to confirm correct operation of SAPF under Scenario B, while applying the proposed STF-*dq*0 technique. Figures 12 and 14 provide the related results recorded for Loads 1 and 2, respectively. As expected from the findings, all dc-link voltages of the SAPF are effectively regulated and maintained at the desired level, i.e., at 880 V for the overall dc-link voltage V_{dc} and at 440 V (half of overall dc-link voltage) for the voltages across two split dc-link capacitors (V_{dc1} and V_{dc2}). Hence, once again, it is certain that the proposed STF-*dq*0 technique can work effectively together with the two PI techniques applied respectively for regulating the dc-link voltage and ensuring voltage balance of the two split dc-link capacitors, and eventually directed the SAPF to work as desired under non-sinusoidal-balanced source voltage scenario.

5.3. Sinusoidal-Unbalanced Source Voltage (Scenario C)

In Scenario C, a sinusoidal-unbalanced (magnitude unbalanced) source voltage is considered. All the simulation waveforms obtained under this scenario are shown in Figures 15–19. Meanwhile,

Table 4 summarizes the findings in comparative manner. Based on Figure 15, the synchronization phase value ωt (appear in the form of sawtooth wave-shape) detected by the proposed STF-dq0 technique is found to work in accordance with the desired phase value. In contrast, for the standard dq0 technique, minor discrepancies can be observed between the detected and desired phase value. Hence, it implies that the standard dq0 technique cannot work exactly as desired when the magnitude of a three-phase source voltage is unbalanced across the three phases.

Subsequently, from Figure 16, it is obvious that by using the proposed STF-dq0 technique, SAPF have successfully mitigated harmonic currents generated by Load 1, where the source currents have regained sinusoidal shape with THD values (as tabulated in Table 4) complying with the 5% harmonic limit. In contrast, SAPF that applies the standard dq0 technique fails to perform in accordance to IEEE standard 519, where the recorded THD values are beyond 5% and the mitigated source currents fail to regain a complete sinusoidal shape. Nevertheless, both techniques are able to remove excessive neutral currents caused by connection of single-phase loads. Furthermore, as indicated in Table 4, both techniques are found to be able to direct their respective SAPF in minimizing the large phase differences that resulted between the source current and voltage. With minimum phase differences, an almost unity power factor of 0.999 can be achieved when the proposed STF-dq0 technique is applied. However, due to higher distortion level of the mitigated source current, the standard dq0 technique can only provide a power factor up to 0.998 even though the phase differences have been minimized.

On the other hand, for the case of Load 2 as illustrated in Figure 18, both the proposed STF-dq0 and the standard dq0 techniques are found to perform effectively as the THD values have been maintained below the 5% harmonic limit, excessive neutral current have been removed, the large phase differences have been minimized, and almost unity power factor of 0.999 is achieved. Nevertheless, the proposed STF-dq0 technique is revealed to outperform the standard dq0 technique by providing THD values of 1.88–2.13% lower (as indicated in Table 4). Hence, as an overall, judging from the performance of each technique in dealing with Loads 1 and 2, the proposed STF-dq0 technique can be claimed to be more reliable than the standard dq0 technique when they are required to work under sinusoidal-unbalanced source voltage scenario.
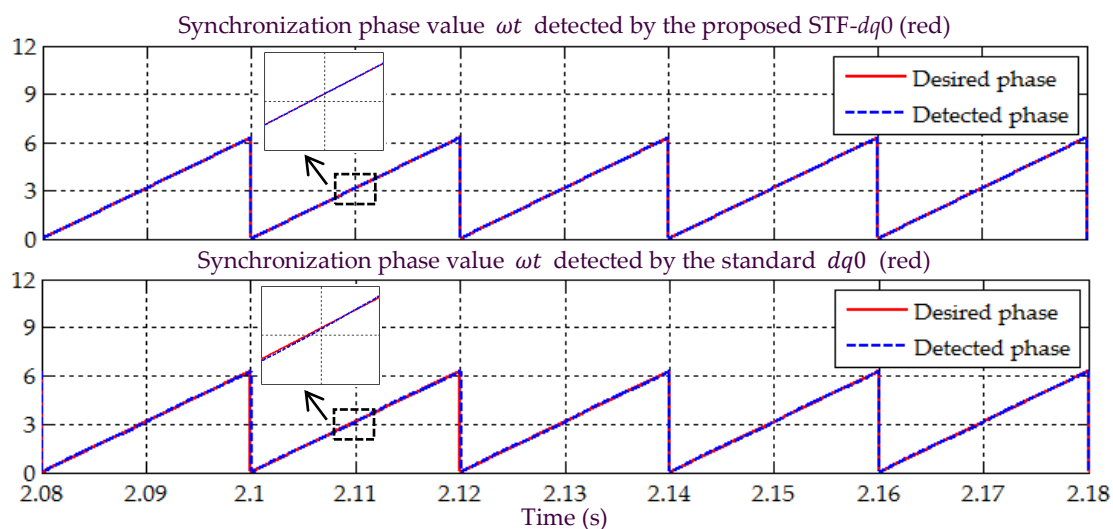

Figure 15. Simulation result showing the detected synchronization reference phase value ωt under Scenario C.

Table 4. Comparative analysis of the proposed STF-*dq*0 and the standard *dq*0 techniques under Scenario C.

Performance Parameter	Load 1			Load 2		
	Phase *a*	Phase *b*	Phase *c*	Phase *a*	Phase *b*	Phase *c*
Before connecting SAPF						
THD value (%)	118.27	25.99	114.73	12.84	45.09	13.77
Phase difference (°)	9.80	15.60	7.50	9.90	7.40	9.40
Power factor	0.636	0.932	0.651	0.977	0.904	0.977
After connecting SAPF with the proposed STF-*dq*0 technique						
THD value (%)	2.86	2.79	2.89	1.11	1.09	1.17
Phase difference (°)	0.30	0.20	0.50	0.30	0.40	0.20
Power factor	0.999	0.999	0.999	0.999	0.999	0.999
After connecting SAPF with the standard *dq*0 technique						
THD value (%)	5.20	5.09	5.72	3.24	2.97	3.13
Phase difference (°)	0.30	0.10	0.30	0.90	0.10	0.90
Power factor	0.998	0.998	0.998	0.999	0.999	0.999
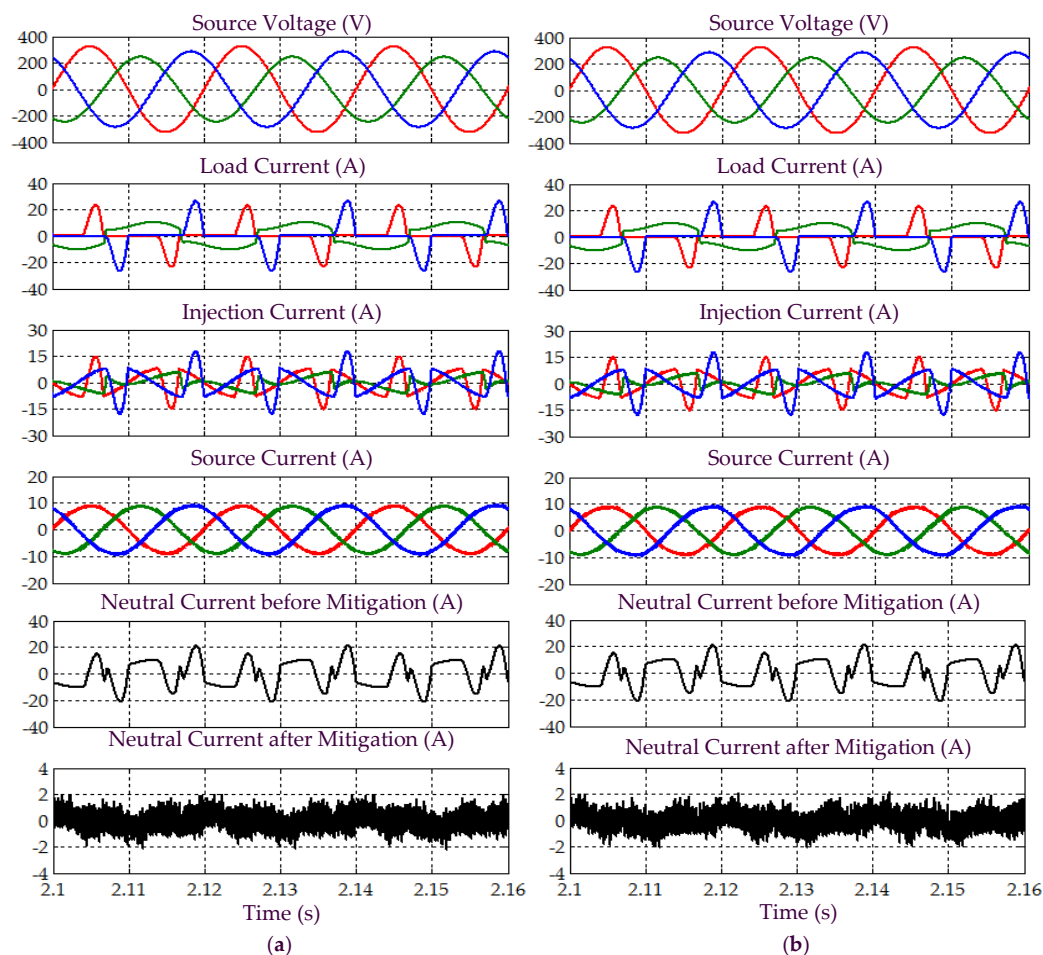
Figure 16. Simulation results obtained under Scenario C for Load 1, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-*dq*0 and (**b**) standard *dq*0 techniques.
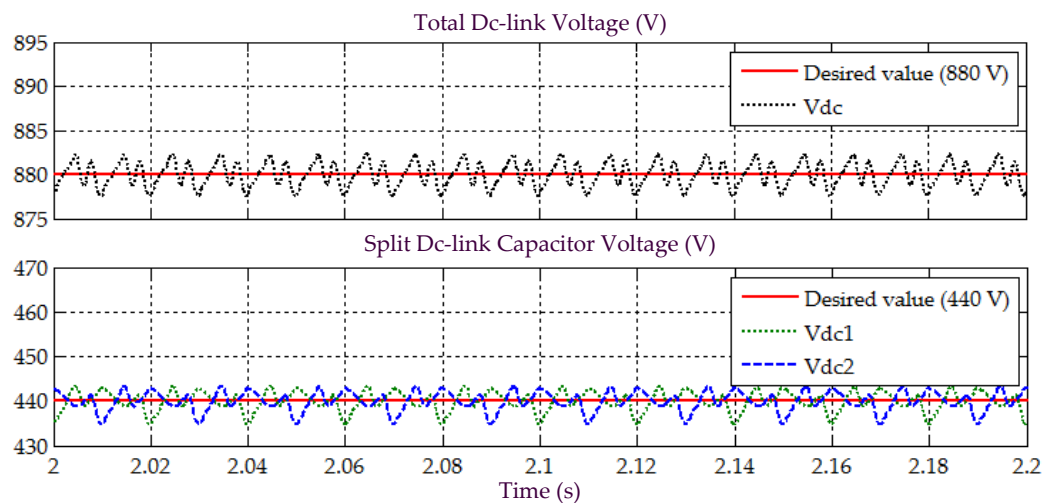
Figure 17. Simulation result obtained under Scenario C for Load 1, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-dq0 technique.
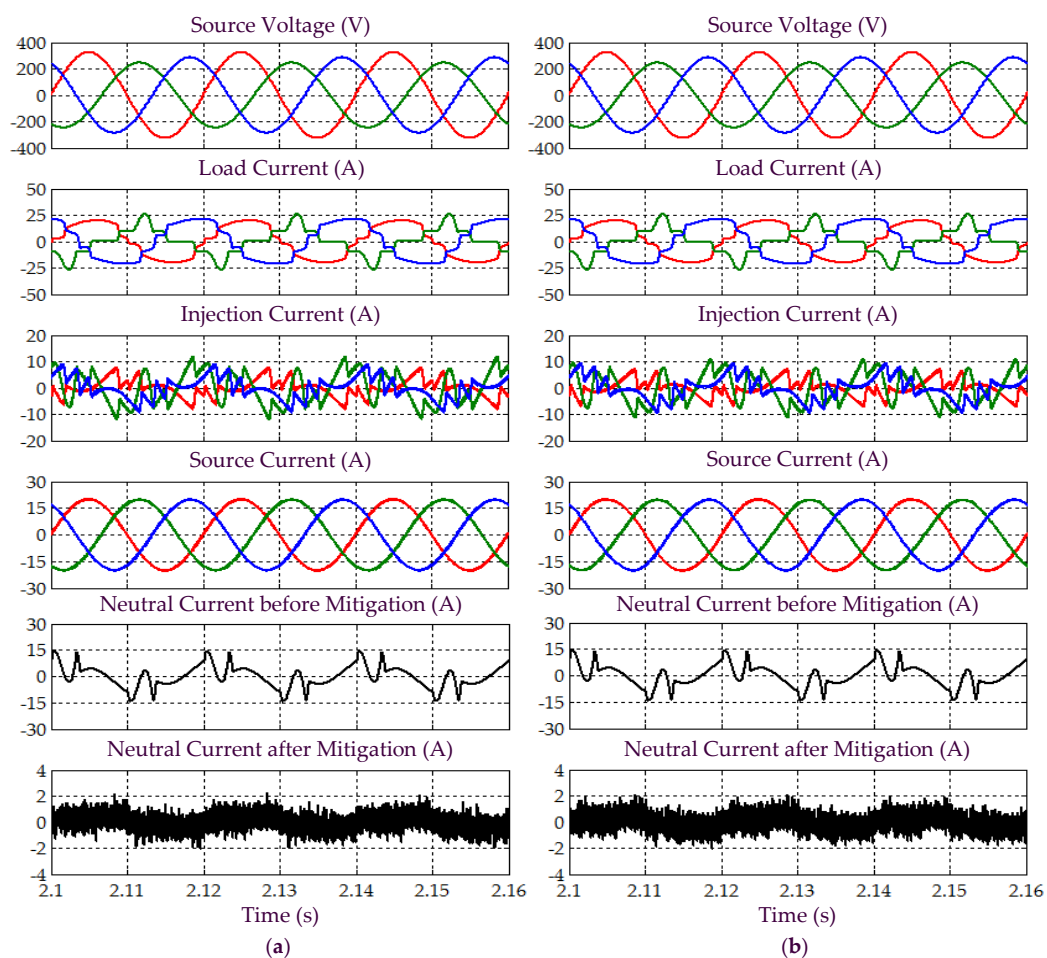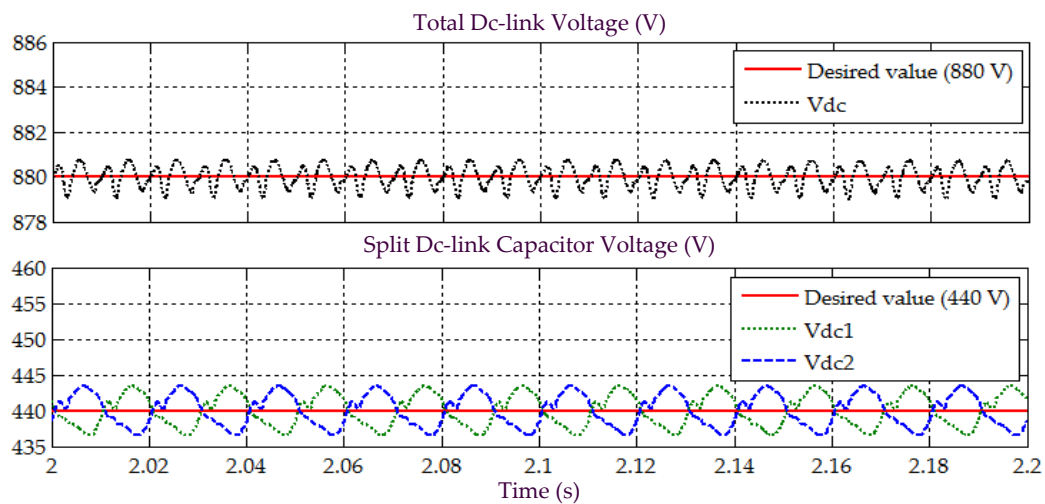

(**a**)   (**b**)

Figure 18. Simulation results obtained under Scenario C for Load 2, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-dq0 and (**b**) standard dq0 techniques.

Figure 19. Simulation result obtained under Scenario C for Load 2, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-*dq*0 technique.

Moreover, assessment on behavior of dc-link voltage is also conducted to further justify that the SAPF is working correctly under Scenario C, while applying the proposed STF-*dq*0 technique. Figures 17 and 19 provide the related results obtained for Loads 1 and 2, respectively. As expected, all dc-link voltages of the SAPF are effectively regulated and maintained at the desired level, i.e., overall dc-link voltage V_{dc} at 880 V and voltages across the two split dc-link capacitors (V_{dc1} and V_{dc2}) at 440 V (half of overall dc-link voltage). Hence, once again, it is certain that the SAPF can work appropriately under sinusoidal-unbalanced source voltage scenario while applying the proposed STF-*dq*0 technique.

5.4. Non-Sinusoidal-Unbalanced Source Voltage (Scenario D)

In Scenario D, a non-sinusoidal-unbalanced (harmonic distorted and magnitude unbalanced) source voltage is considered. All the simulation waveforms obtained under this scenario are shown in Figures 20–24. Meanwhile, Table 5 summarizes the findings in comparative manner. As shown in Figure 20, the synchronization phase value ωt (appear in the form of sawtooth wave-shape) detected by the proposed STF-*dq*0 technique is in line with the desired phase value. In contrast, for the standard *dq*0 technique, the detected phase value seems to be oscillating along the desired phase value. Hence, once again the findings show that the proposed STF-*dq*0 technique can accurately track the desired phase value when the source voltage is distorted and unbalanced, while the standard *dq*0 technique has failed to do so.

Next, from Figures 21 and 23, it is clear that by using the proposed STF-*dq*0 technique, the SAPF have successfully mitigated harmonic currents generated by Loads 1 and 2, where the mitigated source currents for both cases have regained sinusoidal shape with THD values (as tabulated in Table 5) complying with the 5% harmonic limit. However, SAPF that applies the standard *dq*0 technique fails to comply with IEEE standard 519 in both cases, where the recorded THD values are beyond 5% and the mitigated source currents fail to recover the desired sinusoidal shape. Nevertheless, both techniques are able to remove excessive neutral currents caused by connection of single-phase loads.

In addition, as indicated in Table 5, both techniques have effectively minimized the large phase differences between the source current and voltage caused by connection of Loads 1 and 2. With minimum phase differences, almost unity power factor of 0.999 can be achieved when the proposed STF-*dq*0 technique is applied. However, due to higher distortion level of the mitigated source current, the standard *dq*0 technique can only provide a power factor up to 0.998 even though the phase differences have been minimized.
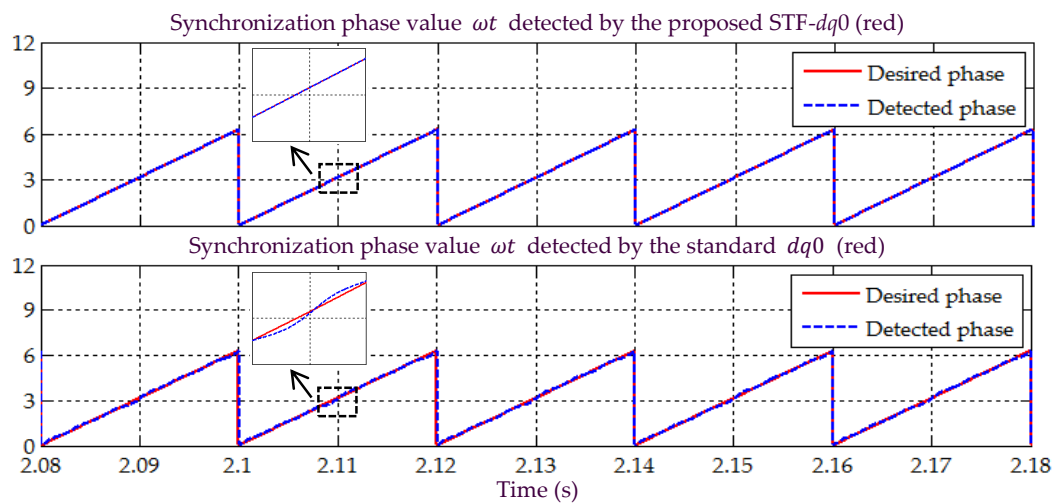
Figure 20. Simulation result showing the detected synchronization reference phase value ωt under Scenario D.
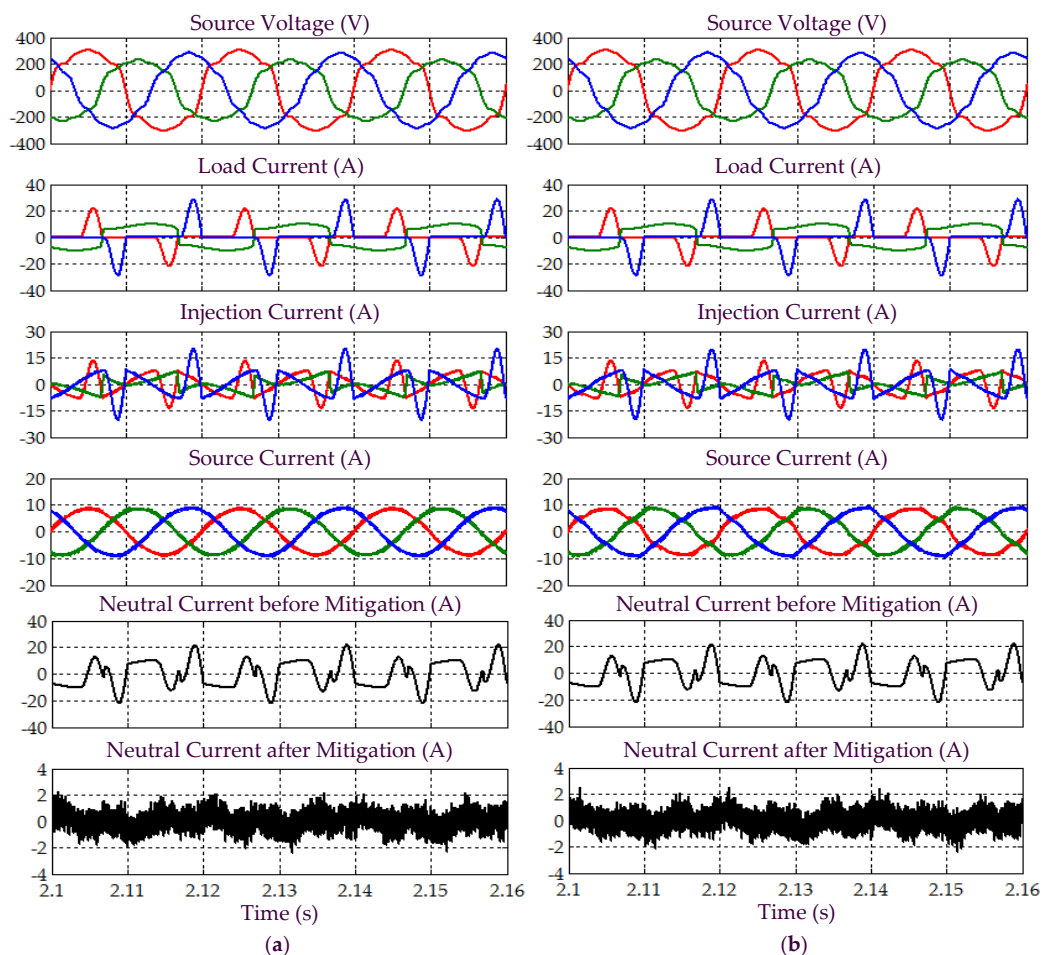

Figure 21. Simulation results obtained under Scenario D for Load 1, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-*dq*0 and (**b**) standard *dq*0 techniques.
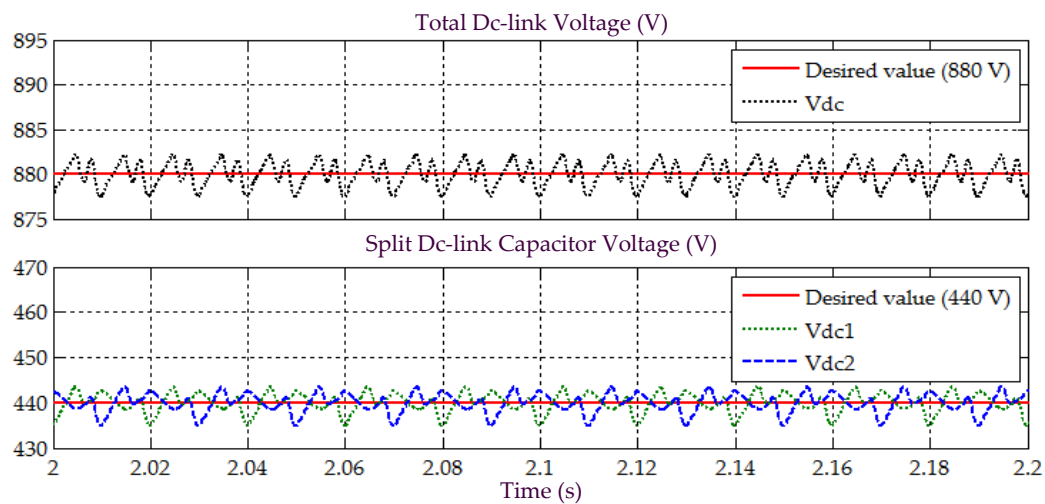
Figure 22. Simulation result obtained under Scenario D for Load 1, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-$dq0$ technique.
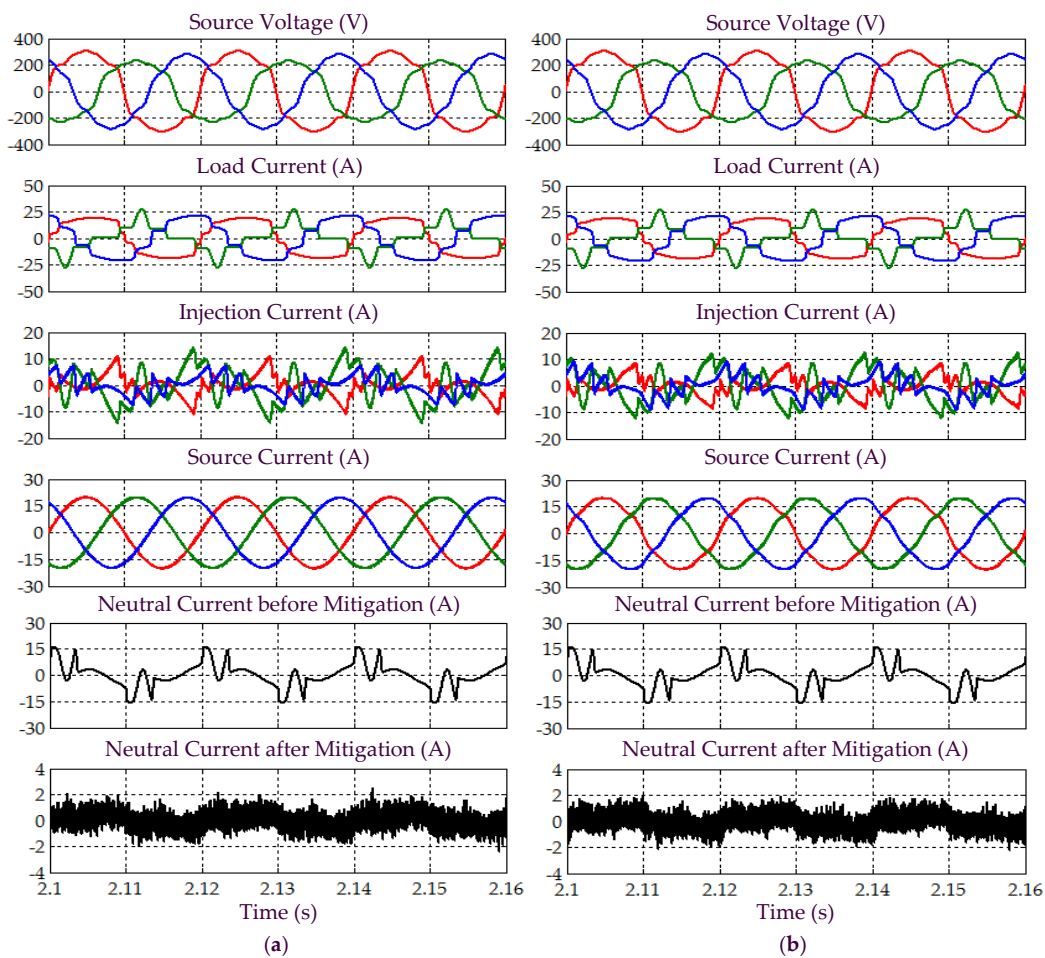

Figure 23. Simulation results obtained under Scenario D for Load 2, which include three-phase source voltage v_{Sabc}, load current i_{Labc}, injection current i_{injabc}, source current i_{Sabc}, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) proposed STF-$dq0$ and (**b**) standard $dq0$ techniques.
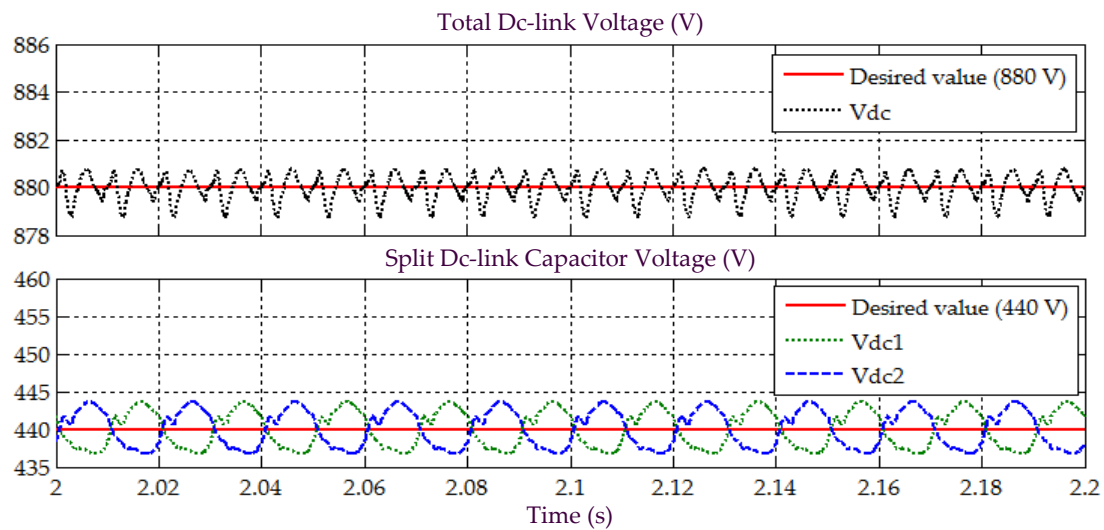
Figure 24. Simulation result obtained under Scenario D for Load 2, showing the total dc-link voltage V_{dc}, and voltages across split dc-link capacitors V_{dc1} and V_{dc2}, demonstrated by SAPF while applying the proposed STF-dq0 technique.

Table 5. Comparative analysis of the proposed STF-dq0 and the standard dq0 techniques under Scenario D.

Performance Parameter	Load 1			Load 2		
	Phase *a*	Phase *b*	Phase *c*	Phase *a*	Phase *b*	Phase *c*
	Before connecting SAPF					
THD value (%)	116.53	33.38	121.45	19.78	49.10	13.89
Phase difference (°)	10.40	11.40	8.40	8.70	11.90	8.20
Power factor	0.640	0.929	0.628	0.969	0.878	0.980
	After connecting SAPF with the proposed STF-dq0 technique					
THD value (%)	2.97	2.60	2.91	1.09	1.07	1.12
Phase difference (°)	0.40	0.10	0.50	0.20	0.50	0.20
Power factor	0.999	0.999	0.999	0.999	0.999	0.999
	After connecting SAPF with the standard dq0 technique					
THD value (%)	8.64	5.87	5.74	6.85	5.14	5.04
Phase difference (°)	0.20	0.50	0.70	0.40	0.40	1.30
Power factor	0.996	0.998	0.998	0.997	0.998	0.998

Furthermore, assessment on behaviour of dc-link voltage is also conducted to justify that the SAPF is working correctly under Scenario D, while applying the proposed STF-dq0 technique. Figures 22 and 24 provide the related results obtained for Loads 1 and 2, respectively. From the results obtained, all dc-link voltages of the SAPF are revealed to have effectively been regulated and maintained at the desired level, i.e., overall dc-link voltage V_{dc} at 880 V and voltages across the two split dc-link capacitors (V_{dc1} and V_{dc2}) at 440 V (half of overall dc-link voltage). Hence, once again, it is certain that the SAPF can work appropriately under non-sinusoidal-unbalanced source voltage scenario while applying the proposed STF-dq0 technique.

Overall, based on all the findings obtained in Scenarios A to D, design concept and functionality of the proposed STF-dq0 technique can be confirmed to be correct. By applying the proposed STF-dq0 technique, the SAPF is revealed to perform effectively in dealing with both unbalanced nonlinear loads and all the scenarios of source voltages which have been considered in this work. The highly distorted source currents have regained the desired sinusoidal shape with low THD values ranging from 0.92%

to 2.97%, complying with IEEE standard 519. Next, excessive neutral currents have been reduced to a level that the mitigated source currents are balanced. In addition, large phase differences have been reduced to the range of 0.00–0.80°, thereby achieving power factor of 0.999 which is almost unity. Furthermore, all dc-link capacitor voltages have been regulated as desired and are balanced, thus ensuring that the SAPF is able to mitigate harmonics appropriately. More importantly, the proposed STF-*dq*0 technique outperforms and is more reliable than the standard *dq*0 technique when dealing with distorted and unbalanced source voltages.

6. Conclusions

In this paper, a control technique that generates reference current to manage operation of a three-phase four-wire SAPF has successfully been demonstrated. The proposed technique is named as the STF-*dq*0 technique, as it is developed by integrating together the strengths of STF and working concept of the *dq*0 principle, without relying on any PLL element. Comprehensive tests and analyses involving two types of unbalanced nonlinear rectifier loads and four distinct scenarios of source voltages are conducted to evaluate performance of the proposed STF-*dq*0 technique in comparison to the standard *dq*0 technique. Based on the exhaustive simulation results presented, the proposed technique is revealed to perform effectively regardless of specifications of nonlinear loads and scenarios of source voltages. More importantly, the proposed STF-*dq*0 technique is demonstrated to be superior and more reliable than the standard *dq*0 technique especially when dealing with distorted and unbalanced source voltages. Low THD values complying with IEEE standard 519, synchronized operation of SAPF, minimized neutral current and power factor reaching almost unity, are the benefits granted by the proposed technique when it is applied in three-phase four-wire system.

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