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# The Parallel Virtual Infinite Capacitor Applied to DC-Link Voltage Filtering for Wind Turbines

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**Abstract:** We propose the parallel virtual infinite capacitor (PVIC) concept, which refers to two virtual infinite capacitors (VIC) connected to the same DC link and sharing one capacitor, one tuned to low frequencies (LF) and one tuned to high frequencies (HF). A PVIC can suppress voltage variations (ripple) in a wider frequency range than a usual VIC. The LF-VIC is controlled by a sliding mode controller to regulate the low-frequency component of the voltage to its reference value, and by a proportional-integral (PI) controller to maintain its state of charge within the desired operating range and achieve the 'plug-and-play' pattern of PVIC. The HF-VIC is controlled by another sliding mode controller to limit the high-frequency ripples and also to keep its state of charge within a reasonable operating interval. As our main application, we use the PVIC to replace a DC-link capacitor for voltage filtering on the DC link of a doubly fed induction generator (DFIG), which is driven by a WindPact (WP) 1.5-MW wind turbine under different grid conditions with turbulent wind input. The simulation study indicates that the PVIC provides much better voltage stabilisation than a DC-link capacitor with the same capacitance, especially in the low frequency range.

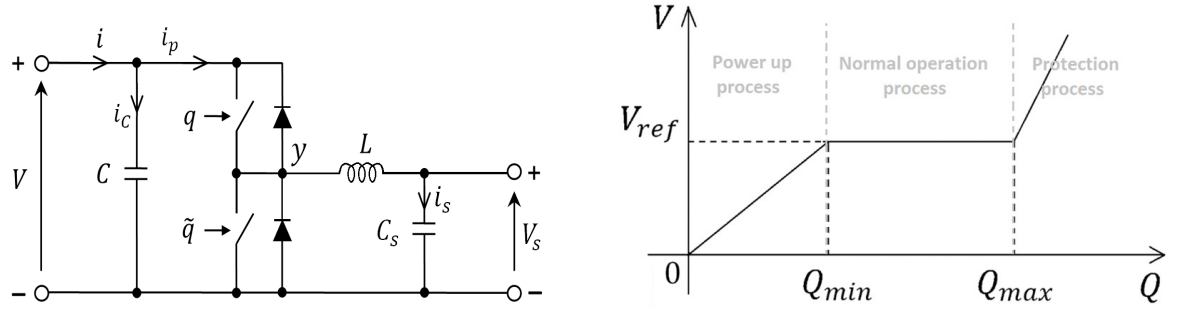
**Keywords:** capacitors; power filters; wind power generation; sliding mode control

## 1. Introduction

Capacitors are commonly used for DC voltage smoothing (ripple elimination) in power electronic circuits, such as in photovoltaic systems, fuel cells, LED drivers, electric (or hybrid) vehicles and their chargers, power factor correctors (PFC), the power train of wind power generators, etc. Low-frequency ripple suppression requires large capacitance, which could be provided by electrolytic or super-capacitors. However, such capacitors suffer from low reliability and low operating voltages [1–3]. Many ideas have been proposed as alternatives to large capacitors (or to achieve better performance with the same capacitance), and such circuits are known as "power filters", "active capacitors" or "ripple eliminators" (see, for instance, [4,5] (for the output voltage variations of controlled rectifiers) Refs. [6,7] (using stacked swithed capacitors for LED drivers), Refs. [8–11] and there are many more). We refer to [10,12] for nice surveys of this area. In this line of research, the *virtual infinite capacitor (VIC)* concept has been introduced in [13], which is a circuit able to eliminate random low-frequency voltage fluctuations [13–15]. The idea is to create a nonlinear capacitor where the plot of voltage as a function of charge has a flat segment, where the dynamic capacitance is infinity (see Figure 1b).

The VIC circuit contains a bidirectional DC–DC converter which (using the terminology from Kassakian et al. [16]) is a canonical switching cell (see Figure 1a for a simplified circuit not showing sensing, control or drivers). In [17], the control algorithm and operation of the VIC have been redesigned to work in discontinuous conduction mode (DCM), which has enabled substantially

reducing the switching frequency (and using snubber circuits to reduce the switching losses). As can be seen in Figure 1b, there are three regions of operation for the VIC. The control algorithms are designed individually for these three regions. The most important is the *normal operating range* (the middle segment in Figure 1b) where the voltage $V$ across the VIC remains at a reference value $V_{ref}$, while the charge $Q$ can vary in the interval $[Q_{min}, Q_{max}]$. In this range, the gate control signals $q$ and $\tilde{q}$ are controlled in such a way as to transfer the excess charge that would create voltage ripples in $V$ to the capacitor $C_s$ and thus constrain the voltage $V$ to a small neighbourhood of $V_{ref}$. This VIC configuration was found to be quite effective in suppressing unpredictable voltage fluctuations, through both simulations [17,18] and experiments [15,19].




(**a**) Simplied VIC circuit, the terminals of the VIC are on the left of the figure.

(**b**) Charge–voltage characteristics of VIC, comprising the power up, normal operation, and protection regions. $Q$ represents the charge stored in the VIC, the integral of $i$ from subfigure (**a**).

**Figure 1.** Simplified VIC circuit and its charge–voltage characteristics.

When we compute the output impedance of a VIC (as is done, for instance, in [15]), we find that it is high for frequencies near zero (as it should), it has a region where it is very low (as desired), but it grows for higher frequencies. The region of low impedance depends on the control algorithm. There are applications where there are two main sources of ripple, in two distinct frequency ranges. For instance, in the power conversion system of a wind turbine, the DC-link voltage ripple can originate from variations of wind speed (low frequency), grid imbalance (twice the grid frequency) and switching ripple from the main converters (relatively high frequency). To deal with such situations, we introduce here the *parallel virtual infinite capacitor* (PVIC) concept. The PVIC is composed of two VICs, one for low-frequency (LF) and one for high frequency (HF), which share a common capacitor. We also propose a new soft switching topology (see Figure 2) to be used for both the LF-VIC and the HF-VIC, which of course improves the efficiency compared with earlier designs. The operation of this new circuit will be explained in Section 2. For the LF-VIC, we design a sliding mode controller (SMC) to regulate the DC-link voltage in the frequency range of this VIC. A proportional-integral (PI) controller is used to maintain the charge in this VIC in its normal operating range and realise the 'plug-and-play' feature of the PVIC. Another sliding mode controller is designed for the HF-VIC to suppress the high-frequency component of the ripple voltage and at the same time to keep the state of charge (SoC) of this VIC within the normal operating range. Note that sliding mode controllers are robust and appropriate for nonlinear variable structure systems [20–23] such as power converters [24–28].

The PVIC can be applied to many systems where voltage filtering in a wide frequency range is required. In this paper, a wind power generator is chosen to demonstrate the performance of the PVIC. Wind power will continue to be an important source of electric power. At the end of 2017, the cumulative installed wind turbine capacity was over 539 GW, which can cover over 5% of the electric power demand of the world. Wind power capacity is expected to rise to 840 GW in 2020 [29,30]. Doubly fed induction generators (DFIG) have been widely used for wind turbines with power ratings of 1.5-MW and above since 1996 [31]. In this paper, the PVIC is used for DC-link voltage filtering on the DC link of a 1.5-MW DFIG wind turbine system.

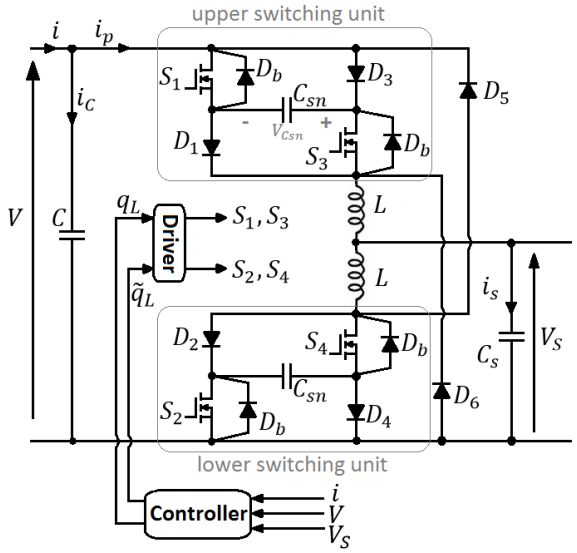



**Figure 2.** The proposed new VIC circuit, $D_b$, denotes a body diode of a MOSFET switch.

A DFIG wind turbine is quite vulnerable to grid faults because the DFIG stator is directly connected to the grid. Grid faults may cause voltage variations at the DFIG terminals, which may lead to high currents causing the DC-link voltage to drop, preventing the converters from working, or to rise too high, which may damage the capacitors and IGBTs [32,33]. During grid faults, the DC-link voltage should be maintained at the normal level to enable the converters to apply the voltage ride through an algorithm, especially to guarantee the control performance of the rotor side converter. Even without grid faults, DC-link voltage fluctuations need to be limited to guarantee accurate power regulation [33]. PVIC serves as a solution to maintain the DC-link voltage within reasonable bounds, regardless of the grid conditions. Different electronic circuits used for active ripple suppression on the DC link of wind turbine have been proposed (see [34,35] and the references therein). Figure 3 shows the configuration of a DFIG driven by a 1.5-MW wind turbine connected to the power grid via back-to-back converters and transformers. Typically, the rotor side converter is controlled to maximize wind power extraction, and the grid side converter is controlled to stabilise the DC-link voltage.

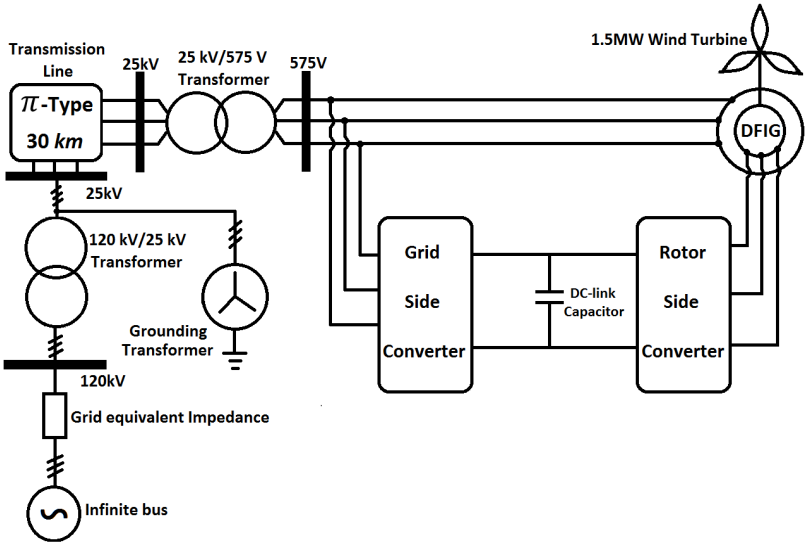



**Figure 3.** Configuration of the grid-connected doubly fed induction generator (DFIG) wind turbine system.

In this paper, we use a grid-connected DFIG model [36,37], driven by the popular WindPact (WP) 1.5-MW wind turbine [38–40] under turbulent wind generated by NREL Turbsim [41]. We have replaced the DC-link capacitor seen in Figure 3 with a PVIC with the same total capacitance and we compare the performance of the DC-link capacitor with that of the PVIC in stabilizing the DC-link voltage. The comparisons under different grid faults demonstrate the capability of the PVIC in handling unpredictable voltage fluctuations. In order to introduce disturbances to the DC link, we have simulated faults at the infinite bus. The simulations indicate that the PVIC is more effective in suppressing the voltage fluctuations than the equivalent DC-link capacitor (i.e., a DC-link capacitor with the same capacitance), regardless if there are grid disturbances or not.

The structure of the paper is as follows. In Section 2, we briefly explain the operation principle and control of the VIC and especially of the soft switching version from Figure 2. In Section 3, we present our simulation results for the the DC-link voltage filtering performance of the PVIC. We compare the performance of the PVIC with that of the equivalent (in capacitance) DC-link capacitor.

## 2. The PVIC and Its Control

To improve efficiency, we use a new soft switching circuit shown in Figure 2, where the two snubber capacitors $C_{sn}$ are small. This is an improvement of the circuit appearing in ([42], Figure 2). The upper switching unit is composed of the $S_1$, $S_3$, $C_{sn}$, $D_1$ and $D_3$, in which $S_1$ is synchronized with $S_3$. The lower switching unit is similar. The inductors are not coupled.

We take the upper switching unit (see Figure 2) as an example to explain the soft switching mechanism. This is really soft switching only in discontinuous conduction mode (DCM), while in continuous conduction mode (CCM) it is only zero voltage switching-off. Immediately after $S_1$ and $S_3$ are turned off, the voltage on the left side of $C_{sn}$ will remain close to $V$ without dropping abruptly because $C_{sn}$ takes time to get charged via $D_1$ and $D_3$ until $V_{C_{sn}}$ reaches $V$, which implies zero voltage switching-off of $S_1$ and $S_3$. The main current will flow via $D_6$, decreasing at a slope of $-V_s/L$, until one of the following two events occurs: either the current reaches zero and then remains zero for some time (DCM) or the switches are controlled to turn on again. Immediately after $S_1$ and $S_3$ are turned on, the voltage on the right side of $C_{sn}$ will suddenly jump to $V + V_{C_{sn}} \approx 2V$. Then, $C_{sn}$ starts to release energy through the switches and the upper inductor $L$ to charge $C_s$, until $V_{C_{sn}}$ reaches nearly zero or the switches are controlled to turn off. This discharging period of $C_{sn}$ is relatively short because the time constant $\sqrt{LC_{sn}}$ is small. Hence, practically all the energy that was stored in $C_{sn}$ is saved into $C_s$. However, if the inductor current at the moment of switching-on is not zero, then we do not have zero current switch-on. After switch-on and after $C_{sn}$ is emptied, the inductor current (flowing through the switches and the diodes D1 and D3) grows, at a slope of $(V - V_s)/L$. Of course, the rising current will stop once the switches are turned off, which closes the whole cycle. The story for the lower switching unit is similar.

Figure 4 shows the circuit realisation of a PVIC, which replaces the DC-link capacitor. $q_L$, $\tilde{q}_L \in \{0, 1\}$ are binary signals, and $\tilde{q}_L = 1 - q_L$. The switches $S_{1_L}$ and $S_{3_L}$ are on if $q_L = 1$. The switches $S_{2_L}$ and $S_{4_L}$ are on if $\tilde{q}_L = 1$. The binary signals $q_H$ and $\tilde{q}_H$ are defined in a similar way. The capacitor $C_{s_H}$ is smaller than the capacitor $C_{s_L}$. The remaining components in the HF-VIC are same as in the LF-VIC. The control of PVIC is attained by the LF-VIC controller and HF-VIC controller. The former regulates low-frequency components of the voltage $V$ to the neighbourhood of its reference, while the latter suppresses the high-frequency ripples of the voltage $V$. During the power up process (see the left segment in Figure 1b), a constant duty cycle $D_{pow\_up}$ and a constant PWM switching frequency $f_{pow\_up}$ are applied to both VICs. During the protection region of operation (the right segment in Figure 1b), all the switches are turned off to avoid the overcharge of $C_{s_L}$ and $C_{s_H}$. The transitions between the three processes are controlled using a state machine, which was detailed in [19]. Next, we discuss the control algorithm in the normal operation range.

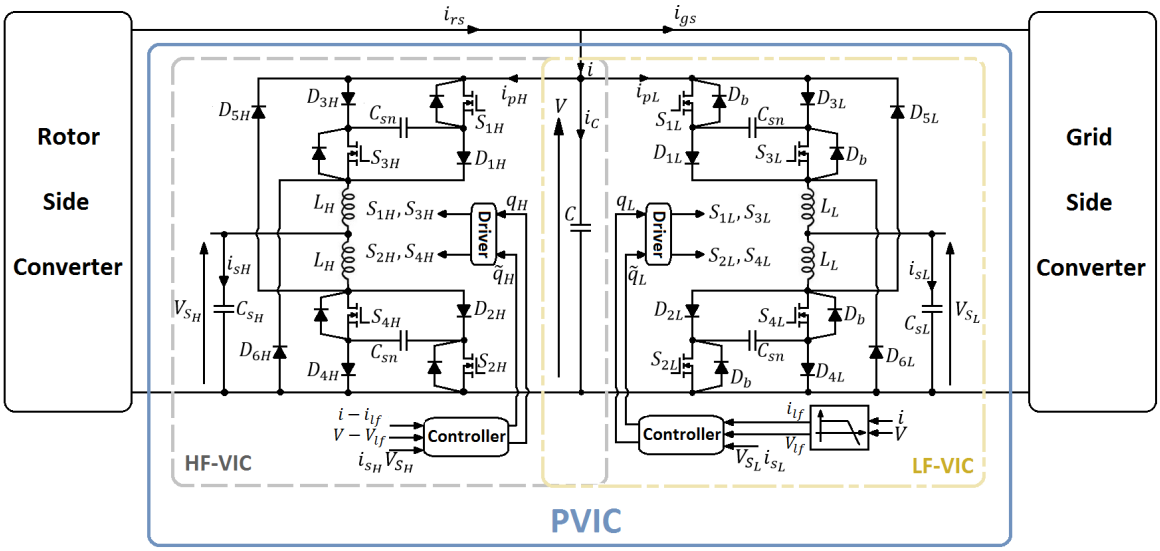



**Figure 4.** The PVIC in place of a DC-link capacitor.

The low-frequency signals $V_{lf}$ & $i_{lf}$ and high-frequency signals $V_{hf}$ and $i_{hf}$ are acquired by passing $V$ and $i$ through a low pass filter with the corner frequency $f_l$:

$$\begin{aligned} V_{lf} &= \frac{2\pi f_l}{s+2\pi f_l} V, \qquad V_{hf} = V - V_{lf}, \\ i_{lf} &= \frac{2\pi f_l}{s+2\pi f_l} i, \qquad i_{hf} = i - i_{lf}. \end{aligned} \tag{1}$$

According to Figure 4, we have

$$i_C = C\dot{V} = i - q_L i_{s_L} - q_H i_{s_H}. \tag{2}$$

Considering (1), we can rewrite (2) as

$$C\left(\dot{V}_{lf} + \dot{V}_{hf}\right) = i_{lf} + i_{hf} - q_L\left(i_{s_{L_L}} + i_{s_{L_H}}\right) - q_H\left(i_{s_{H_L}} + i_{s_{H_H}}\right), \tag{3}$$

where $i_{s_{L_L}}$, $i_{s_{L_H}}$, $i_{s_{H_L}}$, and $i_{s_{H_H}}$ are defined by

$$\begin{aligned} i_{s_{L_L}} &= \frac{2\pi f_l}{s+2\pi f_l} i_{s_L}, \qquad i_{s_{L_H}} = i_{s_L} - i_{s_{L_L}}, \\ i_{s_{H_L}} &= \frac{2\pi f_l}{s+2\pi f_l} i_{s_H}, \qquad i_{s_{H_H}} = i_{s_H} - i_{s_{H_L}}. \end{aligned} \tag{4}$$

Multiplying both sides of (2) with $\frac{2\pi f_l}{s+2\pi f_l}$, we get

$$C\dot{V}_{lf} = i_{lf} - q_L i_{s_{L_L}} - q_H i_{s_{H_L}}. \tag{5}$$

Subtracting (5) from (2), we get

$$C\dot{V}_{hf} = i_{hf} - q_H i_{s_{H_H}} - q_L i_{s_{L_H}}.$$

Then, the state equations of the PVIC can be written as:

$$\begin{cases} C\dot{V}_{lf} = i_{lf} - q_L i_{s_{L_L}} - q_H i_{s_{H_L}}, \\ C\dot{V}_{hf} = i_{hf} - q_H i_{s_{H_H}} - q_L i_{s_{L_H}}, \\ L_L \dot{i}_{s_L} = q_L(V_{lf} + V_{hf}) - V_{s_L}, \\ L_H \dot{i}_{s_H} = q_H(V_{hf} + V_{lf}) - V_{s_H}, \\ C_{s_L}\dot{V}_{s_L} = i_{s_L}, \\ C_{s_H}\dot{V}_{s_H} = i_{s_H}. \end{cases} \tag{6}$$

These state equations are considered only in the operating range, which is $\Omega$ defined by:

$$\begin{array}{ll} i_{s_L} \in [-i_{smax_L}, i_{smax_L}], & i_{s_H} \in [-i_{smax_H}, i_{smax_H}], \\ V_{s_L} \in [V_{smin_L}, V_{smax_L}], & V_{s_H} \in [V_{smin_H}, V_{smax_H}], \\ V_{lf} > V_{min_L}, & \left|V_{hf}\right| < V_{max_H}. \end{array} \tag{7}$$

Note that $0 < V_{s_{min_L}} < V_{s_{max_L}} < V_{min_L} < V_{ref} < V_{max_L}$ and $0 < V_{max_H} < V_{s_{min_H}} < V_{s_{max_H}}$. For subsequent analysis, we set the following lower and upper bounds:

$$\begin{array}{ll} V \in [0, V_{max_L} + V_{max_H}], & \\ i_{lf} \in [-i_{max_L}, i_{max_L}], & i_{hf} \in [-i_{max_H}, i_{max_H}], \\ i_{s_{H_L}} \in [-i_{smax_{HL}}, i_{smax_{HL}}], & i_{s_{H_H}} \in [-i_{smax_{HH}}, i_{smax_{HH}}], \\ i_{s_{L_L}} \in [-i_{smax_{LL}}, i_{smax_{LL}}], & i_{s_{L_H}} \in [-i_{smax_{LH}}, i_{smax_{LH}}]. \end{array} \tag{8}$$

### *2.1. Control of the LF-VIC*

The LF-VIC controller is composed of a sliding mode voltage controller and a PI charge controller. Their control objectives are to control the low-frequency component of the voltage to its expected reference in normal operation process and, restrain the LF-VIC's SoC within its normal operating range, respectively.

#### 2.1.1. Voltage Control of the LF-VIC

We use a sliding mode controller to regulate the low-frequency component of $V$. We employ a sliding function with the states $x = \begin{bmatrix} V_{lf} & i_{s_L} & V_{s_L} \end{bmatrix}^T$ and disturbance $i_{lf}$, based on ([13], Section 6):

$$\begin{aligned} S_L(x) =& (V_{ref} - V_{lf}) + k_1 \int_0^t (V_{ref} - V_{lf}) d\tau \\ & - k_2 (V_{ref} i_{lf} - V_{s_L} i_{s_L}), \end{aligned} \tag{9}$$

where we set $k_1 > 0$. The sliding surface $\Gamma_L$ is the set of all the possible $x \in \Omega$ for which

$$S_L(x) = 0. \tag{10}$$

Note that the energy stored in the two inductors of the PVIC can be roughly written as $V_{ref} i_{lf} + V_{ref} i_{hf} - V_{s_L} i_{s_L} - V_{s_H} i_{s_H}$. The nonlinear term $V_{ref} i_{lf} - V_{s_L} i_{s_L}$ in (9) represents the energy in $L_L$. The remaining part $V_{ref} i_{hf} - V_{s_H} i_{s_H}$, which represents the energy in $L_H$, is included in the HF-VIC controller, which will be discussed in Section 2.2. The absolute values of $k_1$ and $k_2$ should be small enough to diminish deviation between $V_{lf}$ and $V_{ref}$ when $x$ is controlled to be within $\Gamma_L$.

To reduce chattering effects and limit operating frequencies within a controllable range, we use the hysteresis-modulation (HM) sliding mode control [24] to determine the binary switching signals $q_L$ and $\tilde{q}_L$:

$$\begin{cases} q_L = \begin{cases} 1, \text{if } S_L < -\epsilon, \\ 0, \text{if } S_L > \epsilon, \\ \text{previous state, if } S_L \in [-\epsilon, \epsilon]. \end{cases} \\ \tilde{q}_L = 1 - q_L, \end{cases} \tag{11}$$

where $\epsilon$ is a small positive number. In the stability analysis later, we assume $\epsilon = 0$ for simplicity but without loss of generality.

The sliding mode controller is designed according to the following steps. Firstly, the hitting condition should be satisfied to ensure that the state trajectory is guided to the sliding surface. After that, when the states are within a small vicinity of the sliding surface, the existence condition needs to be satisfied to maintain the states within the neighbourhood of the sliding surface and always direct the states towards the desired surface [20,25].

In this paper, we describe the hitting condition by

$$S_L(x) \cdot \dot{S}_L(x) < 0 \quad \text{for all } x \in \Omega \backslash \Gamma_L, \tag{12}$$

where

$$\begin{aligned} \dot{S}_L(x) = &- \dot{V}_{lf} + k_1(V_{ref} - V_{lf}) \\ &- k_2(V_{ref}\dot{i}_{lf} - V_{s_L}\dot{i}_{s_L} - \dot{V}_{s_L} i_{s_L}). \end{aligned} \tag{13}$$

Combining (6) and (13), we get

$$\begin{aligned} \dot{S}_L(x) = &- \frac{i_{lf} - q_L i_{s_{L_L}} - q_H i_{s_{H_L}}}{C} + k_1(V_{ref} - V_{lf}) \\ &+ k_2\left(\frac{q_L(V_{lf} + V_{hf})V_{s_L} - V_{s_L}^2}{L_L} + \frac{i_{s_L}^2}{C_{s_L}} - V_{ref}\dot{i}_{lf}\right). \end{aligned} \tag{14}$$

When $S_L(x) > 0$ for all $x \in \Omega \backslash \Gamma_L$, $q_L = 0$. To satisfy (12), we require that

$$\begin{aligned} \dot{S}_L = &- \frac{i_{lf} - q_H i_{s_{H_L}}}{C} + k_1(V_{ref} - V_{lf}) \\ &+ k_2\left(-\frac{V_{s_L}^2}{L_L} + \frac{i_{s_L}^2}{C_{s_L}} - V_{ref}\dot{i}_{lf}\right) < 0. \end{aligned} \tag{15}$$

Here, $\dot{i}_{lf}$ is set to be $\dot{i}_{lf} \in [-\dot{i}_{max_L}, \dot{i}_{max_L}]$. Note that it is hard to limit a current derivative term in reality. This limit is allowed to be violated under some circumstances such as the abrupt current change due to some faults. However, it will be brought back by the control schemes. A sufficient condition for (15) is

$$\begin{aligned} &\dot{S}_{Lmax} \leq k_1(V_{ref} - V_{min_L}) + k_2\left(-\frac{V_{smin_L}^2}{L_L} + \frac{i_{smax_L}^2}{C_{s_L}}\right. \\ &\left. + V_{ref}\dot{i}_{max_L}\right) + \frac{i_{max_L} + i_{smax_{HL}}}{C} < 0. \end{aligned} \tag{16}$$

When $S_L(x) < 0$ for all $x \in \Omega \backslash \Gamma_L$, $q_L = 1$. To satisfy (12), we have

$$\begin{aligned} \dot{S}_L = &- \frac{i_{lf} - q_H i_{s_{H_L}} - i_{s_{L_L}}}{C} + k_1(V_{ref} - V_{lf}) \\ &+ k_2\left(\frac{(V_{lf} + V_{hf})V_{s_L} - V_{s_L}^2}{L_L} + \frac{i_{s_L}^2}{C_{s_L}} - V_{ref}\dot{i}_{lf}\right) > 0. \end{aligned} \tag{17}$$

That is, a sufficient condition for (17) is

$$\begin{aligned}\dot{S}_{Lmin} \geq \; & k_1(V_{ref} - V_{max_L}) \\ & + k_2\left(\frac{V_{smax_L}(V_{min_L} - V_{max_H}) - V_{smax_L}^2}{L_L}\right. \\ & \left. - V_{ref}\dot{i}_{max_L}\right) - \frac{i_{max_L} + i_{smax_{LL}} + i_{smax_{HL}}}{C} > 0.\end{aligned} \tag{18}$$

From (16) and (18) we set

$$\begin{cases} k_1 > 0, \qquad k_2 > 0, \\ 0 < \dot{i}_{max_L} < minF_{Lb}, \\ F_{Lb} = \left\{ \frac{V_{s_{min_L}}^2}{L_L V_{ref}} - \frac{i_{smax_L}^2}{C_{s_L} V_{ref}}, \frac{V_{smax_L}(V_{min_L} - V_{smax_L} - V_{max_H})}{L_L V_{ref}} \right\}, \end{cases} \tag{19}$$

where $F_{Lb}$ is derived from:

$$-\frac{V_{smin_L}^2}{L_L} + \frac{i_{smax_L}^2}{C_{s_L}} + V_{ref}\dot{i}_{max_L} < 0 \tag{20}$$

and

$$\frac{V_{smax_L}(V_{min_L} - V_{max_H}) - V_{smax_L}^2}{L_L} - V_{ref}\dot{i}_{max_L} > 0. \tag{21}$$

Note that it is reasonable to have inequalities (20) and (21) since $L_L \ll C_{s_L} \ll i_{smax_L} < V_{smin_L} < V_{ref} \ll \dot{i}_{max_L}$ and $L_L \ll V_{max_H} \ll V_{smax_L} < V_{min_L} < V_{ref} \ll \dot{i}_{max_L}$.

Then, the existing condition for this SMC is

$$\begin{cases} \lim_{S_L(x)\to S_L(x_0)^+} \dot{S}_L(x) < 0, \\ \lim_{S_L(x)\to S_L(x_0)^-} \dot{S}_L(x) > 0, \end{cases} \quad \text{for all } x_0 \in \Gamma_L. \tag{22}$$

From (10), we have

$$i_{lf} = \frac{V_{ref} - V_{lf} + k_1\int_0^t (V_{ref} - V_{lf})d\tau + k_2 V_{s_L} i_{s_L}}{k_2 V_{ref}}, \tag{23}$$

based on which the inequalities (15) and (17) can be written as

$$\begin{aligned}\dot{S}_L = & -\frac{V_{ref} - V_{lf} + k_1\int_0^t (V_{ref} - V_{lf})d\tau + k_2 V_{s_L} i_{s_L}}{C k_2 V_{ref}} \\ & + \frac{q_H i_{s_{H_L}}}{C} + k_1(V_{ref} - V_{lf}) \\ & + k_2\left(-\frac{V_{s_L}^2}{L_L} + \frac{i_{s_L}^2}{C_{s_L}} - V_{ref}\dot{i}_{lf}\right) < 0,\end{aligned} \tag{24}$$

and

$$\begin{aligned}\dot{S}_L = & -\frac{V_{ref} - V_{lf} + k_1\int_0^t (V_{ref} - V_{lf})d\tau + k_2 V_{s_L} i_{s_L}}{C k_2 V_{ref}} \\ & + \frac{q_H i_{s_{H_L}}}{C} + \frac{i_{s_{L_L}}}{C} + k_1(V_{ref} - V_{lf}) \\ & + k_2\left(\frac{(V_{lf} + V_{hf})V_{s_L} - V_{s_L}^2}{L_L} + \frac{i_{s_L}^2}{C_{s_L}} - V_{ref}\dot{i}_{lf}\right) > 0.\end{aligned} \tag{25}$$

Since $Ck_2V_{ref} > 0$, (24) and (25) can be written as

$$\begin{aligned} &-k_1\int_0^t (V_{ref}-V_{lf})d\tau - k_2(V_{s_L}i_{s_L} - q_H i_{s_{H_L}}V_{ref}) \\ &+k_1k_2(CV_{ref}^2 - CV_{ref}V_{lf}) \\ &+k_2^2(\frac{-CV_{ref}V_{s_L}^2}{L_L} + \frac{CV_{ref}i_{s_L}^2}{C_{s_L}} - CV_{ref}^2\dot{i}_{lf}) < V_{ref}-V_{lf}, \end{aligned} \tag{26}$$

and

$$\begin{aligned} &-k_1\int_0^t (V_{ref}-V_{lf})d\tau + k_2(i_{s_{L_L}}V_{ref} - i_{s_L}V_{s_L} + q_H i_{s_{H_L}}V_{ref}) \\ &+k_2^2(\frac{CV_{ref}V_{s_L}(V_{lf}+V_{hf}-V_{s_L})}{L_L} + \frac{CV_{ref}i_{s_L}^2}{C_{s_L}} - CV_{ref}^2\dot{i}_{lf}) \\ &+k_1k_2(CV_{ref}^2 - CV_{ref}V_{lf}) > V_{ref}-V_{lf}. \end{aligned} \tag{27}$$

The parameters $k_1$ and $k_2$ should be chosen to fulfill the inequalities (15), (17), (26), and (27) to satisfy both the hitting condition and existing condition, which are the sufficient conditions to attain the successful control. The details about the selection of $k_1$ and $k_2$ will be discussed in Section 2.3.

#### 2.1.2. Charge Control of the LF-VIC

In the application of grid connected DFIG system, a charge control scheme is developed to regulate the LF-VIC's state of charge ($V_{s_L}$) by coupling a PI controller with the controller of grid side converter. Since the charge controller is required to operate more slowly than the voltage controller, the average of $V_{s_L}$ (i.e., $V_{s_{Lavg}}$) is controlled, which is acquired by passing $V_{s_L}$ through a low pass filter with the corner frequency $f_c$ (see Figure 5). In the voltage control of DC-link capacitor, the voltage $V$ is fed back to the controller of grid side converter. Herein, the voltage $V^*$ rather than $V$ is injected. $V^*$ is the estimated value of $V$ obtained from the LF-VIC's state of charge through a PI controller:

$$V^* = V_{ref} - k_P(V_{sref_L} - V_{s_{Lavg}}) - k_I\int_0^t (V_{sref_L} - V_{s_{Lavg}})d\tau.$$

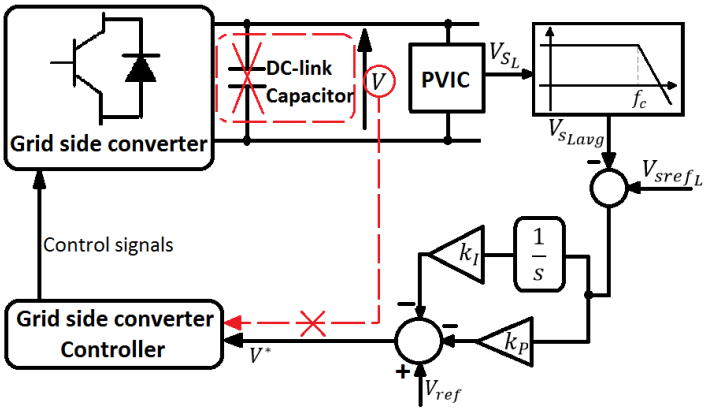



**Figure 5.** Charge control scheme of the LF-VIC. The estimated voltage $V^*$ replaces the measurement of the DC-link voltage for the grid side converter.

In this way, the control scheme of the grid side converter is not violated, realising a 'plug-and-play' pattern for the PVIC.

### 2.2. Control of the HF-VIC

For the control of HF-VIC, both voltage control and charge control are implemented by a sliding mode controller whose sliding function is

$$\begin{aligned} S_H(x) = (0 - V_{hf}) - k_3(V_{ref} i_{hf} - V_{s_H} i_{s_H}) \\ + k_4(V_{sref_H} - V_{s_{Havg}}). \end{aligned} \tag{28}$$

The sliding surface $\Gamma_H$ is the set of all the possible $x = \begin{bmatrix} V_{hf} & i_{s_H} & V_{s_H} \end{bmatrix}^T \in \Omega$ for which

$$S_H(x) = 0. \tag{29}$$

The expression $V_{ref} i_{hf} - V_{s_H} i_{s_H}$ appearing in (28) represents the power stored in $L_H$, which is included in the HF-VIC controller. $V_{sref_H} - V_{s_{Havg}}$ is the charge control term in this sliding function. As with the charge control of the LF-VIC, the average of $V_{s_H}$ (i.e., $V_{s_{Havg}}$) is regulated to realise a much slower response of the charge control than the voltage control. $V_{s_{Havg}}$ is obtained by passing $V_{s_H}$ through a low pass filter with the corner frequency $f_c$. The absolute values of the parameters $k_3$ and $k_4$ should be very small to guarantee the accuracy of the control.

The hysteresis-modulation (HM) sliding mode control is also applied to the HF-VIC, using the same $\epsilon$ as in (11):

$$\begin{cases} q_H = \begin{cases} 1, \text{if } S_H < -\epsilon, \\ 0, \text{if } S_H > \epsilon, \\ \text{previous state, if } S_H \in [-\epsilon, \epsilon]; \end{cases} \\ \tilde{q}_H = 1 - q_H. \end{cases}$$

The hitting condition is described as

$$S_H(x) \cdot \dot{S}_H(x) < 0$$

for all $x \in \Omega \backslash \Gamma_H$. Here, $\dot{V}_{s_{Havg}}$ is limited as $\dot{V}_{s_{Havg}} \in [-\dot{V}_{s_{Havg_{max}}}, \dot{V}_{s_{Havg_{max}}}]$, where $\dot{V}_{s_{Havg_{max}}}$ should be small due to the slow change of $V_{s_{Havg}}$. Similarly as in Section 2.1, when $S_H(x) > 0$ and $S_H(x) < 0$, we have

$$\dot{S}_H(x) = \frac{-i_{hf} - q_L i_{s_{L_H}}}{C} - k_3 \left( V_{ref} \dot{i}_{hf} - \frac{i_{s_H}^2}{C_{s_H}} + \frac{V_{s_H}^2}{L_H} \right) - k_4 \dot{V}_{s_{Havg}} < 0 \tag{30}$$

and

$$\begin{aligned} \dot{S}_H(x) = & \frac{-i_{hf} - i_{s_{H_H}} - q_L i_{s_{L_H}}}{C} \\ & -k_3 \left( -\frac{V_{s_H}(V_{hf} + V_{lf})}{L_H} + \frac{V_{s_H}^2}{L_H} + V_{ref} \dot{i}_{hf} - \frac{i_{s_H}^2}{C_{s_H}} \right) - k_4 \dot{V}_{s_{Havg}} > 0, \end{aligned} \tag{31}$$

respectively. Here, $\dot{i}_{hf}$ is limited as $\dot{i}_{hf} \in [-\dot{i}_{max_H}, \dot{i}_{max_H}]$, that is, the sufficient conditions for (30) and (31) are

$$\begin{aligned} \dot{S}_{Lmax} \leq & k_3 \left( \frac{i_{smax_H}^2}{C_{s_H}} + V_{ref} \dot{i}_{max_H} - \frac{V_{smin_H}^2}{L_H} \right) \\ & + k_4 \dot{V}_{s_{Havg_{max}}} + \frac{i_{max_H} + i_{smax_{LH}}}{C} < 0, \end{aligned} \tag{32}$$

and

$$\begin{aligned}\dot{S}_{Lmin} \geq & -k_3\left(\frac{V_{smax_H}(V_{max_H}-V_{min_L})+V_{smax_H}^2}{L_H}+V_{ref}\dot{i}_{max_H}\right)\\ & -k_4\dot{V}_{s_{Havg_{max}}}-\frac{i_{max_H}+i_{smax_{HH}}+i_{smax_{LH}}}{C}>0.\end{aligned} \tag{33}$$

To fulfil (32) and (33), we set

$$\begin{cases} k_3>0, \qquad k_4<0,\\ 0<\dot{i}_{max_H}<\min F_{Hb},\\ F_{Hb}=\{\frac{V_{smin_H}^2}{L_H V_{ref}}-\frac{i_{smax_H}^2}{C_{s_H}V_{ref}},-\frac{V_{smax_H}(V_{max_H}-V_{min_L})+V_{smax_H}^2}{L_H V_{ref}}\}, \end{cases} \tag{34}$$

where $F_{Hb}$ is derived from

$$\frac{i_{smax_H}^2}{C_{s_H}}+V_{ref}\dot{i}_{max_H}-\frac{V_{smin_H}^2}{L_H}<0 \tag{35}$$

and

$$\frac{V_{smax_H}(V_{max_H}-V_{min_L})+V_{smax_H}^2}{L_H}+V_{ref}\dot{i}_{max_H}<0. \tag{36}$$

To fulfil the inequalities (35) and (36), we set $L_H \ll C_{s_H} \ll i_{smax_H} < V_{smin_H} < V_{ref} \ll \dot{i}_{max_H}$ and $L_H \ll V_{max_H} \ll V_{smax_H} < V_{min_L} < V_{ref} \ll \dot{i}_{max_H}$. The existing condition for this SMC is

$$\begin{cases} \lim_{S_H(x)\to S_H(x_0)^+}\dot{S}_H(x)<0,\\ \lim_{S_H(x)\to S_H(x_0)^-}\dot{S}_H(x)>0, \end{cases} \quad \text{for all } x_0\in\Gamma_H. \tag{37}$$

Similarly as in Section 2.1, we get

$$\begin{aligned}& -k_3(V_{s_H}i_{s_H}+q_L V_{ref}i_{s_{L_H}})-k_4(V_{s_{ref_H}}-V_{s_{Havg}})\\ & -k_3k_4CV_{ref}\dot{V}_{s_{Havg}}+k_3^2CV_{ref}(V_{ref}\dot{i}_{hf}+\frac{i_{s_H}^2}{C_{s_H}}-\frac{V_{s_H}^2}{L_H})<-V_{hf},\end{aligned} \tag{38}$$

and

$$\begin{aligned}& k_3(i_{s_{H_H}}V_{ref}-q_L i_{s_{L_H}}V_{ref}-V_{s_H}i_{s_H})\\ & +k_3^2CV_{ref}(V_{ref}\dot{i}_{hf}+\frac{i_{s_H}^2}{C_{s_H}}+\frac{(V_{hf}+V_{lf}-V_{s_H})V_{s_H}}{L_H})\\ & -k_4(V_{sref_H}-V_{s_{Havg}})-k_3k_4CV_{ref}\dot{V}_{s_{Havg}}>-V_{hf}.\end{aligned} \tag{39}$$

The parameters $k_3$ and $k_4$ should be chosen to satisfy the inequalities (30), (31), (38) and (39), so that the state trajectory will converge and stabilise at the sliding surface $\Gamma_H$. The details about the selection of $k_3$ and $k_4$ will be discussed in Section 2.3.

### *2.3. Parameter Selection*

In order to limit the deviation between $V$ and its reference $V_{ref}$, the absolute values of the parameters $k_1$, $k_2$, $k_3$ and $k_4$ should be small. We apply the interior-point optimization algorithm to find the boundaries of these four parameters, which are embedded in the nonlinear programming solver '*fmincon*' in Matlab (MathWorks).

The optimization for LF-VIC controller parameters is conducted to minimize $|k_1|+|k_2|$ under the inequality constraints (7), (8), (15), (17), (19), (26), (27), and equality constraint (10). Similarly,

the objective function for parameter optimization of the HF-VIC controller is $|k_3| + |k_4|$, with the inequalities constraints (7), (8), (30), (31), (34), (38), (39), and equality constraint (29). The results of these optimizations provide the boundaries for $k_1, k_2, k_3$ and $k_4$ to ensure the successful control of both LF-VIC controller and HF-VIC controller.

The parameters' initial values are all set to be zero. The related operating boundaries are listed in Table 1. The optimal boundaries for the parameters $k_1$~$k_4$ are

$$\begin{cases} k_{1min} = 2.66 \times 10^{-7}, & k_{2min} = 5.77 \times 10^{-6}, \\ k_{3min} = 2.55 \times 10^{-7}, & k_{4max} = -1.01 \times 10^{-4}. \end{cases}$$

**Table 1.** Operating boundaries.

| Parameters | Values | Parameters | Values |
|---|---|---|---|
| $V_{smax_L}$ | 920 V | $V_{smax_H}$ | 920 V |
| $i_{smax_L}$ | 50 A | $i_{smax_H}$ | 200 A |
| $i_{smax_{HL}}$ | 50 A | $i_{smax_{LH}}$ | 200 A |
| $i_{smax_{LL}}$ | 50 A | $i_{smax_{HH}}$ | 200 A |
| $i_{max_L}$ | 100 A | $i_{max_H}$ | 500 A |
| $V_{min_L}$ | 1140 V | $\dot{V}_{s_{Havg_{max}}}$ | 100 V/s |
| $V_{max_H}$ | 10 V | $V_{s_{Havg_{max}}}$ | 770 V |
| $V_{max_L}$ | 1160 V | $\dot{i}_{max_L}$ | $2.76 \times 10^6$ A/s |
| $V_{s_{Havg_{min}}}$ | 570 V | $\dot{i}_{max_H}$ | $2.75 \times 10^6$ A/s |

## 3. Simulation Study

The simulations are conducted using a grid-connected DFIG model [36,37] driven by the WP 1.5-MW wind turbine model [38–40]. The parameters of the DFIG are listed in Table 2. The hub height of wind turbine is 84 m. The rated wind speed is about 12 m/s. The blade length is 33.25 m and the maximum blade chord is 8% of blade radius [43].

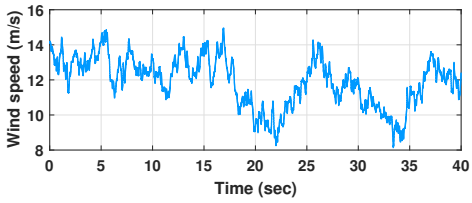
**Table 2.** Parameters of the 1.5-MW doubly fed induction generator (DFIG) model [36,37].

| DFIG Parameters | Values |
|---|---|
| Frequency | 60 Hz |
| Pole pairs | 3 |
| Magnetizing inductance | 2.9 p.u. |
| Stator resistance | 0.023 p.u. |
| Stator inductance | 0.18 p.u. |
| Rotor type | Wound |
| Rotor resistance | 0.016 p.u. |
| Rotor inductance | 0.16 p.u. |
| Inertia | 0.685 p.u. |

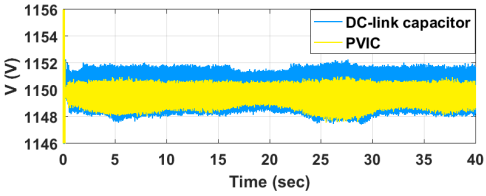
The NREL FAST (Fatigue, Aerodynamics, Structures, and Turbulence) code [38] is used to simulate dynamic responses of the turbine. FAST takes aerodynamics, control and electrical (servo) dynamics, and structural (elastic) dynamics of the turbine into account. FAST is interfaced with Matlab/Simulink through a Simulink S-Function block. During simulations, this block calls the FAST Dynamic Library, which has integrated all the FAST modules [38] and is compiled as a dynamic-link-library (DLL).

NREL TurbSim [41] is utilised to generate stochastic, full-field, and turbulent wind flows for simulation studies. The International Electro-technical Commission (IEC) Kaimal spectral model [44,45] in Turbsim is applied to generate the wind condition as shown in Figure 6a, with the category A (most turbulent) IEC NTM (normal turbulence model). The mean hub-height longitudinal wind speed

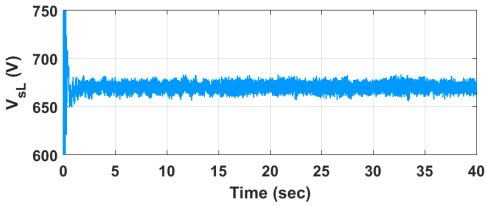
is 12 m/s. Note that the average sampling frequency of the LF-VIC controller is smaller than that of HF-VIC controller in the simulations, which are approximately 45 kHz and 100 kHz, respectively.



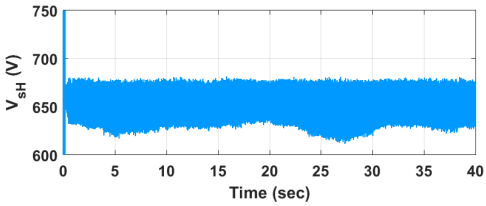

(**a**) The turbulent wind input.




(**b**) DC-link voltage $V$ stabilised by DC-link capacitor and PVIC.




(**c**) State of charge of the LF-VIC (i.e., $V_{s_L}$).




(**d**) State of charge of the HF-VIC (i.e., $V_{s_H}$).

**Figure 6.** Wind input and performances of PVIC under normal grid operation.

The voltage filtering performances of two configurations are compared: a 15 mF DC-link capacitor and a PVIC as in Figure 4, where the total capacitance of $C$, $C_{s_L}$ and $C_{s_H}$ is 15 mF. Tables 3 and 4 list the parameters of the electronic components in PVIC and control parameters of PVIC, respectively.

**Table 3.** Parameters of the electronic components in PVIC (see Figure 4).

| Components in PVIC | Configuration |
|---|---|
| $C$ | 7 mF |
| $C_{s_L}$ | 6 mF |
| $C_{s_H}$ | 2 mF |
| $C_{sn}$ | 1 nF |
| $L_L$ | 10 µH |
| $L_H$ | 10 µH |

**Table 4.** Control parameters of the PVIC.

| Parameters | Values | Parameters | Values |
|---|---|---|---|
| $V_{ref}$ | 1150 V | $\epsilon$ | 0.5 |
| $V_{sref_L}$ | 670.5 V | $V_{sref_H}$ | 670.5 V |
| $k_1$ | $5 \times 10^{-5}$ | $k_2$ | $6 \times 10^{-6}$ |
| $k_3$ | $2.5 \times 10^{-5}$ | $k_4$ | $-2.5 \times 10^{-2}$ |
| $D_{pow\_up}$ | 0.3 | $f_{pow\_up}$ | 30 kHz |
| $k_P$ | 0.0169 | $k_I$ | 0.0225 |
| $f_l$ | 120 Hz | $f_c$ | 60 Hz |

Firstly, the simulation is conducted without grid disturbance under the turbulent wind input (see Figure 6). Figure 6a,b demonstrate the turbulent wind input and the DC-link voltage stabilised by DC-link capacitor and PVIC. Figure 6c,d illustrate the SoC of PVIC (i.e., $V_{s_L}$ and $V_{s_H}$). It is clear that when there is no grid disturbance, both configurations can stabilise the DC-link voltage $V$ to its reference, and PVIC reduces about 30% of the voltage fluctuations compared with the equivalent DC-link capacitor (see Figure 6b), which is mainly achieved by HF-VIC controller to suppress the high-frequency ripple due to the fast switching of two converters. The SoC of the LF-VIC and HF-VIC are successfully controlled to the vicinity of their references by the charge control schemes explained in Section 2.

Then, the simulations are conducted under four types of grid disturbances with the same turbulent wind input (Figure 6a). The first case is the frequency variation. In reality, the frequency, as a key factor to judge the power quality, is allowed to vary within a very narrow range during normal operation. Here, we test the performance of the PVIC and a DC-link capacitor under a one-second large sinusoidal grid frequency variation with an amplitude of 1 Hz and a period of 0.5 s. Figure 7a,c show this grid condition and the performances of PVIC and DC-link capacitor. Note that the $V_{lf}$ and $V_{hf}$ of the DC-link voltage are obtained according to (1).

The second type of the tested grid disturbances is the balanced three-phase voltage sag and swell. This is one of the most common power disturbances, which is usually caused by abrupt reduction or increase in loads. The grid voltage is altered four times by $\pm 0.15$ p.u. and each change is kept for 15 grid cycles (250 ms) (see Figure 7b,d).

The third case of the disturbance test is the harmonics. In reality, a small range of harmonics due to the nonlinear loads, transformer magnetisation nonlinearities, rectification, etc. is allowed in the power system, which may introduce the high-frequency ripple to DC-link voltage. We inject a combination of a negative-sequence 1st order harmonic (with the magnitude of 0.1 p.u.) and negative-sequence 3rd order harmonic (with the magnitude of 0.1 p.u. and phase shift of 35°), lasting for 1 s. Figure 8a,c show this grid condition and the voltage filtering performance.

Finally, we combine the above frequency variation and harmonic disturbances as the fourth case. That is, both high-frequency and low-frequency ripples are introduced to the DC-link voltage. The grid condition and the voltage filtering performance are shown in Figure 8b,d.

From Figures 7 and 8, it is clear that the PVIC achieves 10–20 times smaller variations in the DC-link voltage than the equivalent DC-link capacitor during these tested grid disturbances. This is because the oscillations in the DC-link voltage are transferred into the capacitors $C_{s_L}$ and $C_{s_H}$ of the PVIC. The same conclusion can be obtained under other grid conditions, such as unbalanced voltage sag and swell, the phase shift in voltage, different harmonic injections, frequency steps variations, or the combinations of some of these faults.

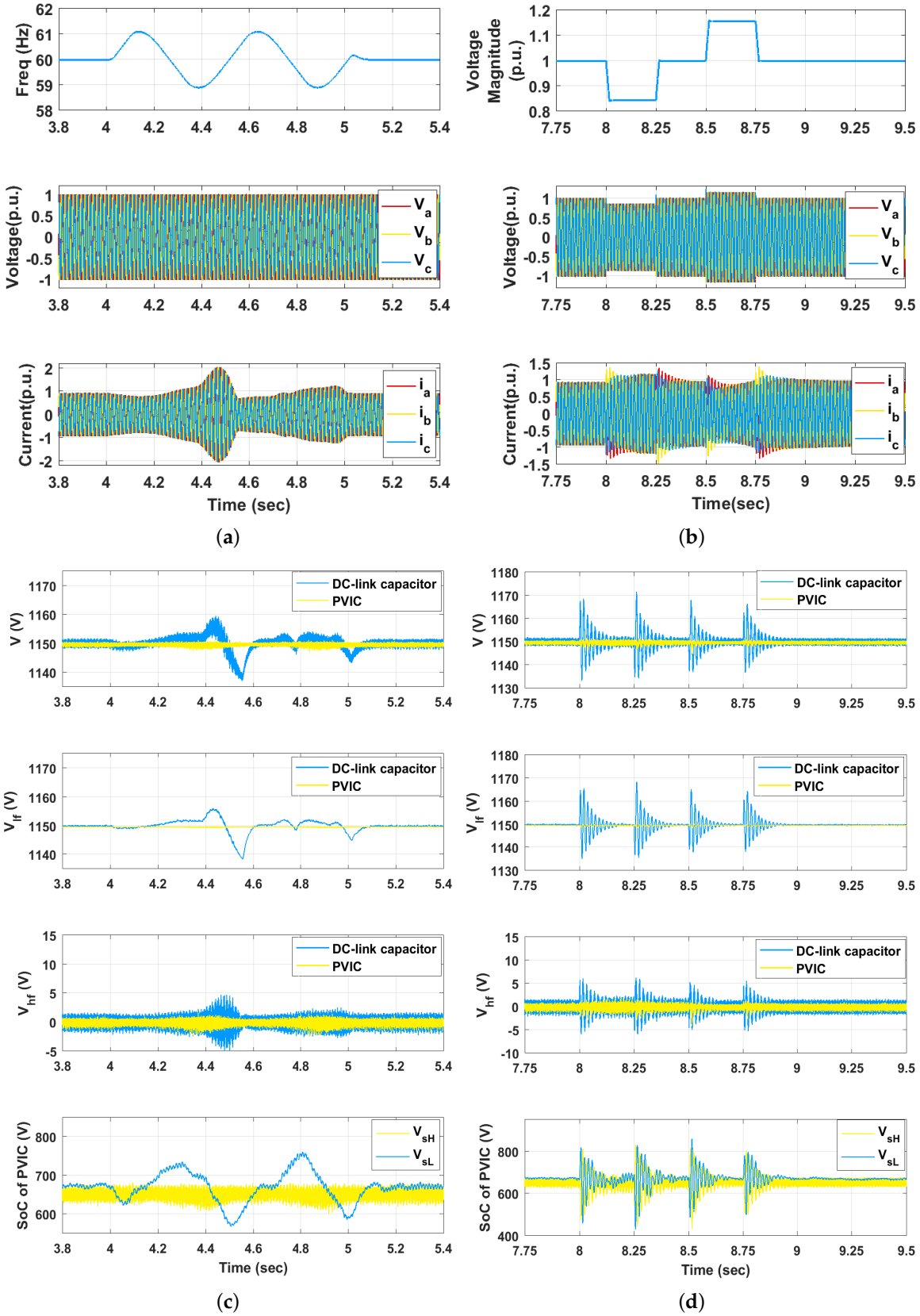



**Figure 7.** (**a**) shows frequency variation and three-phase grid voltage and current; (**b**) describes the grid voltage magnitude variation and three-phase grid voltage and current; (**c**) illustrates voltage filtering performance ($V$, $V_{lf}$, $V_{hf}$) of DC-link capacitor and PVIC, and PVIC's state of charge ($V_{s_L}$, $V_{s_H}$) under the grid conditions of (**a**); (**d**) exhibits the voltage filtering performance ($V$, $V_{lf}$, $V_{hf}$) of DC-link capacitor and PVIC, and PVIC's state of charge ($V_{s_L}$, $V_{s_H}$) under the grid conditions of (**b**).

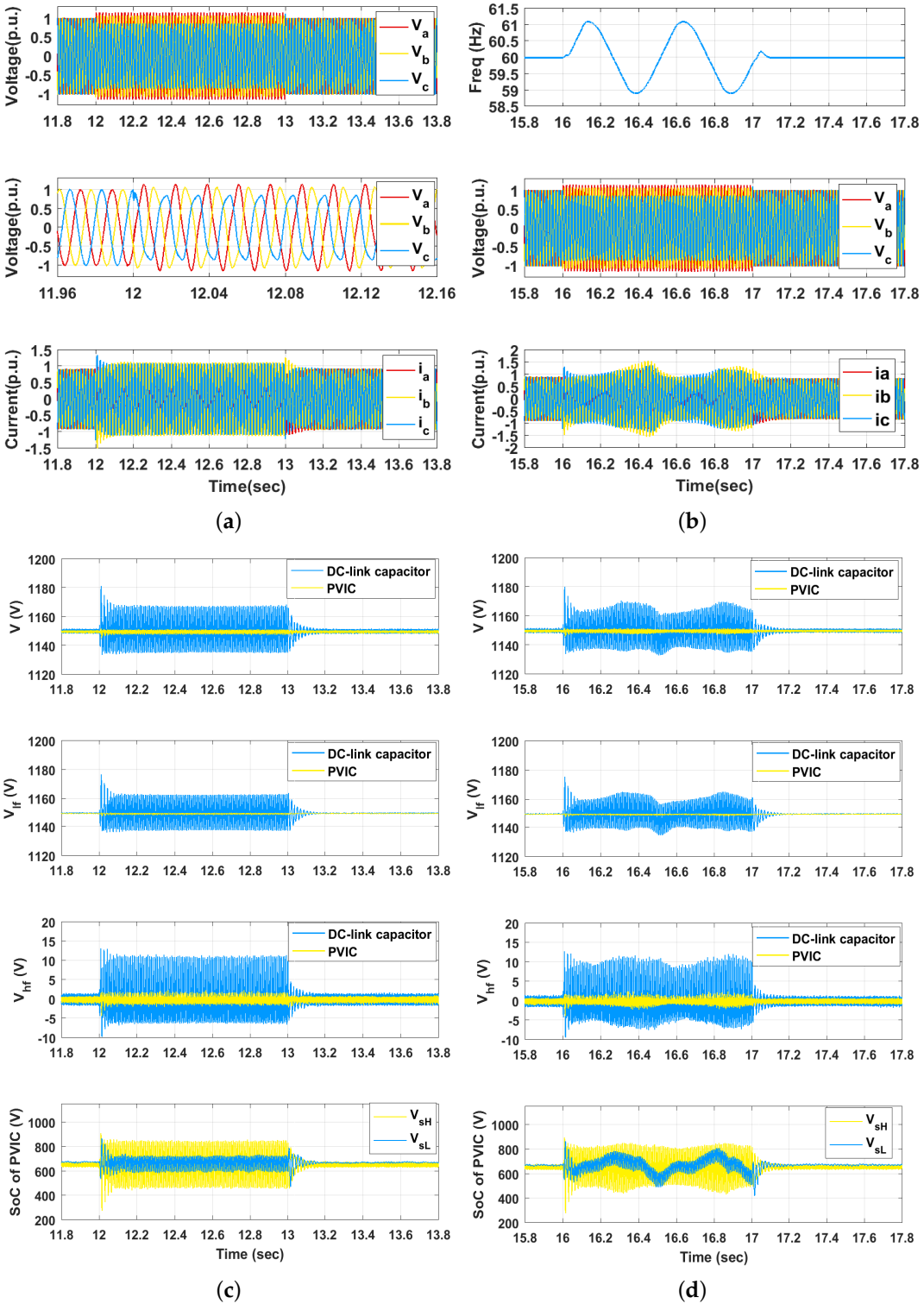



**Figure 8.** (**a**) shows the three-phase grid voltage and current when there is negative sequence 1st order harmonic (with magnitude of 0.1 p.u.) and negative sequence 3rd order harmonic (with magnitude of 0.1 p.u. and phase shift of 35°) injected; (**b**) demonstrates the frequency variation, three-phase grid voltage and current when the situations in Figure 7a and (**a**) both occur; (**c**) describes voltage filtering performance ($V$, $V_{lf}$, $V_{hf}$) of DC-link capacitor and PVIC, and PVIC's state of charge ($V_{s_L}$, $V_{s_H}$) under the grid conditions of (**a**); (**d**) displays voltage filtering performance ($V$, $V_{lf}$, $V_{hf}$) of the DC-link capacitor and PVIC, and PVIC's state of charge ($V_{s_L}$, $V_{s_H}$) of under the grid conditions of (**b**).

## 4. Conclusions

We have introduced the concept of parallel virtual infinite capacitor (PVIC), which refers to a low-frequency (LF) virtual infinite capacitor (VIC) and a high-frequency (HF) VIC working on a common DC link and sharing one capacitor. It is meant to suppress voltage ripple in a wider frequency band than what one VIC could achieve. The low frequency ripple is regulated by a sliding mode controller, and a PI controller is applied to maintain the LF-VIC within its operating range. Another sliding mode controller is applied to suppress high-frequency fluctuations while at the same time keeping the HF-VIC's state of charge within the normal range. The PVIC has been applied to replace the DC-link capacitor between two back-to-back converters in a grid-connected DFIG wind turbine system. The simulations were conducted under normal grid operation and four types of grid disturbances with turbulent wind (frequency variation, three-phase voltage sag and swell, harmonics and frequency variation with harmonics). The results indicate that the PVIC provides outstanding ripple suppression performance regardless of the low-frequency and high-frequency fluctuations, individually or together. In comparison with an equivalent DC-link capacitor, the PVIC reduces the DC-link voltage ripple by about 30% during normal grid operation, and approximately 10–20 times during the tested grid disturbances. The PVIC can also be applied to other systems that have a large capacitor for voltage filtering, such as PFC, photovoltaic power generators, vehicle chargers, etc.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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