

## Article

# Improvement in Harmonic Compensation of a Smart Charger with a Constant DC-Capacitor Voltage-Control-Based Strategy for Electric Vehicles in Single-Phase Three-Wire Distribution Feeders

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**Abstract:** This paper presents an improvement in harmonic compensation performance of a previously proposed smart charger (SC) with a constant dc-capacitor voltage-control (CDCVC) strategy for electric vehicles (EVs) in single-phase three-wire distribution feeders (SPTWDFs). A controller for 3rd harmonic currents in  $d$ - $q$  coordinates is added to the previously proposed SC. This addition improves harmonic compensation performance of the source currents. We briefly introduce harmonic current compensation using the previously proposed CDCVC-based algorithm for the SC. Then, the basic principles of the proposed controller for the 3rd harmonic currents in  $d$ - $q$  coordinates are discussed in detail. It is shown that synchronization of the current controllers for both the fundamental and 3rd harmonic components is required. The switching frequency of a three-leg pulse-width modulated rectifier with a bidirectional dc–dc converter, which performs the SC, is determined considering the synchronization of the current controllers. Simulation and experimental results demonstrate that balanced and sinusoidal source currents with a unity power factor are achieved during both battery charging and discharging operations in EVs, improving the harmonic compensation performance of the previously proposed SC. Experimental results also demonstrate that the total harmonic distortion values of source currents are improved by 8.4% and 3.6% with the proposed controller for 3rd harmonic currents, when the SC is discharging, for example.

**Keywords:** smart charger; single-phase three-wire distribution feeders (SPTWDFs); harmonics compensation; constant DC-capacitor voltage control (CDCVC); three-leg PWM rectifier; bidirectional DC-DC converter; single-phase PLL circuit; single-phase  $d$ - $q$  coordinate; 3rd harmonic currents

## 1. Introduction

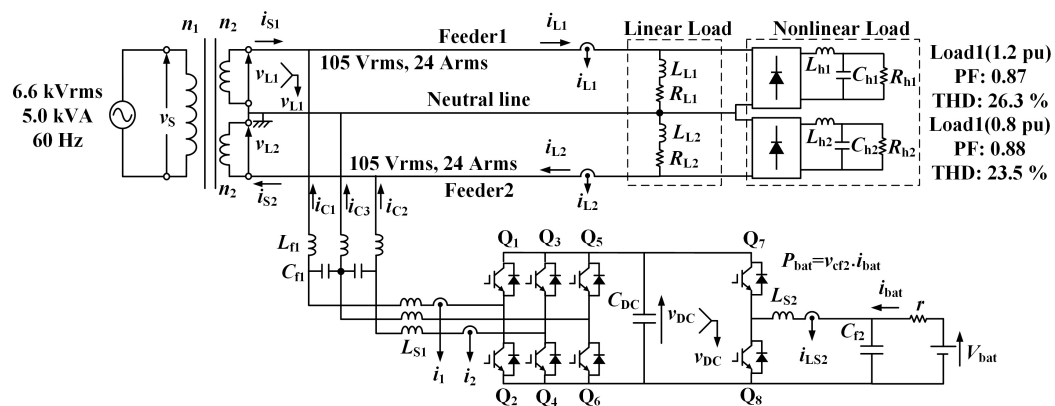
Single-phase three-wire distribution feeders (SPTWDFs) with pole-mounted distribution transformers (PMDTs) are widely used for home appliances in Japan. However, load conditions in the two feeders are always unbalanced, because the home appliances used by domestic consumers are often changed. Load conditions cause unbalanced source voltages and affect power quality on the secondary side of the PMDT. Domestic consumers who affect the power quality should pay extra charges to the power companies, as these cause economic losses in the distribution feeders. Conversely, domestic

consumers with high-quality home appliances that improve the power quality on the secondary side of PMDTs may be entitled to buy power at a reduced rate. It is natural that domestic consumers should be responsible for improving the power quality in the distribution feeders. The present authors, therefore, proposed a smart charger (SC) for electric vehicles (EVs) with a power-quality compensator, which can improve the power quality for domestic consumers [1]. The proposed SC is comprised of a three-leg pulse-width modulated (PWM) rectifier and a bidirectional dc–dc converter. The rectifier can compensate fundamental reactive and fundamental unbalanced active currents in SPTWDFs. For the control strategy, a constant dc-capacitor voltage-control (CDCVC) strategy was used. The CDCVC-based control strategy achieves balanced source currents with a unity power factor (PF). Many diode rectifiers are included in modern home appliances and connected to SPTWDFs. These diode rectifiers generate harmonic currents. The authors also dealt with harmonic current compensation with a CDCVC-based strategy in SPTWDFs with diode rectifiers [2]. Simulation and experimental results demonstrated that balanced and sinusoidal source currents with a unity PF are obtained during both battery charging and discharging operations in EVs. The 3rd harmonic currents remained in the source currents and affect the total harmonic distortion (THD) values of the source currents. The 3rd harmonic currents are dominant in single-phase circuits while the 5th and 7th harmonic currents are dominant in three-phase circuits. Therefore, suppressing these 3rd harmonic currents of the sources is necessary to improve the THD values in SPTWDFs.

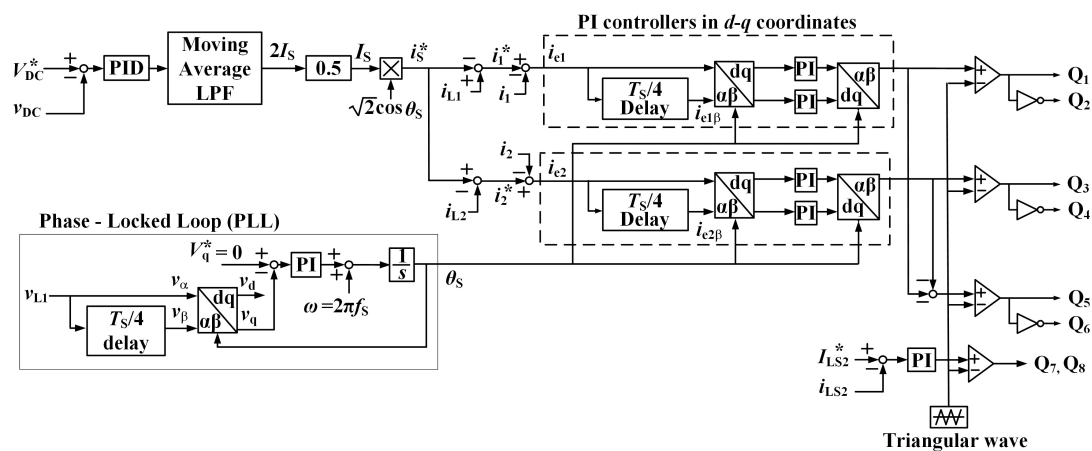
In this paper, an improvement in harmonic compensation performance of the proposed SC with a CDCVC strategy is presented. A current controller for the 3rd harmonic currents with proportional-integral (PI) controllers in  $d$ - $q$  coordinates is added to the previously proposed SC. Addition of the current controller for the 3rd harmonic currents improves the harmonic compensation performance of the CDCVC strategy. First, we briefly introduce harmonic current compensation with the previously proposed CDCVC-based algorithm for SC. Then, the basic principles of the proposed current controller for the 3rd harmonic current in  $d$ - $q$  coordinates are discussed in detail. It is shown that a synchronization of the current controllers in  $d$ - $q$  coordinates for both the fundamental and 3rd harmonic components is required. The switching frequency of the three-leg PWM rectifier with a bidirectional dc-dc converter, which performs SC, is determined considering the synchronization of the current controllers. Simulation and experimental results demonstrate that balanced and sinusoidal source currents with a unity PF are obtained during both battery charging and discharging operations in EVs, thereby improving the harmonic compensation performance of the SC.

## 2. Smart Charger for EVs

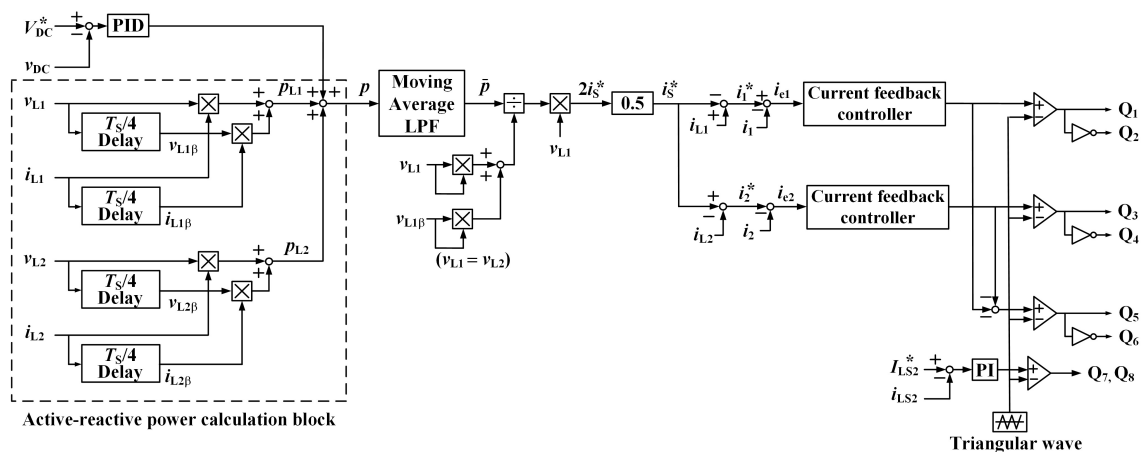
Figure 1 shows the system configuration of the previously proposed SC [1] and Figure 2 shows the control circuit diagram of the CDCVC-based strategy for Figure 1. The instantaneous active–reactive power theory in three-phase circuits, the so-called pq theory, was proposed by H. Akagi et al. [3] and is widely used for active power-line conditioners in three-phase circuits. Additionally, this theory was applied to three-phase four-wire systems by F. Z. Peng et al. [4]. Other methods in three-phase systems were proposed [5–7]. A single-phase pq theory was proposed [8]. If the single-phase pq theory is used for the SC in Figure 2, we obtain the control circuit diagram of Figure 3. The part enclosed by the dotted line shows the instantaneous active power calculation block. Note that the CDCVC block is also included in Figure 3. However, in Figure 2 only the CDCVC is included; no operation blocks for the reactive, unbalanced active, and harmonic components are included. Therefore, the proposed CDCVC-based strategy for SCs is simple. This simplified strategy attains balanced-sinusoidal source currents with a unity power factor (PF).



**Figure 1.** Power circuit diagram of the previously proposed smart charger (SC).



**Figure 2.** Control circuit diagram of the previously proposed constant dc-capacitor voltage-control (CDCVC) strategy.



**Figure 3.** Control circuit diagram for the SC in Figure 1, if the single-phase pq theory is applied.

### 2.1. Constant DC-Capacitor Voltage-Control Strategy for Harmonic Compensation

The previously proposed CDCVC-based strategy, of Figure 2 for the system in Figure 1, is briefly introduced. If the primary-side voltage  $v_S$  and the secondary-side voltages  $v_{L1}$  and  $v_{L2}$  are purely sinusoidal,  $v_S$ ,  $v_{L1}$ , and  $v_{L2}$  are expressed as:

$$\begin{aligned}
v_S &= \sqrt{2}V_S \cos \omega_S t, \\
v_L &= v_{L1} = v_{L2} \\
&= \sqrt{2}V_L \cos \omega_S t.
\end{aligned} \tag{1}$$

With the nonlinear loads, the load currents  $i_{L1}$  and  $i_{L2}$  in feeders 1 and 2 are given by:

$$\begin{aligned}
i_{L1} &= \sqrt{2}I_{L1F} \cos(\omega_S t - \phi_{L1F}) + \sqrt{2} \sum_{n=2}^{\infty} I_{L1n} \cos(n\omega_S t - \phi_{L1n}), \\
i_{L2} &= \sqrt{2}I_{L2F} \cos(\omega_S t - \phi_{L2F}) + \sqrt{2} \sum_{n=2}^{\infty} I_{L2n} \cos(n\omega_S t - \phi_{L2n}).
\end{aligned} \tag{2}$$

Assume that the source-side currents  $i_{S1}$  and  $i_{S2}$  are balanced and sinusoidal with a unity PF by the SC using the CDCVC-based strategy, while the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted. The aimed source-currents  $i_S^*$ ,  $i_{S1}^*$ , and  $i_{S2}^*$  are expressed as:

$$\begin{aligned}
i_S^* &= i_{S1}^* = i_{S2}^* \\
&= \sqrt{2}I_S \cos \omega_S t,
\end{aligned} \tag{3}$$

where  $I_S$  is the root-mean square (RMS) value of  $i_S^*$ . In Figure 1, the reference values of the output currents  $i_1^*$ ,  $i_2^*$ , and  $i_3^*$  of the three-leg PWM rectifier are given by:

$$\begin{aligned}
i_1^* &= i_{L1} - i_{S1}^*, \\
i_2^* &= -i_{L2} + i_{S2}^*, \\
i_3^* &= -(i_1^* + i_2^*).
\end{aligned} \tag{4}$$

When the output currents  $i_{C1}$ ,  $i_{C2}$ , and  $i_{C3}$  of the three-leg PWM rectifier are perfectly controlled to  $i_1^*$ ,  $i_2^*$ , and  $i_3^*$ , the output currents  $i_{C1}$ ,  $i_{C2}$ , and  $i_{C3}$  are expressed as:

$$\begin{aligned}
i_{C1} &= i_1^*, \\
i_{C2} &= i_2^*, \\
i_{C3} &= i_3^*.
\end{aligned} \tag{5}$$

The instantaneous power flow  $p_{SC}$  into the SC, which contains the three-leg PWM rectifier, is given by:

$$\begin{aligned}
p_{SC} &= -v_{L1} \cdot i_{C1} + v_{L2} \cdot i_{C2} \\
&= V_L \left\{ (-I_{L1F} \cos \phi_{L1F} - I_{L2F} \cos \phi_{L2F} + 2I_S) \right. \\
&\quad + (-I_{L1F} \cos \phi_{L1F} - I_{L2F} \cos \phi_{L2F}) \cos 2\omega_S t \\
&\quad + (-I_{L1F} \sin \phi_{L1F} - I_{L2F} \sin \phi_{L2F}) \sin 2\omega_S t \\
&\quad - \sum_{n=2}^{\infty} (I_{L1n} \cos \phi_{L1n} + I_{L2n} \cos \phi_{L2n}) \cos n\omega_S t \cos \omega_S t \\
&\quad \left. - \sum_{n=2}^{\infty} (I_{L1n} \sin \phi_{L1n} + I_{L2n} \sin \phi_{L2n}) \sin n\omega_S t \cos \omega_S t \right\}.
\end{aligned} \tag{6}$$

If the dc-capacitor voltage,  $v_{DC}$ , is kept constant by the CDCVC strategy, the average value  $\bar{p}_{SC}$  should be  $P_{bat}$  because the power charged or discharged to/from the battery is exchanged to the utility grid with the dc capacitor  $C_{DC}$ . Therefore,  $\bar{p}_{SC}$  is given by:

$$\begin{aligned}
\bar{p}_{SC} &= V_L (-I_{L1F} \cos \phi_{L1F} - I_{L2F} \cos \phi_{L2F} + 2I_S) \\
&= P_{bat}.
\end{aligned} \tag{7}$$

Given  $\bar{p}_{SC} = P_{bat}$ , the RMS value  $I_S$ —of  $i_S^*$ ,  $i_{S1}^*$ , and  $i_{S2}^*$  in Equation (3)—is expressed as:

$$I_S = \frac{I_{L1F} \cos \phi_{L1F} + I_{L2F} \cos \phi_{L2F}}{2} + \frac{P_{bat}}{2V_L}. \tag{8}$$

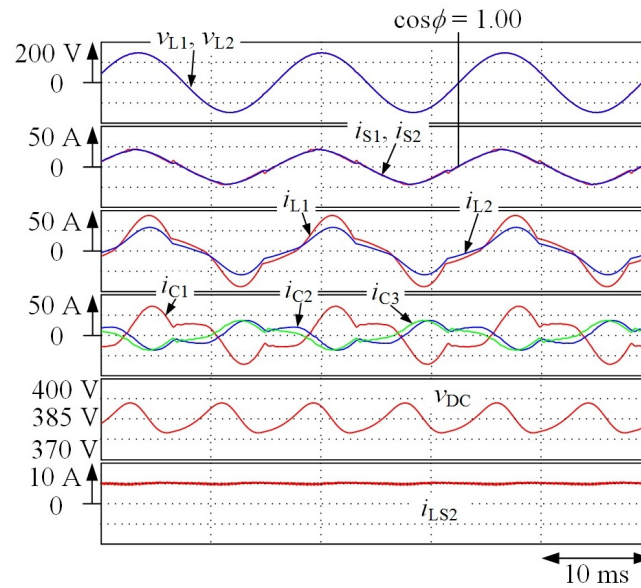
In Figure 2, the targeted source currents  $i_s^*$ ,  $i_{s1}^*$ , and  $i_{s2}^*$  are generated by  $2I_s$ , which is the output value of the proportional–integral–derivative (PID) controller, with  $\sqrt{2} \cos \omega_s$ . Equation (8) gives us an important implication that the average value  $\bar{p}_{SC}$  is  $P_{bat}$  when the output value of the PID controller in the CDCVC equals  $2I_s$ . Using the CDCVC-based strategy of Figure 2 achieves balanced and sinusoidal source currents  $i_{s1}$  and  $i_{s2}$  with a unity PF, as expressed by Equation (3), when charging or discharging the power  $P_{bat}$  from/to the utility grid, even though the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted.

The dc-capacitor voltage  $v_{DC}$  is detected. The difference  $\Delta v_{DC}$  between the reference value  $V_{DC}^*$  and  $v_{DC}$  is amplified by the PID controller, and then the RMS value  $I_s$  (of  $i_s^*$ ,  $i_{s1}^*$ , and  $i_{s2}^*$ ) is calculated. A moving-average low-pass filter (MALPF) is used to remove the  $2\omega_s$  component in the output signal of the PID controller, where  $\omega_s$  is the angular frequency of the source voltage  $v_s$ . The reference active current  $i_s^*$ , which is given by Equation (3), is calculated by multiplying  $I_s$  with  $\sqrt{2} \cos \theta_s$ . Here, to generate the electric angle  $\theta_s = \omega_s t$  of  $v_s$ , a phase-locked loop (PLL) with a single phase is used [9,10]. The primary-side voltage  $v_s$  is detected. This  $v_s$  corresponds to the  $\alpha$ -phase component  $v_\alpha$ . The detected voltage is delayed by  $T_s/4$ , where  $T_s$  is a cycle of  $v_s$ , and this delayed voltage corresponds to the  $\beta$ -phase component  $v_\beta$ . These  $v_\alpha$  and  $v_\beta$  are transformed to  $v_d$  and  $v_q$  in  $d$ - $q$  coordinates with  $\theta_s$ , respectively [11]. Controlling  $v_q$  to zero by a PI controller in  $d$ - $q$  coordinates, an electric angle  $\theta_s = \omega_s t$ , which is synchronized with  $v_s$ , can be generated. Finally, by subtracting the calculated  $i_s^*$  from the detected  $i_{L1}$  and  $i_{L2}$ , the reference values  $i_1^*$ ,  $i_2^*$ , and  $i_3^*$  for the three-leg PWM rectifier are calculated as:

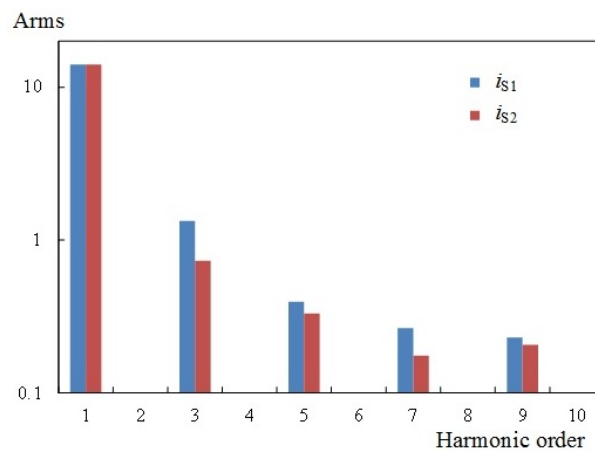
$$\begin{aligned} i_1^* &= i_{L1} - i_s^*, \\ i_2^* &= -i_{L2} + i_s^*, \\ i_3^* &= -(i_1^* + i_2^*). \end{aligned} \quad (9)$$

Steady-state error persists when a triangle intersection method current controller with a PI controller in a single-phase PWM rectifier is used. To suppress this steady-state error, a current feedback control method in  $d$ - $q$  coordinates for single-phase circuits was proposed [11]. In feeder 1 in Figure 1, for example, the difference  $i_{e1}$  between the reference value  $i_1^*$  and the detected  $i_1$  is calculated. This calculated difference  $i_{e1}$  corresponds to the  $\alpha$ -phase component in  $\alpha$ - $\beta$  coordinates. The calculated difference  $i_{e1}$  is then delayed by  $T_s/4$ , where this delayed component correspond to the  $\beta$ -phase component. These are transformed into  $d$ - $q$  coordinates with  $\theta_s$ , which is generated by the single-phase PLL. The current controllers in  $d$ - $q$  coordinates for the fundamental components are achieved. These current controllers in  $d$ - $q$  coordinates can suppress steady-state error because only the fundamental components in  $\alpha$ - $\beta$  coordinates will become dc components in  $d$ - $q$  coordinates.

Figure 4 shows simulation results for the previously proposed SC with the CDCVC-based strategy of Figure 2.  $v_{L1}$  and  $v_{L2}$  are the secondary-side voltage waveforms, and  $i_{s1}$  and  $i_{s2}$  are the secondary-side current waveforms.  $i_{L1}$  and  $i_{L2}$  are the load-side current waveforms at the domestic consumer's end;  $i_{C1}$ ,  $i_{C2}$ , and  $i_{C3}$  are the output currents waveforms of the SC;  $v_{DC}$  is the dc-capacitor voltage waveform; and  $i_{LS2}$  is the inductor current waveform. Although the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted, the source currents  $i_{s1}$  and  $i_{s2}$  are balanced with unity PF. However, the source currents  $i_{s1}$  and  $i_{s2}$  were slightly distorted. The THD values of  $i_{s1}$  and  $i_{s2}$  were 10.8% and 7.7%, respectively. Figure 5 shows the spectra of the source currents  $i_{s1}$  and  $i_{s2}$  from the simulation. It is well known that the 3rd harmonic currents are dominant in single-phase circuits. In Figure 5, a large contribution from 3rd harmonic currents is found in the source currents  $i_{s1}$  and  $i_{s2}$ . These 3rd harmonic components affect the THD values of  $i_{s1}$  and  $i_{s2}$ . Therefore, this paper introduces an improvement of harmonic compensation performance on the source side in Figure 1.



**Figure 4.** Simulation results for the previously proposed SC during a battery discharging operation from Reference [2].



**Figure 5.** Spectra of the source currents from the same simulation as Figure 4.

## 2.2. Improvement in Harmonic Compensation for a Smart Charger

The authors propose a current controller in  $d$ - $q$  coordinates for the 3rd harmonic currents to improve harmonic compensation on the source side for the system in Figure 1. Figure 6 shows the proposed control circuit diagram for the SC of Figure 1. The part enclosed by the dotted line shows the proposed PI controllers in  $d$ - $q$  coordinates for the 3rd harmonic components. For example, feeder 1 in Figure 6 detects the output current  $i_1$ , and then the difference  $i_{e1}$  between the reference value  $i_1^*$  and the detected output current  $i_1$  is calculated. This  $i_{e1}$  corresponds to the  $\alpha$ -phase component. For the sake of simplicity, only the fundamental, 3rd, and 5th components are included in  $i_{e1}$ :

$$i_{e1} = \sqrt{2}I_F \cos(\omega_S t - \phi_F) + \sqrt{2}I_3 \cos(3\omega_S t - \phi_3) + \sqrt{2}I_5 \cos(5\omega_S t - \phi_5). \quad (10)$$

Then,  $i_{e1}$  is delayed by  $T_S/12$ , where  $T_S/12$  equals  $\pi/2$  for the 3rd harmonic components in the electric angle. Delaying  $i_{e1}$  by  $T_S/12$  is an original concept to construct the current controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents. The delayed component  $i_{e31\beta}$  is given by:

$$\begin{aligned}
 i_{e31\beta} &= \sqrt{2}I_F \cos(\omega_S t - \phi_F - \frac{\pi}{6}) + \sqrt{2}I_3 \cos(3\omega_S t - \phi_3 - \frac{\pi}{2}) + \sqrt{2}I_5 \cos(5\omega_S t - \phi_5 - \frac{5\pi}{6}) \\
 &= \sqrt{2}I_F \cos(\omega_S t - \phi_F - \frac{\pi}{6}) + \sqrt{2}I_3 \sin(3\omega_S t - \phi_3) + \sqrt{2}I_5 \cos(5\omega_S t - \phi_5 - \frac{5\pi}{6}).
 \end{aligned}
 \quad (11)$$

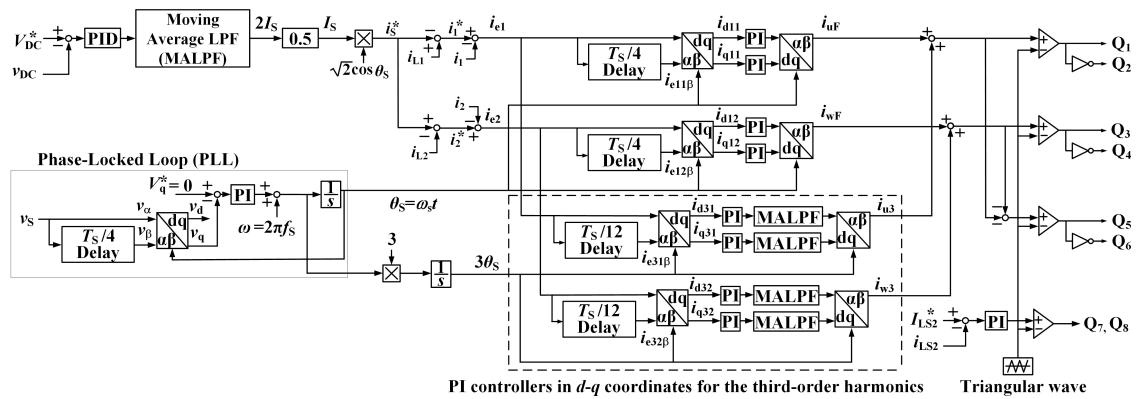


Figure 6. Proposed control circuit diagram for the SC of Figure 1.

With the angular frequency  $3\omega_S$  for the 3rd harmonic component,  $i_{d31}$  and  $i_{q31}$  in  $d$ - $q$  coordinates are generally expressed as:

$$\begin{pmatrix} i_{d31} \\ i_{q31} \end{pmatrix} = \begin{pmatrix} \cos 3\omega_S & \sin 3\omega_S \\ -\sin 3\omega_S & \cos 3\omega_S \end{pmatrix} \begin{pmatrix} i_{e1} \\ i_{31\beta} \end{pmatrix}. \quad (12)$$

Substituting  $i_{e1}$  in Equation (10) and  $i_{e31\beta}$  in Equation (11) into Equation (12) gives:

$$\begin{aligned}
 i_{d31} &= \frac{\sqrt{2}}{2}I_F \left\{ \cos(4\omega_S t - \phi_F) + \cos(2\omega_S t + \phi_F) \right. \\
 &\quad \left. + \sin(4\omega_S t - \phi_F - \frac{\pi}{6}) + \sin(2\omega_S t + \phi_F + \frac{\pi}{6}) \right\} \\
 &\quad + \sqrt{2}I_3 \cos \phi_3 \\
 &\quad + \frac{\sqrt{2}}{2}I_5 \left\{ \cos(8\omega_S t - \phi_5) + \cos(2\omega_S t - \phi_5) \right. \\
 &\quad \left. + \sin(8\omega_S t - \phi_5 - \frac{5\pi}{6}) + \sin(2\omega_S t - \phi_5 - \frac{5\pi}{6}) \right\}, \\
 i_{q31} &= \frac{\sqrt{2}}{2}I_F \left\{ \cos(4\omega_S t - \phi_F - \frac{\pi}{6}) + \cos(2\omega_S t + \phi_F + \frac{\pi}{6}) \right. \\
 &\quad \left. - \sin(4\omega_S t - \phi_F) - \sin(2\omega_S t + \phi_F) \right\} \\
 &\quad - \sqrt{2}I_3 \sin \phi_3 \\
 &\quad + \frac{\sqrt{2}}{2}I_5 \left\{ \cos(8\omega_S t - \phi_5 - \frac{5\pi}{6}) + \cos(2\omega_S t - \phi_5 - \frac{5\pi}{6}) \right. \\
 &\quad \left. - \sin(8\omega_S t - \phi_5) + \sin(2\omega_S t - \phi_5) \right\}.
 \end{aligned}
 \quad (13)$$

MALPFs are used to extract the dc component in  $d$ - $q$  coordinates. The dc components  $\bar{i}_{d31}$  and  $\bar{i}_{q31}$  in Equation (13) are given by:

$$\begin{aligned}
 \bar{i}_{d31} &= +\sqrt{2}I_3 \cos \phi_3, \\
 \bar{i}_{q31} &= -\sqrt{2}I_3 \sin \phi_3.
 \end{aligned}
 \quad (14)$$

As described before,  $i_{e31\beta}$  is calculated with the delay time of  $T_S/12$ . Hence, the dc components in Equation (14) originate from the 3rd harmonic components in Equations (10) and (11). A current



controller in  $d$ - $q$  coordinates for the 3rd harmonic currents can be constructed to improve the harmonic compensations performance of the source-side currents in Figure 1. This current controller for the 3rd harmonic currents suppresses the 3rd harmonic of the source currents.

In the literature [2], the switching frequency  $f_s$  of the three-leg PWM rectifier was 12 kHz. Thus, the number of sampled data points over a cycle  $T_s$  of the fundamental frequency is 200 since the frequency of the source voltage  $v_s$  is 60 Hz. The number of data points for the quarter cycle was 50 for the fundamental component. Therefore, synchronization of the  $T_s/4$  delay block was achieved to the source voltage  $v_s$ . However, for the 3rd harmonic components, the number of data points for the quarter cycle was 16.67. This means that it is impossible to construct PI controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents. In this paper, therefore, a switching frequency  $f_s$  of 9.36 kHz was employed. The number of the sampled data over a cycle of the fundamental frequency is then 156 points. The number of data points for the quarter cycle of the fundamental component is 39. Therefore, the quarter cycle delay block is synchronized to the source voltage  $v_s$ . The number of data points for the quarter cycle of the 3rd harmonic components is 13. In this manner, synchronization of the quarter cycle delay block for the 3rd harmonic components to the source voltage  $v_s$  is achieved. The current controllers in  $d$ - $q$  coordinates for the 3rd harmonic components are achieved, in addition to the current controllers in  $d$ - $q$  coordinates for the fundamental component. Adding the current controllers for the 3rd harmonic components improves the harmonic compensation performance on the source side in Figure 1.

### 3. Simulation Results

The validity and high practicality of the proposed PI controllers in  $d$ - $q$  coordinates for the 3rd harmonic components of the currents in the proposed SC are confirmed by computer simulation using the PSIM software. In the following simulation results, the constants shown in Table 1 are used. The unbalanced ratio between feeders 1 and 2 in SPTWDF is defined as:

$$\text{Unbalanced ratio} = \frac{S_1 - S_2}{S_A \times 0.5} \times 100 \quad [\%], \quad (15)$$

where  $S_1$  is the apparent power of load 1 in feeder 1, and  $S_2$  is the apparent power of load 2 in feeder 2.  $S_A$  is the sum of  $S_1$  and  $S_2$ . According to Japanese guidelines, the unbalanced ratio should be less than 40% [12]. Therefore, load conditions in feeders 1 and 2 were decided as shown in Figure 1. Table 1 shows the circuit constants, which are used in the following simulation and experimental results. Additionally, in the simulation and experiments:

- $K_P = 0.6$ ,  $T_I = 0.03$  s, and  $T_D = 0.01$  ms are used in the PID controller of the CDCVC;
- $K_P = 0.06$  and  $T_I = 8$  ms are used in the PI controllers in  $d$ - $q$  coordinates for both fundamental and the 3rd harmonic components of the currents; and
- $K_P = 0.15$  and  $T_I = 3$  ms are used in the PI controller for the current feedback of the bidirectional dc-dc converter.

The Ziegler–Nichols ultimate sensitivity method was used to initially decide these parameters, and they were improved by the computer simulation.

Figure 7 shows the simulation results when the SC charges power to the battery with constant battery current control, for the proposed control strategy of Figure 6. The source currents  $i_{s1}$  and  $i_{s2}$  are balanced with unity PF even though the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted. The THD values of  $i_{s1}$ ,  $i_{s2}$ ,  $i_{L1}$ , and  $i_{L2}$  are 2.00%, 1.81%, 26.3%, and 23.6%, respectively. In Reference [2], without the current controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents, the THD values of  $i_{s1}$  and  $i_{s2}$  were 3.92% and 2.50%, respectively. The addition of the current controllers for the 3rd harmonic currents reduces the THD values of  $i_{s1}$  and  $i_{s2}$  by 1.92% and 0.69%, respectively.



**Table 1.** Circuit Constants for following simulation and experimental results.

Item	Symbol	Value	
		Simulation	Experiment
Filter inductor for three-leg PWM rectifier	$L_{f1}$	0.46 mH	
Filter capacitor for three-leg PWM rectifier	$C_{f1}$	10.4 $\mu$ F	
Switching inductor for three-leg PWM rectifier	$L_{S1}$	1.0 mH	
dc capacitor	$C_{DC}$	2700 $\mu$ F	
dc-capacitor voltage	$V_{DC}^*$	385 Vdc	360 Vdc
Switching inductor for dc-dc converter	$L_{S2}$	4.4 mH	
Filter capacitor for dc-dc converter	$C_{f2}$	1000 $\mu$ F	
Battery voltage	$V_{bat}$	360 Vdc	257 Vdc
Inductor current for dc-dc converter	$I_{LS2}^*$	5 Adc	4.29 Adc
Internal resistance of battery	$r$	72 m $\Omega$	
Switching frequency	$f_{SW}$	9.36 kHz	
Dead time	$T_d$	3.5 $\mu$ s	

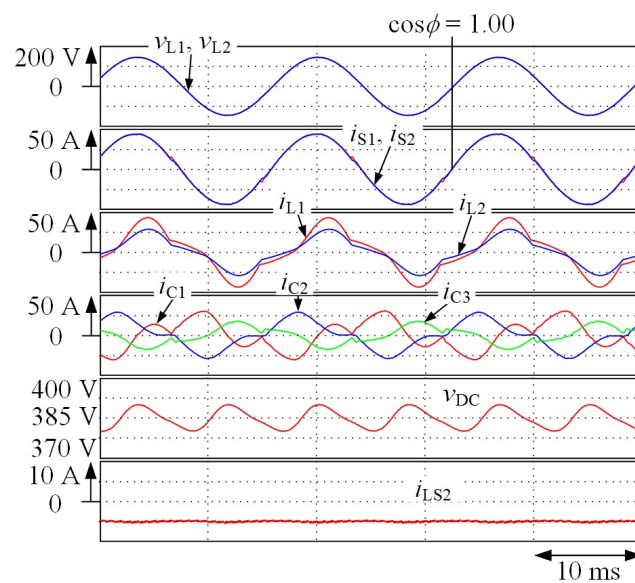
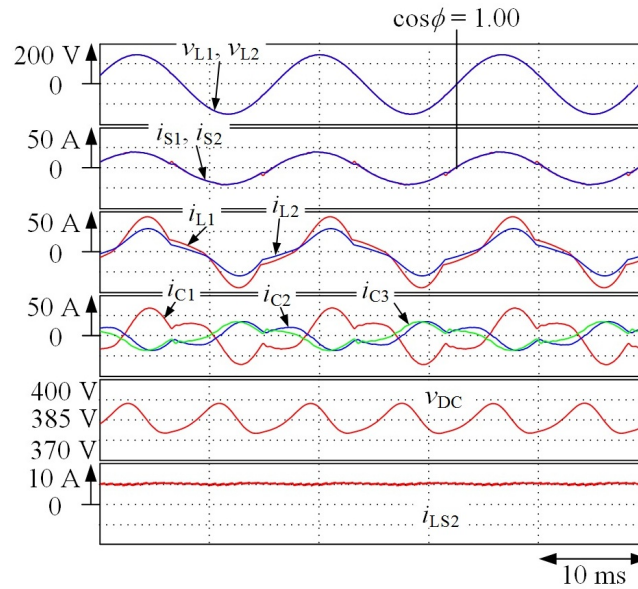
**Figure 7.** Simulation results for the SC in Figure 1 during a battery charging operation.

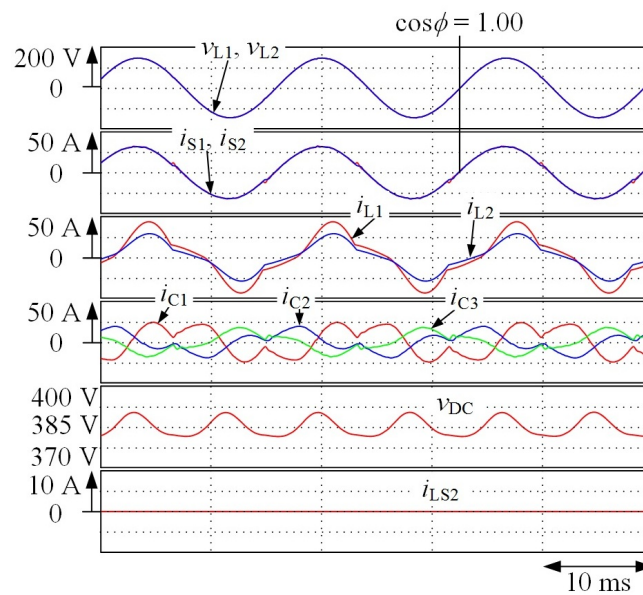
Figure 8 shows the simulation results when the SC discharges the power from the battery with constant battery current control. The source currents  $i_{S1}$  and  $i_{S2}$  are balanced with a unity PF even though the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted. The THD values of  $i_{S1}$  and  $i_{S2}$  are 4.93% and 3.73%, respectively. In Reference [2], without the controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents, the THD values of  $i_{S1}$  and  $i_{S2}$  were 10.8% and 7.7%, respectively. The addition of these current controllers in reduces the THD values of  $i_{S1}$  and  $i_{S2}$  by 5.77% and 2.66%, respectively.

Figure 9 shows the simulation results when the battery  $v_{bat}$  is not connected. The bidirectional dc-dc converter consisting of  $Q_7$  and  $Q_8$  is not under operation. Therefore, the SC performs as an active power-line conditioner for a domestic consumer. Balanced and sinusoidal source currents  $i_{S1}$  and  $i_{S2}$  are attained. The THD values of  $i_{S1}$  and  $i_{S2}$  are 2.97% and 2.30%, respectively. In Reference [2], without the controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents, the THD values of  $i_{S1}$  and  $i_{S2}$

were 5.51% and 2.94%, respectively. Adding of the current controllers for the 3rd harmonic currents reduces the THD values of  $i_{S1}$  and  $i_{S2}$  by 2.54% and 0.64%, respectively. The THD values of  $i_{S1}$  and  $i_{S2}$  in Figures 7–9 satisfy the regulations [13].



**Figure 8.** Simulation results during a battery discharging operation for the SC in Figure 1.

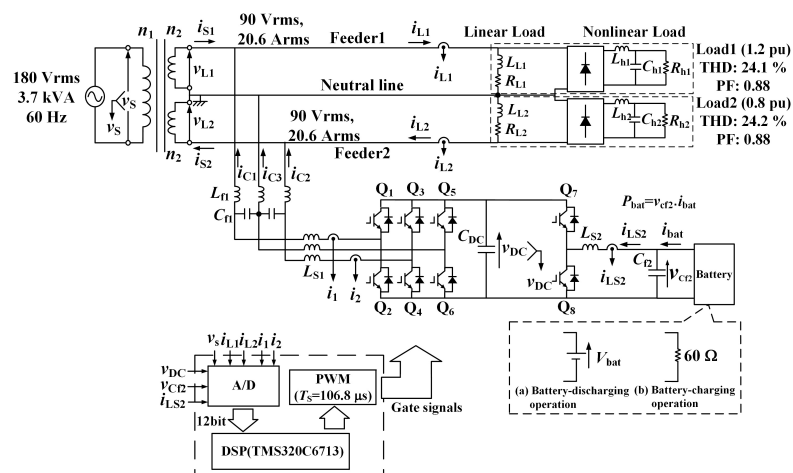


**Figure 9.** Simulation results for the SC in Figure 1 without the battery connected; when the SC performs as an active power-line conditioner.

#### 4. Experimental Results

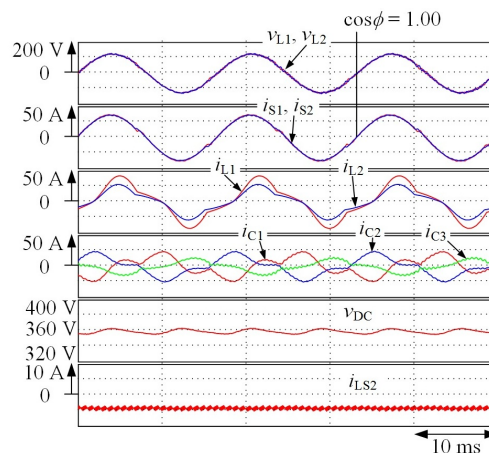
It is difficult to construct an experimental setup for the SC of Figure 1 because of the high-voltage rating on the primary side of the PMDT. A reduced-scale experimental model was, therefore, constructed and tested to show the validity and high applicability of the proposed CDCVC strategy for the SC. Figure 10 shows a block diagram of the constructed reduced-scale prototype experimental setup. The unbalanced ratio in feeders 1 and 2 is 40%. As shown in Figure 10a, a resistor  $R$  of 60  $\Omega$

is connected in parallel to a capacitor  $C_{f2}$  under the battery charging operation of the bidirectional dc-dc converter. The charged power, which is from the utility grid, is consumed by the resistor  $R$ . A dc power supply (Takasago: HX0300-25) is connected to  $C_{f2}$  during the battery discharging operation as shown in Figure 10b. The battery voltage  $V_{\text{bat}}$  is 257 Vdc. The detected voltages and currents  $v_s$ ,  $v_{\text{dc}}$ ,  $v_{Cf2}$ ,  $i_{L1}$ ,  $i_{L2}$ ,  $i_1$ ,  $i_2$ , and  $i_{LS2}$  are fed into a digital signal processor (DSP) (TMS320C6713, 225 MHz) through 12-bit A/D converters. The sampling time  $T_s$  is 0.107 ms. The reference values  $i_1^*$ ,  $i_2^*$ , and  $i_3^*$  for the source currents  $i_s^*$ ,  $i_{s1}^*$ , and  $i_{s2}^*$  are calculated by Equation (9). With the DSP, the dc-capacitor voltage  $v_{\text{dc}}$  is controlled. The output currents  $i_{C1}$ ,  $i_{C2}$ , and  $i_{C3}$  of the SC, formed by the three-leg PWM rectifier, are controlled with current feedback control in  $d$ - $q$  coordinates for both the fundamental and 3rd harmonic components. The output current  $i_{LS2}$  of the bidirectional dc-dc converter is also controlled by the DSP. The circuit constants shown in Table 1 are used in the following experimental results.



**Figure 10.** Block diagram of the constructed experimental model for the SC in Figure 1.

Figure 11 shows the experimental results when the SC discharges the power from the battery with constant battery current control, for the SC model of Figure 10 with the proposed control strategy of Figure 6. The source currents  $i_{s1}$  and  $i_{s2}$  are balanced with a unity PF even though the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted. The THD values of  $i_{s1}$ ,  $i_{s2}$ ,  $i_{L1}$ , and  $i_{L2}$  are 4.44%, 3.05%, 24.1%, and 24.2%, respectively. In Reference [2], without current controllers for the 3rd harmonic currents, the THD values of  $i_{s1}$  and  $i_{s2}$  were 7.49% and 5.13%, respectively. The addition of the current controllers for the 3rd harmonic currents reduces the THD values of  $i_{s1}$  and  $i_{s2}$  by 3.05% and 2.08%, respectively.



**Figure 11.** Experimental results during battery charging for the SC in Figure 10.

Figure 12 shows the experimental results, when the SC discharges power from the battery with constant battery current control. The source currents  $i_{S1}$  and  $i_{S2}$  are balanced with unity PF, even though the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted. The THD values of  $i_{S1}$  and  $i_{S2}$  are 8.60% and 6.60%, respectively. In Reference [2], without the current controllers for the 3rd harmonic currents, the THD values of  $i_{S1}$  and  $i_{S2}$  were 17.0% and 10.2%, respectively. The THD values of  $i_{S1}$  and  $i_{S2}$  are improved by 8.40% and 3.60%, respectively, with the controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents.

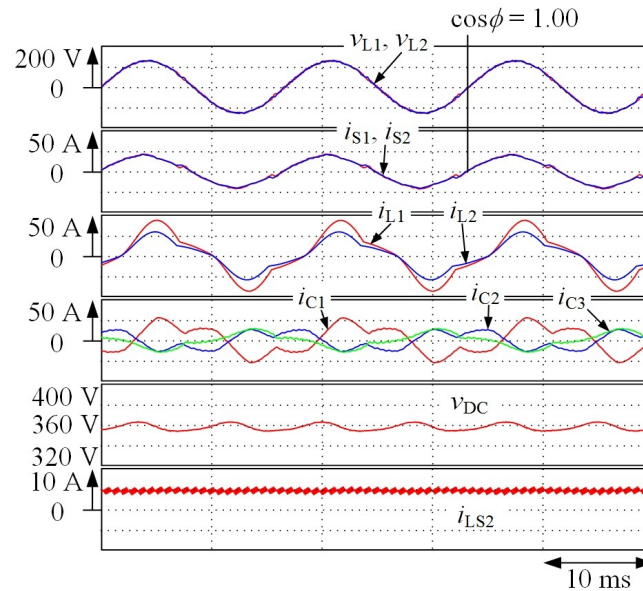


Figure 12. Experimental results during battery discharging for the SC in Figure 10.

Figure 13 shows the experimental results, when the battery  $v_{bat}$  is not connected. The source currents  $i_{S1}$  and  $i_{S2}$  are balanced with unity PF, even though the load currents  $i_{L1}$  and  $i_{L2}$  are unbalanced and distorted. The THD values of  $i_{S1}$  and  $i_{S2}$  are 6.00% and 4.24%, respectively. In Reference [2], without the current controllers for the 3rd harmonic currents, the THD values of  $i_{S1}$  and  $i_{S2}$  were 9.83% and 5.58%, respectively. The THD values of  $i_{S1}$  and  $i_{S2}$  are improved by 3.83% and 1.34%, respectively.

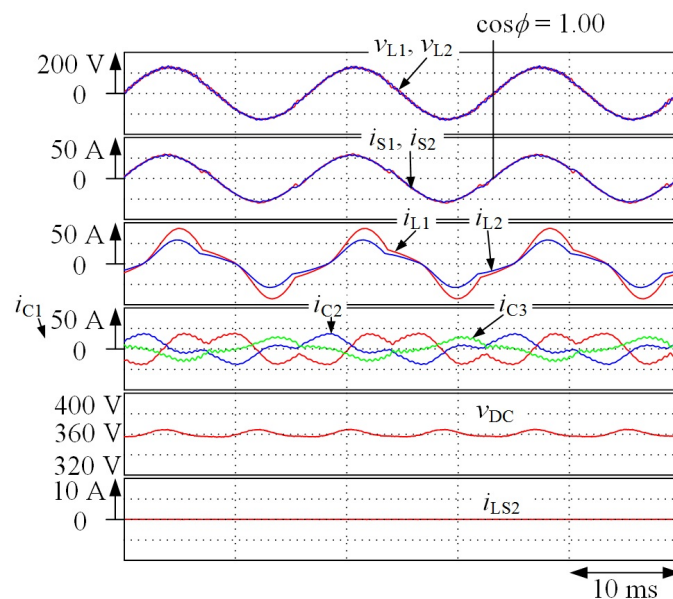


Figure 13. Experimental results for the SC in Figure 10 without the battery connected.

The THD values of  $i_{s1}$  and  $i_{s2}$  in Figures 11–13 satisfy the regulations [13]. The experimental results of Figures 11–13 agree well with the simulation results of Figures 7–9. The authors conclude that the addition of the PI controllers in  $d$ - $q$  coordinates for the 3rd harmonic currents reduces the THD values of  $i_{s1}$  and  $i_{s2}$ .

## 5. Conclusions

This paper has introduced an improvement in the harmonic compensation performance of the previously proposed SC with a CDCVC strategy for EVs in SPTWDFs. A controller for the 3rd harmonic currents in  $d$ - $q$  coordinates is added to the current controller for the fundamental component in  $d$ - $q$  coordinates of the previously proposed control strategy for the SC. Adding the controller for the 3rd harmonic currents improves the harmonic compensation performance on the source side. Harmonic current compensation with the previously proposed CDCVC strategy for SC has been briefly introduced. Then, the basic principles of the proposed controller for the 3rd harmonic currents in  $d$ - $q$  coordinates have been discussed in detail. It has been shown that synchronization of the current controllers in  $d$ - $q$  coordinates for both the fundamental and 3rd harmonic components is required. The switching frequency of a three-leg PWM rectifier with a bidirectional dc-dc converter has been determined based on the synchronization of the current controllers. Simulation and experimental results have demonstrated that balanced and sinusoidal source currents with unity PF are obtained both during battery charging and discharging operations in EVs, thus improving the harmonic compensation performance of the SC compared to the previously proposed scheme. Experimental results also have demonstrated that the THD values of the source currents are improved by 8.4% and 3.6% with the proposed current controller for 3rd harmonic currents in  $d$ - $q$  coordinates, when the SC is under the battery discharging, for example.

**Author Contributions:** K.N. significantly contributed to demonstrate the basic principle of the constant dc-capacitor voltage-control-based strategy and contributed to demonstrate the validity and practicability of the proposed control strategy by the reduced-scale experimental setup. F.I. also significantly contributed to implement the digital computer simulation and helped with the writing of this paper. Y.O. contributed to help the construction on the reduced-scale experimental setup. T.T. proposed the control strategy and helped with the writing of this paper. H.Y. and M.O. were responsible for guidance and key suggestions.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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