energies

MDPI

Article

Research on the Neutral-Point Voltage Balance for NPC Three-Level Inverters under Non-Ideal Grid Conditions

Jian Guo Lyu [1,2,*], Ji Dong Wang [1], Wen Bin Hu [1] and Zhao Feng Wu [1]

[1] Nanjing University of Science and Technology, Nanjing 210094, China; wangjidong_5058@163.com (J.D.W.); hwb_njust@163.com (W.B.H.); wuzhaofeng@njust.edu.cn (Z.F.W.)
[2] Jiangsu Collaborative Innovation Center for Smart Distribution Network, Nanjing 211167, China
* Correspondence: jianguolyu@njust.edu.cn; Tel.: +86-025-8431-5415

Received: 8 April 2018; Accepted: 19 May 2018; Published: 23 May 2018



Abstract: In order to solve the neutral-point voltage unbalancing problem for neutral-point clamped (NPC) three-level inverters under non-ideal grid conditions, a novel zero-sequence component injection method for modulation signals was proposed in this paper. Based on the mathematical expressions of neutral-point voltage unbalancing, the fluctuation of the neutral-point voltage under different grid conditions was studied. The proposed method dynamically calculates the zero-sequence component for modulation signals by region selections based on sinusoidal pulse width modulation (DCR-SPWM). Under non-ideal grid conditions, this DCR-SPWM method can control the neutral-point voltage balance for NPC three-level inverters with different grid and output power conditions, and improves the grid current quality. The simulation results verified the correctness of the theoretical analysis in this paper, and the feasibility and effectiveness of this method were verified by the experiments in the experimental platform of the NPC three-level grid-connected inverter based on DSP-CPLD controllers.

Keywords: non-ideal grid; three-level inverters; neutral-point voltage balance; modulation signals; region selection

1. Introduction

The neutral-point clamped (NPC) three-level inverter has been widely used in medium or high voltage and high power conversions, especially as a dc/ac converter for a photovoltaic (PV) power generation system [1,2], which influences the safety and stability of the PV system for grid connection. Compared with two level inverters, the NPC three-level inverter has lower voltage stress on power devices, lower electromagnetic noise, and lower total harmonic distortion (THD) [3,4], which is shown in Figure 1.

In the NPC three-level inverter circuit, two capacitors for the dc bus are used in series to clamp the neutral-point (NP) potential. Ideally, the voltage of the two capacitors are both half of the dc bus voltage. However, due to the capacitance parameter error, the inconsistent characteristics of the switching devices, the unbalancing of three phase operation, etc. [5], the NP voltage unbalancing problem appears, which will increase the voltage stress on switching devices [6,7], and lead low-order harmonic currents into the grid [8]. Therefore, the NP voltage balance has been the research emphasis of three-level inverters.

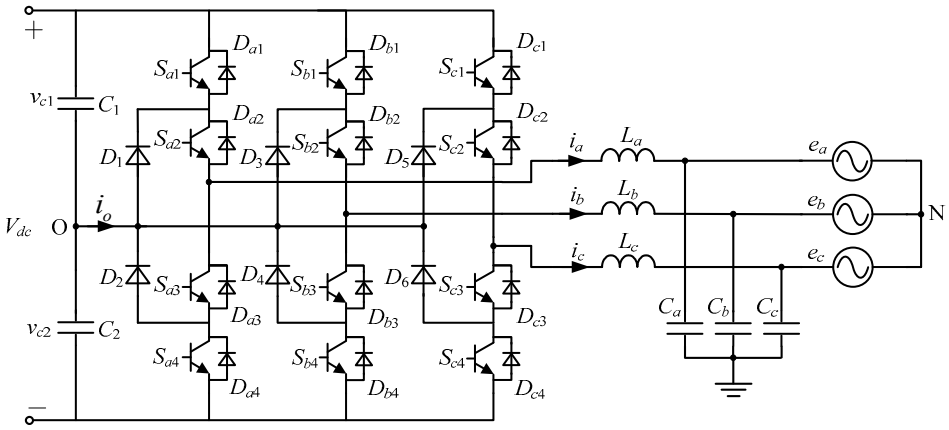


Figure 1. Main circuit of the NPC three-level grid-connected inverter.

Most of the research has focused on the NP voltage unbalancing problem under symmetrical load or ideal grid conditions. Based on space vector pulse width modulation (SVPWM), ref. [9] proposed a control strategy that replaced the small switching states with other switching states. Using sinusoidal pulse width modulation (SPWM), ref. [10] proposed a closed-loop space vector modulation using converter redundant switching states combined to the controller to balance the neutral point, and the dc link had very low voltage ripples due to lower harmonic components flowing through those capacitors via the harmonic current. In [11], a proportional integral (PI) controller was used to modify the reference current to maintain the NP voltage balance. NP balance methods based on zero-sequence component injection were proposed in [12,13], which calculated the zero-sequence component in the switching period. Based on the average NP voltage model in a line cycle, the PI controllers were proposed for the NP voltage balance in some papers, and the PI parameters for the controllers were usually selected for the maximum output power condition [14,15].

However, due to the nonlinear loads and transient grid faults, the three phase grid can become unbalanced and distorted [16–18]. Under the non-ideal conditions described above, the NP voltage module is different from that under ideal grid conditions, and the NP voltage unbalancing problem leads more low order harmonic currents into the grid [19,20], which significantly deteriorates the performance of the inverter. Therefore, as NP voltage balance methods designed under ideal grid conditions are not suitable for non-ideal grid conditions, it is important to research balancing the NP voltage under non-ideal grid conditions. Recently, some studies have focused on this problem. In [21,22], the redundant switching state was dictated based on the voltage feedback from the dc link to balance the NP voltage, which can balance the NP voltage under various load conditions with fast response and good dynamic performance. In [23,24], the expressions of NP voltage under unbalanced grid conditions were derived, and the relationship between the ripple of NP voltage and the unbalanced grid was studied. The authors in [20] analyzed the form and spectrums of NP voltage under low-voltage ride-through (LVRT) conditions, and proposed an optimized SVPWM method to control the NP voltage balance. In [25,26], the dc/dc converter was added to balance the NP voltage and suppress the common mode voltage under unbalanced grid conditions.

The objective of this paper was to propose a new method to control the NP voltage balance under non-ideal grid conditions. This method dynamically calculates the zero-sequence component for modulation signals by region selections based on SPWM (DCR-SPWM). Section 2 studies the NP voltage under different grid conditions and presents the expressions of NP voltage under non-ideal grid conditions. In Section 3, the DCR-SPWM method for non-ideal grid is proposed. Based on the mathematical expressions of NP voltage, the modulation signals are divided in different regions, and the expressions of zero-sequence component are derived, which is added to the modulation signals. Section 4 analyzes the NP voltage ripple and the harmonic performance of the grid currents with the

DCR-SPWM method and compared it with the traditional SPWM method under different grid and output power conditions. Section 5 presents the simulated and experimental results of the proposed DCR-SPWM method and the method in [14] under different grid and output power conditions. The analysis and experiments showed that the DCR-SPWM method could control the NP voltage balance for NPC three-level inverters under non-ideal grid conditions, and improved the grid current quality.

2. Mathematical Analysis of the Neutral-Point Voltage under Non-Ideal Grid Conditions

In Figure 1, v_{c1} is the voltage of capacitor C_1, v_{c2} is the voltage of capacitor C_2, and V_{dc} is the dc bus voltage. Supposing that v_{c1} and v_{c2} are equal, each phase leg of the NPC three-level inverter can output three levels ($V_{dc}/2$, $-V_{dc}/2$, 0), and the "P", "N", and "0" states represent $V_{dc}/2$, $-V_{dc}/2$, and 0, respectively.

In this paper, the SPWM method uses the single polar SPWM strategy, which is shown in Figure 2 where u_x is the modulation signal of phase x ($x = a, b, c$) and v_x is the leg voltage of phase x ($x = a, b, c$).

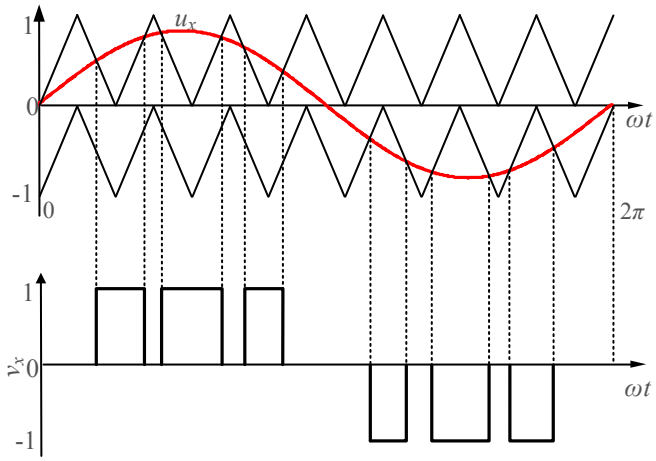


Figure 2. Single polar SPWM method for NPC three-level inverters.

The NP current i_o can be defined as the average current in a switching cycle, which flows out from the neutral point O in Figure 1, it can be expressed as:

$$i_o = \sum_{x=a,b,c} d_{x0} i_x \tag{1}$$

where d_{x0} and i_x represent the duty cycle of "0" state and the three phase grid current, d_{x0} can be derived as:

$$\begin{cases} d_{a0} = 1 - \left| u_{a_ref} \right| \\ d_{b0} = 1 - \left| u_{b_ref} \right| \\ d_{c0} = 1 - \left| u_{c_ref} \right| \end{cases} \tag{2}$$

where u_{a_ref}, u_{b_ref}, u_{c_ref} are three phase modulation signals. By substituting Equation (2) into Equation (1), i_o can be derived as:

$$i_o = -\sum_{x=a,b,c} \left| u_{x_ref} \right| i_x \tag{3}$$

Defining v_c as the difference between v_{c1} and v_{c2} in Figure 1, v_c is expressed as:

$$v_c = v_{c1} - v_{c2} \tag{4}$$

Meanwhile, the NP voltage v_c can be expressed as:

$$v_c = \frac{1}{C}\int i_o dt \tag{5}$$

where C is the capacitance of C_1 and C_2.

Substituting Equation (3) into Equation (5), v_c can be derived as:

$$v_c = -\frac{1}{C}\int (\sum_{x=a,b,c} \left|u_{x_ref}\right| i_x) dt \tag{6}$$

Under the non-ideal grid condition, according to the symmetrical components method, three phase unbalance components are composed with symmetrical positive/negative/zero-sequence components. As the zero-sequence component can be neglected in the Three-phase Three-wire inverter system, therefore, the modulation signals can be expressed as:

$$\begin{cases} u_{a_ref} = u_{ap_ref} + u_{an_ref} \\ u_{b_ref} = u_{bp_ref} + u_{bn_ref} \\ u_{c_ref} = u_{cp_ref} + u_{cn_ref} \end{cases} \tag{7}$$

where u_{ap_ref}, u_{bp_ref}, u_{cp_ref} represent the positive-sequence components of three phase modulation signals and u_{an_ref}, u_{bn_ref}, u_{cn_ref} represent the negative-sequence components of three phase modulation signals.

Commonly, to describe the proportion of negative-sequence component to the positive-sequence component for the non-ideal grid, the unbalance factor λ is introduced here [27]:

$$\lambda = \frac{A_n}{A_p} \tag{8}$$

where A_p and A_n represent the amplitudes of positive and negative sequence components, respectively.

Supposing that the voltage of the filter inductor is ignored, the positive-sequence and negative-sequence components of three phase modulation signals can be expressed as:

$$\begin{cases} u_{ap_ref} = \frac{2E_{mp}}{V_{dc}} \sin(\omega t + \varphi_{up}) \\ u_{bp_ref} = \frac{2E_{mp}}{V_{dc}} \sin(\omega t + \varphi_{up} - 2\pi/3) \\ u_{cp_ref} = \frac{2E_{mp}}{V_{dc}} \sin(\omega t + \varphi_{up} + 2\pi/3) \end{cases} \tag{9}$$

$$\begin{cases} u_{an_ref} = \lambda\frac{2E_{mp}}{V_{dc}} \sin(\omega t + \varphi_{un}) \\ u_{bn_ref} = \lambda\frac{2E_{mp}}{V_{dc}} \sin(\omega t + \varphi_{un} + 2\pi/3) \\ u_{cn_ref} = \lambda\frac{2E_{mp}}{V_{dc}} \sin(\omega t + \varphi_{un} - 2\pi/3) \end{cases} \tag{10}$$

In Equations (9) and (10), E_{mp} represents the amplitude of the positive-sequence grid voltages; ω is the line angle frequency; and φ_{up} and φ_{un} represent the phase angle of positive-sequence and negative-sequence modulation signals, respectively, which also represent the phase angle of positive-sequence and negative-sequence grid voltages, respectively.

Under non-ideal grid conditions, unbalance grid voltages cause a double line frequency ripple at the output power of the inverter [28]. If the control target of the grid side is suppressing the ripple component at active power, the three phase grid currents can be expressed as:

$$\begin{cases} i_a = i_{ap} + i_{an} \\ i_b = i_{bp} + i_{bn} \\ i_c = i_{cp} + i_{cn} \end{cases} \tag{11}$$

where i_{ap}, i_{bp}, i_{cp} represent the positive-sequence components of three phase grid currents and i_{an}, i_{bn}, i_{cn} represent the negative-sequence components of three phase grid currents.

In Equation (11), the positive-sequence and negative-sequence components of three phase grid currents are as follows:

$$\begin{cases} i_{ap} = I_{mp}\sin(\omega t + \varphi_{up} - \varphi_{ui}) \\ i_{bp} = I_{mp}\sin(\omega t + \varphi_{up} - \varphi_{ui} - 2\pi/3) \\ i_{cp} = I_{mp}\sin(\omega t + \varphi_{up} - \varphi_{ui} + 2\pi/3) \end{cases} \tag{12}$$

$$\begin{cases} i_{an} = -\lambda I_{mp}\sin(\omega t + \varphi_{un} - \varphi_{ui}) \\ i_{bn} = -\lambda I_{mp}\sin(\omega t + \varphi_{un} - \varphi_{ui} + 2\pi/3) \\ i_{cn} = -\lambda I_{mp}\sin(\omega t + \varphi_{un} - \varphi_{ui} - 2\pi/3) \end{cases} \tag{13}$$

In Equations (12) and (13), I_{mp} represents the amplitude of the positive-sequence grid currents, and φ_{ui} is the phase difference between positive-sequence grid voltage and positive-sequence grid current.

Substituting Equations (7) and (11) into Equation (6), v_c can be derived as:

$$v_c = -\frac{1}{C}\int [\sum_{x=a,b,c} \left| u_{xp_ref} + u_{xn_ref} \right| (i_{xp} + i_{xn})]dt \tag{14}$$

By substituting Equations (9), (10), (12), and (13) into Equation (14), the waveforms of v_c under different grid conditions are shown in Figure 3, where C and I_{mp} are normalized.

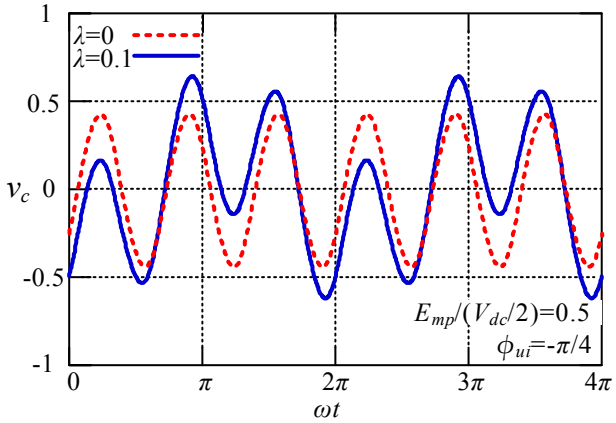


Figure 3. The waveforms of v_c under different grid conditions.

Under ideal grid condition (λ = 0) in Figure 3, it can be seen that v_c fluctuates at three times the line frequency. Under non-ideal grid conditions, when λ = 0.1, the fluctuating frequency of v_c changes to the line frequency, and the ripple of v_c is also larger than that under ideal grid conditions.

3. Proposed NP Voltage Balance Method under Non-Ideal Grid Conditions

In Section 2, from Equation (14), it can be seen that the fluctuation of NP voltage is caused by the NP current i_o. Therefore, by adding the appropriate zero-sequence component into the modulation signals, i_o can be controlled, then the NP voltage balance can be achieved.

3.1. Analysis of Zero-Sequence Component for Modulation Signals

Defining u_0 as the zero-sequence component, which is added to the modulation signals, three phase modulation signals can be expressed as:

$$\begin{cases} u'_{a_ref} = u_{ap_ref} + u_{an_ref} + u_0 \\ u'_{b_ref} = u_{bp_ref} + u_{bn_ref} + u_0 \\ u'_{c_ref} = u_{cp_ref} + u_{cn_ref} + u_0 \end{cases} \tag{15}$$

By substituting Equations (11) and (15) into Equation (3), the expression of i_o is derived as:

$$i_o = -\sum_{x=a,b,c} \left[\left| u_{xp_ref} + u_{xn_ref} + u_0 \right| (i_{xp} + i_{xn}) \right] \tag{16}$$

Defining φ'_{ua0}, φ'_{ub0}, φ'_{uc0} as the positively sloped zero-crossing points s of u'_{a_ref}, u'_{b_ref}, u'_{c_ref}, respectively. Aiming at eliminating the ripple of NP voltage, i_o is controlled to be zero in Equation (16), when $\varphi'_{ua0} > 0$, u_0 can be expressed as:

$$u_0 = \begin{cases} -\frac{(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})-(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})+(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{(i_{ap}+i_{an})-(i_{bp}+i_{bn})+(i_{cp}+i_{cn})}, & \varphi'_{ua0} \le \omega t < \varphi'_{uc0} - \pi \\ -\frac{(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})-(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})-(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{(i_{ap}+i_{an})-(i_{bp}+i_{bn})-(i_{cp}+i_{cn})}, & \varphi'_{uc0} - \pi \le \omega t < \varphi'_{ub0} \\ -\frac{(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})+(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})-(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{(i_{ap}+i_{an})+(i_{bp}+i_{bn})-(i_{cp}+i_{cn})}, & \varphi'_{ub0} \le \omega t < \varphi'_{ua0} + \pi \\ -\frac{-(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})+(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})-(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{-(i_{ap}+i_{an})+(i_{bp}+i_{bn})-(i_{cp}+i_{cn})}, & \varphi'_{ua0} + \pi \le \omega t < \varphi'_{uc0} \\ -\frac{-(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})+(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})+(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{-(i_{ap}+i_{an})+(i_{bp}+i_{bn})+(i_{cp}+i_{cn})}, & \varphi'_{uc0} \le \omega t < \varphi'_{ub0} + \pi \\ -\frac{-(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})-(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})+(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{-(i_{ap}+i_{an})-(i_{bp}+i_{bn})+(i_{cp}+i_{cn})}, & \begin{matrix} \varphi'_{ub0} + \pi \le \omega t < 2\pi \\ 0 \le \omega t < \varphi'_{ua0} \end{matrix} \end{cases} \tag{17}$$

When $\varphi'_{ua0} < 0$, u_0 can be expressed as:

$$u_0 = \begin{cases} -\frac{(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})-(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})+(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{(i_{ap}+i_{an})-(i_{bp}+i_{bn})+(i_{cp}+i_{cn})}, & \begin{matrix} \varphi'_{ua0} + 2\pi \le \omega t < 2\pi \\ 0 \le \omega t < \varphi'_{uc0} - \pi \end{matrix} \\ -\frac{(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})-(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})-(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{(i_{ap}+i_{an})-(i_{bp}+i_{bn})-(i_{cp}+i_{cn})}, & \varphi'_{uc0} - \pi \le \omega t < \varphi'_{ub0} \\ -\frac{(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})+(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})-(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{(i_{ap}+i_{an})+(i_{bp}+i_{bn})-(i_{cp}+i_{cn})}, & \varphi'_{ub0} \le \omega t < \varphi'_{ua0} + \pi \\ -\frac{-(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})+(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})-(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{-(i_{ap}+i_{an})+(i_{bp}+i_{bn})-(i_{cp}+i_{cn})}, & \varphi'_{ua0} + \pi \le \omega t < \varphi'_{uc0} \\ -\frac{-(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})+(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})+(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{-(i_{ap}+i_{an})+(i_{bp}+i_{bn})+(i_{cp}+i_{cn})}, & \varphi'_{uc0} \le \omega t < \varphi'_{ub0} + \pi \\ -\frac{-(u_{ap_ref}+u_{an_ref})(i_{ap}+i_{an})-(u_{bp_ref}+u_{bn_ref})(i_{bp}+i_{bn})+(u_{cp_ref}+u_{cn_ref})(i_{cp}+i_{cn})}{-(i_{ap}+i_{an})-(i_{bp}+i_{bn})+(i_{cp}+i_{cn})}, & \varphi'_{ub0} + \pi \le \omega t < \varphi'_{ua0} + 2\pi \end{cases} \tag{18}$$

The positively sloped zero-crossing points φ'_{ua0}, φ'_{ub0}, φ'_{uc0} can be expressed as:

$$\varphi'_{ua0} = \frac{1}{2}\left[\arcsin\left(\frac{C_a}{\sqrt{A_a^2 + B_a^2}} \right) - \arctan\left(\frac{B_a}{A_a} \right) \right] \tag{19}$$

$$\varphi'_{ub0} = \frac{1}{2}\left[\arcsin\left(\frac{C_b}{\sqrt{A_b^2 + B_b^2}}\right) - \arctan\left(\frac{B_b}{A_b}\right)\right] \tag{20}$$

$$\varphi'_{uc0} = \frac{1}{2}\left[\arcsin\left(\frac{C_c}{\sqrt{A_c^2 + B_c^2}}\right) - \arctan\left(\frac{B_c}{A_c}\right)\right] \tag{21}$$

In Equations (19)–(21), the expressions of coefficients A_i, B_i, C_i, ($i = a, b, c$) are shown in Table 1.

Table 1. Expressions of A_i, B_i and C_i.

Coefficient	Expressions
A_a	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[\sqrt{3}\lambda^2\cos(\varphi_{ui}-2\varphi_{un})+\sqrt{3}\lambda\cos(\varphi_{ui}-\varphi_{un}-\varphi_{up})+\sqrt{3}\cos(\varphi_{ui}-2\varphi_{up})\right]$
B_a	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[-\sqrt{3}\lambda^2\sin(\varphi_{ui}-2\varphi_{un})-\sqrt{3}\lambda\sin(\varphi_{ui}-\varphi_{un}-\varphi_{up})-\sqrt{3}\sin(\varphi_{ui}-2\varphi_{up})\right]$
C_a	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[-\frac{\sqrt{3}}{2}(\lambda^2+1)\sin(\varphi_{ui})-2\sqrt{3}\lambda\sin(\varphi_{ui})\cos(\varphi_{un}-\varphi_{up})\right]$
A_b	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[-\sqrt{3}\lambda^2\sin(\varphi_{ui}-2\varphi_{un}+\frac{\pi}{6})+\sqrt{3}\lambda\cos(\varphi_{ui}-\varphi_{un}-\varphi_{up})+\sqrt{3}\sin(\varphi_{ui}-2\varphi_{up}-\frac{\pi}{6})\right]$
B_b	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[\sqrt{3}\lambda^2\sin(\varphi_{ui}-2\varphi_{un}-\frac{\pi}{3})-\sqrt{3}\lambda\sin(\varphi_{ui}-\varphi_{un}-\varphi_{up})+\sqrt{3}\sin(\varphi_{ui}-2\varphi_{up}+\frac{\pi}{3})\right]$
C_b	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[-\frac{\sqrt{3}}{2}(\lambda^2+1)\sin(\varphi_{ui})+2\sqrt{3}\lambda\sin(\varphi_{ui})\cos(\varphi_{un}-\varphi_{up}+\frac{\pi}{3})\right]$
A_c	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[\sqrt{3}\lambda^2\sin(\varphi_{ui}-2\varphi_{un}-\frac{\pi}{6})+\sqrt{3}\lambda\cos(\varphi_{ui}-\varphi_{un}-\varphi_{up})-\sqrt{3}\sin(\varphi_{ui}-2\varphi_{up}+\frac{\pi}{6})\right]$
B_c	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[\sqrt{3}\lambda^2\sin(\varphi_{ui}-2\varphi_{un}+\frac{\pi}{3})-\sqrt{3}\lambda\sin(\varphi_{ui}-\varphi_{un}-\varphi_{up})+\sqrt{3}\sin(\varphi_{ui}-2\varphi_{up}-\frac{\pi}{3})\right]$
C_c	$I_{mp}\frac{2E_{mp}}{V_{dc}}\left[-\frac{\sqrt{3}}{2}(\lambda^2+1)\sin(\varphi_{ui})+2\sqrt{3}\lambda\sin(\varphi_{ui})\cos(\varphi_{un}-\varphi_{up}-\frac{\pi}{3})\right]$

As shown in Figure 4, when $E_{mp}/(V_{dc}/2) = 0.5$, $\lambda = 0.1$, and $\varphi_{ui} = -\pi/4$, u_0 is calculated in different regions I–VI, which is divided by the zero-crossing points of u'_{x_ref} ($x = a, b, c$).

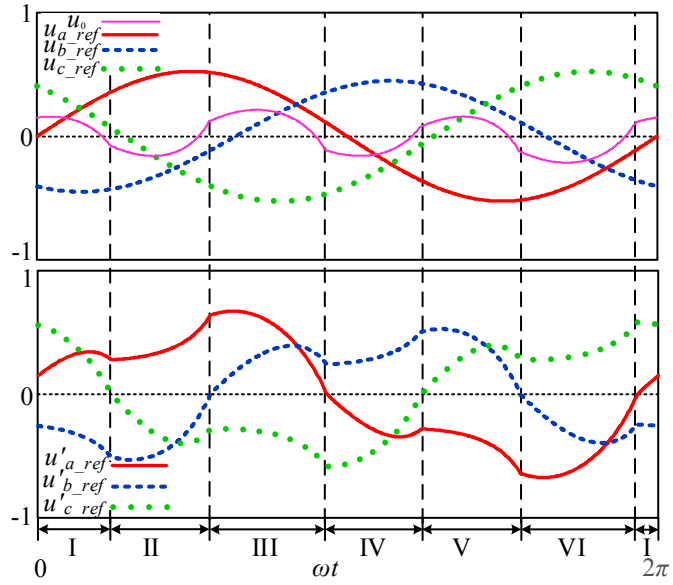


Figure 4. Three phase modulation signals with u_0 in different regions under the non-ideal grid condition.

3.2. Design of the NP Voltage Balance Controller

The control principle diagram of the NPC three-level grid-connected inverter under non-ideal grid conditions is shown in Figure 5, where the DDSRF-PLL represents the decoupling double synchronous reference frame phase-locked loop unit, and the DCR unit dynamically calculates the zero-sequence component for modulation signals by region selections (DCR).

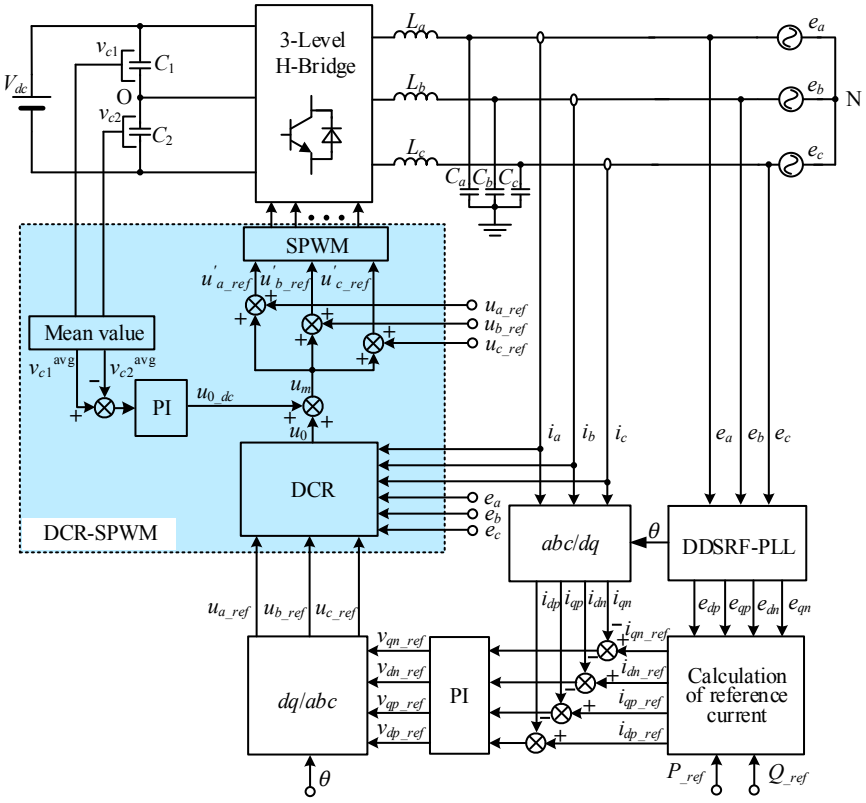


Figure 5. Control principle diagram of the NPC three-level grid-connected inverter.

In Figure 5, according to three phase modulation signals u_{a_ref}, u_{b_ref}, u_{c_ref}, three phase grid voltages e_a, e_b, e_c, grid currents i_a, i_b, i_c and average capacitor voltages ${v_{c1}}^{\mathrm{avg}}$, ${v_{c2}}^{\mathrm{avg}}$, the DCR-SPWM block generates the modified modulation signals with zero-sequence voltage u_m for balancing the NP voltage, where ${v_{c1}}^{\mathrm{avg}}$, ${v_{c2}}^{\mathrm{avg}}$ are the average voltage of v_{c1} and v_{c2} in a line cycle. Additionally, u'_{a_ref}, u'_{b_ref}, u'_{c_ref} are the modified modulation signals with u_m, which are compared with carrier waves to generate driving signals for the switches of the inverter.

Inside the DCR-SPWM block, the input signals u_{a_ref}, u_{b_ref}, u_{c_ref} of the DCR unit are modulation signals without zero-sequence voltage, i_a, i_b, i_c are three phase grid currents, e_a, e_b, e_c are three phase grid voltages, and the output signals u_0 of the DCR unit is the zero-sequence component for the modulation signals, which are used for suppressing the ripple of the NP voltage v_c.

In order to eliminate the ripple of the NP voltage v_c, the DCR unit dynamically calculates the zero-sequence component u_0 in different regions of the modulation signal, which is divided by the positively sloped zero-crossing points φ'_{ux0} of u'_{x_ref} ($x = a, b, c$), where φ'_{ux0} is calculated according to the grid currents and grid voltages at different grid conditions in a line cycle. The detailed flowchart of the DCR unit is shown in Figure 6. Furthermore, a PI controller is used to restrain the dc unbalanced voltage of v_c, and the input signals of the PI controller are ${v_{c1}}^{\mathrm{avg}}$, ${v_{c2}}^{\mathrm{avg}}$. The design of this controller for the NP voltage balance has been previously presented in many papers, so the detailed design is not given here. In order to make the difference between ${v_{c1}}^{\mathrm{avg}}$ and ${v_{c2}}^{\mathrm{avg}}$ zero, this controller outputs the

signal u_{0_dc}, which is added to the modulation signals. Therefore, u_m is the sum of u_{0_dc} and u_0, which is the zero-sequence voltage that is added to the modulation signals to balance the NP voltage.

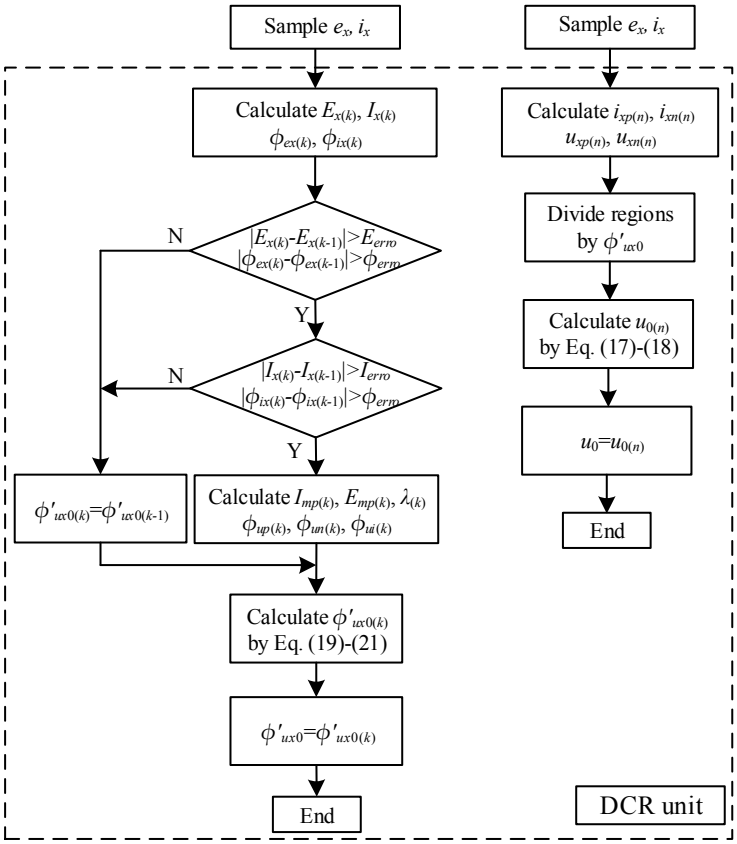


Figure 6. The flowchart of the DCR unit.

Figure 6 shows the main working flowchart of the DCR unit where E_x ($x = a, b, c$) and I_x represent the root mean square (RMS) value of the grid voltages e_x and grid currents i_x, respectively, φ_{ex} and φ_{ix} represent the phase angle of grid voltages and grid currents, respectively. $\varphi'_{ux0(k)}$ and $u_{0(n)}$ are the calculated value of φ'_{ux0} and u_0, respectively. E_{erro}, I_{erro}, and φ_{erro} are allowable errors, E_{mp} and I_{mp} are the amplitudes of positive-sequence grid voltages and positive-sequence grid currents, respectively, φ_{up} and φ_{un} are the phase angles of the positive-sequence and negative-sequence modulation signals, respectively, φ_{ui} is the phase difference between the positive-sequence grid voltage and positive-sequence grid current, λ is the unbalance factor, i_{xp} and i_{xn} represent the positive-sequence and negative-sequence components of three phase grid currents, and u_{xp} and u_{xn} represent the positive-sequence and negative-sequence components of the three phase modulation signals.

In the k-th line cycle, the RMS value $E_{x(k)}$, $I_{x(k)}$, and phase angle $\varphi_{ex(k)}$, $\varphi_{ix(k)}$ are calculated, and are compared with $E_{x(k-1)}$, $I_{x(k-1)}$, $\varphi_{ex(k-1)}$, and $\varphi_{ix(k-1)}$, respectively, which are the calculated values in the $(k-1)$th line cycle. If the absolute differences between the values of variables in the kth and $(k-1)$th line cycle are greater than the allowable errors, the positively sloped zero-crossing points $\varphi'_{ux0(k)}$ of u'_{x_ref} ($x = a, b, c$) need to be calculated by Equations (19)–(21), if not, $\varphi'_{ux0(k)}$ of u'_{x_ref} ($x = a, b, c$) are equal to $\varphi'_{ux0(k-1)}$ of u'_{x_ref} ($x = a, b, c$), which are calculated in the $(k-1)$th line cycle. In the nth switching cycle, $u_{xp(n)}$, $u_{xn(n)}$, $i_{xp(n)}$, and $i_{xn(n)}$ are calculated, and a line cycle is divided into six regions I-VI by φ'_{ux0}, then $u_{0(n)}$ is calculated by Equations (17) and (18) in the present region.

4. Performance Analysis

4.1. Analysis of the NP Voltage Fluctuation

According to Equations (6) and (16), when the proposed DCR-SPWM method is applied, v_c can be expressed as:

$$v_c = -\frac{1}{C}\int [\sum_{x=a,b,c} \left| u_{xp_ref} + u_{xn_ref} + u_0 \right| (i_{xp} + i_{xn})]dt \tag{22}$$

Supposing that $E_{mp}/(V_{dc}/2)$ = 0.5, C, and I_{mp} are normalized, according to Equations (9)–(14) and (22), the ripple of v_c is related to λ and φ_{ui}. With the traditional SPWM and proposed DCR-SPWM method, surfaces for the ripple of v_c are plotted as shown in Figure 7.

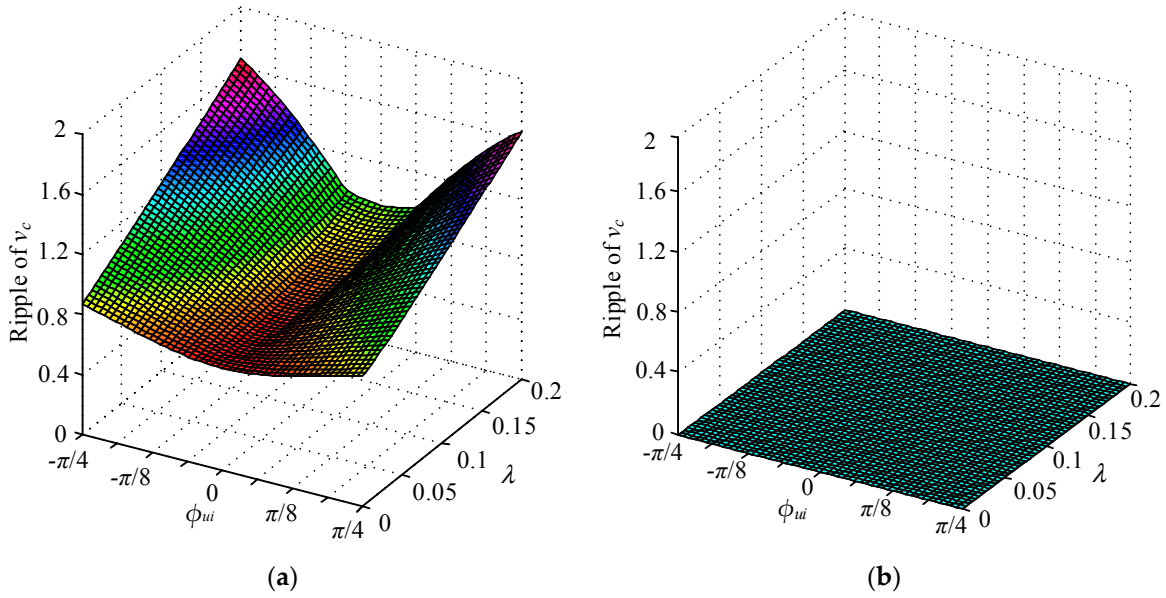


Figure 7. Surfaces of the ripple of v_c as the function with φ_{ui} and λ: (**a**) Traditional SPWM; (**b**) DCR-SPWM.

In Figure 7a, with the traditional SPWM method, the ripple of v_c increases when φ_{ui} varies from 0 to $\pi/4$ (or $-\pi/4$ to 0), and λ varies from 0 to 0.2. In Figure 7b, with the proposed DCR-SPWM method, the ripple of v_c is almost zero, which is not varied with φ_{ui} and λ.

From the comparison above, it can be seen that the proposed DCR-SPWM method can suppress the NP voltage ripple under different λ and φ_{ui} conditions.

4.2. Analysis of the Grid Current Harmonics

Suppose that v_{x_SPWM} and v_{x_DCR} are the leg voltages of the inverter with the traditional SPWM and proposed DCR-SPWM method, respectively, considering the influence of NP voltage, v_{x_SPWM} and v_{x_DCR} are expressed as follows:

$$v_{x_SPWM} = (u_{xp_ref} + u_{xn_ref})\frac{V_{dc}}{2} + \left| u_{xp_ref} + u_{xn_ref} \right| \frac{v_c}{2} + v_{\text{xh_mod}} \tag{23}$$

$$v_{x_DCR} = (u_{xp_ref} + u_{xn_ref} + u_0)\frac{V_{dc}}{2} + \left| u_{xp_ref} + u_{xn_ref} + u_0 \right| \frac{v_c}{2} + v_{\text{xh_mod}} \tag{24}$$

In Equations (23) and (24), v_{xh_mod} represents the harmonic component caused by the modulation method, which was analyzed in [29].

In the Three-phase Three-wire inverter system, the grid currents of the inverter can be expressed as:

$$i_x = \frac{1}{L}\int \left[v_x - e_x - \frac{1}{3}\sum_{x=a,b,c}(v_x + e_x) \right] dt \tag{25}$$

where L is inductance of the filter inductor, and the THD value of the grid currents can be calculated as per [29]:

$$\mathrm{THD} = \sqrt{\frac{\int_0^{2\pi} i_x^2(\omega t)d\omega t}{\int_0^{2\pi} i_{x1}^2(\omega t)d\omega t} - 1} \tag{26}$$

where i_{x1} represents the fundamental component of the grid currents.

According to Equations (9)–(14) and (22)–(26), the THD value of the grid currents is related to λ and φ_{ui}. The surfaces for THD of grid current i_b with the traditional SPWM and DCR-SPWM method are shown in Figure 8. Compared with the traditional SPWM method, the THD value was lower when the proposed DCR-SPWM method was applied, and was lower than 4% under different λ and φ_{ui} conditions.

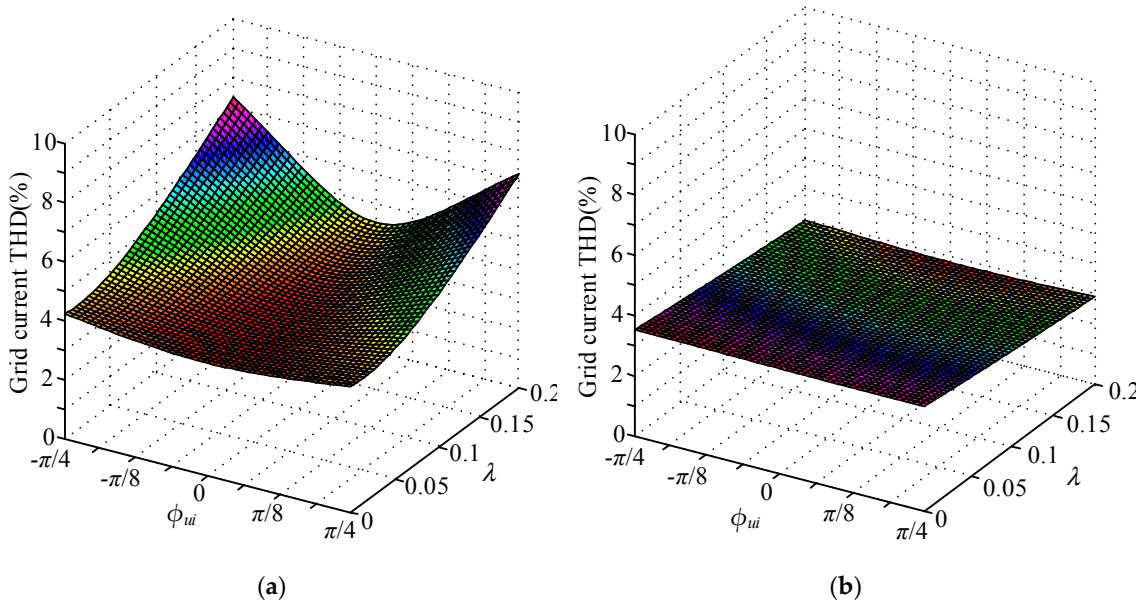


Figure 8. Surfaces of the THD results as the function with φ_{ui} and λ: (**a**) Traditional SPWM; (**b**) DCR-SPWM.

From the analysis above, it can be seen that the proposed DCR-SPWM method can improve the quality of grid currents under different λ and φ_{ui} conditions.

5. Simulation and Experimental Verification

5.1. Simulation Analysis

In order to verify the validity of the proposed DCR-SPWM method, a simulation model of the NPC three-level grid-connected inverter was built using Matlab tools, and the specifications of the simulation model are shown in Table 2.

Table 2. Specifications of the prototype for simulation.

Specifications of the Prototype	
DC bus voltage	V_{dc} = 200 V
DC bus capacitors	$C_1 = C_2$ = 150 μF
Switching frequency	f_s = 16 kHz
Apparent power	S = 600 VA
The amplitude of grid voltages	E_{ma} = 55 V, E_{mb} = 40 V, E_{mc} = 55 V
Output phase filter	L: 1.5 mH, C: 15 μF

Figure 9 shows the simulated waveforms of capacitor voltage v_{c1}, v_{c2}, leg voltage v_b, grid current i_b, and three phase grid voltages e_x ($x = a, b, c$). In Figure 9a,b, the DCR-SPWM method was applied at 0.25 s, where it can be seen that before using the DCR-SPWM method, the capacitor voltage ripple was 20 V at $\varphi_{ui} = 0$, and 30 V at $\varphi_{ui} = -\pi/4$, respectively. After the DCR-SPWM method was applied, the NP voltage ripple was reduced effectively and the grid current quality improved. In Figure 9c, a parallel resistor was connected to the dc bus capacitor C_2 for the NPC three-level grid-connected inverter, resulting in the 40 V dc unbalanced voltage between v_{c1} and v_{c2}, which made the positive and negative half line cycle of the output leg voltage asymmetric, so as to the grid current. When the DCR-SPWM method was applied, the NP voltage ripple and dc unbalanced voltage could be controlled effectively, and quality of the grid current was improved.

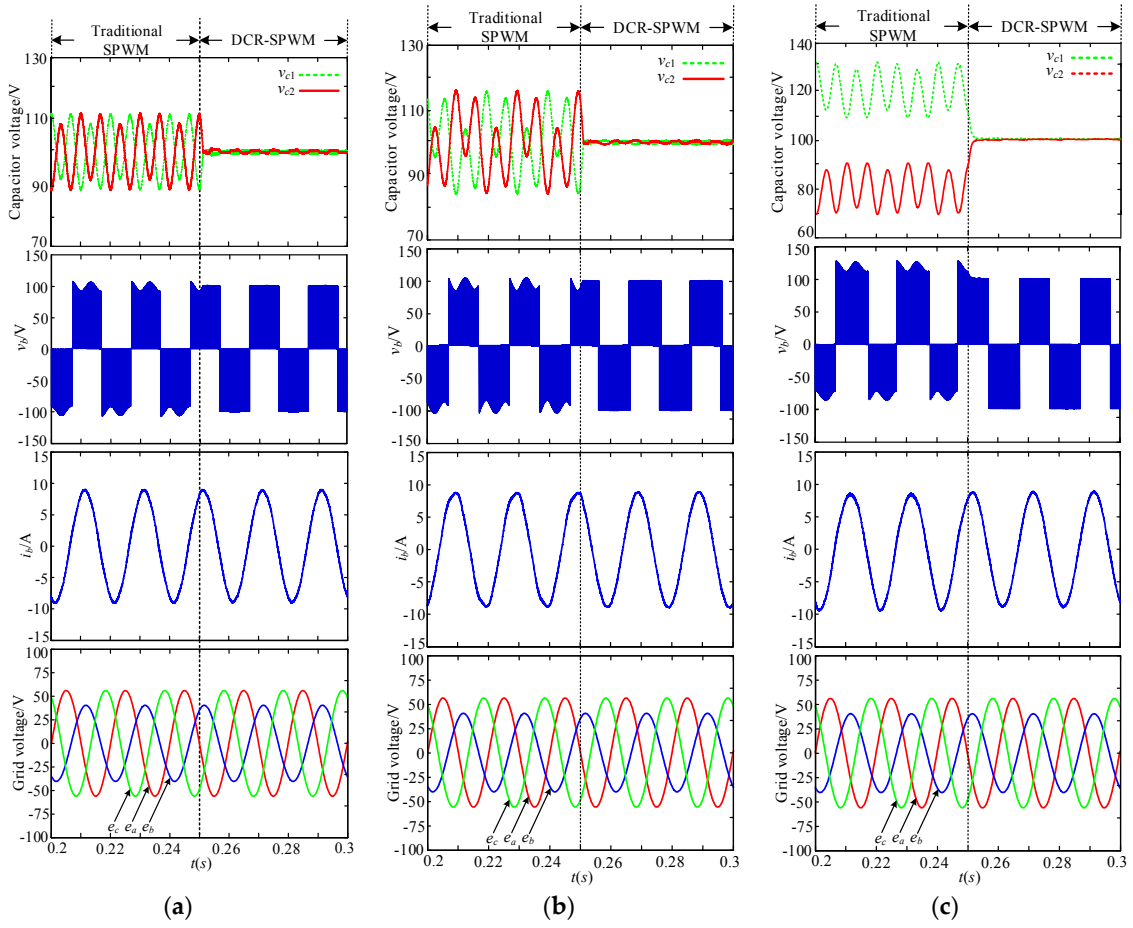


Figure 9. Simulated waveforms of the traditional SPWM and the proposed DCR-SPWM method: (**a**) $\varphi_{ui} = 0$, ${v_{c1}}^{\mathrm{avg}} - {v_{c2}}^{\mathrm{avg}} = 0$; (**b**) $\varphi_{ui} = -\pi/4$, ${v_{c1}}^{\mathrm{av}} - {v_{c2}}^{\mathrm{avg}} = 0$; (**c**) $\varphi_{ui} = 0$, ${v_{c1}}^{\mathrm{avg}} - {v_{c2}}^{\mathrm{avg}} = 40$ V.

5.2. Experimental Verification

As shown in Figure 10a, the proposed DCR-SPWM method was tested in the experimental platform of an NPC three-level grid-connected inverter based on DSP-CPLD. The experimental platform is shown in Figure 10b where the oscilloscope and power analyzer are Tektronix MDO3000 (Tektronix, Shanghai, China) and HIOKI PW6001 (HIOKI, Nagano, Japan), respectively. The specifications of the experimental prototype are shown in Table 3.

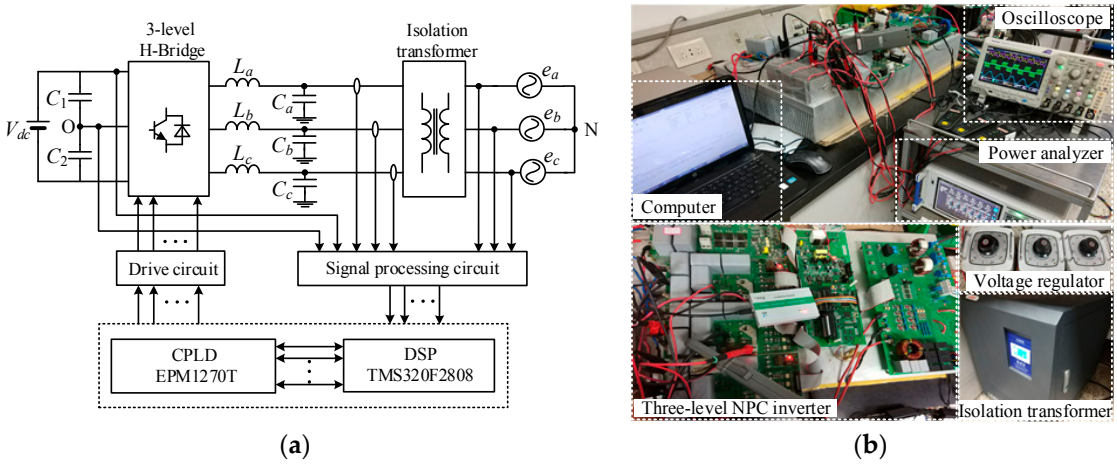


Figure 10. The schematic diagram and experimental photograph of the system: (**a**) Schematic diagram of the system; (**b**) Experimental photograph of the system.

Table 3. Specifications of the experimental prototype.

The Specifications of the Experimental Prototype	
DC bus voltage	V_{dc} = 200 V
DC bus capacitors	$C_1 = C_2$ = 150 μF
Switching frequency	f_s = 16 kHz
Apparent power	S = 600 VA
Digital Process Unit	DSP: TMS320F2808, CPLD: EPM1270T
Power switches module	IGBT FZ06NPA070FP
Output phase filter	L: 1.5 mH, C: 15 μF

Figures 11 and 12 show the experimental waveforms of v_{c1}, v_{c2}, i_b, v_b e_x ($x = a, b, c$) and u_m at different λ and φ_{ui} conditions, where v_b is the leg voltage of phase b and u_m is zero-sequence voltage that added to the modulation signals, which is added to modulation signals. From Figure 11, it can be seen that when using the traditional SPWM method, the ripple of capacitor voltage v_{c1} was about 20 V at $\varphi_{ui} = 0$, $\lambda = 0.1$ in Figure 11a, and was about 32 V at $\varphi_{ui} = -\pi/4$, $\lambda = 0.1$ in Figure 11b, after the proposed DCR-SPWM method was applied, the ripple of NP voltage was suppressed effectively. In Figure 11c,d, the PI-SPWM method proposed in [14] was applied and it can be seen that the proposed method had better performance in terms of the system steady-state error when compared with the PI-SPWM method.

In Figure 12, before using the DCR-SPWM method, the ripple of v_{c1} was about 20 V at $\lambda = 0.15$, $\varphi_{ui} = 0$ in Figure 12a, and was 24 V at $\lambda = 0.2$, $\varphi_{ui} = 0$ in Figure 12b. The NP voltage ripple was very low with the DCR-SPWM method.

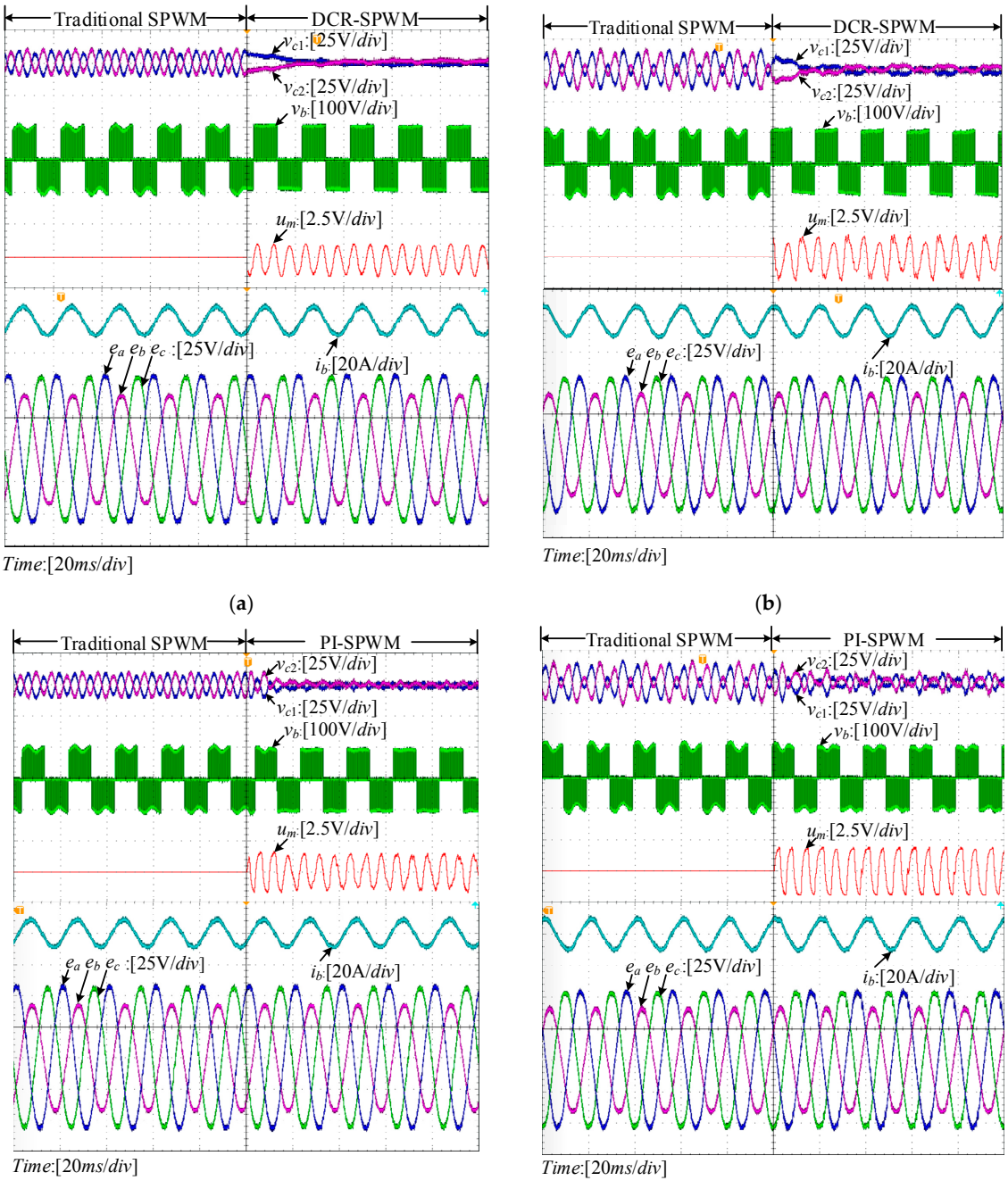


Figure 11. Experimental waveforms under different φ_{ui} conditions: (**a**) DCR-SPWM $\varphi_{ui} = 0$, $\lambda = 0.1$, ${v_{c1}}^{\mathrm{av}} - {v_{c2}}^{\mathrm{avg}} = 0$; (**b**) DCR-SPWM $\varphi_{ui} = -\pi/4$, $\lambda = 0.1$, ${v_{c1}}^{\mathrm{avg}} - {v_{c2}}^{\mathrm{avg}} = 0$; (**c**) PI-SPWM $\varphi_{ui} = 0$, $\lambda = 0.1$, ${v_{c1}}^{\mathrm{avg}} - {v_{c2}}^{\mathrm{avg}} = 0$; (**d**) PI-SPWM $\varphi_{ui} = -\pi/4$, $\lambda = 0.1$, ${v_{c1}}^{\mathrm{avg}} - {v_{c2}}^{\mathrm{avg}} = 0$.

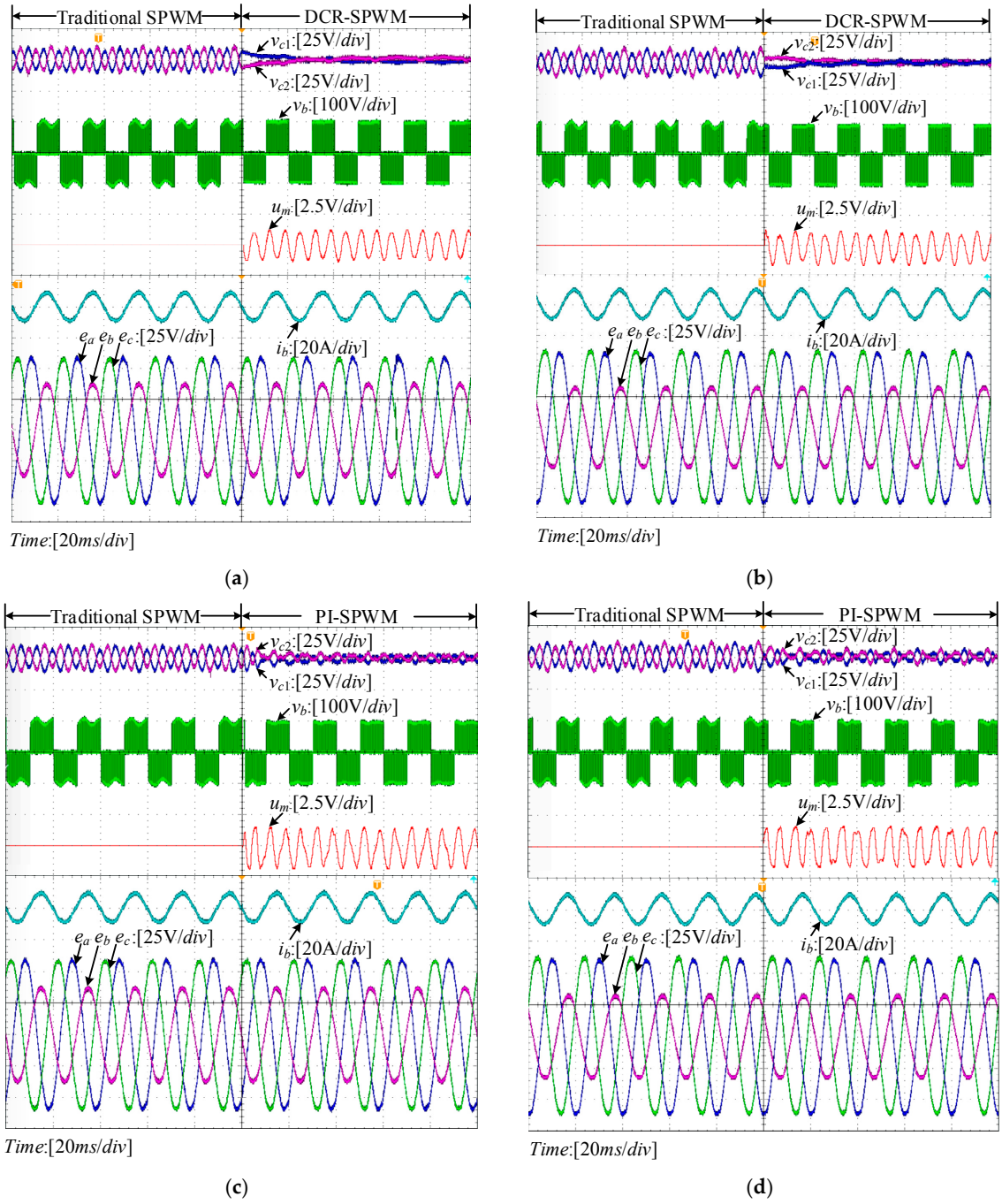


Figure 12. Experimental waveforms under different λ conditions: (**a**) DCR-SPWM $\varphi_{ui} = 0$, $\lambda = 0.15$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 0$; (**b**) DCR-SPWM $\varphi_{ui} = 0$, $\lambda = 0.2$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 0$; (**c**) PI-SPWM $\varphi_{ui} = 0$, $\lambda = 0.15$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 0$; (**d**) PI-SPWM $\varphi_{ui} = 0$, $\lambda = 0.2$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 0$.

When a parallel resistor connected to the dc bus capacitor C_2 for the NPC three-level grid-connected inverter, experimental waveforms of v_{c1}, v_{c2}, i_b, v_b, e_x, and u_m under different conditions are shown in Figure 13, defined that ${v_{c1}}^{\text{avg}}$ and ${v_{c2}}^{\text{avg}}$ were the average voltage of v_{c1} and v_{c2}, respectively, and before using the DCR-SPWM method, the NP voltage was unbalanced, the voltage difference between ${v_{c1}}^{\text{avg}}$ and ${v_{c2}}^{\text{avg}}$ was about 80 V. In a line cycle, the amplitude of the leg voltage in the positive half cycle was higher than in the negative half cycle, and the quality of the grid current was not beneficial to the grid connections.

When the DCR-SPWM method was applied, the voltage difference between v_{c1} and v_{c2} decreased to almost zero, and the ripple of v_{c1} and v_{c2} was very low. From Figure 13a,b,e, it can be seen that under different unbalanced grid and output power conditions, the system reached the steady-state rapidly, and the quality of the grid current was improved.

Figure 14 shows the harmonics analysis of the grid current i_b under different λ conditions, when $\varphi_{ui} = -\pi/4$, it can be seen that when the DCR-SPWM method was applied, much low order harmonics were decreased, and the THD value decreased so that the quality of the grid current was beneficial to grid connections.

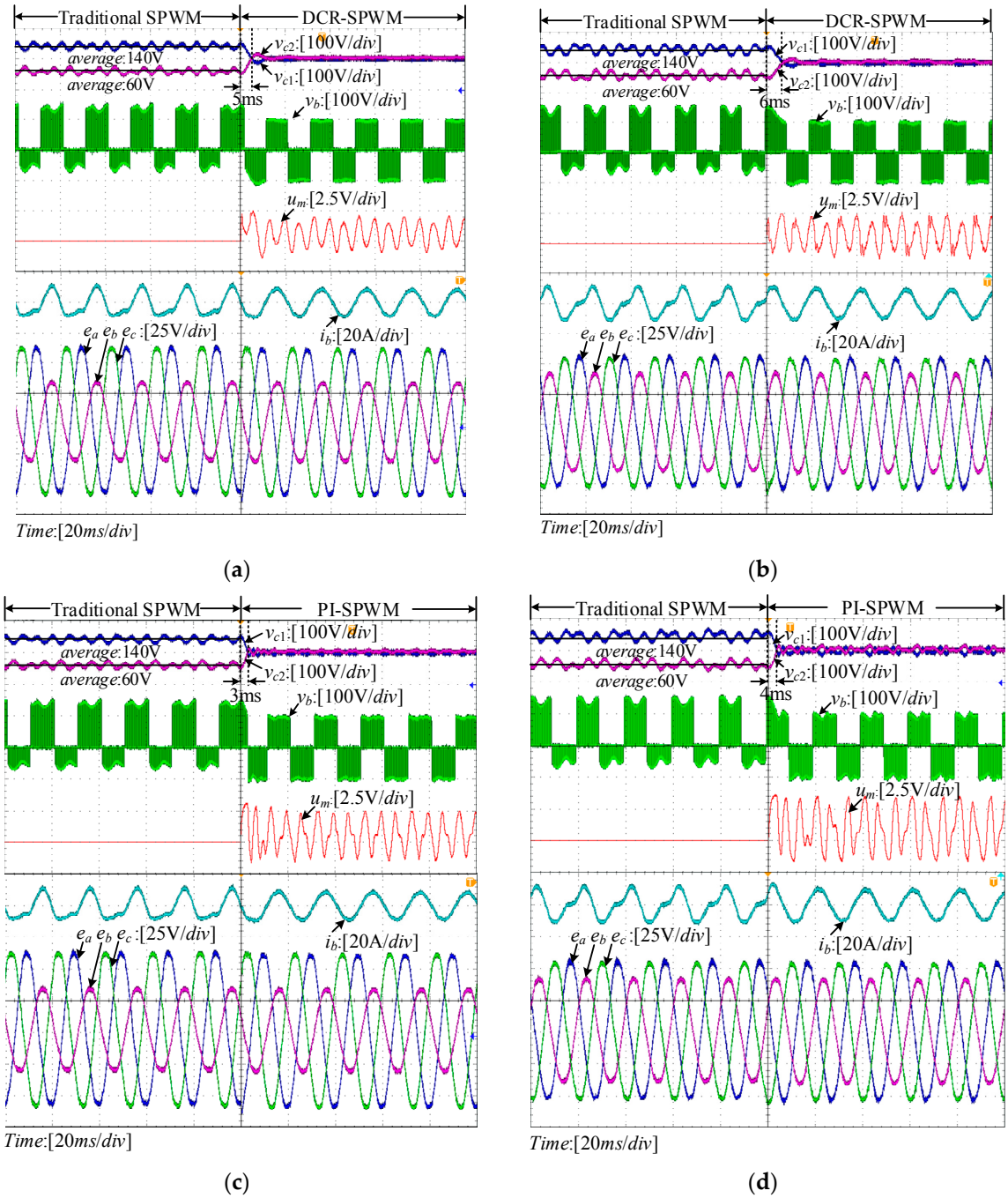


Figure 13. *Cont.*

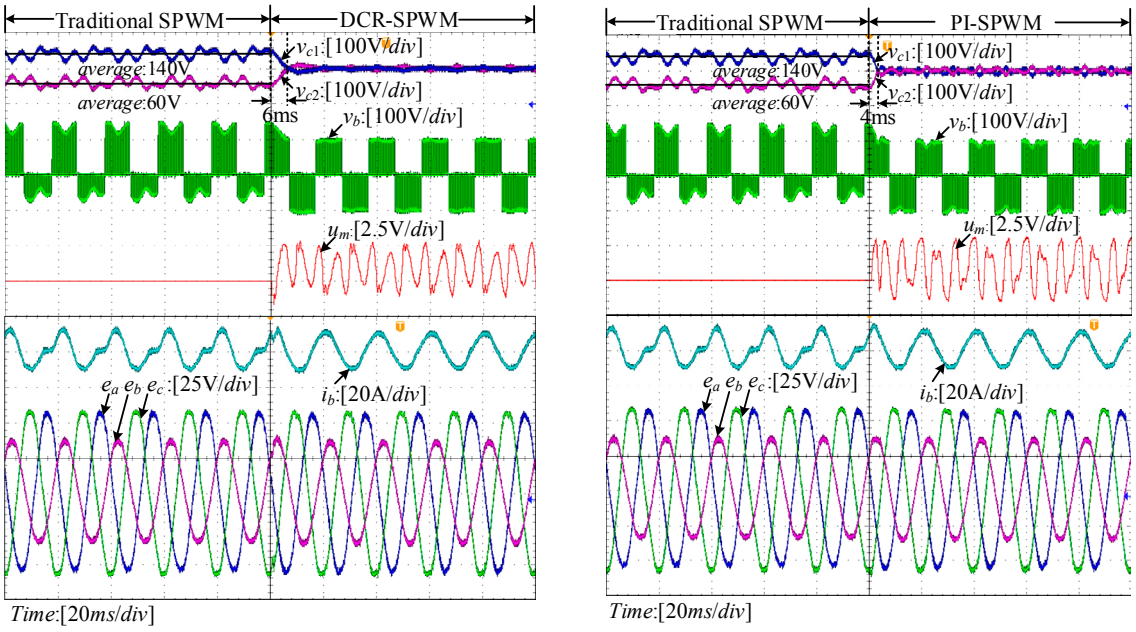


Figure 13. Experimental waveforms under dc unbalanced NP voltage conditions: (**a**) DCR-SPWM $\varphi_{ui} = 0$, $\lambda = 0.2$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 80$ V; (**b**) DCR-SPWM $\varphi_{ui} = -\pi/4$, $\lambda = 0.1$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 80$ V; (**c**) PI-SPWM $\varphi_{ui} = 0$, $\lambda = 0.2$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 80$ V; (**d**) PI-SPWM $\varphi_{ui} = -\pi/4$, $\lambda = 0.1$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 80$ V; (**e**) DCR-SPWM $\varphi_{ui} = -\pi/4$, $\lambda = 0.15$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 80$ V; (**f**) PI-SPWM $\varphi_{ui} = -\pi/4$, $\lambda = 0.15$, ${v_{c1}}^{\text{avg}} - {v_{c2}}^{\text{avg}} = 80$ V.

Figures 15 and 16 show the ripple of v_{c1} and the THD results of i_b at different unbalanced grid conditions with different control methods. It can be seen that with the traditional SPWM method, the ripple of v_{c1} increased much higher and the THD value was higher than 5% when λ varied from 0 to 0.2 at $\varphi_{ui} = -\pi/4$, instead, when compared with the PI-SPWM method, the DCR-SPWM method proposed in this paper decreased the ripple of v_{c1} effectively, and the THD value of grid current was decreased, which was lower than 4%.

According to the experimental and simulation results, under different unbalanced grid and output power conditions, the proposed DCR-SPWM method can suppress the ripple of the NP voltage effectively; when the NP voltage has dc unbalanced voltage, the NP voltage is controlled to be balanced fast, furthermore, this DCR-SPWM method improved the grid current quality and reduced its THD effectively when compared with the PI-SPWM method proposed in [14].

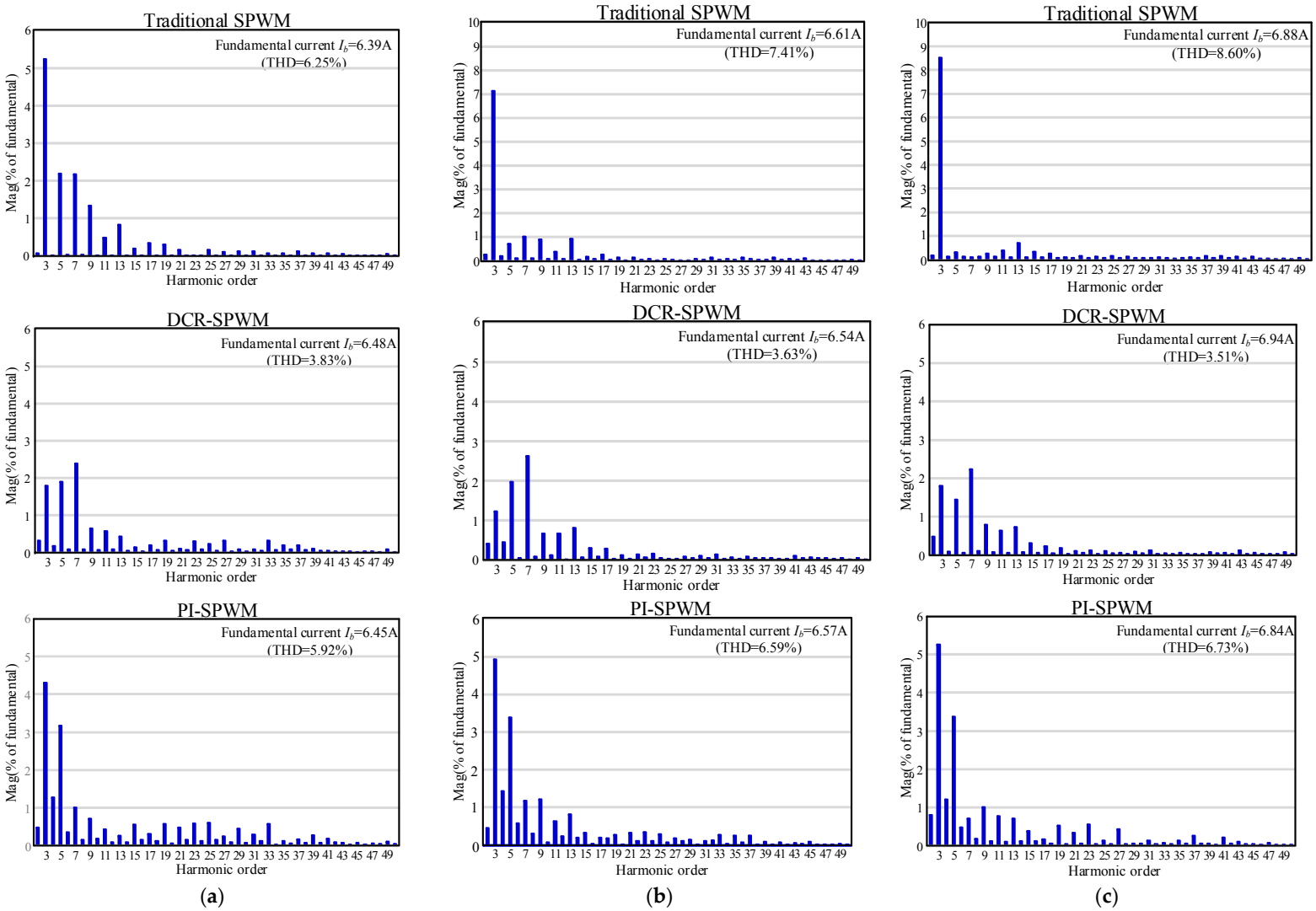


Figure 14. Harmonics distribution of i_b: (**a**) λ = 0.1; (**b**) λ = 0.15; (**c**) λ = 0.2.

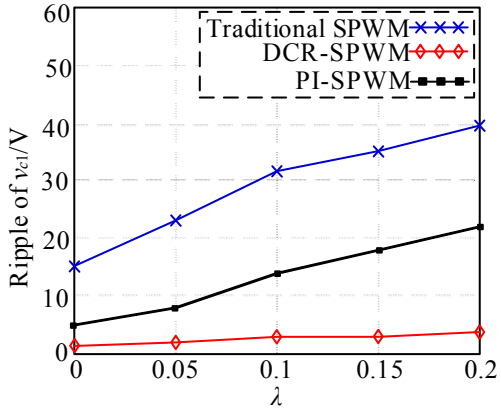


Figure 15. Measured NP voltage ripple.

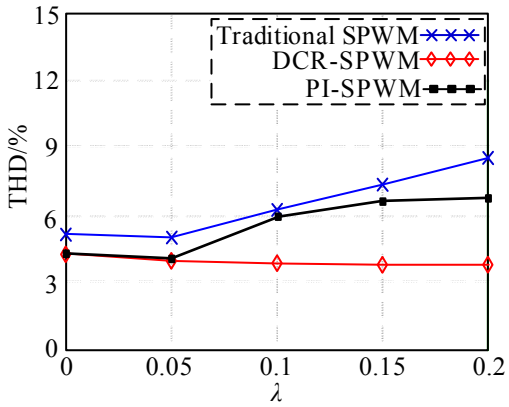


Figure 16. Measured THD.

6. Conclusions

In order to solve the NP voltage unbalancing problem for NPC three-level grid-connected inverter under non-ideal grid conditions, the unbalanced form of NP voltage under non-ideal grid conditions was studied, and the DCR-SPWM method under non-ideal grid conditions was proposed. This proposed DCR-SPWM method dynamically calculates the zero-sequence component for modulation signals by region selections, and the theoretical analysis and experiment results showed that the proposed method had a good ability to control the NP voltage balance, and improved the grid current quality effectively.

Author Contributions: J.G.L. conducted the theory analysis and designed the whole project, W.B.H. conducted the experiments, J.D.W. performed the simulation, Z.F.W. and J.D.W. completed the experimental tests. J.D.W. and J.G.L. edited the manuscript.

Acknowledgments: This project was supported by the National Natural Science Foundation of China (51707097), the Fundamental Research Funds for the Central Universities (30917011331), and the Open Research Fund of Jiangsu Collaborative Innovation Center for Smart Distribution Network, Nanjing Institute of Technology (XTCX201708).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wang, Y.; Wang, F. Novel Three-Phase Three-Level-Stacked Neutral Point Clamped Grid-Tied Solar Inverter with a Split Phase Controller. *IEEE Trans. Power Electron.* **2013**, *28*, 2856–2866. [CrossRef]

2. Teymour, H.R.; Sutanto, D.; Muttaqi, K.M.; Ciufo, P. Solar PV and Battery Storage Integration Using a New Configuration of a Three-Level NPC Inverter with Advanced Control Strategy. *IEEE Trans. Energy Convers.* **2014**, *29*, 354–365.
3. Zhang, Y.; Li, J.; Li, X.; Cao, Y.; Sumner, M.; Xia, C. A Method for the Suppression of Fluctuations in the Neutral-Point Potential of a Three-Level NPC Inverter with a Capacitor-Voltage Loop. *IEEE Trans. Power Electron.* **2017**, *32*, 825–836. [CrossRef]
4. Nabae, A.; Takahashi, I.; Akagi, H. A New Neutral-Point-Clamped PWM Inverter. *IEEE Trans. Ind. Appl.* **1981**, *IA-17*, 518–523. [CrossRef]
5. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E. A Survey on Neutral-Point-Clamped Inverters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2219–2230. [CrossRef]
6. Zaragoza, J.; Pou, J.; Ceballos, S.; Robles, E.; Ibanez, P.; Villate, J.L. A Comprehensive Study of a Hybrid Modulation Technique for the Neutral-Point-Clamped Converter. *IEEE Trans. Ind. Electron.* **2009**, *56*, 294–304. [CrossRef]
7. Choi, U.M.; Lee, H.H.; Lee, K.B. Simple Neutral-Point Voltage Control for Three-Level Inverters Using a Discontinuous Pulse Width Modulation. *IEEE Trans. Energy Convers.* **2013**, *28*, 434–443. [CrossRef]
8. Shen, J.; Schröder, S.; Rösner, R.; El-Barbari, S. A Comprehensive Study of Neutral-Point Self-Balancing Effect in Neutral-Point-Clamped Three-Level Inverters. *IEEE Trans. Power Electron.* **2011**, *26*, 3084–3095. [CrossRef]
9. Choi, U.M.; Lee, J.S.; Lee, K.B. New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems. *IEEE Trans. Energy Convers.* **2014**, *29*, 91–100. [CrossRef]
10. Sebaaly, F.; Vahedi, H.; Kanaan, H.Y.; Al-Haddad, K. Novel Current Controller Based on MPC With Fixed Switching Frequency Operation for a Grid-Tied Inverter. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6198–6205. [CrossRef]
11. Sebaaly, F.; Vahedi, H.; Kanaan, H.Y.; Moubayed, N.; Al-Haddad, K. Sliding Mode Fixed Frequency Current Controller Design for Grid-Connected NPC Inverter. *IEEE Trans. Power Electron.* **2016**, *4*, 1397–1405. [CrossRef]
12. López, I.; Ceballos, S.; Pou, J.; Zaragoza, J.; Andreu, J.; Ibarra, E.; Konstantinou, G. Generalized PWM-based method for multiphase neutral-point-clamped converters with capacitor voltage balance capability. *IEEE Trans. Power Electron.* **2017**, *32*, 4878–4890. [CrossRef]
13. Wang, C.; Li, Y. Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2262–2271. [CrossRef]
14. Chaturvedi, P.; Jain, S.; Agarwal, P. Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter. *IEEE Trans. Ind. Electron.* **2014**, *61*, 613–624. [CrossRef]
15. Maheshwari, R.; Munk-Nielsen, S.; Busquets-Monge, S. Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1861–1871. [CrossRef]
16. Shayestehfard, A.; Mekhilef, S.; Mokhlis, H. IZDPWM-based feedforward controller for grid-connected inverters under unbalanced and distorted conditions. *IEEE Trans. Ind. Electron.* **2017**, *64*, 14–21. [CrossRef]
17. Yan, Q.; Wu, X.; Yuan, X.; Geng, Y. An Improved Grid-Voltage Feedforward Strategy for High-Power Three-Phase Grid-Connected Inverters Based on the Simplified Repetitive Predictor. *IEEE Trans. Power Electron.* **2016**, *31*, 3880–3897. [CrossRef]
18. Teodorescu, R.; Liserre, M.; Rodríguez, P. *Grid Converters for Photovoltaic and Wind Power Systems*; John Wiley & Sons: Hoboken, NJ, USA, 2011; pp. 171–172.
19. Ma, K.; Blaabjerg, F. Modulation Methods for Neutral-Point-Clamped Wind Power Converter Achieving Loss and Thermal Redistribution under Low-Voltage Ride-Through. *IEEE Trans. Ind. Electron.* **2014**, *61*, 835–845. [CrossRef]
20. Shao, Z.; Zhang, X.; Wang, F.; Cao, R.; Ni, H. Analysis and Control of Neutral-Point Voltage for Transformerless Three-Level PV Inverter in LVRT Operation. *IEEE Trans. Power Electron.* **2017**, *32*, 2347–2359. [CrossRef]
21. Vahedi, H.; Labbe, P.A.; Al-Haddad, K. Balancing three-level neutral point clamped inverter DC bus using closed-loop space vector modulation: Real-time implementation and investigation. *IET Power Electron.* **2016**, *9*, 2076–2084. [CrossRef]

22. Sebaaly, F.; Vahedi, H.; Kanaan, H.Y.; Moubayed, N.; Al-Haddad, K. Design and Implementation of Space Vector Modulation-Based Sliding Mode Control for Grid-Connected 3L-NPC Inverter. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7854–7863. [CrossRef]
23. Jung, K.; Suh, Y. Compensation of neutral point deviation in 3-level NPC converter under unbalanced grid conditions. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA, USA, 20–24 March 2016; pp. 17–24.
24. Jung, K.; Suh, Y. Analysis of neutral point deviation in 3-level NPC converter under unbalanced 3-phase AC grid. In Proceedings of the IEEE Energy Conversion Congress and Exposition, Milwaukee, WI, USA, 18–22 September 2016; pp. 1–8.
25. Von Jouanne, A.; Dai, S.; Zhang, H. A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination. *IEEE Trans. Ind. Electron.* **2002**, *49*, 739–745. [CrossRef]
26. Yaramasu, V.; Wu, B. Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems. *IEEE Trans. Power Electron.* **2014**, *29*, 5308–5322. [CrossRef]
27. Zhang, M.; Hang, L.; Yao, W.; Lu, Z.; Tolbert, L.M. A Novel Strategy for Three-Phase/Switch/Level (Vienna) Rectifier under Severe Unbalanced Grids. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4243–4252. [CrossRef]
28. Nejabatkhah, F.; Li, Y.W.; Wu, B. Control Strategies of Three-Phase Distributed Generation Inverters for Grid Unbalanced Voltage Compensation. *IEEE Trans. Power Electron.* **2016**, *31*, 5228–5241.
29. Holmes, D.G.; Lipo, T.A. *Pulse width Modulation for Power Converters: Principles and Practice*; John Wiley & Sons: Hoboken, NJ, USA, 2003; pp. 473–479.



© 2018 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).