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# DC Fault Analysis and Clearance Solutions of MMC-HVDC Systems

**Zheng Xu *, Huangqing Xiao, Liang Xiao and Zheren Zhang**

College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China; xhqhz@zju.edu.cn (H.X.); xlxiaoliang@zju.edu.cn (L.X.); zhangzheren@zju.edu.cn (Z.Z.)

* Correspondence: xuzheng007@zju.edu.cn; Tel.: +86-0571-8795-2074

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**Abstract:** In this paper, the DC short-circuit fault and corresponding clearance solutions of modular multilevel converter-based high-voltage direct current (MMC-HVDC) systems are analyzed in detail. Firstly, the analytical expressions of DC fault currents before and after blocking the MMC are derived based on the operation circuits. Before blocking the MMC, the sub-module (SM) capacitor discharge current is the dominant component of the DC fault current. It will reach the blocking threshold value in several milliseconds. After blocking the MMC, the SM capacitor is no longer discharged. Therefore, the fault current from the AC system becomes the dominant component. Meanwhile, three DC fault clearance solutions and the corresponding characteristics are discussed in detail, including tripping AC circuit breaker, adopting the full-bridge MMC and employing the DC circuit breaker. A simulation model of the MMC-HVDC is realized in PSCAD/EMTDC and the results of the proposed analytical expressions are compared with those of the simulation. The results show that the analytical DC fault currents coincide well with the simulation results.

**Keywords:** modular multilevel converter; DC fault current; operation circuit; DC fault clearance solution; AC circuit breaker; full-bridge MMC; DC circuit breaker

## 1. Introduction

With the growth of energy demand and the gradual exhaustion of fossil fuels, the development and integration of renewable energy sources has become increasingly important in recent years. According to practical experience, voltage source converter-based high-voltage direct current (VSC-HVDC) systems are considered to be one of the best solutions for renewable energy integration [1,2].

The modular multilevel converter (MMC) is considered to be the most promising VSC topology [3–5]. Because of the modular construction, the series connection of power electronic devices is avoided. So the difficulty in manufacturing is reduced [6–8]. The MMC-HVDC system can provide excellent outputs of modulated voltage and current, and has been widely used in commercial projects [9–11].

Up till now, a lot of studies have been focused on the modeling [12–14], control [15–17] and steady-state analysis [18,19] of the MMC-HVDC. When the MMC is used in long-distance overhead line transmissions or DC grids, the DC fault characteristics and the corresponding clearance solutions should be analyzed in depth. A mathematical model of two-terminal VSC-HVDC under various DC fault conditions is built in [20]. In [21], theoretical analysis of VSC cable fault with three stages is proposed. However, both [20,21] are based on two-level converters. The performance of MMC under pole-to-ground fault is analyzed and expression for DC current is derived in [22]. However, the equivalent DC voltage is achieved with the conventional half-wave rectifier bridge. It should be noted that the equivalent circuit after blocking the MMC is different from the conventional half-wave rectifier bridge, as the former one has an inductor in each arm. A pole-to-pole fault analysis of multi-terminal MMC systems is proposed in [23]. However, the fault current is obtained

by electromagnetic transient simulations. Analytical fault current calculation method of pole-to-pole fault for one terminal MMC and MMC-based DC grids are introduced in [24,25]. However, the fault current expressions are valid only before blocking the MMC. Reference [26] derives the detailed differential equations of MMC in both pre-blocking and post-blocking conditions, and also proposes the corresponding solving method. However, this method belongs to numerical analysis and the analytical solution cannot be given.

DC fault isolation is the most important technical obstacle that limits the application of MMC in long-distance overhead line transmissions or DC grids. Generally, there have been three solutions for solving this problem [27,28]:

- The first solution is to trip the AC circuit breaker (ACCB). The advantages of this method are the good economic efficiency and the high technical maturity. That is the reason most practical commercial VSC-HVDC projects use this method to clear DC line faults. Noted the slow response of the ACCB, it will take a long time for the system to recover from the DC line faults [27].
- Adopting fault blocking converters is another option [29]. To prevent IGBT damage due to overheating, converters will be blocked when the current flowing through the IGBT reaches 2 times of its rated value. Some converters may produce reversed electromotive force to impede the fault current, such as full-bridge MMC. For this solution, the speed of resuming power transmission from temporary DC faults is fast. However, more power electronic devices are needed, and the device cost and power losses increase accordingly. Compared with the half-bridge sub-modules (SMs) MMC, the converter based on full-bridge SMs needs twice insulated gate bipolar transistor (IGBT) modules and the power losses increase by about 100%; the converter based on clamp-double SMs needs 1.25 times IGBT modules and the power losses increase by about 35% [30].
- The employing of DC circuit breakers (DCCBs) is the third method for handling DC fault. In late 2012, ABB released a hybrid DCCB that can break a maximum DC fault current of 9 kA within 5 ms [31]. Technically speaking, there have been some drawbacks for the existing DCCBs, such as high manufacture cost and low technology maturity.

Moreover, the fault recovery characteristics of the MMC with the above three solutions are not analyzed in detail.

In this paper, the analytical expressions of DC currents under pole-to-pole fault are derived and the fault characteristics of the MMC with different solutions are analyzed. Firstly, the analytical DC fault current expression of MMC before blocking is derived based on the operation circuit in complex frequency domain. Secondly, after the MMC is blocked, the DC current expression is also derived. Besides, three DC fault clearance solutions and the corresponding characteristics are discussed in detail.

This paper is organized as follows. The analytical expressions of the fault currents before and after blocking the MMC are studied in Sections 2 and 3 respectively. In Section 4 the three DC fault clearance solutions are discussed. In Section 5, an MMC-HVDC model is built in PSCAD/EMTDC to verify the accuracy and feasibility of the proposed analytical expressions. Section 6 concludes the paper.

## 2. DC Fault Analysis of MMC before Blocking

Figure 1 shows the DC short-circuit fault of MMC. The arm voltage and the arm current are $u_{rj}$ ($r$ = p, n denotes the upper and lower arms; $j$ = a, b, c denotes the three phases a, b, c) and $i_{rj}$ respectively. $U_{\mathrm{dc}}$ is the DC voltage and $I_{\mathrm{dc}}$ is the DC line current. The fault current mainly contains the SM capacitor discharge current and three-phase short-circuit current of the AC system. Before blocking the MMC, the SM capacitor discharge current is the dominant component. The fault current rises so fast that it can reach several tens of kA in a few milliseconds.

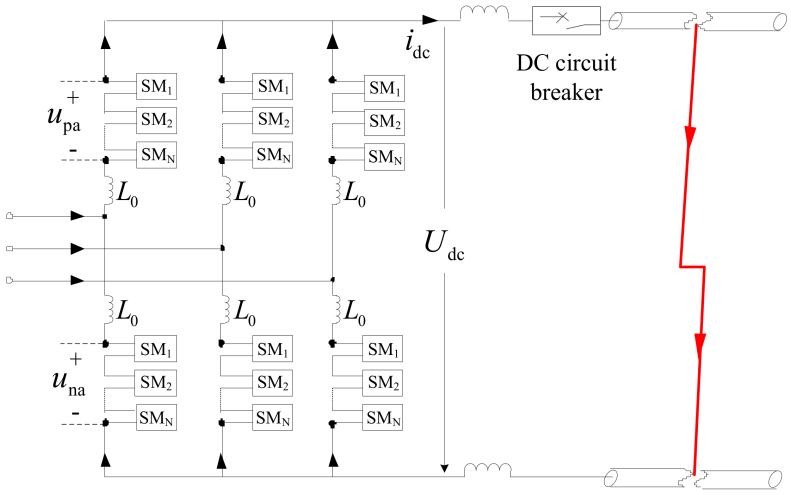


**Figure 1.** Configuration of MMC under DC short-circuit fault.

In this stage, the number of inserted SMs in each arm changes constantly. This is a nonlinear time-varying circuit. However, if the period of the analysis is sufficiently short that the inserted SMs remain unchanged, then the MMC is a linear circuit during this period.

The operation circuit analysis (also called complex frequency domain analysis) is an effective method to analyze the transient process of a linear circuit. The specific approach is to replace the impedance and admittance with operational impedance and operational admittance respectively. The inductor and capacitor operation circuit model is shown in Figure 2. $sL$ and $1/sC$ are their operation impedances, where $s$ is the Laplace operator. Appendix A shows the detailed derivation.

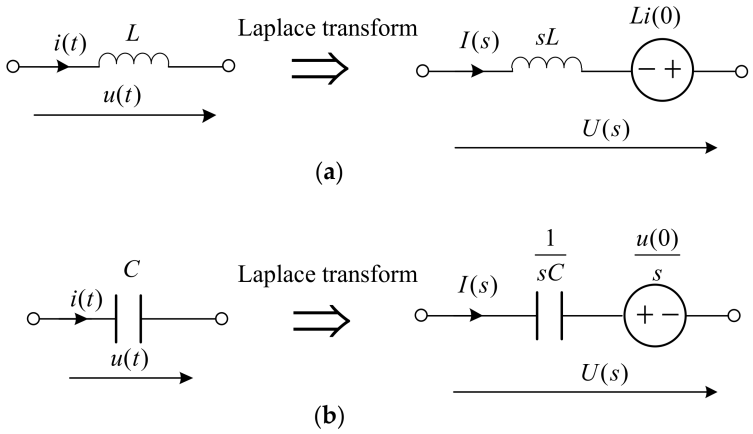


**Figure 2.** Operation circuit model of basic device. (**a**) Inductor; (**b**) Capacitor.

The complete operation circuit of Figure 1 is depicted in Figure 3a. $R_{dc}$ and $L_{dc}$ include the resistance and inductance of smoothing reactor, DC circuit breaker and DC line. $R_0$ represents the loss of each arm. $C_0$ is the SM capacitance. $N$ is the number of SMs in each arm. In the three-phase symmetrical system, the sum of AC system three-phase short-circuit current is zero. Also, as mentioned above, the SM capacitor discharge current is the dominant fault current before blocking the MMC. Therefore, the part of AC system can be ignored here. In this way, Figure 3a can be simplified to Figure 3b. Figure 3c is the equivalent circuit of Figure 3b. It should be noted that the quantities marked zero (i.e., $i_{dc}(0)$, $u_{pc}(0)$, $i_c(0)$, ... ) are their initial values before the fault occurs.

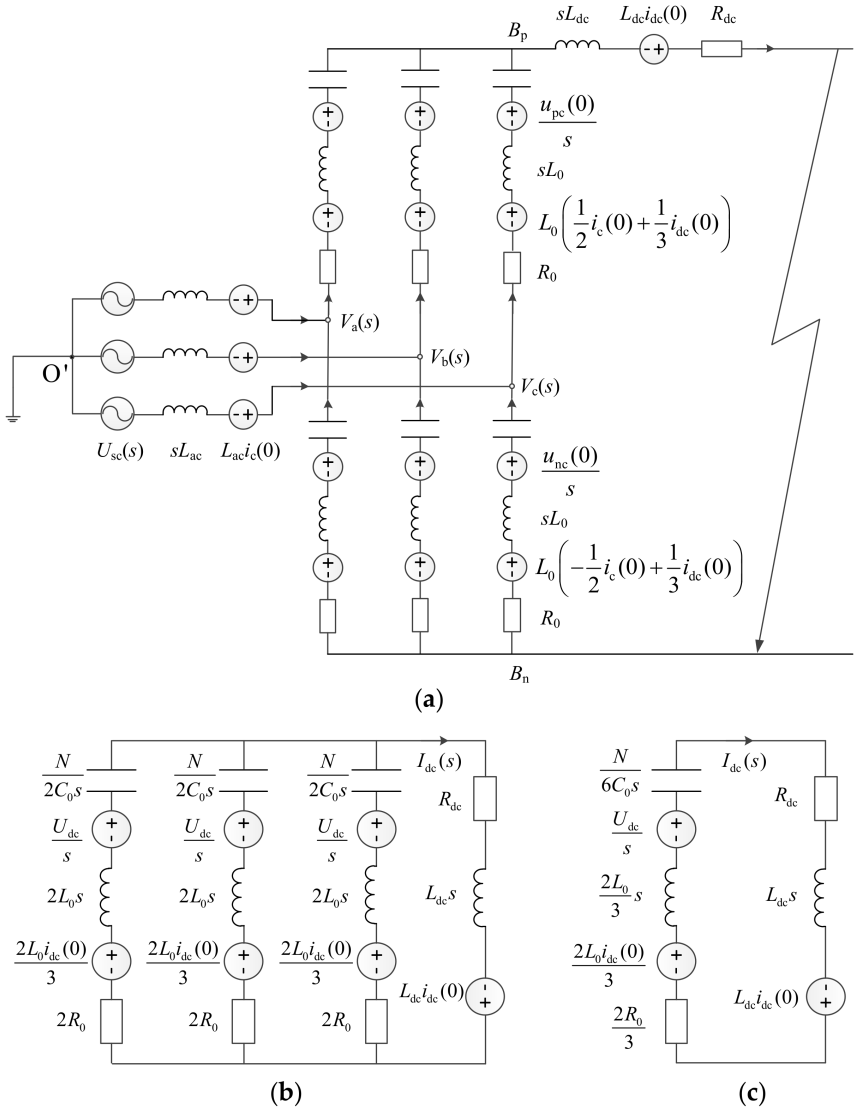


**Figure 3.** Operation circuit of MMC before it is blocked. (**a**) Complete model; (**b**) Simplified model; (**c**) Equivalent simplified model.

Solving the simplified circuit shown in Figure 3c, the following equation can be obtained

$$I_{dc}(s) = \frac{s\left(L_{dc} + \frac{2L_0}{3}\right)i_{dc}(0) + U_{dc}}{s^2\left(\frac{2}{3}L_0 + L_{dc}\right) + s\left(\frac{2}{3}R_0 + R_{dc}\right) + \frac{N}{6C_0}} \tag{1}$$

The Laplace inverse transform of (1) yields

$$i_{dc}(t) = -\frac{1}{\sin\theta_{dc}}i_{dc}(0)e^{-\frac{t}{\tau_{dc}}}\sin(\omega_{dc}t - \theta_{dc}) + \frac{U_{dc}}{R_{dis}}e^{-\frac{t}{\tau_{dc}}}\sin(\omega_{dc}t) \tag{2}$$

where $i_{dc}(0)$ is the initial DC current, and

$$\theta_{dc} = \arctan(\tau_{dc}\omega_{dc}), \tag{3}$$

$$\tau_{dc} = \frac{4L_0 + 6L_{dc}}{2R_0 + 3R_{dc}}, \tag{4}$$

$$\omega_{\mathrm{dc}} = \sqrt{\frac{2N(2L_0 + 3L_{\mathrm{dc}}) - C_0(2R_0 + 3R_{\mathrm{dc}})^2}{4C_0(2L_0 + 3L_{\mathrm{dc}})^2}}, \tag{5}$$

$$R_{\mathrm{dis}} = \sqrt{\frac{2N(2L_0 + 3L_{\mathrm{dc}}) - C_0(2R_0 + 3R_{\mathrm{dc}})^2}{36C_0}}. \tag{6}$$

## 3. DC Fault Analysis of MMC after Blocking

After blocking the MMC, the SM capacitor is no longer discharged. Therefore, the fault current from the AC system becomes the dominant component. Figure 4 shows the equivalent circuit of the MMC after it is blocked. The quantities marked with '∞' (i.e., $i_{\mathrm{a}\infty}$, $i_{\mathrm{pa}\infty}$, $I_{\mathrm{dc}\infty}$, ... ) are their steady state value. To simplify the analysis, short-circuit fault located at the outlet of the smoothing reactor is considered. In this way, the positive common point $B_{\mathrm{p}}$ and negative common point $B_{\mathrm{n}}$ are equipotential. Due to the symmetry of the diode rectifier circuit, it can be considered that point O′ is also equipotential with $B_{\mathrm{p}}$ and $B_{\mathrm{n}}$.

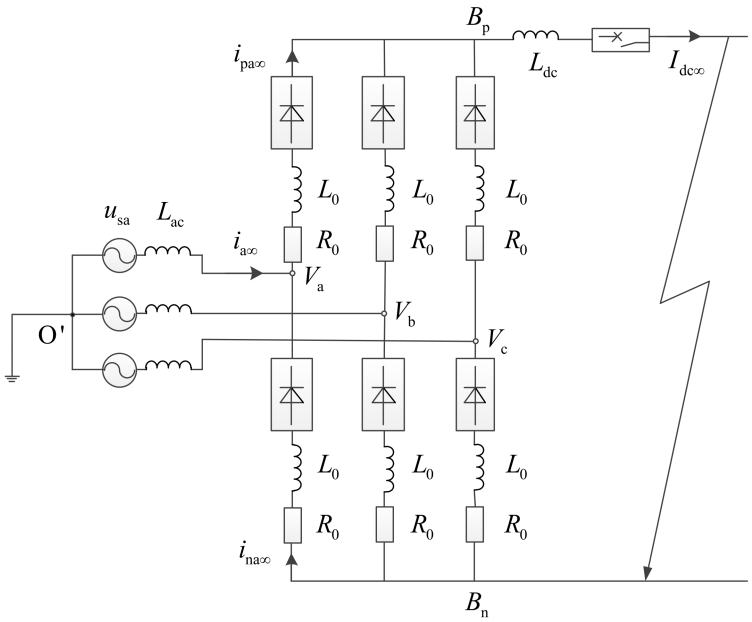


**Figure 4.** Equivalent circuit of MMC after it is blocked.

Take phase a as the example, the AC voltage is given by

$$u_{\mathrm{sa}}(t) = U_{\mathrm{sm}} \sin(\omega t + \eta_{\mathrm{sa}}) \tag{7}$$

According to the MMC operation principle [18], the upper and lower arm currents can be expressed as

$$\left.\begin{aligned} i_{\mathrm{pa}\infty}(t) &= A_0 + \sum_{n=1}^{\infty} A_n \sin(n\omega t + \varphi_n) \\ i_{\mathrm{na}\infty}(t) &= A_0 + \sum_{n=1}^{\infty} (-1)^n A_n \sin(n\omega t + \varphi_n) \end{aligned}\right\} \tag{8}$$

where $A_0$ and $A_n$ are DC component and $n$th harmonic component of the arm current. Based on the relation between arm current and output current [14], the expression of output current $i_{a\infty}$ can be written as

$$i_{\mathrm{a}\infty}(t) = i_{\mathrm{pa}\infty}(t) - i_{\mathrm{na}\infty}(t) = \sum_{n=2k-1}^{\infty} 2A_n \sin(n\omega t + \varphi_n) \tag{9}$$

where $k$ is the positive integer.

Applying Kirchhoff's voltage law (KVL) to phase a of Figure 4 yields

$$u_{\mathrm{sa}}(t) = L_{\mathrm{ac}}\frac{\mathrm{d}i_{\mathrm{a}\infty}}{\mathrm{d}t} + L_0\frac{\mathrm{d}i_{\mathrm{pa}\infty}}{\mathrm{d}t} \tag{10}$$

In (10) $R_0$ is ignored because it is very small; and it is considered that point O′ is equipotential with $B_{\mathrm{p}}$ and $B_{\mathrm{n}}$.

Inserting (7)–(9) to (10), the following expression is obtained

$$U_{\mathrm{sm}}\sin(\omega t + \eta_{\mathrm{sa}}) = L_{\mathrm{ac}}\sum_{n=2k-1}^{\infty} 2n\omega A_n\cos(n\omega t + \varphi_n) + L_0\sum_{n=1}^{\infty} n\omega A_n\cos(n\omega t + \varphi_n) \tag{11}$$

Comparing the left side and right side of (11), we know

$$A_1 = \frac{U_{\mathrm{sm}}}{2\omega L_{\mathrm{ac}} + \omega L_0} \tag{12}$$

$$\varphi_1 = -90^0 + \eta_{\mathrm{sa}} \tag{13}$$

$$A_n = 0(n = 2, 3, 4\cdots) \tag{14}$$

Therefore, the arm current is rewritten as

$$i_{\mathrm{pa}\infty}(t) = A_0 + A_1\sin(\omega t + \varphi_1) \tag{15}$$

Two characteristics of the diode rectifier circuit shown in Figure 4 are used to determine the value of $A_0$. The first characteristic is the unidirectional conductivity of the diode valve, which means $i_{\mathrm{pa}\infty}(t) \geq 0$. So, we have

$$A_0 \geq A_1 \tag{16}$$

The second characteristic is the presence of multiple zeroes in the diode valve current. In fact, for the diode rectifier circuit shown in Figure 4, when $R_0$ is considered, there exists a certain period of time that the arm current $i_{\mathrm{pa}\infty}(t)$ equals zero in each fundamental frequency cycle. Thus, we know

$$A_0 \leq A_1 \tag{17}$$

According to (16) and (17), the value of $A_0$ is given by

$$A_0 = A_1 \tag{18}$$

In this way, the arm current expression is

$$i_{\mathrm{pa}\infty}(t) = \frac{U_{\mathrm{sm}}}{2\omega L_{\mathrm{ac}} + \omega L_0}(1 - \cos(\omega t + \eta_{\mathrm{sa}})) \tag{19}$$

Then the steady-state DC fault current can be expressed as

$$I_{\mathrm{dc}\infty} = \frac{3U_{\mathrm{sm}}}{2\omega L_{\mathrm{ac}} + \omega L_0} \tag{20}$$

It should be noted that, the expression shown in (20) is the steady-state value after blocking the MMC. It takes a certain amount of time for DC current varying from the moment of blocking to the

steady state. This process can generally be described by a first-order inertia process. If we redefine the time starting point as the MMC blocking moment, the complete DC current expression can be given by

$$i_{\mathrm{dc}}(t) = I_{\mathrm{dc}\infty} + (I_{\mathrm{dc}B} - I_{\mathrm{dc}\infty})\mathrm{e}^{-\frac{t}{\tau_{\mathrm{dc}B}}} \tag{21}$$

where $I_{\mathrm{dc}B}$ is the initial DC current after MMC is blocked. $\tau_{\mathrm{dc}B}$ is the first-order inertia time constant, the value of which is closely related to the inductance of the smoothing reactor. For the practical project, $\tau_{dcB}$ is between 10 ms and 200 ms.

## 4. Three DC Fault Clearance Solutions and Corresponding Characteristics

In this section, three DC fault clearance solutions are presented, including (1) tripping the AC circuit breaker; (2) adopting the full-bridge SM-based MMC (F-MMC) and (3) employing the DC circuit breaker. Besides, the DC fault characteristics of these three solutions are analyzed in detail.

### *4.1. Solution 1: Tripping AC Circuit Breaker*

Tripping AC circuit breakers (ACCB) is a straightforward solution to clear DC faults for the MMC-HVDC. The DC fault clearance process can be divided into three states as follows.

State 1: Fault detection and DC blocking. After DC fault occurs, the DC current rises sharply. When the fault is detected, all the IGBTs of the MMC will be blocked. In this state the DC fault characteristics are the same as that presented in Section 2.

State 2: Trip the AC circuit breaker. After blocking the MMC, the tripping signal is sent to the ACCB. However, the response of the ACCB is slow, which requires about 60–100 ms. In this state the DC fault characteristics have been presented in Section 3.

State 3: Fault arc extinguishment. After the ACCB is tripped, the residual DC fault currents will gradually decay through the damping loop shown in Figure 5a. The operation circuit of Figure 5a is illustrated in Figure 5b. Solving the operation circuit, the following equation can be obtained

$$I_{\mathrm{dc}}(s) = \frac{\left(\frac{2}{3}L_0 + L_{\mathrm{dc}}\right)I_{\mathrm{dc}T}}{s\left(\frac{2}{3}L_0 + L_{\mathrm{dc}}\right) + \left(\frac{2}{3}R_0 + R_{\mathrm{dc}}\right)} \tag{22}$$

where $I_{\mathrm{dc}T}$ is the DC current at the moment when the ACCB is tripped. The Laplace inverse transform of (22) yields

$$i_{\mathrm{dc}}(t) = I_{\mathrm{dc}T}\mathrm{e}^{-\frac{t}{\tau_{\mathrm{dc}2}}} \tag{23}$$

where the decay time constant is

$$\tau_{\mathrm{dc}2} = \frac{2L_0 + 3L_{\mathrm{dc}}}{2R_0 + 3R_{\mathrm{dc}}} \tag{24}$$

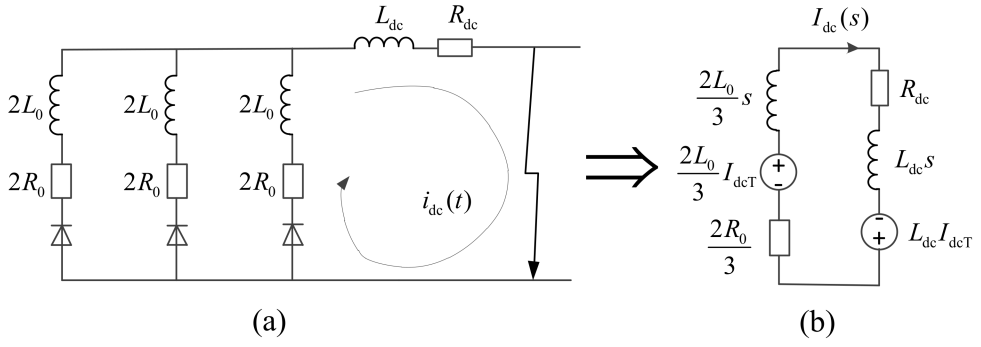


**Figure 5.** Circuit after the ACB is tripped. (**a**) Equivalent circuit; (**b**) Operation circuit.

When the residual DC fault current is less than the DC breaking current of the DC pole switch, the DC pole switch can then be tripped. However, as the decay time constant in (24) is large (more than 5 s), it may take a long time for the fault current to decrease to the threshold value.

### *4.2. Solution 2: Adopting F-MMC with DC Fault Clearance Capability*

Adopting converters with DC fault clearance capability is another alternative. The F-MMC is considered in this paper. The DC fault clearance process contains two states as follows.

State 1: Fault detection and DC blocking. When the fault is detected, all the IGBTs of the F-MMC will be blocked. Before blocking, the fault characteristics of the F-MMC are the same as that of the H-MMC proposed in Section 2.

State 2: Fast fault arc extinguishment. After the F-MMC is blocked, the current path in a full-bridge SM (FBSM) is shown in Figure 6. The back electromotive forces (EMFs) provided by the blocked FBSMs will impede the AC feeding current. The equivalent circuit of the system is depicted in Figure 7a. Figure 7b shows its operation circuit. The DC current can be given by solving the operation circuit

$$I_{\mathrm{dc}}(s) = \frac{s\left(L_{\mathrm{dc}} + \frac{2L_0}{3}\right) I_{\mathrm{dc}B} - U_{\mathrm{dc}B}}{s^2\left(\frac{2}{3}L_0 + L_{\mathrm{dc}}\right) + s\left(\frac{2}{3}R_0 + R_{\mathrm{dc}}\right) + \frac{2N}{3C_0}} \tag{25}$$

where $I_{\mathrm{dc}B}$ and $U_{\mathrm{dc}B}$ are the initial DC current and DC voltage after blocking the F-MMC. The Laplace inverse transform of (25) yields

$$i_{\mathrm{dc}}(t) = -\frac{1}{\sin\theta'_{\mathrm{dc}}} I_{\mathrm{dc}B} \mathrm{e}^{-\frac{t}{\tau_{\mathrm{dc3}}}} \sin\left(\omega'_{\mathrm{dc}} t - \theta'_{\mathrm{dc}}\right) - \frac{U_{\mathrm{dc}B}}{R'_{\mathrm{dis}}} \mathrm{e}^{-\frac{t}{\tau_{\mathrm{dc3}}}} \sin\omega'_{\mathrm{dc}} t \tag{26}$$

where

$$\theta'_{\mathrm{dc}} = \arctan\left(\tau_{\mathrm{dc3}}\omega'_{\mathrm{dc}}\right) \tag{27}$$

$$\tau_{\mathrm{dc3}} = \frac{4L_0 + 6L_{\mathrm{dc}}}{2R_0 + 3R_{\mathrm{dc}}} \tag{28}$$

$$\omega'_{\mathrm{dc}} = \sqrt{\frac{8N(2L_0 + 3L_{\mathrm{dc}}) - C_0(2R_0 + 3R_{\mathrm{dc}})^2}{4C_0(2L_0 + 3L_{\mathrm{dc}})^2}} \tag{29}$$

$$R'_{\mathrm{dis}} = \sqrt{\frac{8N(2L_0 + 3L_{\mathrm{dc}}) - C_0(2R_0 + 3R_{\mathrm{dc}})^2}{36C_0}} \tag{30}$$

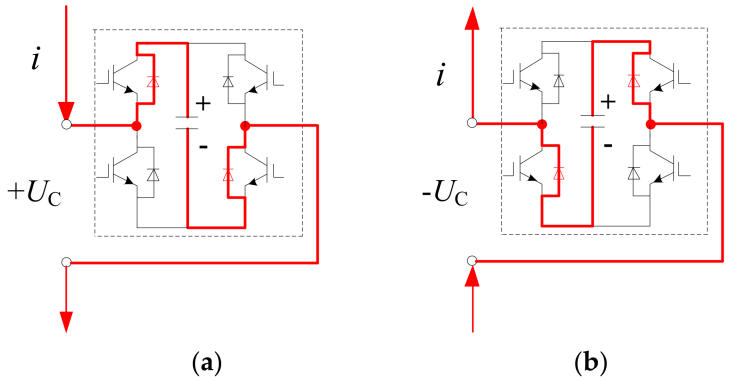


**Figure 6.** Current path in a full-bridge SM. (**a**) When the current is in positive direction; (**b**) When the current is in negative direction.

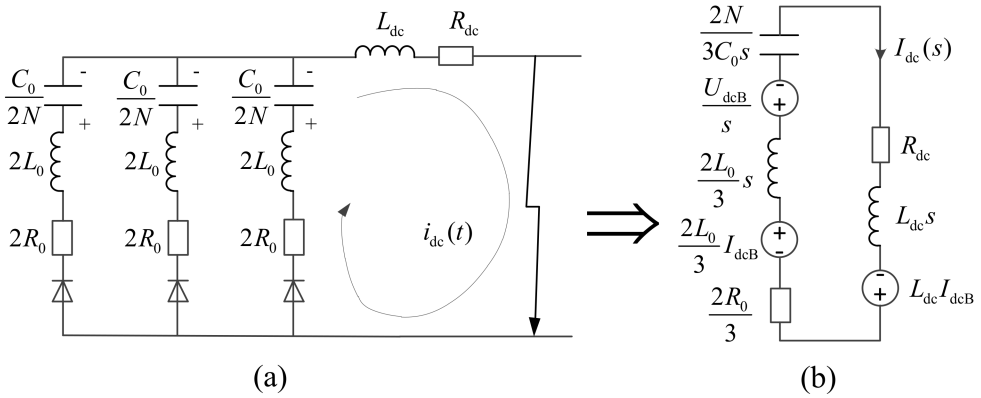


**Figure 7.** Circuit after the FMMC is blocked. (**a**) Equivalent circuit; (**b**) Operation circuit.

### *4.3. Solution 3: Adopting DC Circuit Breaker*

The third method to clear DC fault is employing the DC circuit breaker (DCCB). The hybrid DCCB proposed in [31] is used in this paper, whose basic structure is shown in Figure 8. This DCCB consists of a normal path and a fault path in parallel. In the normal path, a semiconductor-based load commutation switch (LCS) is in series with an ultra-fast disconnector (UFD). The fault path is formed by a main circuit breaker (MB). The procedure of isolating faulty lines is as follows:

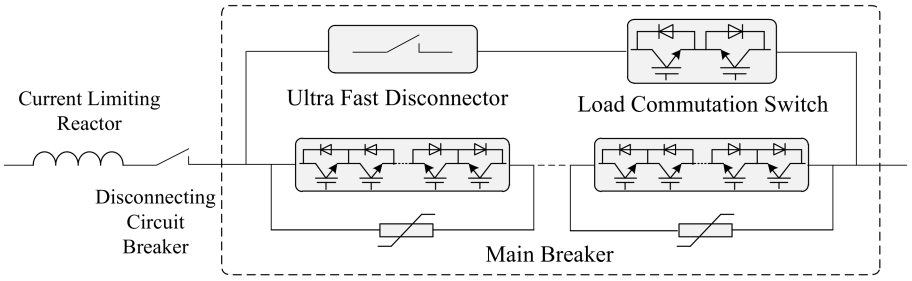


**Figure 8.** Structure of the hybrid HVDC breaker.

State 1: Fault detection. This state is the same as that proposed in Section 2.

State 2: Trip the DC circuit breaker. When a DC fault is detected, the LCS will open immediately and the current will be commutated to the MB. Then the UFD will open within 2 ms and isolate the LCS from the faulted line. With the UFD in open position, the MB will break the current. Finally, the remaining energy is consumed by the arrester banks. In fact, from the start action of the DCCB to MB breaks the current, the MMC still operates in the state presented in Section 2. This process lasts about 2.3 ms. After that, the DC current will decrease quickly due to the access of the arrester. Assume that the DC fault current decreases linearly to zero in a short time $\Delta t$. The expression of the current can be given by

$$i_{dc}(t) = -\frac{I_{dcT2}}{\Delta t}t + I_{dcT2} \tag{31}$$

where $I_{dcT2}$ is the initial DC current when MB is switched off.

## 5. Case Study

### *5.1. Test System*

To verify the accuracy and effectiveness of the analytical expressions derived in this paper, an MMC test system shown in Figure 9 is built in PSCAD/EMTDC. The main circuit parameters are

listed in Table 1. In steady state, the MMC is operated with constant active power control and constant reactive power control. The reference values are 400 MW and 0 Mvar respectively.

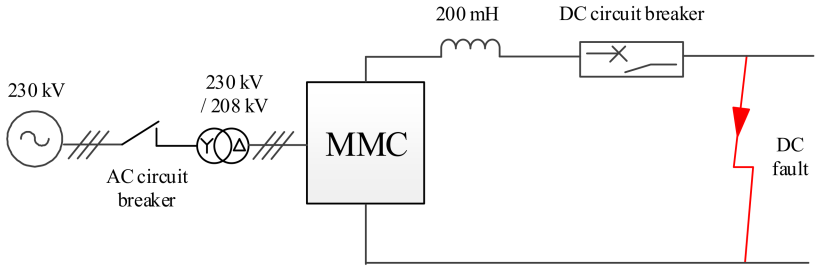


**Figure 9.** Structure of the hybrid HVDC breaker.

**Table 1.** Main Circuit Parameters of the MMC.

| Items | | Values |
|---|---|---|
| AC Side | Rated capacity | 400 MVA |
| | Grid side AC voltage | 230 kV |
| | Transformer MVA | 450 MVA |
| | Transformer ratio | 230 kV/208 kV |
| | leakage inductance | 10% |
| DC Side | Rated DC voltage | 400 kV |
| | Smoothing reactor | 200 mH |
| Converter | Number of SMs per arm | 20 |
| | SM capacitance | 666 μF |
| | Capacitor voltage | 20 kV |
| | Arm inductance | 76 mH |

### *5.2. Performances of MMC Before Blocking*

The system operates in steady state before the fault occurs. At $t$ = 2 s, a DC fault is applied to the DC side outlet of the MMC. Figure 10 shows the simulation result and the analytical result of the DC current. The fault current increases sharply after the DC fault. In 5 ms the fault current rises from 1 kA to over 8 kA. The results also show that the analytical result agrees well with the simulation one.

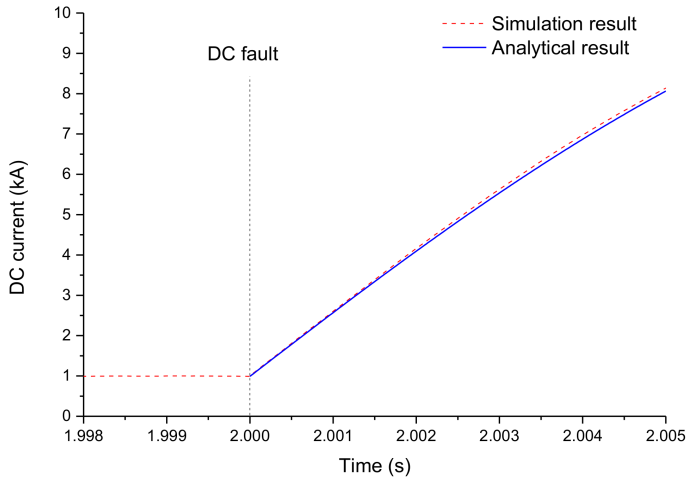


**Figure 10.** DC current of MMC before blocking.

It is a fact that the MMC will be blocked when the arm currents reach two times of IGBT rated value. Figure 11 illustrates the maximum current of the six arms. For this test system the rated current

of the IGBT is 1.5 kA. Therefore, the MMC will be blocked at $t$ = 2.00356 s as the arm current reaches 3.0 kA.

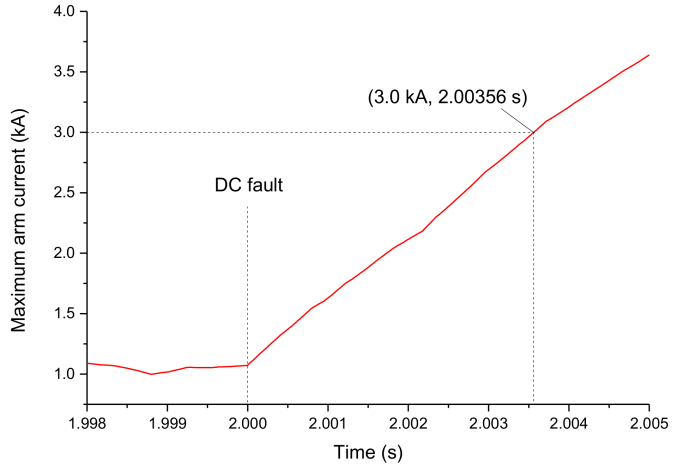


**Figure 11.** Maximum current of six arms of the MMC.

### *5.3. Performances of MMC after Blocking*

A DC fault occurs at $t$ = 2 s, and the MMC is blocked at $t$ = 2.00356 s. The DC currents obtained from the simulation and analytical expression (21) are shown in Figure 12. The two results are consistent with each other, and the error between them is very small. After blocking the MMC, the DC fault current increases to a steady value gradually. In addition, the steady-state DC fault current is about 11.5 kA.

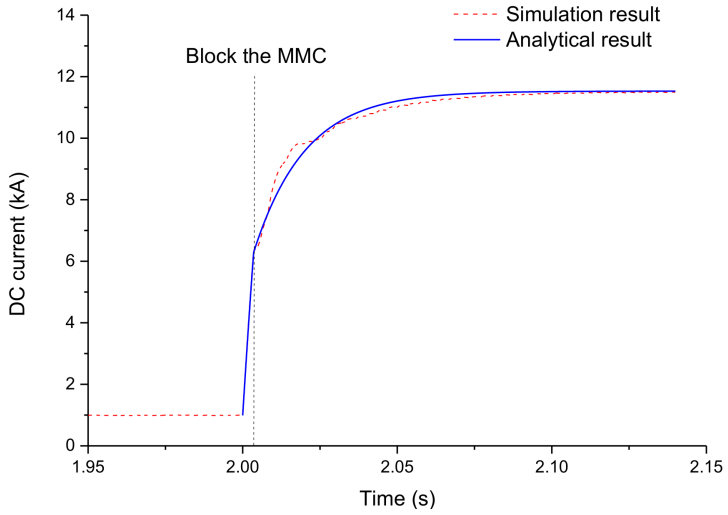


**Figure 12.** DC current of MMC after blocking.

### *5.4. Performances of MMC with Solution 1*

A DC fault occurs at $t$ = 2 s, and the MMC is blocked at $t$ = 2.00356 s. Considering the slow response of the AC circuit breaker, it is tripped at $t$ = 2.06 s. The results are illustrated in Figure 13. The fault current goes down in a very slow speed. It takes about 9258 ms for the fault current reduce to near zero (for example 200 A). The results show a strong agreement between the simulation and the analysis.

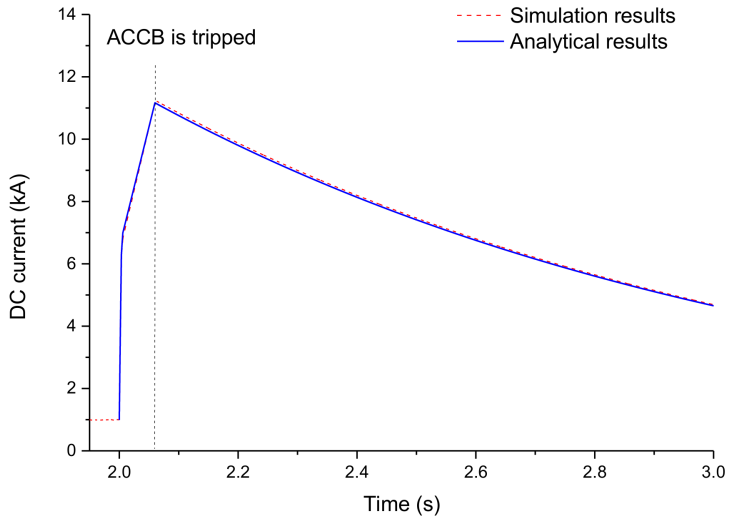


**Figure 13.** DC current of MMC with solution 1.

### *5.5. Performances of MMC with Solution 2*

In this case, the half-bridge SMs are replaced with full-bridge SMs, and the rest parts of the system remain unchanged. A DC fault occurs to the system at $t$ = 2 s, and the F-MMC is blocked at $t$ = 2.00356 s. Figure 14 shows the corresponding DC fault currents. It can be seen that there is some difference between the simulation result and the analytical result. The main reason is that the analytical expression given by (26) neglects the impact of the AC system. In fact, the AC voltage has influence to the decrease of the DC fault current, especially when the DC voltage is smaller than the amplitude of the AC phase voltage. The fault current reduces to zero in about 2.16 ms.

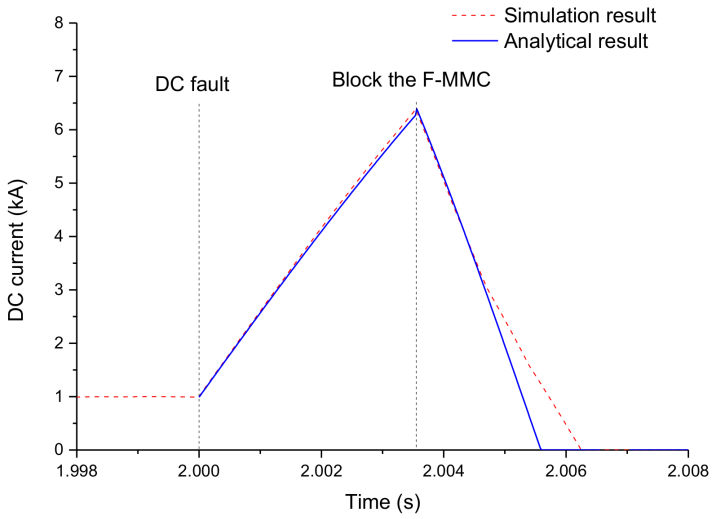


**Figure 14.** DC current of MMC with solution 2 when AC system is considered.

If the F-MMC is blocked and the ACCB is tripped at the same time, the AC system has no influence on the DC current. In addition, the corresponding fault currents given by simulation and analytical expression are shown in Figure 15. The results show that the results obtained by the two methods are consistent.

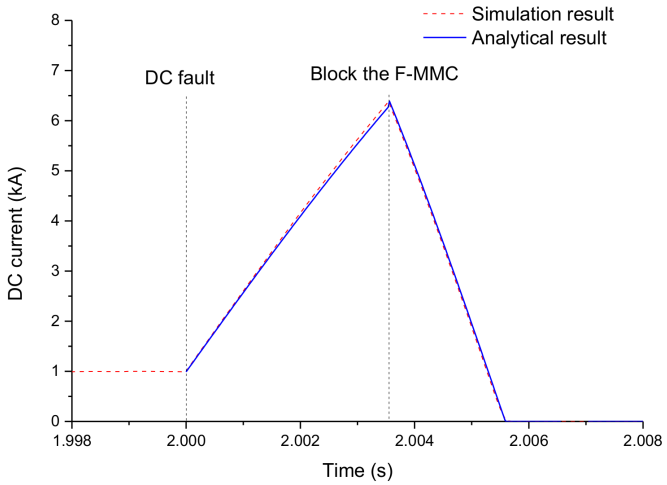


**Figure 15.** DC current of MMC with solution 2 when AC system is not considered.

### *5.6. Performances of MMC with Solution 3*

At $t$ = 2 s, a DC fault occurs at the DC side outlet of the MMC. The relay system completes the fault location detection in 1 ms, and a turn-off signal is sent to the LCS of the DCCB. At $t$ = 2.00125 s the LCS is opened and the UFD starts action. At $t$ = 2.0033 s the UFD is switched off and the MB is activated. Then the fault current will decrease quickly to zero due to the access of the arrester at $t$ = 2.00806 s. The DC fault currents are shown in Figure 16. As the faulty line is isolated at $t$ = 2.0033 s, the maximum arm current is less than the blocking threshold value. Therefore, the MMC will not be blocked. From the figure it can be seen that the analytical result agrees well with the simulation result, which proves the accuracy of the analytical expressions.

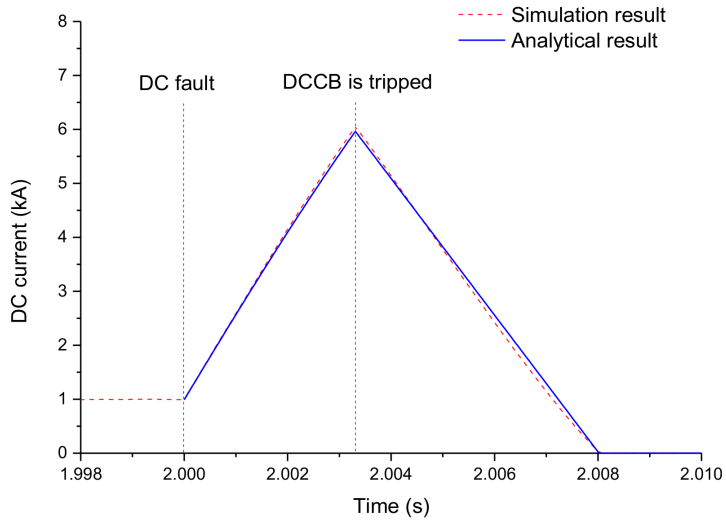


**Figure 16.** DC current of MMC with solution 3.

### *5.7. Comparison of Three Solutions*

Three key quantities of the system with different DC fault clearance solutions are list in Table 2, including the fault clearance time and the maximum fault current. It is seen that Solution 1 has the longest fault clearance time and the largest maximum fault current. Compared with Solution 2, the fault clearance time of Solution 3 is slightly larger but the maximum fault current is smaller. Among the three solutions, the converters under Solution 3 will not be blocked, which means the power can be continuously transmitted when a DC fault occurs in MMC-based DC grids.

**Table 2.** Key quantities of the system with different solutions.

| | Fault Clearance Time (ms) | Maximum Fault Current (kA) | Converter Blocked |
|---|---|---|---|
| Solution 1 | 9318 | 10.8 | Yes |
| Solution 2 | 6.26 | 6.4 | Yes |
| Solution 3 | 8.06 | 6.0 | No |

## 6. Conclusions

This paper analyzes the DC short-circuit fault of the MMC. By operation circuit in complex frequency domain, the analytical DC current expressions of the MMC under short-circuit fault are derived. Before the MMC is blocked, the DC fault current increases sharply and will reach the blocking threshold value in several milliseconds. After the MMC is blocked, the DC fault current will increase to the steady-state value gradually. Three DC fault clearance solutions and their characteristics are discussed in detail. Among these solutions, the fault clearance time of adopting F-MMC is the fastest. The solution of employing DC circuit breaker has the smallest maximum fault current, and the converters will not be blocked during fault period. An MMC model is developed in PSCAD/EMTDC, and the simulation results prove the accuracy and the feasibility of the proposed analytical expressions.

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## Appendix

The detailed derivation of inductor and capacitor operation circuit models are shown in this appendix. As for an inductor shown in the left side of Figure 2a, the voltage equation can be given by

$$u(t) = L\frac{\mathrm{d}i(t)}{\mathrm{d}t} \tag{A1}$$

Applying Laplace transformation to (A1) yields

$$U(s) = L(sI(s) - i(0)) = sLI(s) - Li(0) \tag{A2}$$

From (A2) the inductor operation circuit is obtained in the right side of Figure 2a.
Similarly, as for a capacitor shown in the left side of Figure 2b, the current equation is given by

$$i(t) = C\frac{\mathrm{d}u(t)}{\mathrm{d}t} \tag{A3}$$

Applying Laplace transformation to (A3) yields

$$I(s) = C(sU(s) - u(0)) = sCU(s) - Cu(0) \tag{A4}$$

Solving (A4), the capacitor voltage can be expressed as

$$U(s) = \frac{1}{sC}I(s) + \frac{u(0)}{s} \tag{A5}$$

From (A5) the capacitor operation circuit is obtained in the right side of Figure 2b.

## References


1. Flourentzou, N.; Agelidis, V.G.; Demetriades, G.D. VSC-based HVDC power transmission systems: An overview. *IEEE Trans. Power Electron.* **2009**, *24*, 592–602. [CrossRef]
2. Pinto, R.T.; Bauer, P.; Rodrigues, S.F.; Wiggelinkhuizen, E.J.; Pierik, J.; Ferreira, B. A Novel Distributed Direct-Voltage Control Strategy for Grid Integration of Offshore Wind Energy Systems through MTDC Network. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2429–2441. [CrossRef]
3. Marquardt, R. Stromrichterschaltungen Mit Verteilten Energiespeichern. German Patent DE10103031A1, 24 January 2001.
4. Tu, Q.; Xu, Z. Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter. *IEEE Trans. Power Deliv.* **2011**, *26*, 298–306. [CrossRef]
5. Debnath, S.; Qin, J.; Bahrani, B.; Saeedifard, M.; Barbosa, P. Operation, Control, and Applications of the Modular Multilevel Converter: A Review. *IEEE Trans. Power Electron.* **2015**, *30*, 37–53. [CrossRef]
6. Saeedifard, M.; Iravani, R. Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System. *IEEE Trans. Power Deliv.* **2010**, *25*, 2903–2912. [CrossRef]
7. Xue, Y.; Xu, Z.; Tang, G. Self-Start Control with Grouping Sequentially Precharge for the C-MMC-Based HVDC System. *IEEE Trans. Power Deliv.* **2014**, *29*, 187–198. [CrossRef]
8. Solas, E.; Abad, G.; Barrena, J.A.; Aurtenetxea, S.; Cárcar, A.; Zając, L. Modular Multilevel Converter with Different Submodule Concepts—Part II: Experimental Validation and Comparison for HVDC Application. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4536–4545. [CrossRef]
9. Westerweller, T.; Friedrich, K.; Armonies, U.; Orini, A.; Parquet, D.; Wehn, S. Trans bay cable-world's first HVDC system using multilevel voltage-sourced converter. In Proceedings of the CIGRE Session, Paris, France, 22–27 August 2010.
10. Li, C.; Hu, X.; Guo, J.; Liang, J. The DC grid reliability and cost evaluation with Zhoushan five-terminal HVDC case study. In Proceedings of the 2015 50th International Universities Power Engineering Conference (UPEC), Stoke-on-Trent, UK, 1–4 September 2015.
11. Nicolosi, M. Wind power integration and power system flexibility—An empirical analysis of extreme events in Germany under the new negative price regime. *Energy Policy* **2010**, *38*, 7257–7268. [CrossRef]
12. Gnanarathna, U.N.; Gole, A.M.; Jayasinghe, R.P. Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs. *IEEE Trans. Power Deliv.* **2011**, *26*, 316–324. [CrossRef]
13. Xu, J.; Zhao, C.; Liu, W.; Guo, C. Accelerated Model of Modular Multilevel Converters in PSCAD/EMTDC. *IEEE Trans. Power Deliv.* **2013**, *28*, 129–136. [CrossRef]
14. Xiao, H.; Xu, Z.; Tang, G.; Xue, Y. Complete mathematical model derivation for modular multilevel converter based on successive approximation approach. *IET Power Electron.* **2015**, *8*, 2396–2410. [CrossRef]
15. Guan, M.; Xu, Z. Modeling and Control of a Modular Multilevel Converter-Based HVDC System under Unbalanced Grid Conditions. *IEEE Trans. Power Electron.* **2012**, *27*, 4858–4867. [CrossRef]
16. Bergna, G.; Berne, E.; Egrot, P.; Lefranc, P.; Arzande, A.; Vannier, J.C.; Molinas, M. An Energy-Based Controller for HVDC Modular Multilevel Converter in Decoupled Double Synchronous Reference Frame for Voltage Oscillation Reduction. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2360–2371. [CrossRef]
17. Tu, Q.; Xu, Z.; Chang, Y.; Guan, L. Suppressing DC Voltage Ripples of MMC-HVDC under Unbalanced Grid Conditions. *IEEE Trans. Power Deliv.* **2012**, *27*, 1332–1338. [CrossRef]
18. Ilves, K.; Antonopoulos, A.; Norrga, S.; Nee, H.P. Steady-State Analysis of Interaction between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2012**, *27*, 57–68. [CrossRef]
19. Song, Q.; Liu, W.; Li, X.; Rao, H.; Xu, S.; Li, L. A Steady-State Analysis Method for a Modular Multilevel Converter. *IEEE Trans. Power Electron.* **2013**, *28*, 3702–3713. [CrossRef]
20. Rafferty, J.; Xu, L.; Morrow, D.J. DC fault analysis of VSC based multi-terminal HVDC systems. In Proceedings of the 10th IET International Conference on AC and DC Power Transmission (ACDC 2012), Birmingham, UK, 4–5 December 2012.
21. Yang, J.; Fletcher, J.E.; O'Reilly, J. Short-circuit and ground fault analyses and location in VSC-based DC network cables. *IEEE Trans. Ind. Electron.* **2012**, *59*, 3827–3837. [CrossRef]

22. Vidal-Albalate, R.; Beltran, H.; Rolán, A.; Belenguer, E.; Peña, R.; Blasco-Gimenez, R. Analysis of the Performance of MMC Under Fault Conditions in HVDC-Based Offshore Wind Farms. *IEEE Trans. Power Deliv.* **2016**, *31*, 839–847. [CrossRef]
23. Zhang, Z.; Xu, Z. Short-circuit current calculation and performance requirement of HVDC breakers for MMC-MTDC systems. *IEEJ Trans. Electr. Electron. Eng.* **2016**, *11*, 168–177. [CrossRef]
24. Qin, J.; Saeedifard, M.; Rockhill, A.; Zhou, R. Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits. *IEEE Trans. Power Deliv.* **2015**, *30*, 385–394. [CrossRef]
25. Li, C.; Zhao, C.; Xu, J.; Ji, Y.; Zhang, F.; An, T. A Pole-to-Pole Short-Circuit Fault Current Calculation Method for DC Grids. *IEEE Trans. Power Syst.* **2017**, *32*, 4943–4953. [CrossRef]
26. Li, B.; He, J.; Tian, J.; Feng, Y.; Dong, Y. DC fault analysis for modular multilevel converter-based system. *J. Mod. Power Syst. Clean Energy* **2017**, *5*, 275–282. [CrossRef]
27. Tang, G.; Xu, Z.; Zhou, Y. Impacts of Three MMC-HVDC Configurations on AC System Stability under DC Line Faults. *IEEE Trans. Power Syst.* **2014**, *29*, 3030–3040. [CrossRef]
28. Liu, G.; Xu, F.; Xu, Z.; Zhang, Z.; Tang, G. Assembly HVDC Breaker for HVDC Grids with Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2017**, *32*, 931–941. [CrossRef]
29. Lin, W.; Jovcic, D.; Nguefeu, S.; Saad, H. Full-Bridge MMC Converter Optimal Design to HVDC Operational Requirements. *IEEE Trans. Power Deliv.* **2016**, *31*, 1342–1350. [CrossRef]
30. Modeer, T.; Nee, H.P.; Norrga, S. Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications. In Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 30 August–1 September 2011.
31. Callavik, M.; Blomberg, A.; Häfner, J.; Jacobson, B. *The Hybrid HVDC Breaker*; ABB Grid Systems Technical Paper; ABB: Zurich, Switzerland, 2012.