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Efficient Low-Cost IBC Solar Cells with a Front Floating Emitter: Structure Optimization and Passivation Layer Study

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Abstract: In this paper, we investigate interdigitated back contact solar cells with the front floating emitter structure systematically by using simulated and experimental methods. By comparing the front floating emitter structure with the front surface field structure, it is found that the efficiency of solar cells with the front surface field structure quickly reduces with the increasing of back surface field width; while solar cells with the front floating emitter structure can have a wider front surface field width range with minimum impact on the cell efficiency. More importantly, solar cells with the front floating emitter structure have a larger fabrication process tolerance, especially for the back surface field width, emitter width, and the bulk resistivity, which means that the fabrication process flow can be simplified and the production cost can be reduced. Based on the above results, large area (156.75 mm × 156.75 mm) interdigitated back contact solar cells with the front floating emitter structure are fabricated by using the simplified process with only one masking step. SiO_x:B is used as the passivation layer, which can lead to a higher open circuit voltage and lower surface saturation current density. Finally, an efficiency of 20.39% is achieved for the large area solar cells.

Keywords: solar cells; interdigitated back contact; front floating emitter; SiO_x:B; passivation

1. Introduction

Interdigitated back contact (IBC) crystalline silicon solar cells are attracting much attention in the solar cells research society due to their potential to achieve a high power conversion efficiency by eliminating the shading losses altogether through putting both contacts on the rear of the cells [1,2]. Many institutes such as Fraunhofer ISE, ECN, and ISC-Konstanz are now working on IBC solar cells and their commercialization [3,4]. Some manufacturers such as SunPower and Trina have achieved over 24% efficiency on large area solar cells [5,6]. However, there are still many challenges for IBC solar cells, like a complex process flow and accurate alignment requirement compared with standard Al back surface field (Al-BSF) silicon solar cells, which increase the fabrication cost and become the bottleneck in mass production of IBC solar cells. To solve these problems, optimization of cell structure, simplification of process flow, and reduction of production cost have become the hot topics in IBC solar cells.

For conventional IBC solar cells, there is an n^+-doped layer that forms the front surface field (FSF) on the front and the emitter to collect the minority carriers on the rear side separated by the non-collection area (BSF). The minority carriers generated in the region above BSF need to be

transported laterally to the emitter region for collection. For a wide BSF width design, the travel distance of minority carriers generated in the region above BSF increases and the collection efficiency will be weak. Hermle et al. [7] called this effect an electrical shading effect. Due to the electric shading effect, the BSF width of FSF IBC solar cells should be less than 0.4 mm [8]. Narrow BSF width design means that a high accuracy pattern alignment is required, which will make the IBC solar cell process more complex and costly.

The front floating emitter (FFE) structure can be one optional solution to the electric shading effect. FFE structure with a p^+ doped front surface floating junction instead of an n^+ region on the front side can effectively reduce the composite loss caused by the minority carrier transversal transport process [9,10]. In FFE IBC solar cells, the holes generated in the region above BSF move to the nearest FFE, then laterally transport in the FFE, and finally reach the back emitter [8]. There is a lot of research work about the IBC solar cells with the FSF structure; however, the work about FFE IBC solar cells is relatively less abundant [7,11–13].

In this paper, we investigate FFE IBC solar cells systematically by using the simulated and experimental methods. By comparing the FFE structure with the FSF structure, it is found that FFE IBC solar cells can have a wider BSF width range with minimum impact on the cell efficiency. More importantly, FFE IBC solar cells have a larger structural parameter tolerance, especially for the BSF width, emitter width, and bulk resistivity, which means that the fabrication process flow could be simplified and the production cost is reduced. Based on the above results, we use a simplified process to fabricate large area (156.75 mm × 156.75 mm) FFE IBC cells with only one masking step. By using the SiO_x:B as the passivation layer, an efficiency of 20.39% is achieved.

2. Simulation Results and Discussion

2.1. Carrier Transport Properties

We first investigate the minority carrier transport properties of both FSF and FFE IBC solar cells. Quokka 2D software was used for the simulation study. Figure 1 shows the cross-section of FFE IBC solar cells. The difference for the FSF IBC solar cells is that there is a front surface field instead of the floating emitter. Table 1 shows the parameters used in the simulation.

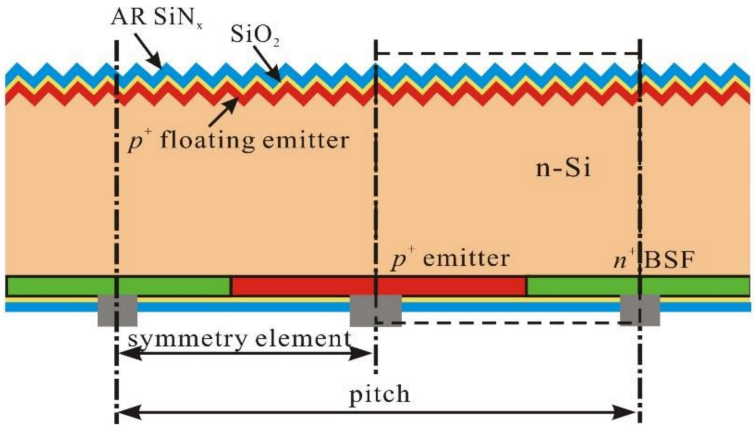


Figure 1. Cross-section of FFE IBC solar cells. The dashed box indicates the unit cells used in the device simulations.

Table 1. Parameters used in this simulation work.

Parameter Name	Value
cell thickness	190
emitter diffusion half width	400

Table 1. *Cont.*

Parameter Name	Value
base diffusion half width	300
emitter contacts width	60
base contact width	60
n-type bulk resistivity	10 Ω·cm
bulk lifetime	2 ms
emitter diffusion sheet resistance	90 Ω/□
base diffusion sheet resistance	70 Ω/□
FSF sheet resistance	100 Ω/□
FFE sheet resistance	100/200 Ω/□
emitter diffusion J_0-passivated	40 fA/cm^2
emitter diffusion J_0-contacted	80 fA/cm^2
base diffusion J_0-passivated	50 fA/cm^2
base diffusion J_0-contacted	100 fA/cm^2
front diffusion J_0	30 fA/cm^2
emitter contact resistance	$<1 \times 10^{-6}$ Ω·cm^2
base contact resistance	1×10^{-4} Ω·cm^2
external series resistance	0.38 Ω·cm^2
effective intrinsic carrier density ni, eff	9.65×10^9 cm^{-3}

Figure 2a shows the calculated holes density gradient in the FSF structure. As is shown, the holes generated above the BSF have to move to the emitter region. The doped front surface produces a space charge region that drives the holes to move along the n-type silicon substrate toward the emitter. Usually, the transport path of the holes is much longer than the thickness of the silicon wafer, and recombination will inevitably occur during the transport process.

Figure 2b shows the calculated holes density gradient in the FFE structure. In the FFE structure, both the front surface floating junction and the back emitter can collect holes. The hole concentration of the front surface is higher than the back emitter hole concentration, so the transport process mainly depends on the FFE. The holes generated above the BSF region are collected by the front surface FFE first, and then propagate in the FFE to the region above the back emitter. Because there is a concentration gradient, the holes are re-injected to the back emitter, and collected by rear metal grids. This phenomenon, of holes passing through the FFE laterally and then being collected by the back emitter, is called the "pumping effect" [14]. Compared with the FSF structure, the recombination in the FFE structure will be smaller when the BSF width is large and then the carrier collection efficiency becomes larger, which will lead to a high solar cell efficiency.

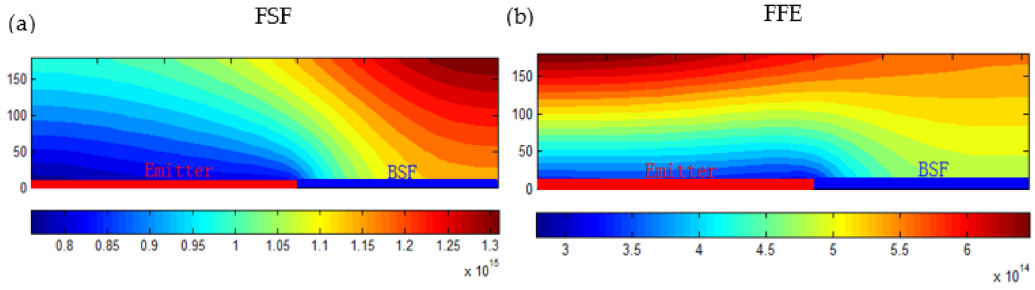


Figure 2. Gradient of the holes density in the simulated IBC cell structures: (**a**) FSF and (**b**) FFE.

2.2. Effects of BSF Width on Solar Cell Efficiency

To investigate the effects of BSF width on the cell efficiency of both FSF and FFE IBC solar cells, the emitter width is fixed and the efficiency change with different BSF widths is shown in Figure 3. It can be seen that in both FSF and FFE structures, a narrower BSF produces a higher solar cell efficiency.

Particularly, in the FSF structure, with the increase of the BSF width, the minority carrier transport path increases greatly, and the electrical shading loss leads to the rapid decrease of the solar cell efficiency, as shown in Figure 3. To avoid this effect, the typical BSF width for the FSF structure cell should be 0.2–0.4 mm. In the FFE structure, with the increase of BSF width, solar cell efficiency decreases at a much slower rate, i.e., the impact of BSF width is less in the FFE structure compared to the FSE structure. We also simulated FFE IBC solar cells with different front floating emitter sheet resistance. It can be seen from Figure 3, when increasing the sheet resistance from 100 Ω/sq to 200 Ω/sq, for 1 mm BSF width design, that cell efficiency only reduces by 0.05%. This indicates that the front surface emitter doping concentration can vary within a wide range with minimal impact on the solar cell conversion efficiency and thus the FFE structure has a wide process window, which is good, especially for mass production.

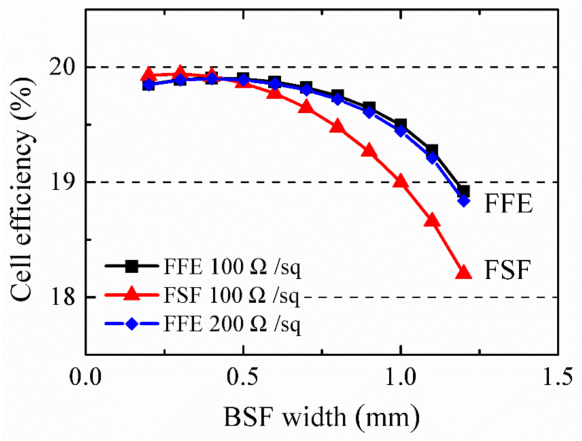


Figure 3. Efficiency of FFE IBC and FSF IBC cells with different BSF widths. Also shows the cell efficiency for different FFE sheet resistance values.

2.3. Influence of Different Resistivity and Emitter Width on FFE IBC Solar Cells

The emitter width ratio is an important factor which can affect the short-circuit current density and series resistance of IBC solar cells. When the BSF width is fixed, the increasing of the emitter width ratio means the increasing of the pitch width. Short-circuit current density J_{sc} [15] can be given by:

$$J_{sc} = J_{sc,\text{int}} - \Delta J_{opt} - \Delta J_{rec} \tag{1}$$

where $J_{sc,\text{int}}$ is the intrinsic short circuit current density, ΔJ_{opt} is the short current density loss due to optical effects (reflection, transmission, and parasitic absorption etc.), and ΔJ_{rec} is the short-circuit current density loss due to recombination. ΔJ_{rec} can be further divided into $\Delta J_{rec,\ emitter}$ and $\Delta J_{rec,\ shad}$, which are the recombination loss due to the emitter and recombination loss due to electrical shadow, respectively [16]. $\Delta J_{rec,\ shad}$ depends on pitch width, which can be given by:

$$\Delta J_{rec.\text{shad}}(Pitch) = \frac{\alpha_{el.\text{shad}}}{Pitch} \tag{2}$$

where $\alpha_{el.\text{shad}}$ is the short-circuit current density loss due to recombination of the base, which is electrical shadow loss.

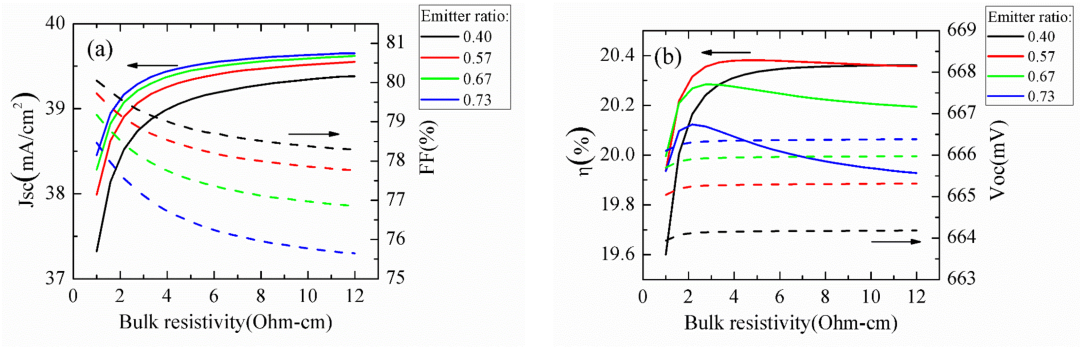
From Equations (1) and (2), $J_{sc} = J_{sc,\text{int}} - \Delta J_{opt} - \Delta J_{rec.\text{emitter}} - \frac{\alpha_{el.\text{shad}}}{Pitch}$, and J_{sc} increases with pitch width.

Series resistance of IBC solar cells can be given as:

$$R_s(V, Pitch) = R_{s,0}(V) + R_{s,1}(V, Pitch) \tag{3}$$

$R_{s,0}(V)$ includes the bulk resistance of vertical direction of the substrate, BSF resistance, contact resistance, and metal grids resistance [17]. $R_{s,1}(V, Pitch)$ is the series resistance depending on the pitch width, including the emitter resistance and the lateral transmission resistance. $R_{s,base,lateral} = \frac{1}{12}\frac{\rho_{base}}{d_{wafer}} \times (a_{n-n})^2$, where d_{wafer} is the wafer thickness, a_{n-n} is the distance between the n^+ and n^+ doped regions, and ρ_{base} is the base resistivity. As the pitch width increases (a_{n-n} increases), the cells' lateral transmission resistance increases and the cells' series resistance increases.

Figure 4 shows solar cell electrical parameters with different emitter width ratio and bulk resistivity values. In the simulation, the BSF area width is fixed at 600 µm, considering the alignment accuracy of the low-cost equipment like the screen printer. The pitch widths of the solar cell structure are 1000 µm, 1400 µm, 1800 µm, and 2200 µm with the corresponding emitter width ratio of 0.40, 0.57, 0.67, and 0.73, respectively. In Figure 4a, with the same resistivity, when the emitter width ratio increases, J_{sc} increases gradually because the increase in emitter width favours the collection of minority carriers. But when the emitter is wider, the transport path of the majority carriers generated in this region is also increased correspondingly, making the transport path larger than the thickness of the solar cell. From Equation (3), it results in an increase in the series resistance and causes a decrease in FF. In Figure 4b, the emitter size increases as the emitter width ratio increases, so that the back surface passivation effect is also increased, resulting in an increase in V_{oc}. For the same emitter width ratio, since V_{oc} is more dependent with the doping process, the simulation uses the same doping process, so as the resistivity increases, V_{oc} remains unchanged. The simulation results show that for the emitter width ratio of 0.57 and corresponding pitch width of 1400 µm, the wafer resistivity can vary between 3 Ω·cm and 12 Ω·cm.



(**a**) (**b**)

Figure 4. Solar cell electrical parameters with different emitter width ratio and bulk resistivity values. (**a**) Change in J_{sc} and FF with different emitter width ratio and bulk resistivity values; (**b**) Change in Efficiency and V_{oc} with different emitter width ratio and bulk resistivity values.

3. Experimental Results and Analysis

We used large area 156.75 mm × 156.75 mm Czochralski n-type monocrystalline silicon wafers for the experiments. The wafer thickness was 190 µm, and the wafer bulk lifetime was 2 ms. Two different resistivity wafers were used: 3 Ω·cm and 10 Ω·cm.

The process flow is shown in Figure 5. First, the wafers are saw damage etched and cleaned, and then the texturing was done by KOH solution to form random pyramids. $POCl_3$ diffusion was used to form BSF on the rear side. After cleaning, the SiN_x mask was deposited by using PECVD. Laser ablation was used to form the emitter area, and a single side etching step was used to remove the phosphorous diffusion at the laser ablation area. A tube diffusion furnace tube was used to form the FFE on the front surface of the silicon wafer, and also to form the emitter at the rear side. PECVD deposited SiN_x layers were used as passivation and antireflective coating. Finally, screen printing metallization was used for IBC solar cells.

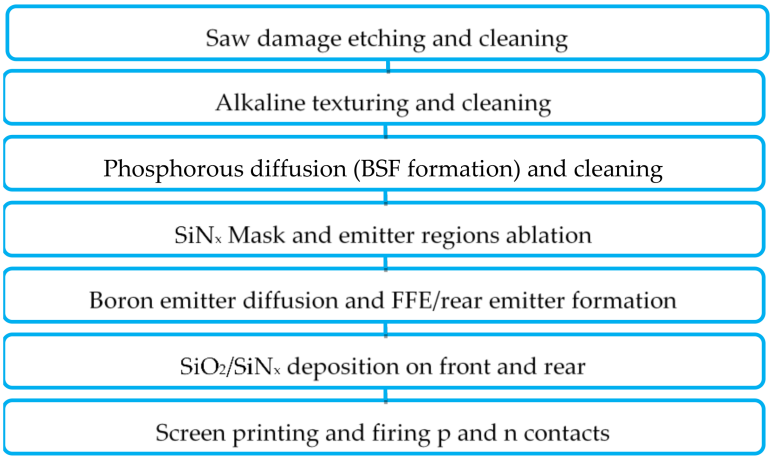


Figure 5. Flow chart of the cells fabrication process steps.

The experiment uses low-cost and simple production process, and the SiO_x:B (boron-containing silicon oxide) is used as the passivation layer. In the process of boron diffusion, first, a layer of BSG was deposited on the surface of the silicon wafer at low temperature (870 °C–920 °C), then oxidized and driven-in at high temperature (950 °C–1000 °C) in oxygen atmosphere. 1% HF was used to remove a certain thickness of BSG layer, and the remaining SiO_x:B layer was used as the passivation layer.

3.1. Influence of Thickness of SiO_x:B Layer on Optical Properties

We conducted a simulation to study the influence of thickness of the SiO_x:B layer on the optical properties. The incident light passes through the SiN_x/SiO_x:B structure to the doped silicon with a refractive index of 3.86. The refractive index of the upper SiN_x antireflection layer is 2.05–2.12, and the refractive index of the lower SiO_x:B passivation layer is 1.46. This structure causes the refractive index mismatch, which makes the SiN_x/SiO_x:B less reflective. The OPAL2 software was used to simulate the thickness matching of SiO_x:B and SiN_x layers. The reflectance, absorbance, and transmittance of different SiN_x/SiO_x:B structures are shown in Table 2.

Table 2. Effect of different SiO_x:B layer thicknesses on the optical properties.

SiO_x:B Thickness (nm)	SiN_x Thickness (nm)	Reflectance (%)	Absorption (%)	Transmittance (%)
5	74	4.1	0.5	95.4
10	71	4.3	0.5	95.2
15	67	4.6	0.5	94.9
20	64	5	0.5	94.5
25	60	5.3	0.5	94.2
30	57	5.8	0.5	93.7

From the simulation, the smaller the thickness of the SiO_x:B layer, the better the transmittance of the SiN_x/SiO_x:B laminate structure. While the SiO_x:B layer is thinner, the optimized SiN_x thickness is closer to the optimized single SiN_x layer, and the reflectivity of the reflected light at the SiN_x and SiO_x:B interfaces is lower.

3.2. Effect of SiO_x:B Layer Thickness on Passivation Quality

The $p^+/n/p^+$ symmetrical test structure is shown in Figure 6, which is used to test the passivation quality of different SiO_x: B thicknesses. J_{0E} and implied V_{oc} were measured with the Sinton WCT-120 at a 1×1016 cm^{-3} injection level, as shown in Figure 7.

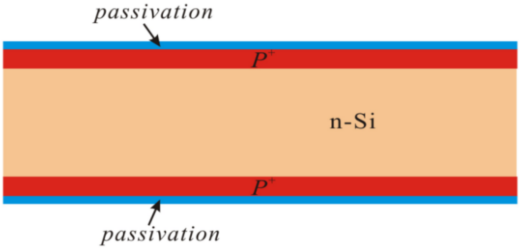


Figure 6. Symmetric structure for passivation quality test.

As shown in Figure 7, when the SiO_x:B layer thickness is below 20 nm, implied V_{oc} decreases with the decrease of SiO_x:B layer thickness. When the SiO_x:B layer thickness is 20 nm or above, J_{0E} and implied V_{oc} (reaches over 700 mV) remain unaffected with the different SiO_x:B layer thicknesses, showing a good and stable passivation quality. This is because, when the SiO_x:B is thin, its structure is not dense, and there are pinhole and induced defects. However, when the SiO_x:B thickness is 20 nm or above, the SiO_x:B layer becomes dense and it can effectively passivate the interface and prevent the effect of the external environment on the SiO_x:B/Si interface.

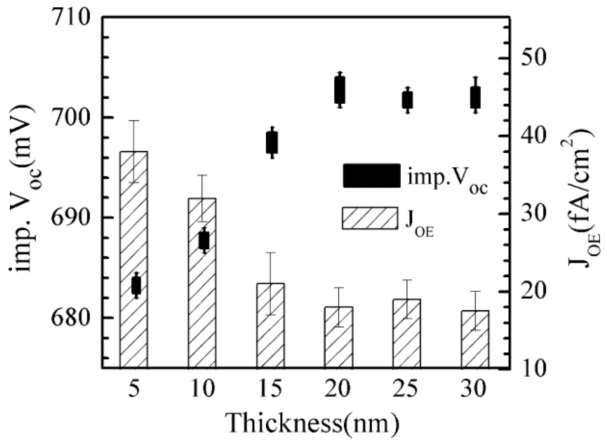


Figure 7. J_{0E} and implied V_{oc} change with SiO_x:B thickness.

On one hand, in order to achieve a better optical transmittance, the SiO_x:B layer should be as thin as possible. On the other hand, in order to achieve a good passivation effect, the SiO_x:B layer should be thicker than 20 nm. To balance the two sides, the optimum thickness of the SiO_x:B layer is 20 nm.

3.3. Comparison of Passivation Effect of Different Passivation Layers

Using the same symmetrical passivation structure shown in Figure 6, we compared four different passivation layers that are commonly used in industrial production. The silicon wafers are alkaline polished and boron diffused with a sheet resistance of 92 Ω/□ on both sides. Then, the samples were passivated by AlO_x (PECVD), SiO_x:B, thermal oxidation SiO_2, and wet chemical SiO_2 (NAOS), respectively. After passivation, the samples were capped on both sides with SiN_x, and the passivation layer was activated with a firing furnace. J_{0E} and implied V_{oc} were measured with the Sinton WCT-120 at a 1×10^{16} cm^{-3} injection level, as shown in Figure 8.

The wet chemical grown SiO_2 thickness is only 5 nm–10 nm, and the SiO_x:B passivation quality is much better than NAOS. In addition, the SiO_x:B passivation layer is grown at a high concentration of pure oxygen during the drive-in process of boron diffusion. On the other hand, the concentration of boron oxide in the BSG has been very low, which will greatly improve the melting point of BSG. The diffusion rate of SiO_2 at the BSG/Si interface is higher than that of boron at the BSG/Si interface, so that the growth rate of SiO_2 is larger than the boron diffusion rate in the BSG. Therefore, the impurity

content of SiO_2 at the silicon surface is very low, and the quality of the SiO_2 layer can reach a similar level of thermal oxidation.

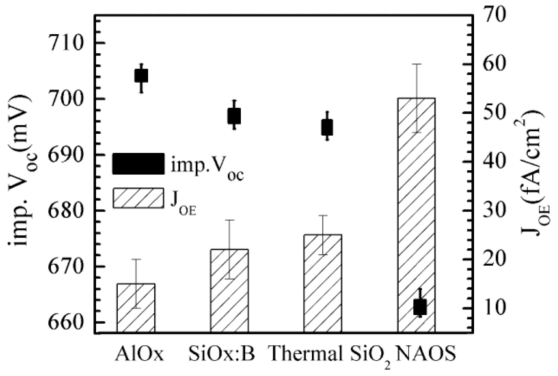


Figure 8. Comparison of J_{0E} and implied V_{oc} with different passivation layers.

Since the SiO_x:B passivation layer growth process can be integrated in the Boron diffusion process, the IBC solar cell process flow can be simplified and it can effectively reduce the production costs. In addition, previous study found that for IBC cell structure, the use of AlO_x as emitter passivation will cause large efficiency degradation with reverse voltage, while the SiO_x:B passivation layer did not find similar degradation [18]. Thus, the SiO_x:B passivation layer is a good choice for the passivation.

Finally, solar cells were formed the base on the above simulation and passivation results using two different resistivity wafers. Table 3 shows the IV results of the cells. For high resistivity wafers, the impurity doped in the wafers is less and the solar cell short-circuit current density increases, while FF decreases with higher resistivity. The experiment results have a good match with the simulation results, as shown in Figure 4.

Table 3. IV results of FFE IBC cells.

Resistivity (Ω·cm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
3	663.1	39.02	78.5	20.31
10	662.9	39.54	77.8	20.39

4. Conclusions

In this paper, we investigated the structure systematically for low cost FFE IBC solar cells. In the FFE structure, the front surface emitter has a pumping effect, which can increase the minority carrier lateral transport, and the electric shading effect is relatively small, which allows a wide BSF design. Simulation results show that for FSF IBC solar cells, the efficiency quickly reduced with the field width increasing; while FFE IBC solar cells can be designed with a wider back width and the efficiency loss is relatively smaller. The best cell efficiency was achieved with the emitter width ratio of 0.57. In addition, SiO_x:B was used in FFE IBC solar cells, and its optical and passivation effects were investigated. High implied V_{oc} and low J_{0E} were achieved with SiO_x:B passivation, which is similar to thermal oxidation passivation. It helps to reduce process steps and the production cost. Finally, large area (156.75 cm × 156.75 cm) IBC solar cells were fabricated with a simplified process flow and a cell efficiency of 20.39% was achieved.

Author Contributions: Y.Z. and C.Z. conceived the idea and guided the experiment; P.D. conducted most of the device simulation, fabrication, and data collection; H.G., C.Z., J.M., and X.Q. helped with the device measurement. All authors read and approved the manuscript.

Conflicts of Interest: The authors declare no conflicts of interest.

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