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Cascaded Multilevel Inverter Topology Based on Cascaded H-Bridge Multilevel Inverter

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Abstract: A three-phase multilevel inverter topology for use in various applications is proposed. The present topology introduces a combination of a cascaded H-bridge multilevel inverter with a cascaded three-phase voltage source inverter (three-phase triple voltage source inverter (TVSI)). This combination will increase the number of voltage levels generated when using fewer components compared with the conventional multilevel inverter topologies for the same voltage levels generated. The other advantage gained from the proposed configuration is the assurance of a continuous power supply to the grid in case of failure in one part of the proposed configuration. In addition, the voltage stresses on switches are reduced by half compared if each part in the proposed topology is working independently. The comparison of the proposed topology with some conventional multilevel inverter topologies is presented. The proposed topology is built in the SIMULINK environment and is simulated under various loads in addition to being connected to the grid. Phase-shifted pulse width modulation technique is used to generate the required switching pulses to drive the switches of the proposed topology. The inverter is experimentally implemented in the lab, and the switching pulses are generated with the help of MicroLabBox produced by dSPACE (digital signal processing and control engineering) company. The simulation and experimental results and their comparisons are presented to verify the proposed topology's effectiveness and reliability.

Keywords: multilevel inverter; cascaded H-bridge multilevel inverter (MLI); triple voltage source inverter (TVSI); open-end windings

1. Introduction

The term “multilevel” began when Nabae performed the three-level converter in 1981. In this study, a three-level neutral point clamp (NPC) was proposed [1]. Subsequently, several multilevel converter topologies have been developed [2–5]. In recent years, many multilevel converter topologies have been proposed and have gained attention in many applications, especially in the interface for the grid connection of photovoltaic (PV) systems [3]. The most common multilevel inverter (MLI) topologies can be classified into three types: neutral point MLI, flying capacitor MLI, and cascaded H-bridge (CHB) MLI.

The cascaded H-bridge multilevel inverter (CHB-MLI) is based on the series connection of the H-bridge inverters. It is an alternative topology with fewer switches when compared with other MLI topologies of the same voltage level. Each H-bridge can be used to generate three output voltage levels by a unipolar modulation technique. CHB-MLI has been used for renewable energy sources,

especially PV modules, due to its separate Direct Current (DC) source feature. Cascaded H-bridge MLI features have proved to be an attractive solution for many applications, such as standalone systems [5], volt ampere reactive (VAR) compensations, and grid-connected PV systems as presented in [6–9].

Generally, the cascaded H-bridge topologies have received more attention. The cascaded H-bridge inverter has a simple layout, extreme modularity, a simple construction, control, and no voltage balance problems, and compared with the other multilevel topologies, it requires the fewest components for generating the same voltage levels [10–12]. However, if more levels are required to improve the current and voltage's quality, the number of switches can be increased. Increasing the number of switches can lead to an increase in the cost, the conduction, and the switching losses, thus reducing the system efficiency. The reliability will also be reduced when the number of switches is increased, and the control system will be more complex.

Many other cascaded inverter topologies have been proposed to increase the number of voltage levels generated, which will improve the system's performance and reduce cost [10]. Asymmetrical CHB-MLI topologies have been proposed to increase the number of levels by combining various ranges of voltage DC sources as shown in Figure 1 [13–15]. In these topologies, the number of levels increase, but the stresses on the switches are not equal. The stress on switches connected to the lower DC input voltage will be lower than that on switches connected to the higher DC input voltage. Unequal loss sharing among switches will cause varying temperatures for switches, and some switches may be burnt. In addition, unequal loss sharing means different voltage ratings will be used for switches, which results in a higher cost. On the other hand, unequal loss sharing requires switches with higher voltage ratings.

On the other hand, modified topologies have been proposed based on CHB to improve the output voltage quality [16,17], but the advantages of the CHB are lost, such as simplicity, simple construction, simple control, and modularity.

Hybrid multilevel inverter topologies were proposed based on three-leg two-level inverter with CHB [18–22]. The hybrid multilevel inverter topology is shown in Figure 2. The authors in [18] proposed a five-level inverter topology based on two-level and floating capacitor H-bridge cells. The proposed inverter topology can be operated as a three-level inverter for the full modulation range, in case of any switch failure in the capacitor-fed H-bridge cell. This will increase the system's reliability. The authors [22] also proposed a nine-level inverter topology based on a conventional hybrid two-level voltage source inverter (VSI) with CHB-MLI using open-end winding (OEW) transformers as shown in Figure 3. These topologies are not reliable, however, because they are based on a two-level three-leg inverter. The inverter system will be out of work if this two-level inverter malfunctions, and the power will not be supplied to the grid. In these topologies, the H-bridges are connected to floating capacitors whose voltages should be controlled carefully to be maintained at required asymmetrical values. This adds more complexity to the control algorithm.

Another type of cascaded MLI topology is based on the conventional two-level voltage source inverter. It has been used in many motor-drive applications as shown in Figure 4 [23,24]. This cascaded MLI can also be used for grid-connected renewable energy applications [23–25]. The author in [23] used this topology to connect the wind farm to the grid, whereas others [25] used the three-phase cascaded VSI for grid-connected PV applications. However, the three-phase currents in each unit are not balanced, which means the current stresses on each leg are not equal. The authors in [26] solved the problem of unbalanced three-phase currents in each unit by using inter-mediate transformers instead of inductors as shown in Figure 5.

However, the inter-mediate transformers are bulky [27]. On the other hand, in both topologies, the number of voltage levels will be limited due to the limitation in the number of cascaded VSI units.

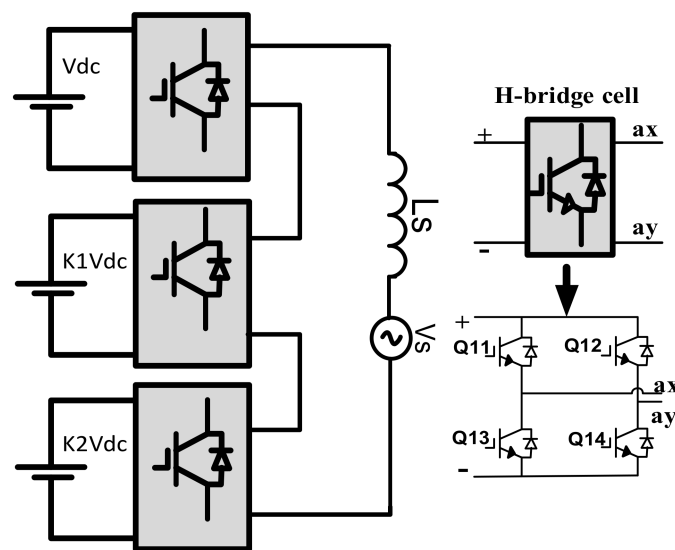


Figure 1. Asymmetrical Cascaded H-bridge topology.

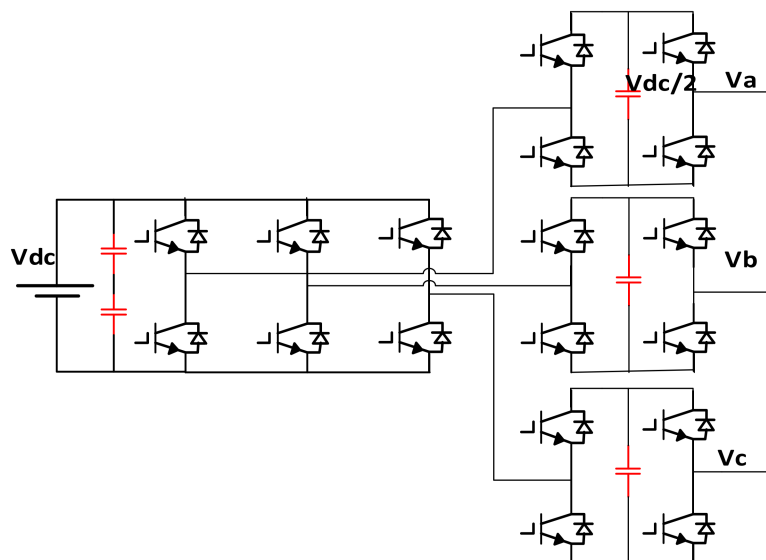


Figure 2. Hybrid multilevel inverter topology.

In this paper, a proposed multilevel inverter configuration introduces a combination of the cascaded H-bridge multilevel inverter and the three-phase cascaded VSI. This combination will increase the number of voltage levels generated from the inverter while using fewer components than the conventional multilevel inverter topologies do for the same voltage levels. The proposed topology is built in the SIMULINK environment (2016a, MathWorks), is simulated under various loads, and is connected to the grid. In Section 2, the proposed topology is described. In Section 3, the analysis of the proposed topology is explained. To validate the good performance of the proposed topology, the simulation results are shown in Section 4. In Section 5, the experimental setup, and the experimental results are demonstrated.

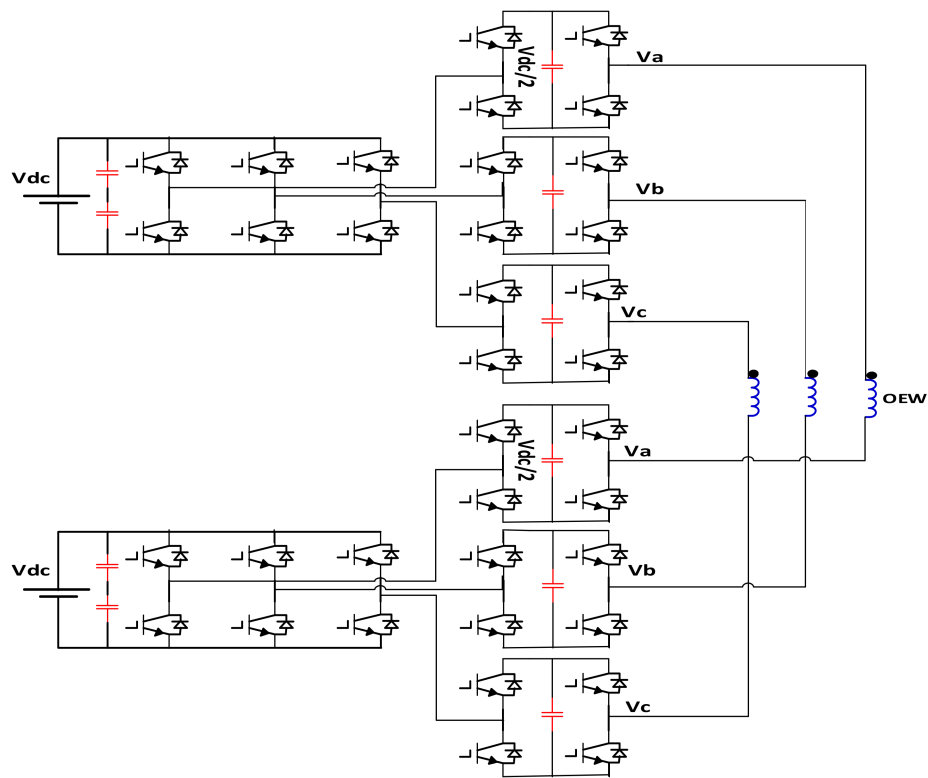


Figure 3. Hybrid multilevel inverter topology using open-end winding (OEW).

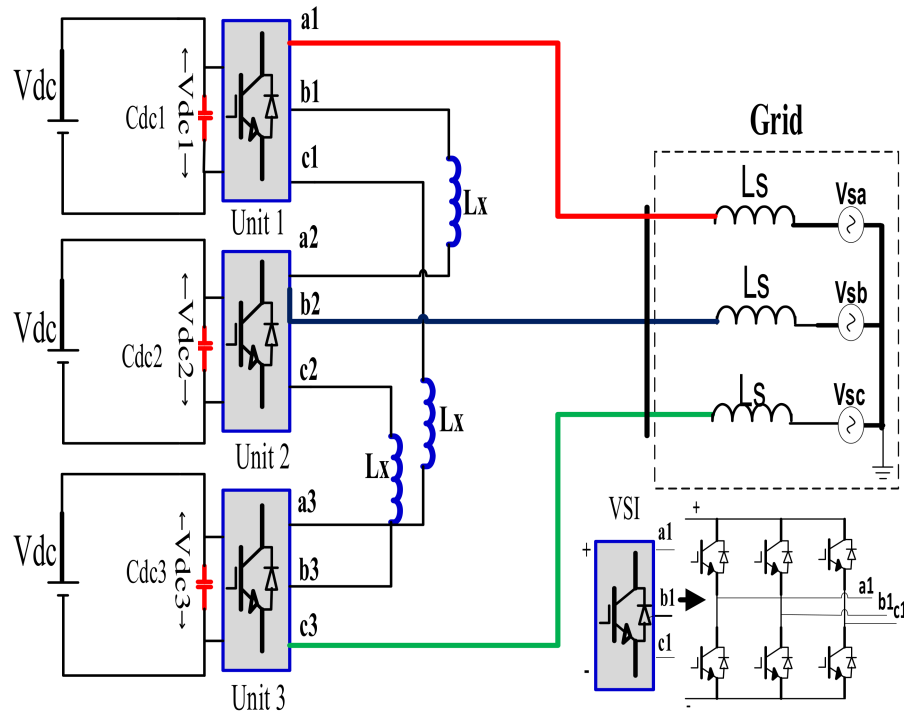


Figure 4. Three-phase cascaded voltage source inverter (VSI) using inductors.

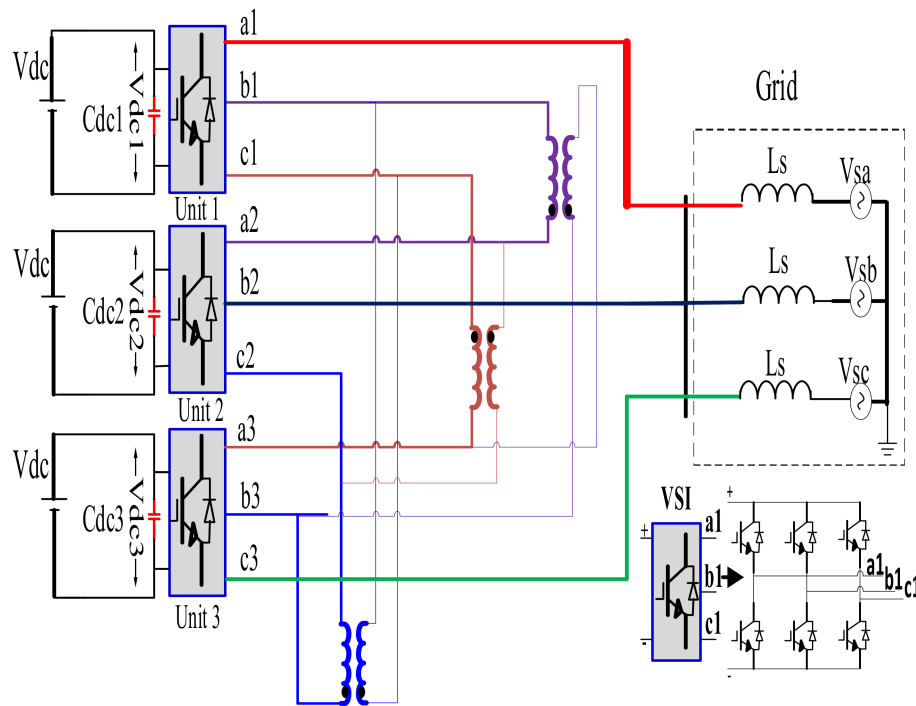


Figure 5. Three-phase cascaded VSI using inter-mediate transformers.

2. Description of the Proposed Topology

The present topology relates to a three-phase multilevel high-voltage/high-power converter, which is a hybrid configuration that conjoins two conventional multilevel configurations: a cascaded H-bridge MLI and a three-phase cascaded VSI (can also be called three-phase triple VSI (TVSI)). Figure 6 reveals the proposed cascaded MLI topology. This new topology can be used for numerous grid-connected applications, such as grid-connected PV systems, power factor correction, and static VAR compensation.

The proposed topology can be used to generate any number of voltage levels using fewer components compared with the conventional multilevel inverter topologies. The proposed inverter topology consists of two parts, which are connected together with open-end winding transformers as shown in Figure 6. To better describe the proposed inverter topology, it has been divided into two parts. The upper part is the cascaded H-bridge MLI, and the lower part is the three-phase triple VSI.

First: Description of the upper part: This part consists of three-phase systems. Each phase consists of N H-bridge cells. These cells are cascaded as shown in the upper part of Figure 6 such that the a_{y1} terminal of H-bridge cell 1 in phase a, for example, is connected to the a_{x2} terminal of the next H-bridge cell. In addition, the $a_{y(N-1)}$ terminal is connected to the a_{xN} terminal of the last H-bridge cell. The same idea is applied phases b and c. The terminals of a_{yN} , b_{yN} , and c_{yN} of phases a, b, and c are connected together to one point, NN .

Second: Description of lower part: The three-phase triple-voltage source inverter consists of three units. Each unit is a three-leg two-level inverter, and the three units are cascaded as shown in the lower part of Figure 6. Each unit consists of three terminals: a_{2k} , b_{2k} , and c_{2k} where k is the unit number. The three units are cascaded with one another by using coupled inductors as shown in the lower part of Figure 6. The coupled inductors are used instead of inter-mediate transformers in the lower part.

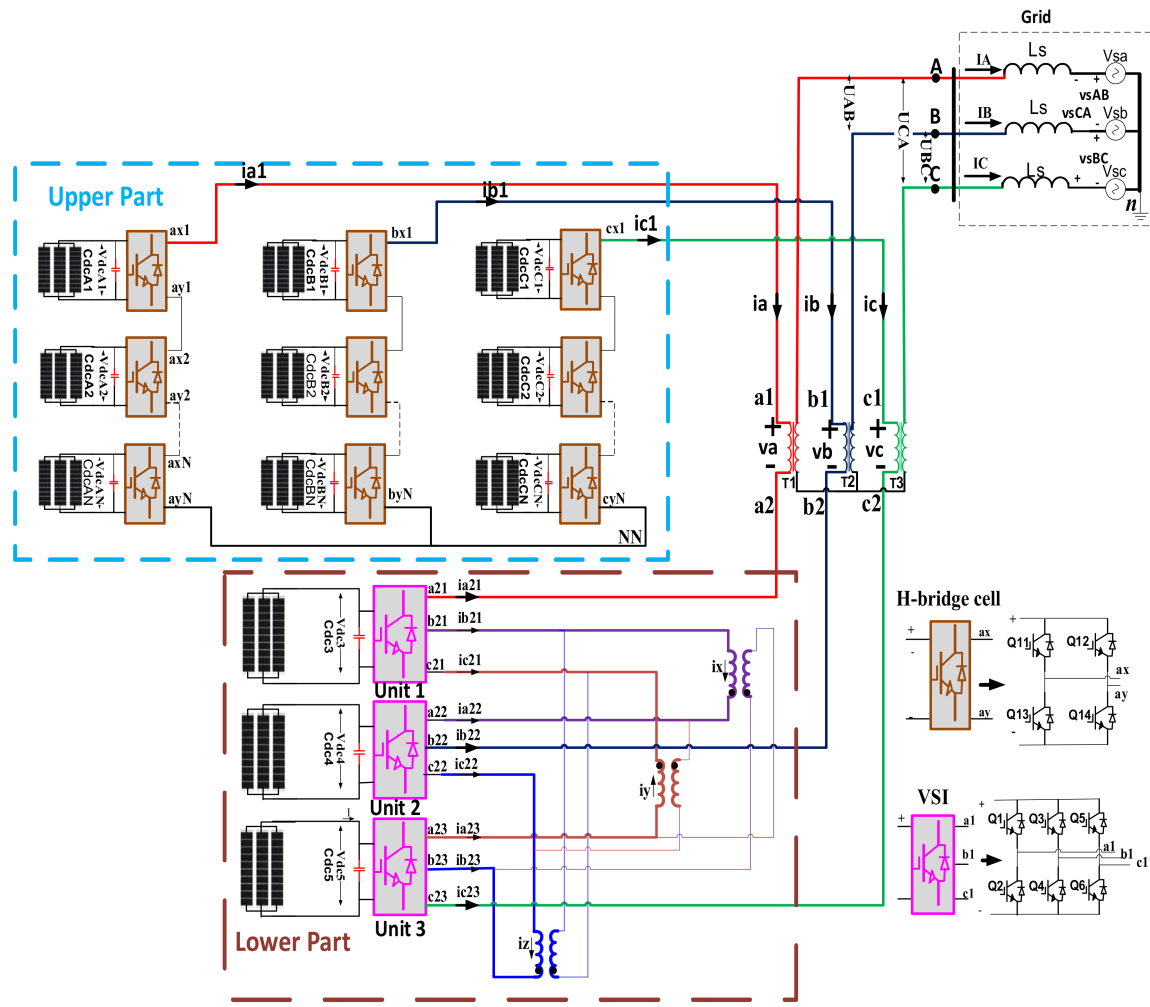


Figure 6. The proposed cascaded multilevel inverter topology.

Finally: The upper and lower parts are connected in such a way that phase a of the upper configuration is connected to phase a of the lower configuration via open-end winding. Terminal a_{x1} from the upper part is connected to terminal a_1 of open-end winding transformer T_1 , and terminal a_{21} of unit 1 in the lower part is connected to terminal a_2 of open-end winding transformer T_1 . The same idea is applied for open-end winding transformers T_2 and T_3 . The secondary windings of transformers T_1 , T_2 , and T_3 are then connected to the three-phase grid. Three single-phase line frequency transformers presented in the proposed topology are used to connect the upper three-phase cascaded H-bridge inverter with the lower three-phase triple voltage source inverter. The operation of the three single-phase transformers are based on the principles of the open-end transformer. The open-end winding transformer has gained advantages to the MLI topologies: (1) The voltage rating of the power devices is reduced by half; (2) the size of the capacitors is reduced; and (3) the DC bus magnitude that the PV modules provide can be reduced by half compared with if only one part (upper or lower) is used. This topology generates higher voltage levels by reducing the number of required switches compared with the conventional multilevel inverter topologies for the same voltage levels. The reduction in the switches leads to a reduction in complexity and dimensions of the converter. In addition, the topology helps reduce the total harmonic distortion (THD) of the voltages and currents. Another important advantage of the proposed inverter topology is that in case of failure in one part, the other part will work independently, and the power will still be available. In addition, if more levels are needed, the number of H-bridge cells in the upper part can be increased. The concept presented in this paper is validated by means of simulation and experimental results.

The advantages of the invention can be summarized as follows:

- More levels can be obtained by using fewer switches compared with the conventional multilevel inverter topologies for the same voltage levels.
- Voltage and quality of current can be improved.
- A continuous power supply to the grid is assured in the case of failure one configuration. Therefore, the proposed topology is reliable.
- The voltage stresses on switches are reduced:
- Stresses on the upper switches:

$$\frac{\sqrt{2}V}{2N\sqrt{3}} \quad (1)$$

where V is the root-mean-square (RMS) of the line–line grid voltage, and N is the number of cascaded H-bridge cells.

- Stresses on the lower switches:

$$\frac{\sqrt{2}V}{6\sqrt{3}} \quad (2)$$

- Equal Current stresses on switches. The current stress on all switches in the proposed topology is the RMS grid current I .

3. Analysis of the Proposed Topology

3.1. Voltage Relationships

The analysis of the circuit voltage on the primary side of the open-end winding transformers shown in Figure 6:

For phases a–b:

$$v_{axy} - v_a - v_{a21b21} - v_{b21a22} - v_{a22b22} + v_b - v_{bxy} = 0 \quad (3)$$

For phases b–c:

$$v_{bxy} - v_b - v_{b22c22} - v_{c22b23} - v_{b23c23} + v_c - v_{cxy} = 0 \quad (4)$$

For phases c–a:

$$v_{cxy} - v_c - v_{c23a23} - v_{a23c21} - v_{c21a21} + v_a - v_{axy} = 0 \quad (5)$$

where:

$$v_{axy} = v_{a1}, \quad v_{bxy} = v_{b1}, \quad \text{and} \quad v_{cxy} = v_{c1}$$

Therefore:

$$\begin{aligned} v_{ab} &= (v_{a1} - v_{b1}) - v_{a21b21} - v_{b21a22} - v_{a22b22} \\ v_{bc} &= (v_{b1} - v_{c1}) - v_{b22c22} - v_{c22b23} - v_{b23c23} \\ v_{ca} &= (v_{c1} - v_{a1}) - v_{c23a23} - v_{a23c21} - v_{c21a21} \end{aligned} \quad (6)$$

The line–line voltage of the lower part is given as follows:

$$v_{a2b2} = v_{a21b21} + v_{b21a22} + v_{a22b22} \quad (7)$$

Due to the transformer action in the lower part:

$$v_{b21a22} = v_{a23b23} \quad (8)$$

Equation (6) can be written as follows:

$$\begin{aligned}v_{ab} &= v_{a1b1} - v_{a2b2} \\v_{bc} &= v_{b1c1} - v_{b2c2} \\v_{ca} &= v_{c1a1} - v_{c2a2}\end{aligned}\quad (9)$$

where v_{a1b1} , v_{b1c1} and v_{c1a1} are the line-line voltages of the upper part; v_{a2b2} , v_{b1c1} and v_{b1c1} are the line-line voltage of the lower part. The generated line-line voltages from the proposed topology are given as:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} U_{AB}^* \\ U_{BC}^* \\ U_{CA}^* \end{bmatrix} = \sqrt{3}m_a \left(\frac{3}{2}V_{dc} + NV_{dc/HB} \right) \begin{bmatrix} \sin(\omega t + 30^\circ) \\ \sin(\omega t - 90^\circ) \\ \sin(\omega t + 150^\circ) \end{bmatrix} \quad (10)$$

where N is the number of H-bridge cells connected to each phase, $V_{dc/HB}$ is the DC link voltage for each H-bridge cell, V_{dc} is the DC link voltage across each unit in the lower part, U_{AB}^* is the line-line voltage in the secondary side of the transformer referred to the primary side (assume 1:1 turns ratio), and m_a is the modulation index.

Equation (10) can be combined using instantaneous space vector, defined as [28]:

$$\vec{v}_{LL} = \frac{2}{3} [v_{ab} + a v_{bc} + a^2 v_{ca}] = \sqrt{2}V_{LL}e^{j(\omega t + 30^\circ)} \quad (11)$$

where $V_{LL} = \frac{\sqrt{3}}{2}m_a \left(\frac{3}{2}V_{dc} + NV_{dc/HB} \right)$, $a = e^{j2\pi/3}$, and $a^2 = e^{j4\pi/3}$.

If it is assumed that $V_{dc} = V_{dc/HB}$, the RMS line-line voltages of the proposed topology can be given as:

$$V_{LL} = \frac{\sqrt{3}}{2\sqrt{2}}m_a V_{dc}(3 + 2N) \quad (12)$$

This means that the generated line-line voltage equals $(3 + 2N)$ times the line-line voltage of each two-level VSI unit. If $N = 2$, the RMS line-line generated voltage is seven times the line-line voltage of each VSI unit.

The space vector of the generated voltage across the open-end windings $\vec{v}_{OEW}$ is given as follows:

$$\vec{v}_{OEW} = \frac{2}{3} [v_{a1a2} + a v_{b1b2} + a^2 v_{c1c2}] = m_a \left(\frac{3}{2}V_{dc} + NV_{dc/HB} \right) e^{j(\omega t)} \quad (13)$$

where V_{a1a2} , V_{b1b2} , and V_{c1c2} are the voltages across the primary sides of the transformers T_1 , T_2 and T_3 , respectively.

3.2. Current Relationships

The instantaneous space vector current $\vec{i}_{OEW}$ flows through the primary windings of the open-end winding transformers:

$$\vec{i}_{OEW} = \frac{2}{3} [1 + a + a^2] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{2}Ie^{j(\omega t)} \quad (14)$$

where I is the RMS grid current.

The phase currents of each unit in the lower part of Figure 6 satisfy the following equations:

$$\begin{bmatrix} i_{a21} + i_{b21} + i_{c21} \\ i_{a22} + i_{b22} + i_{c22} \\ i_{a23} + i_{b23} + i_{c23} \end{bmatrix} = 0 \quad (15)$$

The currents of each unit in the lower configuration of Figure 6 can be expressed as follows:

$$\begin{bmatrix} i_{a21} \\ i_{b21} \\ i_{c21} \end{bmatrix} = \begin{bmatrix} i_{a22} \\ i_{b22} \\ i_{c22} \end{bmatrix} = \begin{bmatrix} i_{a23} \\ i_{b23} \\ i_{c23} \end{bmatrix} = \begin{bmatrix} i_y - i_x \\ i_x - i_z \\ i_z - i_y \end{bmatrix} \quad (16)$$

where i_x , i_y , and i_z are the currents flowing in the primary windings of the coupled inductors as shown in Figure 6.

Assuming that the magnetizing inductance of the coupled inductors are high such that the circulating current is zero:

$$i_x + i_y + i_z = 0 \quad (17)$$

Using (14), (16), and (17), the instantaneous space vector current $\vec{i}_{xyz}$ flowing in the primary windings of the coupled inductors can be expressed as follows:

$$\vec{i}_{xyz} = \frac{2}{3} [1 + a + a^2] \begin{bmatrix} i_x \\ i_y \\ i_z \end{bmatrix} = \frac{\sqrt{2}}{\sqrt{3}} I e^{j(\omega t + 30^\circ)} \quad (18)$$

Substituting (18) into (16), the instantaneous space vector current $\vec{i}_{Low}$ in each unit in the lower part can be given as follows:

$$\vec{i}_{Low_K} = \frac{2}{3} [1 + a + a^2] \begin{bmatrix} i_{a2K} \\ i_{b2K} \\ i_{c2K} \end{bmatrix} = \sqrt{2} I e^{j(\omega t + 180^\circ)} \quad (19)$$

where K could be 1, 2 or 3, which represents unit 1, unit 2, or unit 3, respectively.

As shown from (1) and (19), the current stress on all switches in the proposed topology is I , where I is the RMS grid current.

3.3. Power Relationships

The apparent powers of units 1, 2, and 3 in the lower part are as follows:

$$\begin{bmatrix} VA_{U1} \\ VA_{U2} \\ VA_{U3} \end{bmatrix} = \left(\frac{3}{2\sqrt{2}} m_a V_{dc} \right) \begin{bmatrix} I_{a,rms} \\ I_{b,rms} \\ I_{c,rms} \end{bmatrix} \quad (20)$$

where VA_{U1} , VA_{U2} , and VA_{U3} are the apparent power of units 1, 2 and 3 respectively. In addition, $I_{a,rms}$, $I_{b,rms}$, and $I_{c,rms}$ are the RMS currents of phases a, b, and c, respectively.

The total apparent power of N cascaded H-bridge cells in each phase is as follows:

$$\begin{bmatrix} VA_a \\ VA_b \\ VA_c \end{bmatrix} = \left(\frac{Nm_a}{\sqrt{2}} V_{dc/HB} \right) \begin{bmatrix} I_{a,rms} \\ I_{b,rms} \\ I_{c,rms} \end{bmatrix} \quad (21)$$

where VA_a , VA_b , and VA_c are the apparent power N cascaded H-bridge cells connected to phase a, b, and c, respectively.

The total apparent power of the proposed topology can be given as follows:

$$(VA_T) = 3 \left(\frac{Nm_a}{\sqrt{2}} V_{dc/HB} \right) I_{rms} + \left(\frac{9}{2\sqrt{2}} m_a V_{dc} \right) I_{rms} = \frac{3}{\sqrt{2}} m_a I_{rms} (1.5V_{dc} + NV_{dc/HB}) \quad (22)$$

From another point of view, the total apparent power of phase a of the proposed topology can be given as follows:

$$(VA_{TA}) = V_{a1a2}I_{a,rms} = \frac{1}{\sqrt{2}}m_a I_{a,rms}(1.5V_{dc} + NV_{dc}/HB) \quad (23)$$

Similar for phases b and c, we get:

$$(VA_{TB}) = V_{b1b2}I_{b,rms} = \frac{1}{\sqrt{2}}m_a I_{b,rms}(1.5V_{dc} + NV_{dc}/HB) \quad (24)$$

$$(VA_{TC}) = V_{c1c2}I_{c,rms} = \frac{1}{\sqrt{2}}m_a I_{c,rms}(1.5V_{dc} + NV_{dc}/HB) \quad (25)$$

This means that each unit in the lower part and the cascaded H-bridge cells have connected to share the same amount of output power.

4. Simulation Results

The proposed inverter topology shown in Figure 6 is built in SIMULINK, and the simulation is achieved using the MATLAB/SIMULINK environment (2016a, MathWorks). For simplicity, two cascaded H-bridge cells are used in each phase in the upper part of the proposed topology. The magnitude of the DC voltage used for each cell in the upper and lower parts is 30 V. phase-shifted pulse-width modulation (PWM) technique (PSPWM) is used to generate the required pulses of the insulated-gate bipolar transistors (IGBTs). In this technique, the reference signals are used to generate switching pulses to drive the IGBTs of the proposed topology by comparing them with the generated triangular carrier waveforms as shown in Figure 7. The reference signals are three-phase sine waveforms whose frequencies are 60 Hz. As shown Figure 7, the phase-shift technique is used to generate the pulses to drive the IGBTs of the cascaded H-bridge part (upper part), as the triangular signal of the next H-bridge cell is shifted from the previous H-bridge by $180^\circ/N$, where N is the number of H-bridge cells. Reference voltage signal V_{refa} is compared with these phase-shifted triangular waveforms, and the resulting pulses are used to drive the IGBTs of the H-bridge cells of phase a.

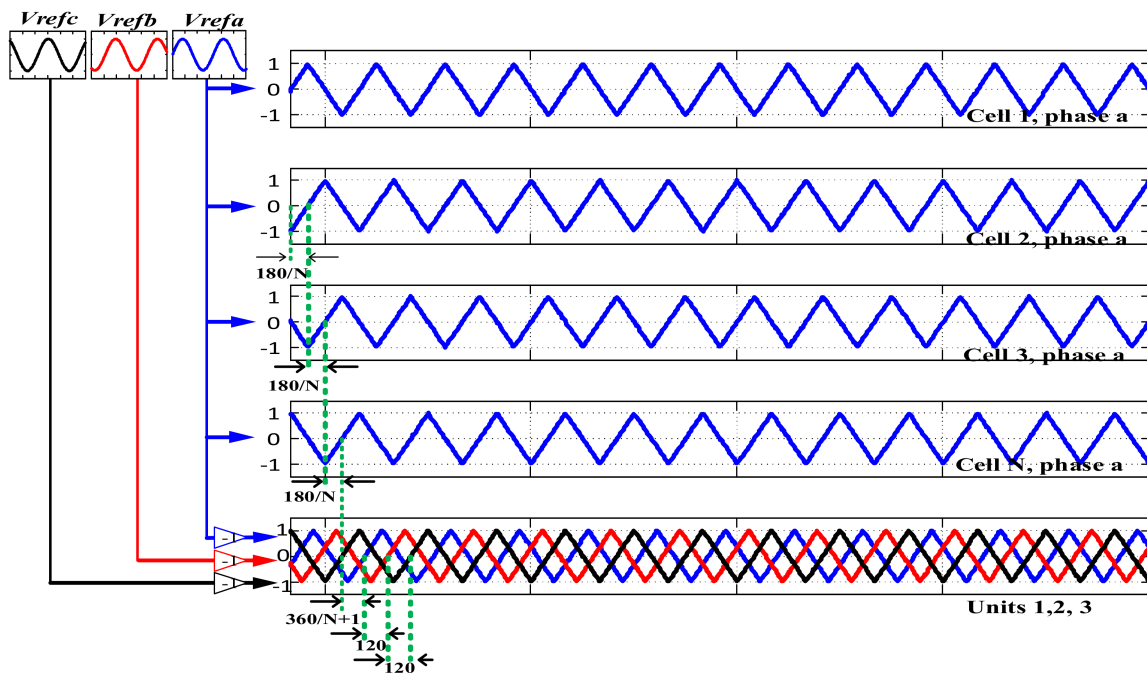


Figure 7. Phase shifted pulse-width modulation (PWM) technique.

In addition, reference voltage signals V_{refb} and V_{refc} are compared with the phase-shifted triangular waveforms to drive the IGBTs of the H-bridge cells of phases b and c of the upper part respectively.

It should be noted that only the phase-shifted triangular waveforms used to drive the IGBTs of H-bridge cells of phase a (phase a in the upper part) are shown in this figure. In addition, to drive the IGBTs of the three-phase triple VSI (lower part) in the proposed topology, the reference voltage signals of V_{refa} , V_{refb} , and V_{refc} are compared with the phase-shifted triangular waveforms as shown in Figure 7. The triangular signal used to generate the PWM pulses of unit 2 is shifted by $(T/3)$ from that of unit 1, and the triangular signal used to generate PWM pulses of unit 3 is shifted by $(T/3)$ from that of unit 2. It is noted that the generated triangular waveforms of the lower part are shifted from the triangular signal of H-bridge cell number N in the upper part by $(T/(N + 1))$, where N is the number of H-bridge cells in one phase in the upper part of the proposed inverter topology.

The performance of the proposed inverter is tested under variable loads: resistive load, resistive inductive loads connected in a series (RLs), resistive inductive loads connected in parallel (RLp), and a series resistive inductive capacitive (RLCs) load. The parameters used for simulation are shown in Table 1. In addition, the modulation index is set 1.85, and the sampling time during simulation is 10 μ s. The parameters of the transformers are set by the default values of the SIMULINK. The three-phase voltages v_{a1a2} , v_{a1a2} , and v_{a1a3} are measured across the two primary terminals of transformers T_1 , T_2 , and T_3 respectively.

Table 1. The parameters used in the simulation and experiment.

The System Parameters		KACST 245 PV Module Parameters	
DC Source	30 V	Maximum Power (P_{max})	245 W
Inverter switching frequency (f_{inv})	1500 Hz	Maximum Power Voltage (V_{max})	28.8 V
Resistive Load	48 Ω	Maximum Power Current (I_{max})	8.5 A
Inductance of the Inductive Load	154 mH	Open Circuit Voltage (V_{oc})	31.5 V
Capacitance of the Capacitive Load	66 μ F	Short Circuit Current (I_{sc})	9.5 A

The instantaneous line-line voltages generated from the proposed topology is shown in Figure 8. As shown in this figure, the total number of voltage levels is 15 level. On the other hand, the total number of voltage levels generated from the proposed topology per phase is 22 levels as revealed in Figure 9.

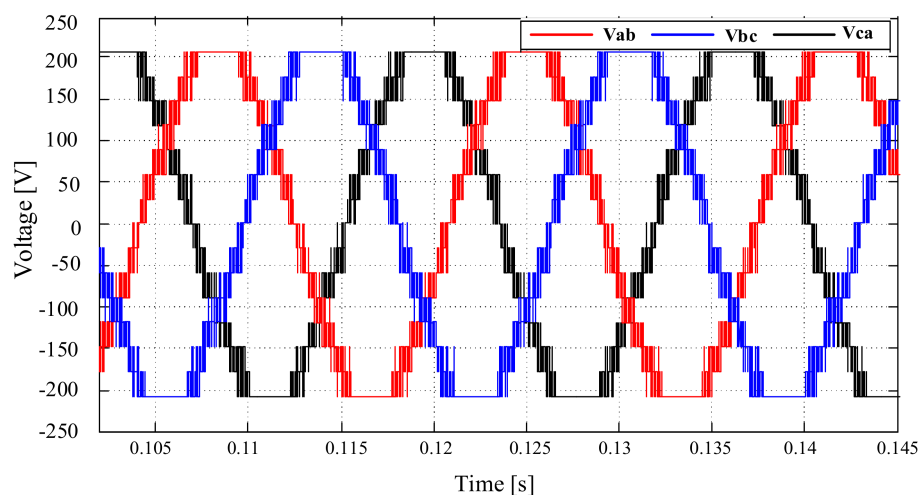


Figure 8. Three-phase line-line voltages generated.

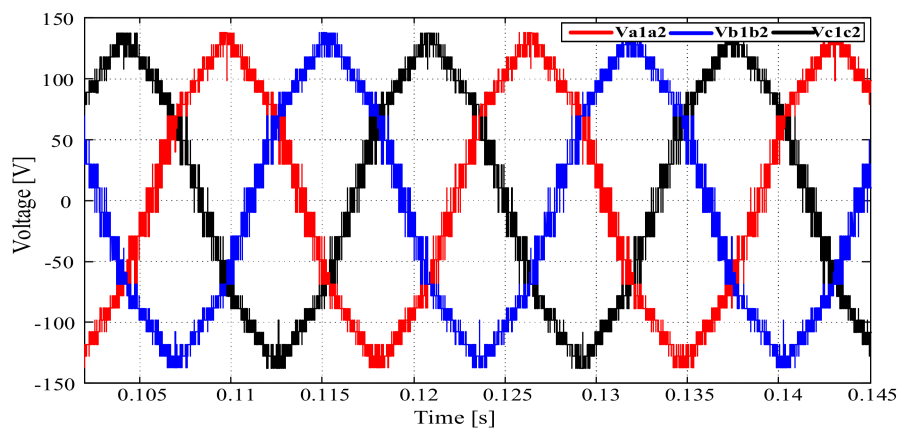


Figure 9. Three-phase phase voltages generated.

To show the performance of the proposed inverter, the harmonic spectrum is measured under various load conditions. The harmonic spectrum of the generated voltage v_{a1a2} is seen in Figure 10. The total harmonic distortion (THD) of v_{a1a2} is 10.29%. As depicted in Figure 10, the first harmonic family appears at five times the fundamental frequency. The fifth, seventh, and 13th harmonic order exists with amplitudes approximately 3%, 2.5%, and 0.9% respectively.

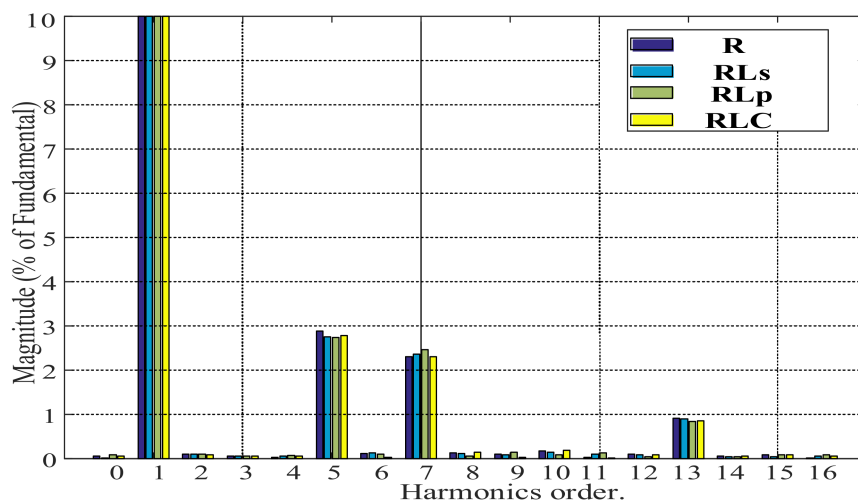


Figure 10. Harmonics spectrum of the voltage v_{a1a2} using under different.

5. Experimental Results

To validate good performance, the proposed topology has been built in the laboratory and experimentally tested under various loads. It is connected to the grid with an open-loop control. In the experimental setup, the PV modules represent the DC voltage sources. For simplicity, two cascaded H-bridge cells are used for each phase in the upper part of the proposed topology. For the three-phase inverter topology, nine PV modules are used since one PV module is connected to each H-bridge cell in the upper part, and one PV module is connected to each unit in the lower part.

The parameters of the PV modules are shown in Table 1. Data acquisition and the control system are implemented using a DS1202 MicroLabBox system (dSPACE Company, Paderborn, Germany) produced by dSPACE. The required switching pulses are generated inside a SIMUNLINK environment and are sent to the IGBTs via the DS1202 board. During hardware implementation, the phase-shifted PWM technique is used.

The hardware setup of the proposed topology is depicted in Figure 11. Three single-phase transformers are used for open-end connection. In addition, three coupled inductors, model 810.1201, produced by the Toroid Company (Salisbury, MD, USA), are used in the lower part of the proposed configuration.

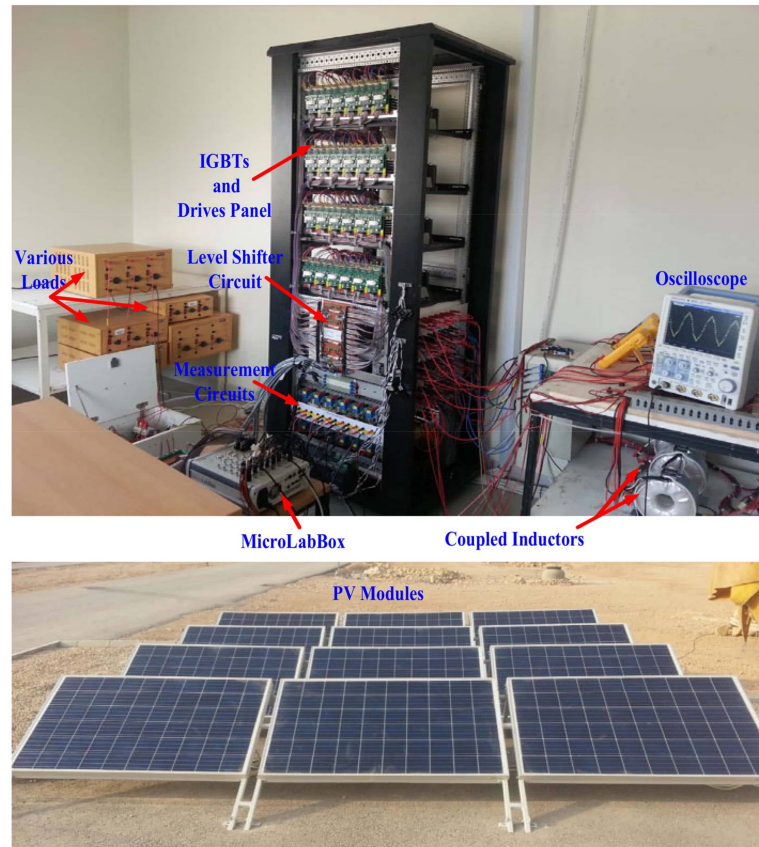


Figure 11. The hardware setup of the proposed topology.

The parameter in the experiment is illustrated in Table 1. The inverter topology is practically tested under the following conditions:

5.1. Various Loads

5.1.1. Resistive load

A three-phase resistive bank is connected to the output terminals of the proposed topology. The three-phase voltages v_{a1a2} , v_{b1b2} , and v_{c1c2} , are generated across the primary sides of the transformers T_1 , T_2 , and T_3 , respectively, taken from oscilloscope, is illustrated in Figure 12a. The THD of the v_{a1a2} is 8.41% and its harmonic spectrum, taken from oscilloscope, is depicted in Figure 12b.

In addition, the three-phase load currents measured via the Hall-effect current sensor, model LTS 25-NP (LEM Company, Milwaukee, WI, USA), are shown in Figure 12c.

As mentioned in the analysis, the three-phase currents of each unit in the lower configuration are symmetrical and balanced, and they equal the three-phase line currents. Therefore, the current stress on each IGBT in the lower configuration equals the current stress on each IGBT in the upper part. The three-phase currents of unit 1 in the lower configuration are displayed in Figure 12d. The circulating currents inside the lower configurations is low because the magnetization inductances of the coupled inductors are high. The circulating current inside the lower configuration is low and can be seen in Figure 12e.

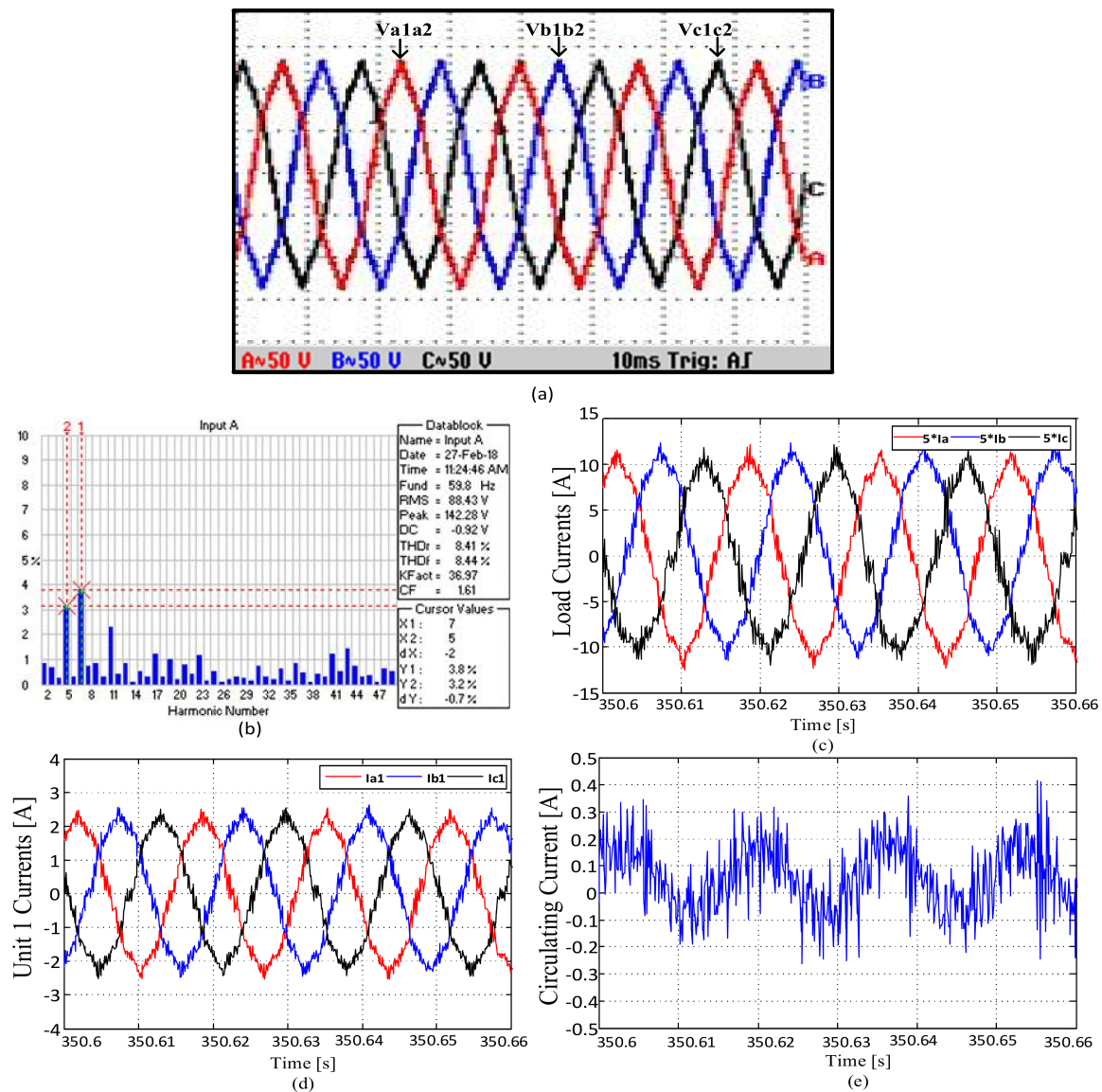


Figure 12. Performance of the proposed inverter under resistive load. (a): The three-phase voltages generated across the primary windings of the open-end winding transformers. (b): Harmonic spectrum of the voltage v_{a1a2} . (c): Three-phase load currents. (d): Three-phase currents of unit 1. (e): The circulating current inside the lower part.

5.1.2. Series Resistive Inductive Capacitive Load

The proposed topology is tested under three-phase RLC series load. The three-phase voltages v_{a1a2} , v_{b1b2} , and v_{c1c2} are generated across the primary sides of the transformers T_1 , T_1 , and T_1 , respectively, taken from oscilloscope, is depicted in Figure 13a. The THD of the v_{a1a2} is 8.53% and its harmonic spectrum, taken from oscilloscope, is depicted in Figure 13b. In addition, the three-phase load currents are revealed in Figure 13c.

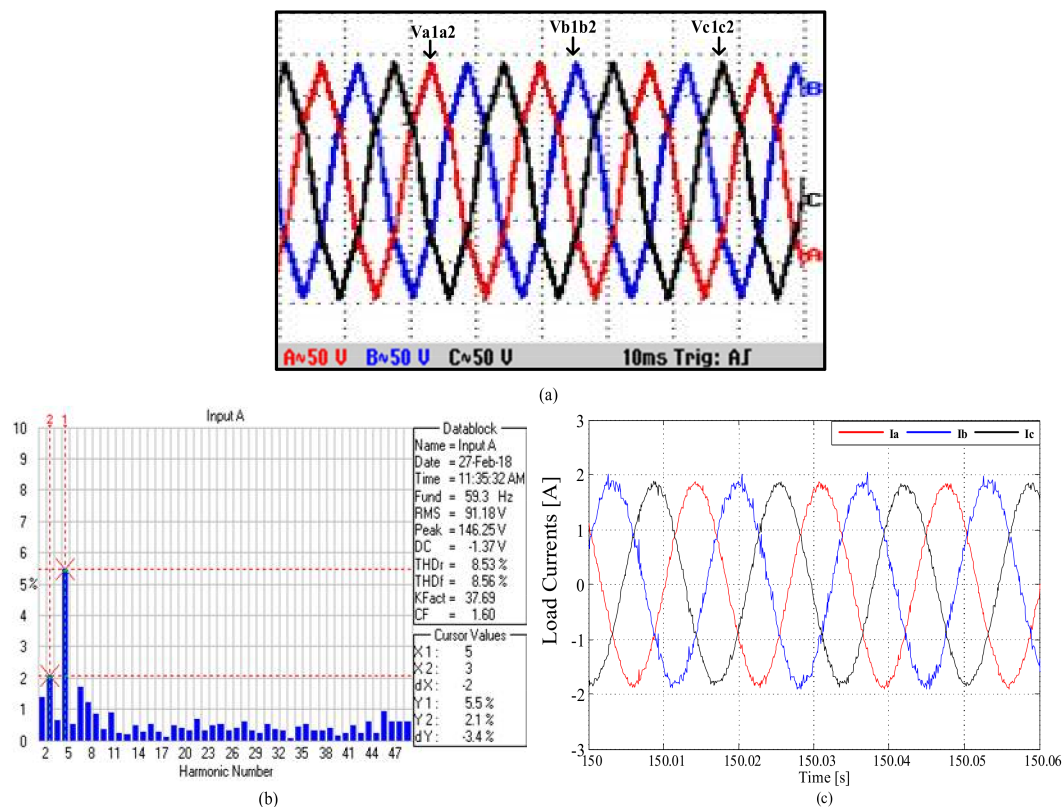


Figure 13. Performance of the proposed inverter under series resistive inductive capacitive (RLC) load. (a): The three-phase voltages generated across the primary windings of the open-end winding transformers. (b) Harmonic spectrum of the voltage v_{a1a2} . (c): Three-phase load currents.

The total harmonic distortion (THD) of v_{a1a2} under all loads described above is practically measured by changing the modulation index (m_a) and validating the simulation results. The variations of the THD of v_{a1a2} with changing m_a under various loads is seen in Figure 14. As shown in these figures, the THD is high when m_a is less than 1, and it decreases with increasing m_a . The minimum THD occurs at m_a between 1.5 and 1.85. To reveal the effectiveness and accuracy of the proposed inverter topology, the same conditions of the experiment are applied to the SIMULINK model to validate the practical results by the simulation results. The practical results are validated via the simulation results by changing the modulation index as shown in Figure 14.

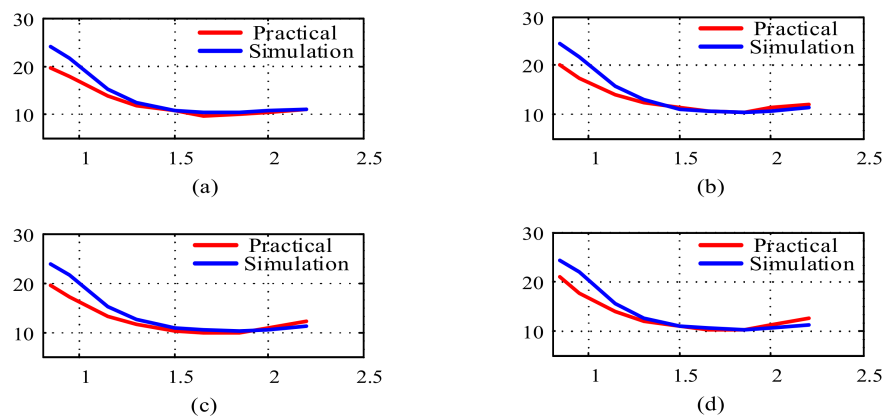


Figure 14. Changing the percentage total harmonic distortion (THD) (y -axis) of the voltage v_{a1a2} with modulation index (m_a) (x -axis) under (a): Resistive load. (b): Series resistive inductive load. (c): Parallel resistive inductive load. (d): Series RLC load.

Figure 14a shows the practical variation of the THD of v_{a1a2} and the validation via simulation under resistive load. On the other hand, the practical variations of the THD of v_{a1a2} under series resistive inductive loads, and their validation via simulation results can be seen in Figure 14b.

Figure 14c reveals the changing in the THD of the v_{a1a2} with changing m_a under parallel resistive inductive load practically, and this is validated via simulation results. The variations of the THD of the v_{a1a2} under series resistive inductive capacitive loads are displayed in Figure 14d and are validated via the simulation results as shown in the same graph.

The experimental harmonic spectrum of the voltage v_{a1a2} under all load variations described above is depicted in Figure 15. As illustrated in this figure, the higher magnitude of harmonics exists at five times the switching frequency with an amplitude of approximately 4.5%. The magnitude of the harmonic contents higher than fifth becomes lower.

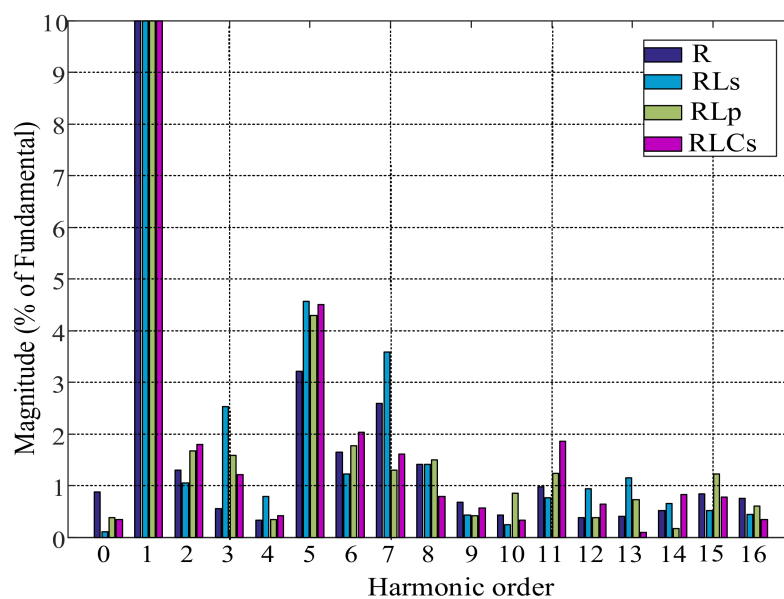


Figure 15. Experimental Harmonic spectrum of the voltage v_{a1a2} under different loads.

5.2. Grid-Connected Condition

In this experiment, the proposed topology is directly connected to the grid via an interface inductor. The value of the interface inductor is 5 mH. The PV modules represent the DC voltage sources in this experiment. The Chroma grid simulator, model 61830, represents the grid. The three-phase voltages of the grid are measured using three voltage sensors, model LV 25-P, and are used to extract the angular frequency (ωt) to be used in the phase-locked loop (PLL). The modulation index is 1.5 in this test condition. In addition, the PSPWM technique displayed in Figure 7 is used to generate the required pulses to drive the IGBTs of the inverter. The generated three-phase voltages v_{a1a2} , v_{b1b2} , and v_{c1c2} taken from oscilloscope, can be seen in Figure 16a. The THD of the generated voltage v_{a1a2} is 6.93% as revealed in the harmonic spectrum of the v_{a1a2} in Figure 16b. As shown in this figure, the highest magnitude is only 2.8% of the fifth harmonic.

Conversely, the proposed inverter topology's performance is tested by changing the modulation index and measuring the THD of the v_{a1a2} as shown in Figure 17. By increasing the modulation index, the THD of the voltage-generated v_{a1a2} is decreased. The minimum THD occurs between modulation indices 1.5 and 1.85 as indicated in the figure. In addition, the harmonic spectrum of v_{a1a2} is plotted in Figure 18. The highest harmonic contents occur at five times the fundamental frequency. The minimum harmonic magnitude occurs at a modulation index of 1.5.

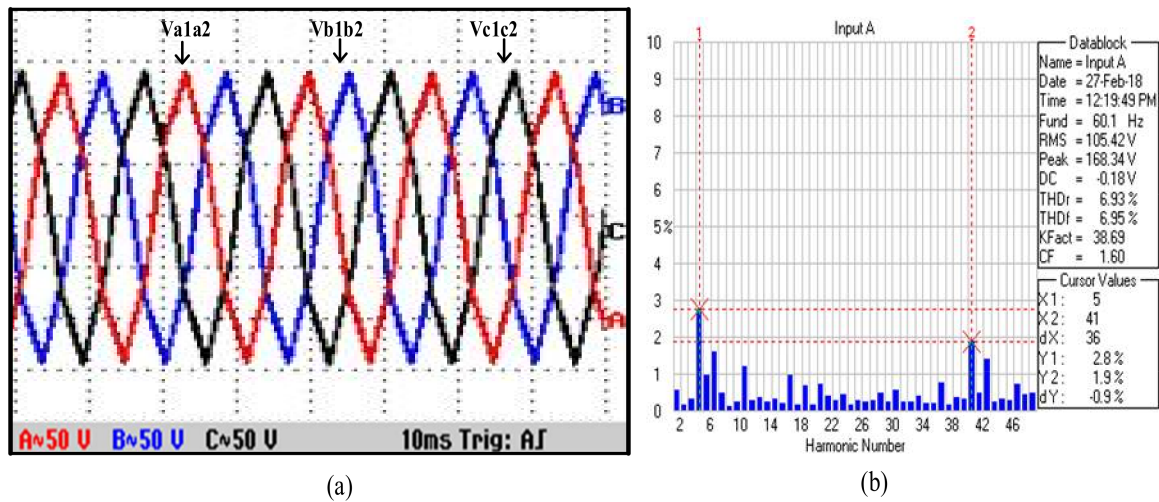


Figure 16. Performance of the proposed inverter under grid interface. (a): The three-phase voltages generated across the primary windings of the open-end winding transformers. (b): Harmonic spectrum of the voltage v_{a1a2} .

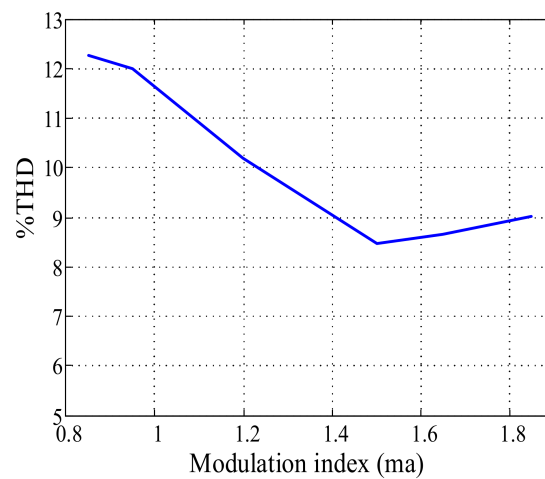


Figure 17. Changing the THD of the voltage v_{a1a2} with m_a .

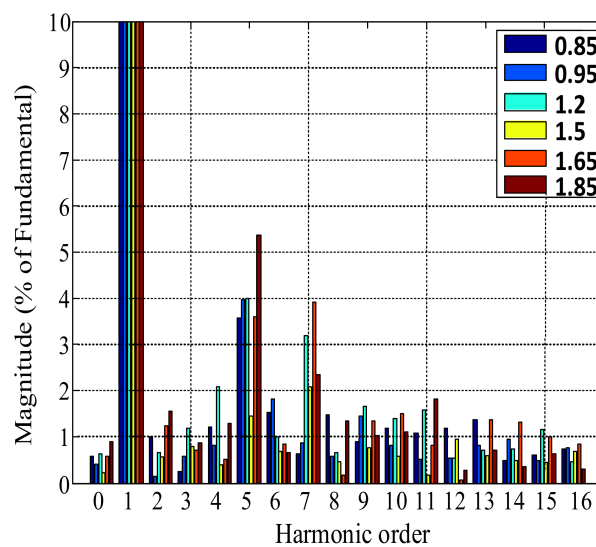


Figure 18. Harmonic spectrum of the voltage v_{a1a2} with m_a .

6. Conclusions

In this paper, a multilevel inverter configuration that uses a cascaded H-bridge multilevel inverter with a three-phase triple VSI is proposed. This combination increased the number of levels generated from the inverter by using fewer components compared with the conventional multilevel inverter topologies to generate the same voltage level. The proposed topology is built in the SIMULINK environment and is simulated under various loads. Fifteenth line-line voltage level and twenty-two voltage levels are generated per phase from this topology by using only 42 switches. A comparison of the proposed topologies with the prior multilevel inverter topologies used to generate 21 (one level lower than the number of levels generated by the proposed topology) voltage levels is illustrated in Table 2. The proposed topologies have the least number of switches compared with the prior art MLI topologies (Neutral Point Converter (NPC), Flying Capacitor (FC) MLI, Cascaded H-bridge (CHB) MLI, and Modular MLI (MMC)). In addition, the reliability of the proposed topologies is higher and the proposed topologies have the least number of DC-link capacitors, which increases the reliability. The proposed topology is modular and has no voltage-balancing problem. The same number of switches used in the proposed topology are then used to compare the voltage and current stresses of the other topologies in order to make the comparison conducting. The comparison according to the voltage and current stresses can be seen in the last two rows of Table 2 (V is the RMS value of the line-line voltage and I is the RMS current). The voltage stress on the switches of both parts in the proposed topology is reduced by half. The inverter is experimentally implemented in the lab, and the switching pulses are generated with the help of a MicroLabBox built by dSPACE. The proposed inverter topology is experimentally tested under various load conditions, and it is connected to the grid. The experimental results have verified the proposed topology's effectiveness and reliability.

Table 2. Comparison results.

Comparison Parameter	NPC	FC	CHB	MMC	Proposed Topology
No. Of Switches	120	120	120	240	42
DC-link Capacitors	20	20	30	60	9
No. Of Inductors	0	0	0	6	3
No. Of Diodes	1140	0	0	0	0
No. Of Flying Capacitors	0	570	0	0	0
Reliability	Low	Low	High	Low	High
Modularity	No	No	Yes	No	Yes
Voltage Balancing Problem	Yes	Yes	No	Yes	No
Separated DC Sources	No	No	Yes	No	Yes
Voltage Stress	$\frac{\sqrt{2}V}{6\sqrt{3}}$	$\frac{\sqrt{2}V}{6\sqrt{3}}$	$\frac{\sqrt{2}V}{3\sqrt{3}}$	$\frac{\sqrt{2}V}{4\sqrt{3}}$ *	Upper Part: $\frac{\sqrt{2}V}{4\sqrt{3}}$ Lower Part: $\frac{\sqrt{2}V}{6\sqrt{3}}$
Current Stress	$\sqrt{2}I$	$\sqrt{2}I$	$\sqrt{2}I$	$\sqrt{2}I$	$\sqrt{2}I$

* 48 switch is used for calculation.

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Conflicts of Interest: The authors declare no conflict of interest.

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