

Article

Multilevel Converter by Cascading Two-Level Three-Phase Voltage Source Converter

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Abstract: This paper proposes a topology using isolated, cascaded multilevel voltage source converters (VSCs) and employing two-winding magnetic elements for high-power applications. The proposed topology synthesizes 6 two-level, three-phase VSCs, so the power capability of the presented converter is six times the capability of each VSC module. The characteristics of the proposed topology are demonstrated through analyzing its current relationships, voltage relationships and power capability in detail. The power rating is equally shared among the VSC modules without the need for a sharing algorithm; thus, the converter operates as a single three-phase VSC. The comparative analysis with classical neutral-point clamped, flying capacitor and cascaded H-bridge exhibits the superior features of fewer insulated gate bipolar transistors (IGBTs), capacitor requirement and fewer diodes. To validate the theoretical performance of the proposed converter, it is simulated in a MATLAB/Simulink environment and the results are experimentally demonstrated using a laboratory prototype.

Keywords: cascaded multilevel converter; phase-shift pulse width modulation (PS-PWM); voltage source converters

1. Introduction

Recently, multilevel voltage source converters (VSCs) have become more attractive than traditional two-level VSCs, as the multilevel versions offer better-quality output voltage waveforms, less electromagnetic interference, lower voltage stress on the power semiconductor switches and lower common-mode voltage. Moreover, multilevel VSCs offer additional features, including high power capability, superior harmonic spectrum, low switching frequency and high system efficiency [1–4]. Consequently, multilevel VSCs are widely used in chemical, oil and other plants (e.g., renewable-energy power plants), as well as in transmission systems and power-quality compensators [4].

The current research is mainly focused on three multilevel VSC topologies: neutral-point clamped (NPC) [5], flying capacitor (FC) [6,7] and cascaded H-bridge (CHB) [8,9]. The main drawback of these multilevel VSCs is the high number of power semiconductor switches required. The NPC VSC needs many clamping diodes to increase the number of voltage levels; this can cause problems related to switches with different ratings, high-voltage rating in the blocking diodes and capacitor voltage imbalance. Along the same lines, the FC VSC has a large number of capacitors, leading to complications in regulating the capacitors' voltages. At low switching frequencies, large capacitors

are needed; having many such capacitors is costly and results in a bulky product. Finally, the CHB VSC provides isolated DC sources, so it is appropriate for use in renewable-energy systems [10]. In addition, this topology's modular structure and its relatively few components (compared to the NPC and FC topologies) means that the CHB VSC can reach the same number of voltage levels as the other VSCs with simpler assembly and maintenance. However, the CHB topology does have three main drawbacks: (i) high overall component count; (ii) high energy-storage requirements (due to the single-phase structure, the instantaneous power at each H-bridge varies at twice the fundamental frequency); and (iii) difficulty in controlling the voltage across the DC-link capacitors.

In recent years, numerous proposed configurations of multilevel VSCs have involved a reduced number of semiconductor switches and gate drivers [11–13]. A double FC VSC was presented in Reference [13]. Compared to conventional FCs, the proposed version has double the output voltage and twice the number of voltage levels; however, the proposed configuration requires a high number of capacitors. In other studies, new topologies of multilevel VSCs have been suggested [12,13]. The proposed converters require fewer switches and gate drivers but need several DC sources and certain switches have high reverse blocking voltage. The high quantity of isolated DC sources has been solved for FC and NPC VSCs (although not for the CHB VSC) but the need to regulate the voltage across the capacitors makes these VSCs more challenging than the CHB version. Therefore, the control algorithm becomes more difficult as the number of voltage steps increases. A new multilevel configuration that employs a cascaded transformer has been presented in References [14,15]. This configuration has the advantage of a single DC source for all of its modules. The main drawback is that this topology still has a high number of switches.

To eliminate the above drawbacks of multilevel converters from the CHB topology, it is helpful to utilize well-known VSCs (such as the two-level, three-phase VSC; NPC; and FC) to obtain multilevel VSC topologies. These VSCs can be combined in series or in parallel using current-limiting inductors. In both configurations, the power capability depends on the number of VSCs. The multilevel VSC based on the conventional three-phase topology reduces the number of DC capacitors that the CHB converters need, the number of clamping diodes that the multilevel diode-clamped converters need and the number of FCs that the multilevel FC converters need. The concept of interconnecting three traditional three-phase VSCs to produce a multilevel converter was first proposed in Reference [16] and has since been applied to medium-voltage variable-speed drives. In Reference [17], 3 three-phase, two-level VSCs were interconnected using three single-phase transformers in a 1:1 turn ratio. These interconnected transformers increase the output voltage and suppress the circulating current inside the converter. The power capacity of the overall converter is thus three times the capacity of each interconnected converter and the volt–ampere rating of each intermediate transformer is equal to that of each interconnected converter. In Reference [18], another topology, the hexagram multilevel converter, was proposed; this topology combines 6 two-level converters using six inductors. It shares many advantages of the CHB topology while using fewer switches and a smaller DC-link capacitor [19]. In Reference [20], another topology, the hexagonal converter, was presented. This hexagonal topology combines 3 three-level NPC converters using six single inductors. The power capability is three times the power rating of each individual VSC. Figure 1 is a schematic diagram illustrating the multilevel topologies of cascaded two-level VSCs in the previous research. The inductors are required to avoid the presence of excessive current between the interconnected VSC modules. The outputs of these topologies must be connected in open-ended configurations. However, these topologies cannot be extended further and their applicable voltage levels are not as high as that of the CHB converter.

In response to the above concerns, this research is intended to develop a multilevel converter configuration that utilizes the traditional two-level, three-phase VSCs, along with two-winding magnetic elements, to generate many output voltage levels with relatively few DC sources. The presented converter has relatively few semiconductor switches and DC sources even though two-winding magnetic elements are added to converter circuit. Moreover, the advantage of the proposed topology, with respect to the topology presented in Reference [20], is that two-winding magnetic elements are used instead of using

six single phase inductances to interconnect the three-phase converters, reducing the VA rating of the magnetic elements. The two-winding magnetic elements impose a high impedance for the circulating current and a relatively low impedance for the line current currents. The impedance imposed to the line current is the leakage inductance which is neglected to simplify the analysis of the converter. Simulation and experimental waveforms validate the presented converter’s voltage-producing capability.

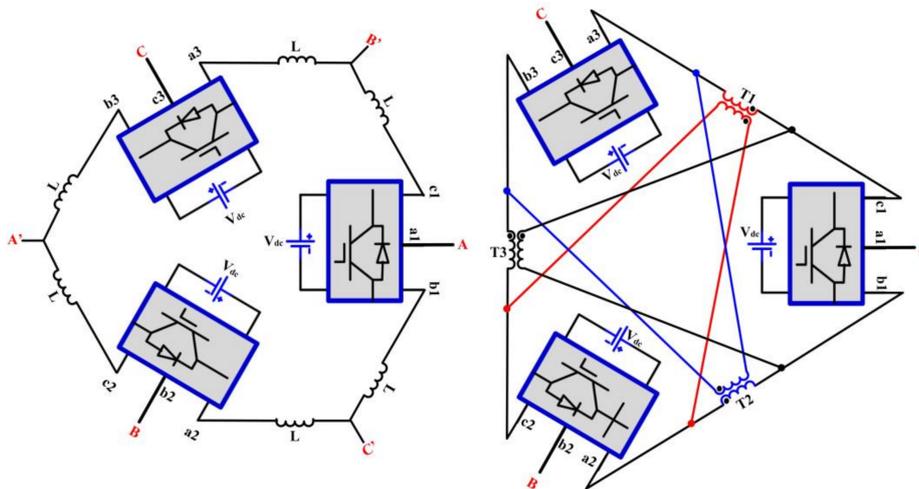


Figure 1. The multilevel converters presented in References [17] (right) and [20] (left).

The paper is organized as follows. Section 2 describes the proposed topology and Section 3 presents the mathematical model for the proposed converter. Section 4 demonstrates the benefits of the two-winding magnetic elements and Section 5 describes the modulation strategy. Sections 6 and 7 includes the simulation results and the experimental discussion, respectively. Finally, Section 8 summarizes the conclusions of the present work.

2. System Description

The proposed configuration of the three-phase grid-connected applications is shown in Figure 2. This configuration is composed of six traditional two-level, three-phase VSC modules that have hexagonal interconnections to produce higher voltage levels, as shown in Figure 2. Each VSC module supplies 1/6 of the converter’s output power.

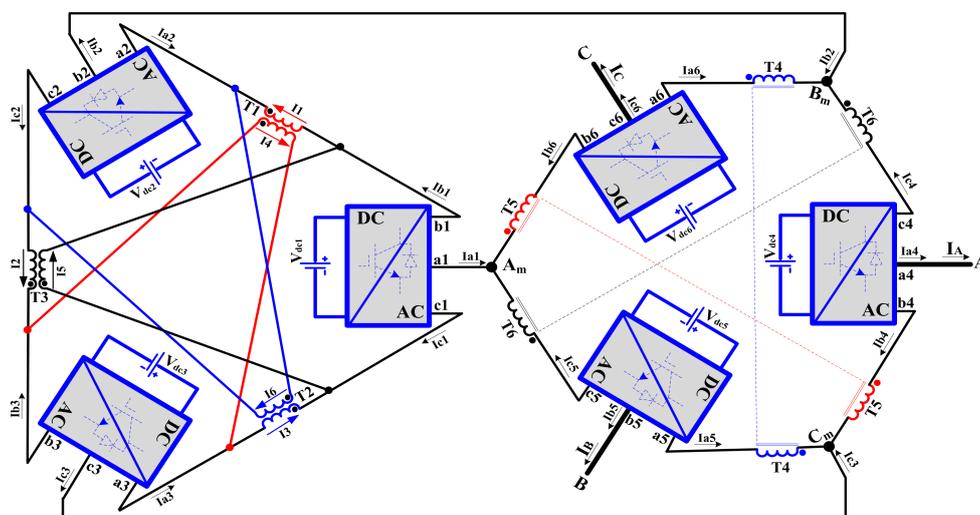


Figure 2. Proposed multilevel Voltage Source Converter (VSC) topology.

The output terminal nodes of the proposed converter are labeled A (AC terminal node a_4 of module 4), B (AC terminal node b_5 of module 5) and C (AC terminal node c_6 of module 6). The other two AC terminal nodes, b_4 of module 4 and a_5 of module 5, are coupled with AC terminal node c_3 of module 3 by way of magnetic element. AC terminal nodes c_4 of module 4 and a_6 of module 6 are coupled by way of a magnetic element with AC terminal node b_2 of module 2. Similarly, AC terminal nodes c_5 of module 5 and b_6 of module 6 are coupled with AC terminal node a_1 of module 1 via a magnetic element. The remaining two AC terminals of each module are connected to adjacent modules through another magnetic element (e.g., T_1 , T_2 and T_3 for modules 1, 2 and 3, respectively). AC terminal b_1 of module 1 is coupled to AC terminal a_3 of module 3 through the primary winding of T_1 ; AC terminal c_1 of module 1 is coupled to AC terminal a_2 of module 2 through the primary winding of T_2 . The remaining modules consist of similar connections, as shown in Figure 2.

3. System Modeling

3.1. Current Relations

The phase currents of the VSC modules fulfill the following expressions:

$$\begin{bmatrix} i_{a1} + i_{b1} + i_{c1} \\ i_{a2} + i_{b2} + i_{c2} \\ i_{a3} + i_{b3} + i_{c3} \\ i_{a4} + i_{b4} + i_{c4} \\ i_{a5} + i_{b5} + i_{c5} \\ i_{a6} + i_{b6} + i_{c6} \end{bmatrix} = 0. \quad (1)$$

Assuming that the intermediate single-phase transformers have large magnetizing inductances, the circulating currents are suppressed to low values and can be ignored; hence,

$$i_1 + i_2 + i_3 = 0 \text{ and} \quad (2)$$

$$i_{b4} + i_{b6} + i_{c4} + i_{c5} + i_{a6} + i_{a5} = 0. \quad (3)$$

From Figure 2, the currents of the VSC Modules 1, 2 and 3 can be written as

$$\begin{bmatrix} i_{a1} \\ i_{b1} \\ i_{c1} \\ i_{a2} \\ i_{b2} \\ i_{c2} \\ i_{a3} \\ i_{b3} \\ i_{c3} \end{bmatrix} = \begin{bmatrix} i_3 - i_1 \\ i_1 - i_5 \\ i_5 - i_3 \\ i_6 - i_1 \\ i_1 - i_2 \\ i_2 - i_6 \\ i_3 - i_4 \\ i_4 - i_2 \\ i_2 - i_3 \end{bmatrix}. \quad (4)$$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} i_4 \\ i_5 \\ i_6 \end{bmatrix}, \text{ and} \quad (5)$$

$$\begin{bmatrix} i_{a1} \\ i_{b2} \\ i_{c3} \end{bmatrix} = - \begin{bmatrix} i_{c5} + i_{b6} \\ i_{c4} + i_{a6} \\ i_{b4} + i_{a5} \end{bmatrix}. \quad (6)$$

The current equations of VSC modules 4, 5 and 6 have the following expressions:

$$\begin{bmatrix} i_{a6} \\ i_{b4} \\ i_{c5} \end{bmatrix} = \begin{bmatrix} i_{a5} \\ i_{b6} \\ i_{c4} \end{bmatrix}. \quad (7)$$

Next, suppose that the proposed converter is linked to a three-phase source load. In that case, the output currents will satisfy the following equations:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} i_{a4} \\ i_{b5} \\ i_{c6} \end{bmatrix} = \begin{bmatrix} I|0 \\ I|-120 \\ I|+120 \end{bmatrix}. \quad (8)$$

Using (1) and (4)–(8), the output current of each VSC module can be shown to be

$$\begin{bmatrix} i_{a1} \\ i_{b1} \\ i_{c1} \end{bmatrix} = \begin{bmatrix} i_{a2} \\ i_{b2} \\ i_{c2} \end{bmatrix} = \begin{bmatrix} i_{a3} \\ i_{b3} \\ i_{c3} \end{bmatrix} = \begin{bmatrix} i_{a4} \\ i_{b4} \\ i_{c4} \end{bmatrix} = \begin{bmatrix} i_{a5} \\ i_{b5} \\ i_{c5} \end{bmatrix} = \begin{bmatrix} i_{a6} \\ i_{b6} \\ i_{c6} \end{bmatrix} = \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} I|0 \\ I|-120 \\ I|+120 \end{bmatrix}. \quad (9)$$

where $[I_A, I_B, I_C]^T$ and I are the converter output-phase currents and their RMS values, respectively. Based on (9), each VSC module within the proposed converter has an identical current under the symmetrical operation condition.

3.2. Voltage Relations

Under the symmetrical operation condition, the fundamental component (RMS) of the output voltages of each VSC module can be described as

$$\begin{bmatrix} V_{a1b1} \\ V_{b1c1} \\ V_{c1a1} \end{bmatrix} = \begin{bmatrix} V_{a3b3} \\ V_{b3c3} \\ V_{c3a3} \end{bmatrix} = \begin{bmatrix} V_{a5b5} \\ V_{b5c5} \\ V_{c5a5} \end{bmatrix} = \begin{bmatrix} V_{a2b2} \\ V_{b2c2} \\ V_{c2a2} \end{bmatrix} = \begin{bmatrix} V_{a4b4} \\ V_{b4c4} \\ V_{c4a4} \end{bmatrix} = \begin{bmatrix} V_{a6b6} \\ V_{b6c6} \\ V_{c6a6} \end{bmatrix} = \begin{bmatrix} V|0 \\ V|-120 \\ V|+120 \end{bmatrix} \text{ and} \quad (10)$$

$$V = \frac{\sqrt{3}}{2\sqrt{2}} V_{dc} m_a, \quad (11)$$

where V , V_{DC} and m_a represent the RMS value of each VSC module's output voltage, the DC-link voltage of each VSC module and the amplitude modulation index, respectively.

The output voltages of the proposed converter are written as:

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} V_{AmBm} \\ V_{BmCm} \\ V_{CmAm} \end{bmatrix} + \left(\begin{bmatrix} V_{AAm} \\ V_{BBm} \\ V_{CCm} \end{bmatrix} - \begin{bmatrix} V_{BBm} \\ V_{CCm} \\ V_{AAm} \end{bmatrix} \right). \quad (12)$$

Based on Figure 3, the following equations can be derived:

$$\begin{bmatrix} V_{AmBm} \\ V_{BmCm} \\ V_{CmAm} \end{bmatrix} = \begin{bmatrix} V_{a1b1} + V_{a3b3} + V_{a2b2} \\ V_{b2c2} + V_{b1c1} + V_{b3c3} \\ V_{c3a3} + V_{c2a2} + V_{c1a1} \end{bmatrix} \text{ and} \quad (13)$$

$$\begin{bmatrix} V_{AAm} \\ V_{BBm} \\ V_{CCm} \end{bmatrix} = \begin{bmatrix} V_{a4c4} + V_{a6b6} \\ V_{b5c5} + V_{b6a6} \\ V_{c6a6} + V_{c4b4} \end{bmatrix}. \quad (14)$$

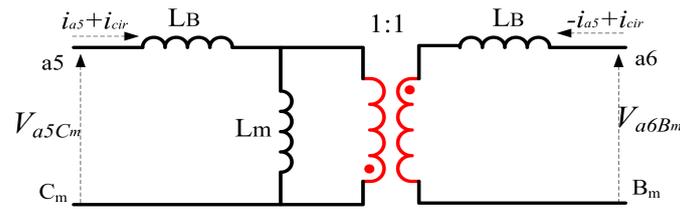


Figure 3. Equivalent circuit for the two-winding magnetic element.

Thus, using (5)–(14), the net output voltages of the proposed converter under the symmetrical operation condition are given by

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} 6 \frac{\sqrt{3}}{2\sqrt{2}} V_{dc} m_a \lfloor 0 \\ 6 \frac{\sqrt{3}}{2\sqrt{2}} V_{dc} m_a \lfloor -120 \\ 6 \frac{\sqrt{3}}{2\sqrt{2}} V_{dc} m_a \lfloor +120 \end{bmatrix}. \tag{15}$$

Consequently, (15) demonstrates that the proposed converter’s three-phase output voltage is approximately six times the line voltage of each VSC module.

The volt-ampere rating (S) of each VSC module within the converter is given by

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \begin{bmatrix} \sqrt{3} V_{a1b1} i_{a1} \\ \sqrt{3} V_{a2b2} i_{a2} \\ \sqrt{3} V_{a3b3} i_{a3} \\ \sqrt{3} V_{a4b4} i_{a4} \\ \sqrt{3} V_{a5b5} i_{a5} \\ \sqrt{3} V_{a6b6} i_{a6} \end{bmatrix}. \tag{16}$$

Based on (8)–(10) and on (16), it can be shown that

$$S_1 = S_2 = S_3 = S_4 = S_5 = S_6 = \frac{3}{2\sqrt{2}} V_{dc} m_a I \quad \text{and} \tag{17}$$

$$S_{total} = \sqrt{3} V_{AB} I_A = \frac{18}{2\sqrt{2}} V_{dc} m_a I. \tag{18}$$

Accordingly, (17) and (18) prove that each VSC module is equally loaded and that the total volt-ampere capability of the proposed converter is six times that of each VSC module.

3.3. Volt-Amperes Rating of the Magnetic Elements

Using (10) to (15), the RMS voltage across the magnetic elements windings are given by

$$V_{T1,RMS} = V_{T2,RMS} = V_{T3,RMS} = \frac{\sqrt{3}}{2\sqrt{2}} V_{dc} m_a, \tag{19}$$

$$V_{T4,RMS} = V_{T5,RMS} = V_{T6,RMS} = \frac{4\sqrt{3}}{2\sqrt{2}} V_{dc} m_a. \tag{20}$$

Using (4)–(7), the RMS currents through T_1, T_2 and T_3 are

$$I_1 = I_2 = I_3 = I_4 = I_5 = I_6 = \frac{I}{\sqrt{3}}. \tag{21}$$

Similarly, using (9), the RMS currents through T_4 , T_5 and T_6 are given by

$$I_{a6} = I_{b6} = I_{b4} = I_{c4} = I_{a5} = I_{c5} = I. \quad (22)$$

Therefore, the volt-amperes rating of the intermediate magnetic elements can be calculated as follows:

$$S_{T_1} = S_{T_2} = S_{T_3} = \frac{1}{2\sqrt{2}} V_{dc} m_a I, \quad (23)$$

$$S_{T_4} = S_{T_5} = S_{T_6} = \frac{4\sqrt{3}}{2\sqrt{2}} V_{dc} m_a I. \quad (24)$$

Comparing (21)–(23) and (18), it is clear that volt-amperes rating of T_1 , T_2 and T_3 is 1/18 of the total rating of the converter, while the volt-amperes rating of T_4 , T_5 and T_6 is $2/3\sqrt{3}$ of the total rating of the converter.

4. The Role of the Magnetic Elements

This section investigates the function of the magnetic elements within the proposed converter. Two inductors with an equal number of turns are coupled together; that is, an input to one side produces an output on both sides, as shown in Figure 3. As the turn ratio is approximately 1:1, the self-inductances of the primary and secondary windings are the same (e.g., $L_p = L_s = L_B$). The two-winding magnetic element T_4 is selected for analysis. Applying the voltage relationships from two-winding transformers results in the following equations:

$$v_{x1y1} = L_{11} \frac{dI_1}{dt} + L_{12} \frac{dI_1}{dt}, \text{ and} \quad (25)$$

$$v_{x2y2} = L_{22} \frac{dI_2}{dt} + L_{21} \frac{dI_2}{dt}, \quad (26)$$

where $L_{22} = L_{11} = L_B + L_m$, $L_m = L_{21} = L_{12}$, $I_1 = i_{a5} + i_{cir}$ and $I_2 = -i_{a5} + i_{cir}$, such that L_B is the leakage inductance (which is expected to be identical for all windings) and L_m is the magnetizing inductance.

It is obvious from Figure 3 that the voltage drop on one of the magnetic elements is

$$v = V_{a5Cm} + V_{a6Bm}.$$

Using (17) and (18), the voltage across the coupled inductor can be expressed as

$$v = (L_B + L_m) \frac{d(i_{a5} + i_{cir})}{dt} + L_m \frac{d(-i_{a5} + i_{cir})}{dt} + (L_B + L_m) \frac{d(-i_{a5} + i_{cir})}{dt} + L_m \frac{d(i_{a5} + i_{cir})}{dt}, \quad (27)$$

$$v = (2L_B + 4L_m) \frac{d(i_{cir})}{dt}.$$

Therefore, the total voltage drop across the magnetic elements can be expressed as

$$v_{total} = 3(2L_B + 4L_m) \frac{d(i_{cir})}{dt} = (6L_B + 12L_m) \frac{d(i_{cir})}{dt}. \quad (28)$$

The magnetizing inductance is much higher than the leakage inductance. Therefore, neglecting the leakage inductance, the two-winding magnetic element imposes twelve times the magnetizing inductance for the circulating current.

5. Modulation Strategy

To obtain an output voltage with low total harmonic distortion, a multicarrier PS-PWM [21] switching strategy is implemented to drive each IGBT in the converter. Optimum harmonic cancellation

is accomplished by shifting each carrier cell by $2\pi T_s/3T$ in sequence, where T_s is the switching time and T is the cycle modulation time. Figure 4 shows the relationship between the modulation waveforms and the three groups of carriers within the converter. As shown in Figure 3, the triangular carriers (carrier 1, carrier 2 and carrier 3) are phase-shifted 120° relative to each other and directly compared with the modulation signals to drive the IGBTs within the VSC modules. To generate the switching signals that are used to drive the IGBTs within module 4, module 5 and module 6, the carrier signals are inverted and then compared with the modulation signals.

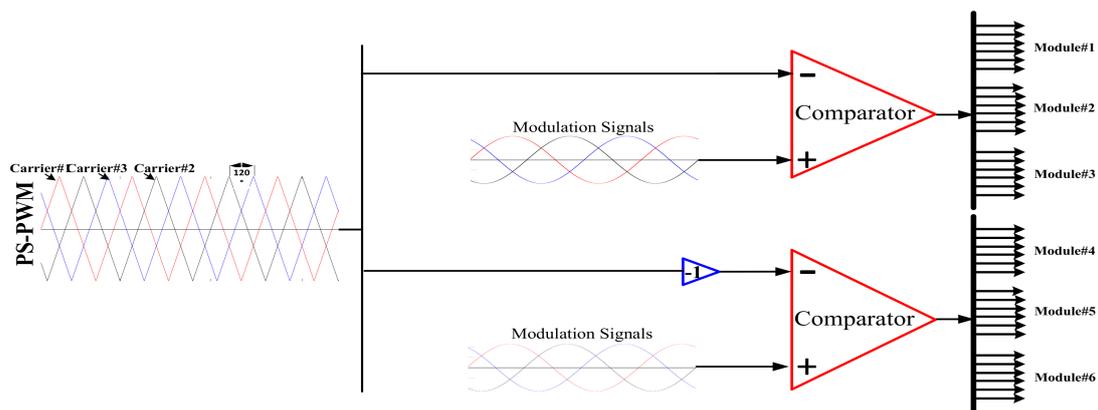


Figure 4. Proposed PS-PWM diagram.

6. Simulation Results

The proposed converter can be implemented using various VSCs with six isolated DC links. The two-level VSC topology is chosen for implementing the present topology because of its simplicity. To confirm the theoretical analysis provided in Section 3, simulations are carried out in the MATLAB/Simulink environment. The DC-link voltage is 30 V. The output terminals of the converter are connected to an inductive load of 77 mH, connected in a wye configuration.

The thirteen-level line-line voltages of the proposed converter (for a modulation index of 1.0 and a switching frequency of 900 Hz) are generated in a steady state, as shown in Figure 5. The voltages are balanced, as demonstrated in (15). It is clear from Figure 5 that the voltage across the load terminals is multistep and, therefore, has low dv/dt and low harmonic content. Figures 6 and 7 show the currents of the VSC modules. Given the configuration of the three-phase converter, the line currents of every VSC module within the converter are symmetrical, thus verifying the relationship in (9). Moreover, the currents inside every VSC module are the same as the output current.

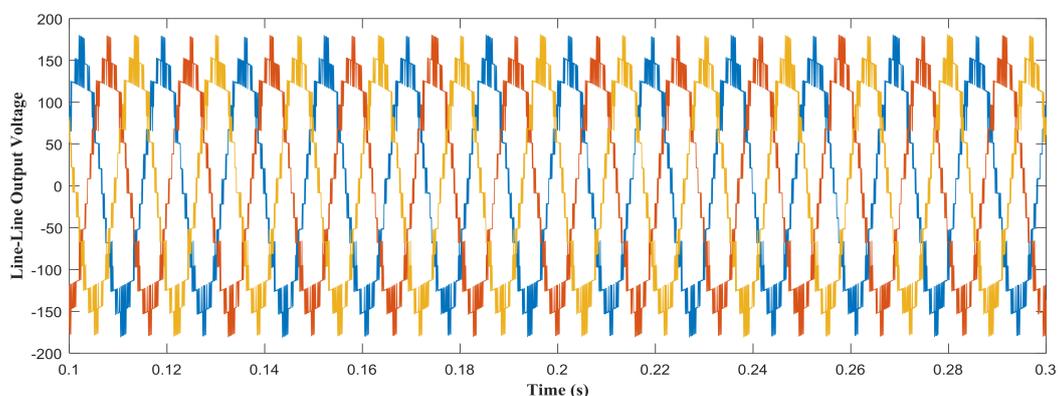


Figure 5. Three-phase line-line output voltage for the proposed converter (blue: V_{AB} ; red: V_{BC} ; yellow: V_{CA}).

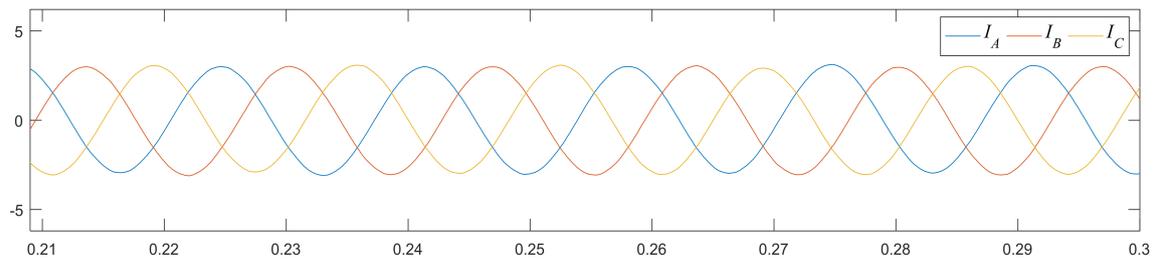


Figure 6. Three-phase output current for the proposed converter.

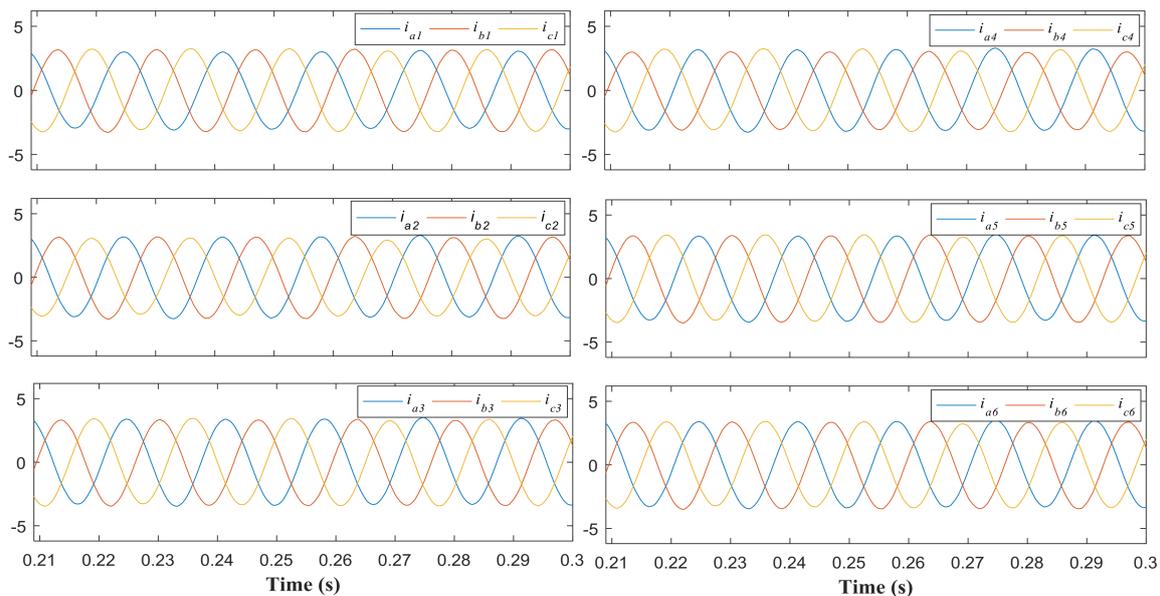


Figure 7. Currents inside the proposed converter.

A third order harmonic with an amplitude of $1/6$ with respect to the fundamental component is injected in order to increase the amplitude of the fundamental output voltage by about 15% without over modulation. A comparative analysis between the line-line voltages based conventional PWM and third harmonics injection PWM (THI-PWM) is shown in Figure 8. It can be observed from Figure 8 that the magnitude of the low order harmonics has been considerably reduced to a negligible value. The total harmonic distortion (THD) of the output line voltage is 12.32%. Because of the 120 phase shifts among VSC converters, all triplen harmonics in line voltages are also very small. Moreover, the first center band harmonics are cancel and shifted to 90 times of fundamental frequency by providing a phase shift of 120 between carrier waves. Consequently, the effective switching frequency of the line-line voltage is six times higher than the switching frequency.

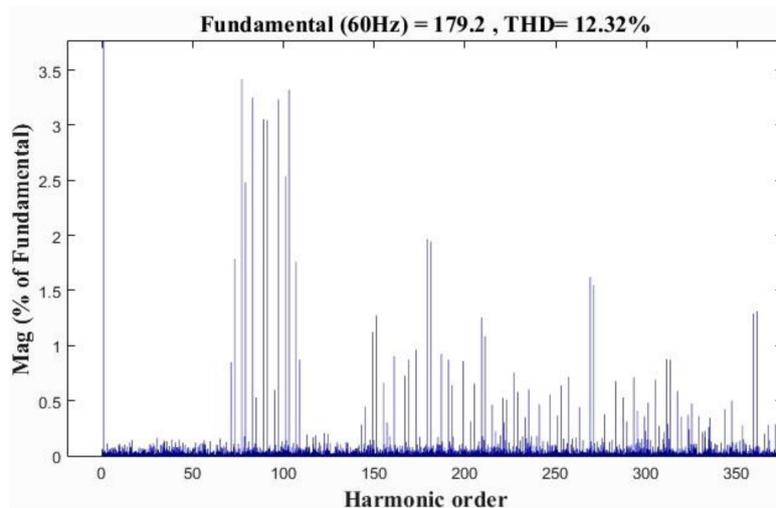


Figure 8. THD spectrum of output voltage (V_{ab}) of THI-PWM.

7. Experimental Results

An experimental prototype of the proposed converter is built to the following specifications:

- DC-link voltage: 30 V;
- Inductive load: 77 mH;
- Resistive load: 48 Ω ;
- Fundamental frequency: 60 Hz; and
- Switching frequency: 900 Hz.

To validate the proposed converter's good performance, the PS-PWM technique shown in Figure 4 is implemented using a ds1202 MicroLabBox. The fundamental frequency of the reference signal is 60 Hz and the switching frequency is 900 Hz. Figure 9 shows a prototype of the proposed converter. It includes six magnetic elements; 6 two-level, three-phase VSC modules; resistive-inductive loads; and the ds1202-based controller. The block diagram of the PWM control system is shown in Figure 4. The gating signals generated in the ds1202 controller are applied to the IGBT via an isolated driver. In the prototype, SKM75GB12V IGBTs (ratings: 1200 V and 75 A) are used as switching devices. The gate driver SKYPER 32R provides both amplification and isolation from the power circuit. An oscilloscope (YOKOGAWA model no. DLM2054) is used to measure the output voltages. The line currents are measured using a Hall effect current sensor (model no. LTS 25-NP). The currents measured using this sensor are applied to the ADC of the ds1202 board and the resulting measured signals are drawn using the Simulink environment. The experimental parameters are shown in Table 1.

Table 1. Prototype parameters.

Parameter	Value
DC supply voltage	$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V_{dc5} = V_{dc6} = 30$ V
Resistive, inductive loads	48 Ω , 77 mH
Carrier frequency	900 Hz
DC links capacitors	4 mF
Two-Winding Magnetic Elements	
Turns ratio	1:1
RMS voltage	120 V
Magnetizing Inductance	1400 mH
Leakage Inductance	90 μ H
Winding resistance	0.3 Ω

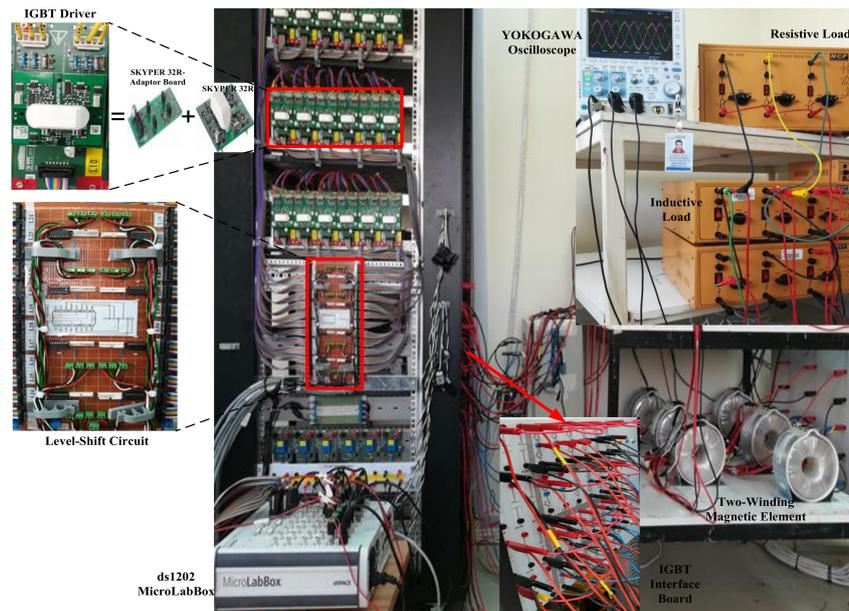


Figure 9. Prototype setup in the laboratory.

Figures 10 and 11 show the line-line voltage waveforms and fast fourier transform (FFT) results for a wye-connected resistive load (48Ω) at different modulation index. The figures show that for both cases, a poor THD are obtained when the converter operated at low modulation index. This is to be expected because at low modulation index, the converter essentially behaves like a conventional seven-level converter. A better THD is obtained when the converter operated at higher modulation index. Moreover, it can be seen from the results that the increase in the index of modulation rejects the first harmonics' non-null worms of the higher frequencies and thus facilitates filtering. A comparative analysis between the line-line voltages based conventional PWM and third harmonics injection PWM (THI-PWM) is shown in Figure 11. It can be observed that the magnitude of the low order harmonics has been considerably reduced to a negligible value. The results also show that the injection of harmonic 3 in the reference signal makes it possible to improve the form of the output voltage and to increase the maximum amplitude of fundamental in the output voltage. Besides, the analysis of the results shows that the spectrum of harmonics of the output voltage is improved compared to the triangular sinusoidal PWM.

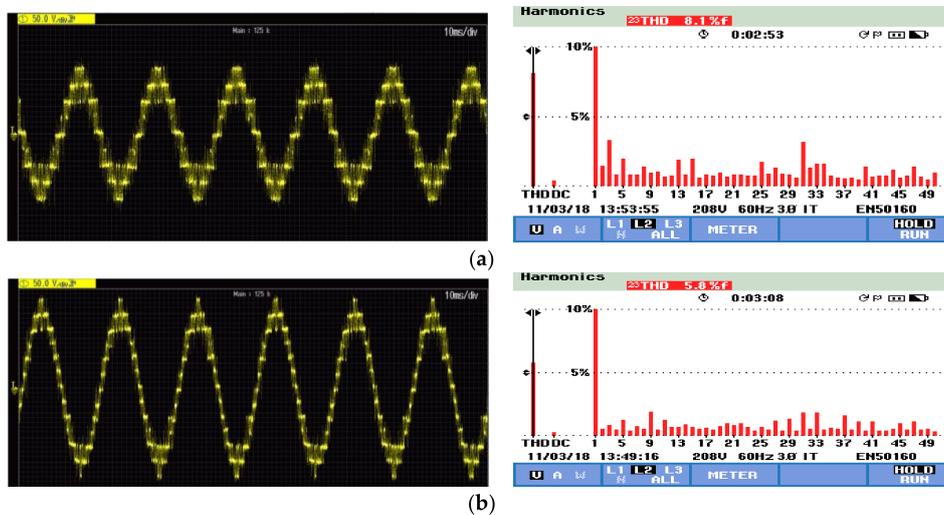


Figure 10. Output voltage and FFT results for a modulation index of (a) 0.65; and (b) 0.95.

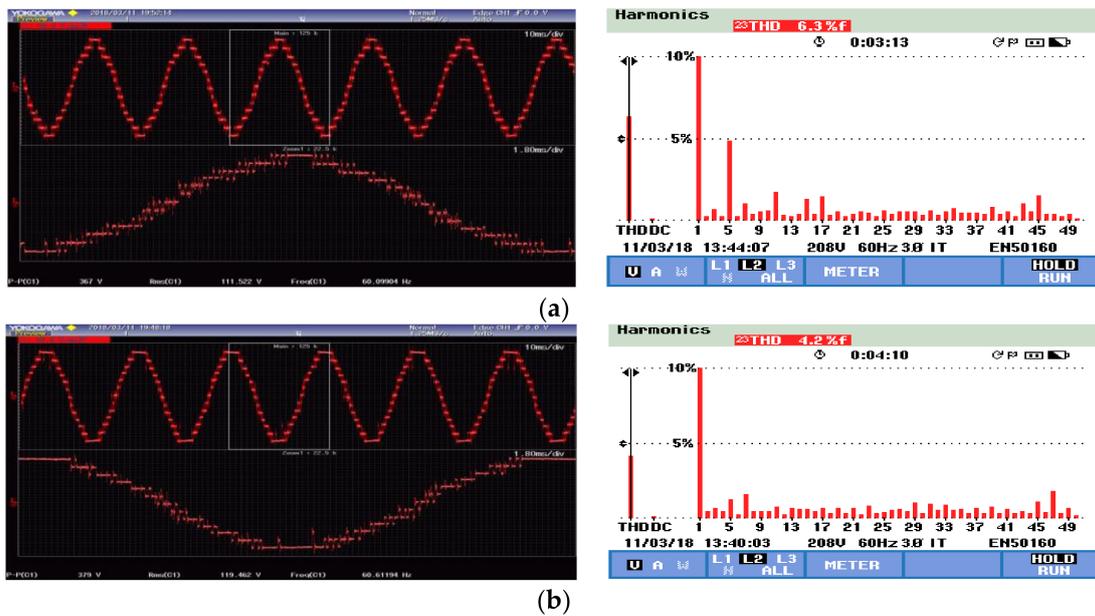


Figure 11. Output voltage and FFT results for a (a) Sinusoidal PWM; and (b) THI-PWM.

The steady-state experimental results of the proposed converter are presented in Figures 12–14. The output terminals of the converter are connected to an inductive and resistive load of 48 Ω resistance and 77 mH inductance and connected in a wye configuration. The thirteen-level line-line voltages of the proposed converter (with a modulation index of 0.95 and a switching frequency of 900 Hz) are shown in Figure 12. As shown in Figures 13 and 14, the line currents of every VSC module within the converter are symmetrical and are the same as the output current, hence verifying the relationships in (9) and the simulation results in Figure 7.

The proposed converter was proposed to generate 13 output voltage levels. If we want to synthesize the same number of output voltage levels with conventional multilevel converters, we can find that they need many components compared with the proposed scheme as given in Table 2. As shown in this table, the proposed topology has the least number of switches compared to the prior art topologies (e.g., NPC, FC, CHB).

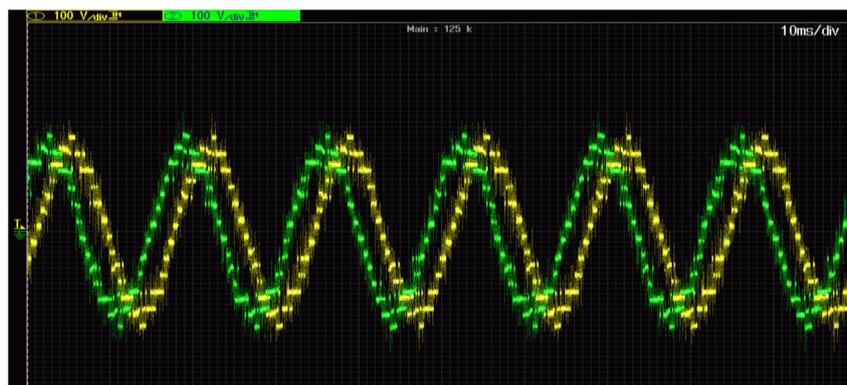


Figure 12. Output voltages V_{AB} and V_{CB} for a modulation index of 0.95.

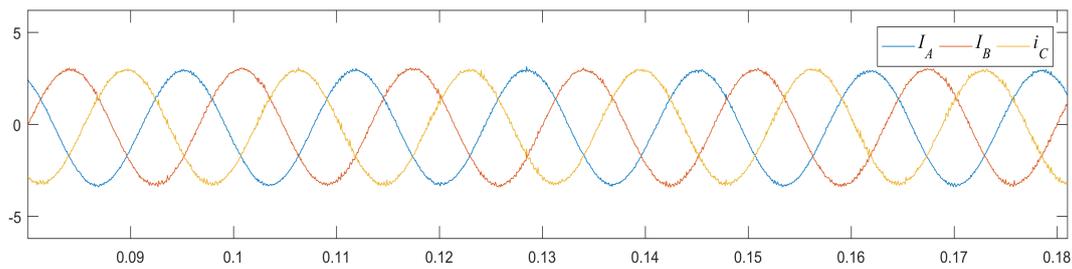


Figure 13. Three-phase load currents.

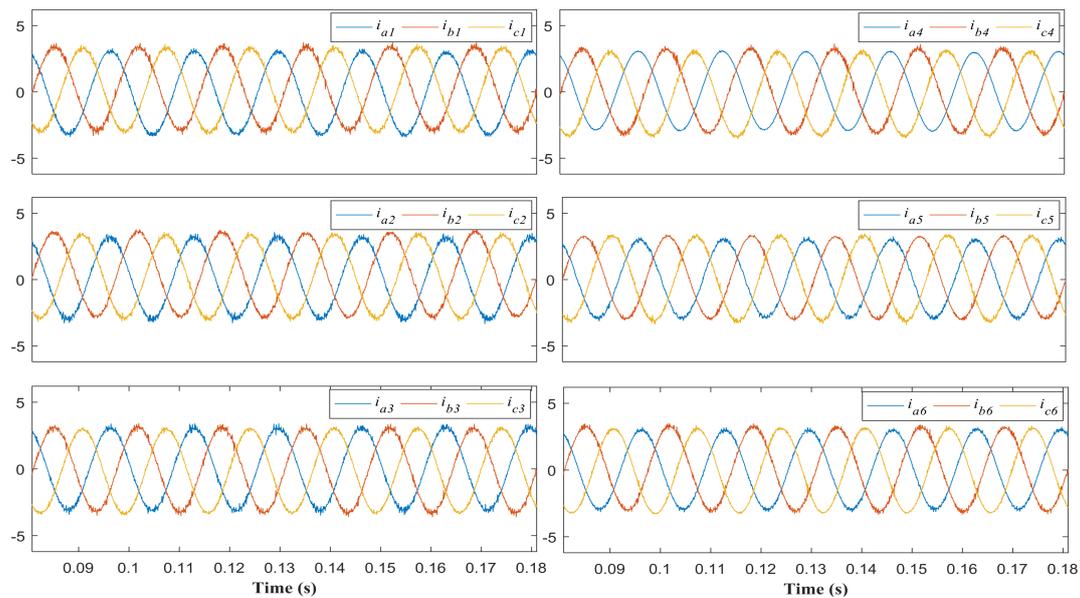


Figure 14. Currents inside the proposed converter.

Table 2. Component comparison of the proposed converter and traditional multilevel converters.

Components	NPC	FC	CHB	Proposed
Switches	36	36	72	36
Magnetic Elements	0	0	0	6
Diodes	396	0	0	0
Capacitors	4	210	18	6
Modularity	No	No	Yes	Yes
Voltage Balancing Problem	Yes	Yes	No	No
Isolated DC Sources	No	No	Yes	Yes

8. Conclusions

This paper introduces an isolated, cascaded, multilevel VSC topology employing two-winding magnetic elements for high-power applications. The topology consists of 6 two-level, three-phase VSCs with isolated DC links and 6 two-winding magnetic elements. The structure of the proposed topology is given and analyzed in detail, including the voltage relationships, current relationship, power allocation and the modulation of PS-PWM. The power capability of the proposed VSC is six times higher than that of each VSC module. Each VSC contributes equally to the total power without the need for a sharing algorithm; thus, the converter operates as a single, three-phase VSC. The comparative analysis with classical NPC, FC and CHB shows superior features of less IGBTs, capacitor requirement and less diodes. It reduces the IGBTs count by 50% and isolated energy sources requirement by 33.3%

compared with a three-phase CHB topology. To confirm the performance of the proposed topology, it is simulated in the MATLAB/Simulink environment; the results are also experimentally demonstrated using a laboratory prototype.

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References

- Rodriguez, J.; Lai, J.S.; Peng, F.Z. Multilevel inverters: A survey of topologies, control and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [[CrossRef](#)]
- Du, Z.; Tolbert, L.M.; Ozpineci, B.; Chiasson, J.N. Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter. *IEEE Trans. Power Electron.* **2009**, *24*, 25–33. [[CrossRef](#)]
- Gupta, K.; Ranjan, A.; Bhatnagar, P.; Sahu, L.; Jain, S. Multilevel inverter topologies with reduced device count: A review. *IEEE Trans Power Electron.* **2016**, *31*, 135–150. [[CrossRef](#)]
- Franquelo, L.; Rodriguez, J.; Leon, J.; Kouro, S.; Portillo, R.; Prats, M. The age of multilevel converters arrives. *Ind. Electron. Mag.* **2008**, *2*, 28–39. [[CrossRef](#)]
- Nabae, A.; Takahashi, I.; Akagi, H. A new neutral-point-clamped PWM inverter. *IEEE Trans. Ind. Appl.* **1981**, *17*, 518–523. [[CrossRef](#)]
- Hammond, P. A new approach to enhance power quality for medium voltage ac drives. *IEEE Trans. Ind. Appl.* **1997**, *33*, 202–208. [[CrossRef](#)]
- Escalante, M.F.; Vannier, J.C.; Arzandé, A. Flying capacitor multilevel inverters and DTC motor drive applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 809–815. [[CrossRef](#)]
- Cengelci, E.; Enjeti, P.; Singh, C.; Blaabjerg, F.; Pederson, J.K. New medium voltage PWM inverter topologies for adjustable speed AC motor drive systems. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 15–19 February 1998; pp. 565–571.
- Pérez, M.A.; Bernet, S.; Rodriguez, J.; Kouro, S.; Lizana, R. Circuit topologies, modeling, control schemes, and applications of modular multilevel converters. *IEEE Trans. Power Electron.* **2015**, *30*, 4–17. [[CrossRef](#)]
- Yu, Y.; Konstantinou, G.; Hredzak, B.; Agelidis, V.G. Power Balance of Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Integration. *IEEE Trans. Power Electron.* **2016**, *31*, 292–303. [[CrossRef](#)]
- Banaei, M.R.; Salary, E. New multilevel inverter with reduction of switches and gate driver. *Energy Convers. Manag.* **2011**, *52*, 1129–1136. [[CrossRef](#)]
- Vazquez, S.; Leon, J.I.; Franquelo, L.G.; Padilla, J.J.; Carrasco, J.M. DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source. *IEEE Trans. Ind. Electron.* **2009**, *56*, 2513–2521. [[CrossRef](#)]
- Chattopadhyay, S.K.; Chakraborty, C. Performance of three-phase asymmetric cascaded bridge (16:4:1) multilevel inverter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 5983–5992. [[CrossRef](#)]
- Kang, F.S.; Park, S.J.; Cho, S.E.; Kim, C.U.; Ise, T. Multilevel PWM inverters suitable for the use of standalone PV power system. *IEEE Trans. Energy Convers.* **2005**, *20*, 906–915. [[CrossRef](#)]
- Park, S.J.; Kang, F.S.; Cho, S.E.; Moon, C.J.; Nam, H.K. A novel switching strategy for improving modularity and manufacturability of cascaded transformer based multilevel inverters. *Electr. Power Syst. Res.* **2005**, *74*, 409–416. [[CrossRef](#)]
- Cengelci, E.; Sulistijo, S.U.; Woo, B.O.; Enjeti, P.N. A new medium-voltage PWM inverter topology for adjustable-speed drives. *IEEE Trans. Ind. Appl.* **1999**, *35*, 628–637. [[CrossRef](#)]
- Teodorescu, R.; Blaabjerg, F.; Pedersen, J.K.; Cengelci, E.; Enjeti, P.N. Multilevel inverter by cascading industrial VSI. *IEEE Trans. Ind. Electron.* **2002**, *49*, 832–838. [[CrossRef](#)]
- Jun, W.; Smedley, K.M. Hexagram Inverter for Medium-Voltage Six-Phase Variable-Speed Drives. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2473–2481. [[CrossRef](#)]
- Wen, J.; Member, S.; Smedley, K.M.; Jun, W. Synthesis of multilevel converters based on single- and/or three-phase converter building blocks. *IEEE Trans. Power Electron.* **2008**, *23*, 1247–1256. [[CrossRef](#)]

20. Laka, A.; Barrena, J.A.; Chivite-Zabalza, J.; Rodriguez, M.A.; Izurza-Moreno, P. New hexagonal three-phase voltage source converter topology for high power applications. *IEEE Trans. Ind. Electron.* **2015**, *62*, 30–39. [[CrossRef](#)]
21. Miguel, M.; Francisco, H.A. A Comparison of modulation techniques of modular multilevel converters. *Energies* **2016**, *9*, 1091.



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