energies

MDPI

Article

Analysis of Non-Isolated Multi-Port Single Ended Primary Inductor Converter for Standalone Applications

C. Anuradha [1], C. Sakthivel [2,*], T. Venkatesan [3] and N. Chellammal [1,*]

[1] Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, SRM Nagar 603203, India; anuradha.c@ktr.srmuniv.ac.in

[2] Department of Electrical and Electronics Engineering, JCT College of Engineering and Technology, Coimbatore 641105, India

[3] Department of Electrical and Electronics Engineering, K. S. Rangasamy College of Technology, Tiruchengode 637215, India; venketesan@ksrct.ac.in

* Correspondence: tcsakthivel107@gmail.com (C.S.); chellammal.n@ktr.srmuniv.ac.in (N.C.); Tel.: +91-984-056-5701 (C.S.); +91-99-6296-4643 (N.C.)

Received: 29 November 2017; Accepted: 5 February 2018; Published: 2 March 2018

Abstract: A non-isolated Multiport Single Ended Primary Inductor Converter (SEPIC) for coordinating photovoltaic sources is developed in this paper. The proposed multiport converter topologies comprise a Single Input Multi yield (SIMO) and Multi Input Multi Output (MIMO). It is having the merits of decreased number of parts and high power density. Steady state analysis verifies the improved situation of both the proposed topologies, which is further checked through simulation results.

Keywords: single input multi output; multi input multi output; single ended primary inductor converter

1. Introduction

Sustainable power sources are of potential interest these days to supplant the conventional fossil fuel power generation. Future power systems will require interfacing of different power sources. To empower multi-source innovation, a multi-input control converter (MIPC) is of practical use. The multi-input control supply could accommodate an assortment of sources and consolidate their features. With numerous data sources, the power source provides unwavering quality and effectively uses power sources. A multi-input control converter (MIPC) contains different sources fed through separate converters as shown in Figure 1. The MIPC structure incorporates a few drawbacks, for example, it requires a different converter for each source which makes the structure complicated and control techniques difficult. As a result of this reason the usage exertion of MIPC is high.

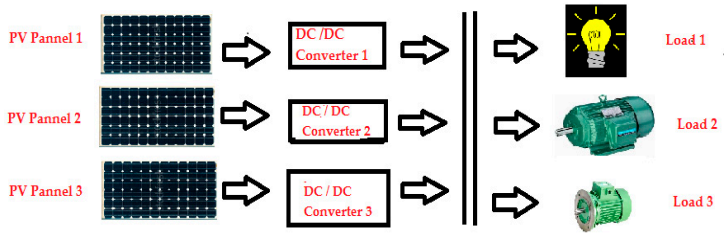


Figure 1. Conventional multi-input converter.

To overcome these challenges in MIPC, multiport converters (MPCs) are of potential interest for applications, for example, the aging grids using numerous sustainable power sources. In MPCs,

different sources are fed to the load through a single power electronics converter as shown in Figure 2. MPC leads to a reduction of the unpredictability of the structure and the control procedure. Different kinds of MPC under DC-DC buck-boost topology have been considered, and limitations of MPC have also been figured out [1–4].

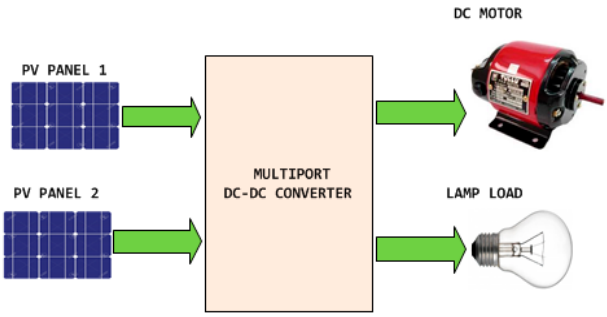


Figure 2. Multiport structure for four ports.

Second, voltage sagging is a fundamental feature in the majority of their new sources, which imposes unnecessary requests and unpredictability to converter designs [5]. Third, very dangerously high electrostatic potentials are frequently introduced to the sources [6,7]. In this manner, parallel-associated topologies have been generally well known [8,9]. Based on coupling, isolated MPCs are typically derived by combining various converters via magnetic coupling such as utilizing multi-winding transformers [10,11], Disconnection and bidirectional abilities of the considerable number of ports can be accomplished in these topologies [12,13]. These MPCs are valuable for the applications where detachment and bidirectional change are essential. However, the real issue is that an excessive number of dynamic switches are available, and the utilization of transformers makes the structure massive [14,15]. The non-isolated structure does not utilize a transformer which makes for an economical and simpler structure [16–20].

The method of developing dual or multi input converters from single input converters was not explained in [21,22]. In [23] the concepts of Pulsating Voltage Source Cell (PVSC) and the Pulsating Voltage Load Cell (PVLC) have been introduced. These PVSC and PVLC are extracted from the basic non-isolated converters like buck, boost, buck- boost, Cuk, zeta, and SEPIC converters. In [24] they used as the single input multi output but no storage device. In this proposed system a non-isolated SEPIC converter is used as the PVSC as well as PVLC with the storage device. Since sustainable power sources are irregular in nature, the use of device capacity is necessary for reliability aspects [25]. A classification of the various multiport converters is given in Figure 3.

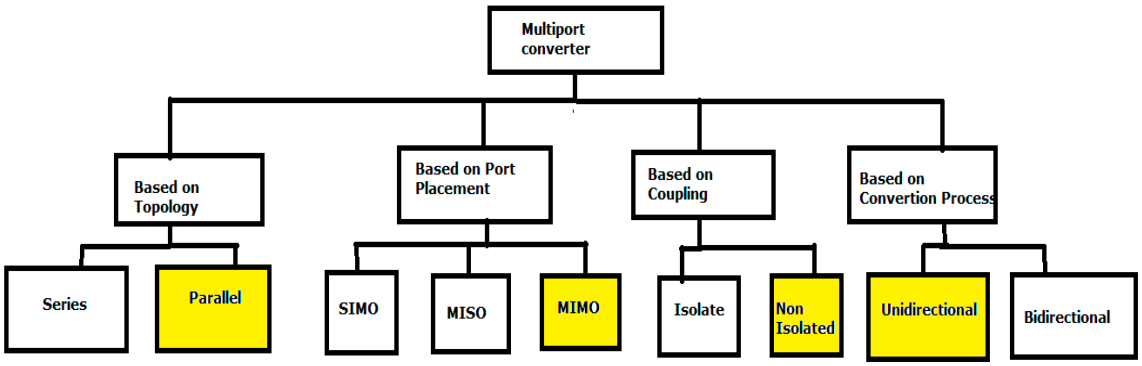


Figure 3. Classificationof Multiport Converter.

In unidirectional MPCs, the arrangement for associating storage device is not available, so this structure is less reliable compared with bidirectional MPC. Bidirectional MPC's contains bidirectional ports which can use for associating storage devices. In this paper, the proposed structure is a parallel connected non-isolated SEPIC/SEPIC bidirectional MPC.

2. SEPIC Converter

DC-DC converters are most prevalently known for their ability to increase or decrease the magnitude of the dc input voltage and furthermore rearrange its polarity [26]. A dc-dc converter works by quickly turning on and off a power electronics switch. A buck-boost, Cuk and SEPIC converter can increase or decrease the output voltage more than the input voltage. In Cuk and SEPIC converters the information current is consistent, unlike in a buck-boost converter, which leads to an advantage of a better power factor. Another advantage of SEPIC converters is that they have non-inverting output unlike in a Cuk converter or buck-boost converter [27]. Also in a SEPIC converter, a series capacitor is used to transfer energy from the input to the output and thus it can respond more smoothly to a short circuit output, being capable of a true shutdown. When the switch is turned off, its output drops to 0 V. The circuit diagram of a SEPIC converter is shown in Figure 4.

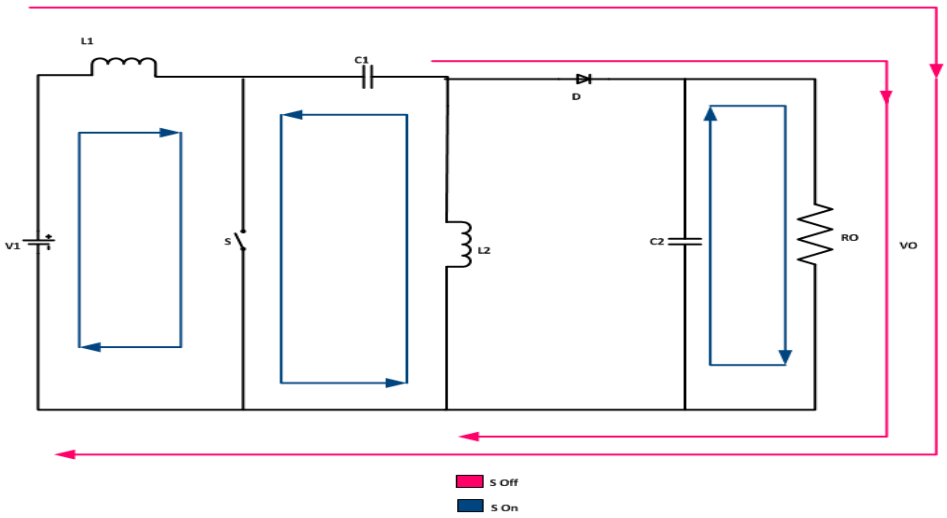


Figure 4. Circuit diagram of a basic SEPIC converter.

In a SEPIC converter, when the pulse is high, the switch S is on, the input voltage charges the inductor L_1, and the capacitor C_1 charges the inductor L_2. The diode D is reverse biased, and the capacitor C_2 maintains the output. When the pulse is low, the switch S is off, the inductors discharge through the diode to the load, and charges the capacitors. The greater the percentage of time (duty cycle) is, the wider the pulse is, and more the output will be, because the longer the inductors charge, the greater their voltage will be.

We assume a SEPIC converter has the small magnitude of switching ripples compared to its respective dc components and that without losses. The link between input and output voltage can be obtained both in continuous current mode (CCM) and in discontinuous current mode (DCM) [4]. CCM is preferable for high efficiency and better utilization of passive components and the converter switches. Converters in both categories provide the same conversion relation given by (1) and (2):

$$V_0(CCM) = V\frac{D}{1-D} \tag{1}$$

$$V_0(DCM) = DV\sqrt{\frac{RT_s}{2L_{eq}}} \tag{2}$$

2.1. Proposed Configuration Description

In this paper, a three port (two inputs and one output) SEPIC/SEPIC converter is proposed as shown in Figure 5. The proposed structure is the combination of pulsating voltage cells (PVC's). PVC's can be of two types. For input side a pulsating voltage source cell (PVSC) is used and for the output side, a pulsating voltage load cell (PVLC). Each PVSC connects with a common PVLC (as it's a MISO structure) through a coupling capacitor forming a complete SEPIC structure. A generalized structure of the proposed circuit shown in Figure 6 indicates that the number of ports can increase/decrease further by connecting/disconnecting the additional PVC's depending on availability of sources [11,14].

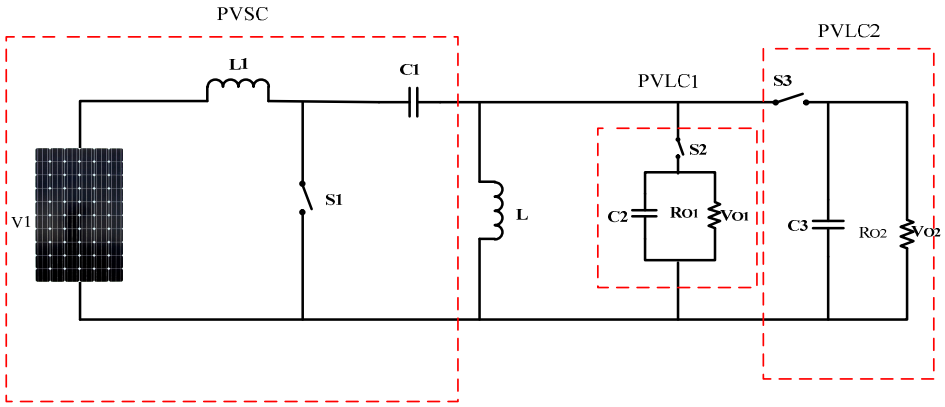


Figure 5. Three port unidirectional SEPIC converter.

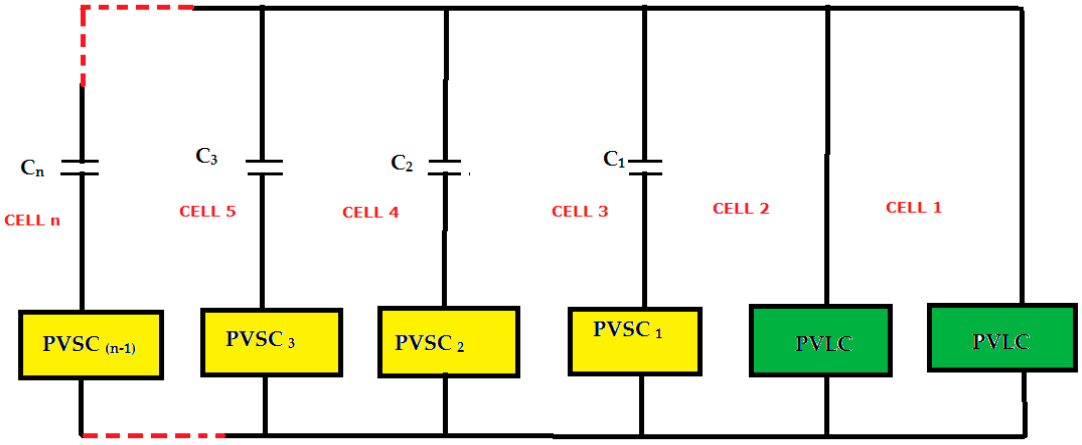


Figure 6. Generalized diagram for SEPIC converter.

2.2. Single Input Multi output SEPIC Converter

Table 1 shows the comparison of components used in proposed n'port SEPIC MPC and conventional MIPC. Here "n" port refers to $(n-1)$ number of sources and one output port or one sources and $(n-1)$ number of output ports [28].

Table 1. Comparison table of components of MPC and MIPC SEPIC.

Components	Multiport Converter	(n) Individual SEPIC Converters
Capacitors	n	$2(n-1)$
Inductors	2	$2(n-1)$
Switches	n	$n-1$
Diodes	0	$n-1$

In the topology, if both the sources are renewable dc sources, for example solar (PV), the converter works as a unidirectional converter as the energy flows from source to load. The switch S1 is provided with a definite duty cycle and is triggered at one time. As the one source is PV it works as a partially unidirectional converter. The reason for becoming particularly unidirectional is that we have a single voltage source. The output power of two loads is varied by varying the duty cycles of the switches. The output can be increased or decreased by varying the duty cycles of the switch S1 with respect to the input voltage. Considering voltage source (PV) having a value of voltage V1. In order to use the source effectively, the source is operated at different duty cycles. The source is operated with higher duty cycle for higher output and for lower duty cycle for lesser value. Assume the input voltage V_1, output voltage to be V_2 and V_3,then D_1, D_2 & D_3 are the respective duty cycles of switch S1, S2 & S3 (PVSC, PVLC1 & PVLC2).

2.3. Modes of Operation

The operation is categorized in three modes as shown in Figure 7.

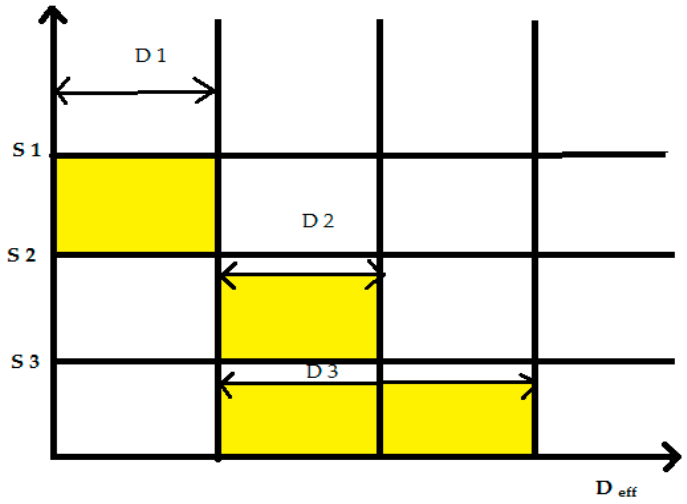


Figure 7. Modes of operation of the topology.

2.3.1. Mode-1: S1 is ON (S1 Conducts) and S2 & S3 are OFF

The equivalent circuit of Mode-1 is shown in Figure 8. In this mode, the input side switch is on and the other switches are turned off. The inductor is charged and the capacitor C_1 is pre-charged and it charges the inductor L. We assume that the capacitor is pre-charged and supplies to the loads. The voltage source provided charges the inductor L_1.

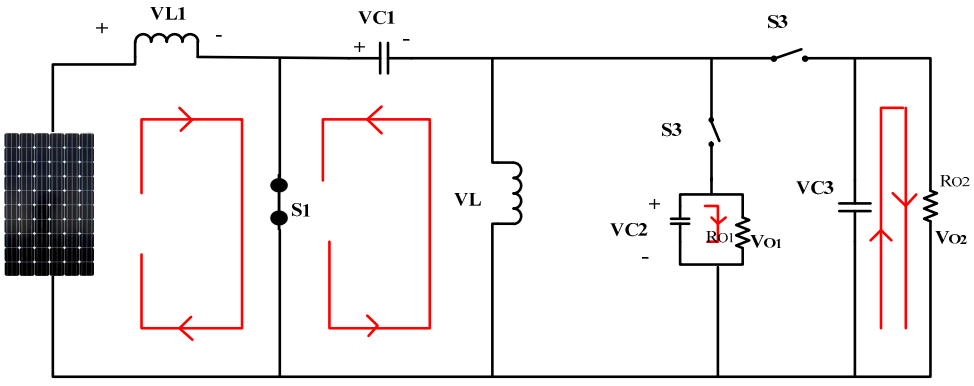


Figure 8. Mode-1 operation of SIMO SEPIC Converter.

2.3.2. Mode-2: S1 OFF and S2 and S3 are ON

The equivalent circuit of Mode-2 is shown in Figure 9. Once the switch S1 is turned on, the switches S2 and S3 are turned off. Now the capacitor C_1 is charged and as the inductors L_1 and common inductor L being charged initially supply current to the load. Now capacitors C_2 and C_3 are charged.

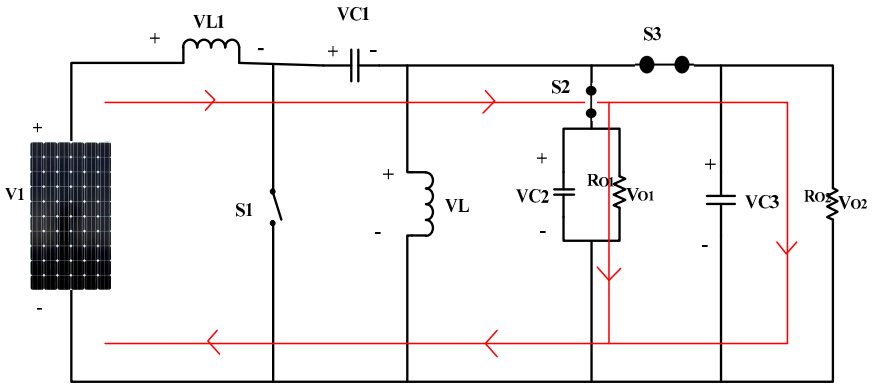


Figure 9. Mode-2 operation of SIMO SEPIC Converter.

2.3.3. Mode-3: S1 and S2 OFF & S3 Conduct

The equivalent circuit of Mode-3 is shown in Figure 10. The switch S1 and S2 are off and S3 is turned on. The inductors L_1 & L_2 supply the current to the load V_3 and the capacitor C_2 supplies the load V_2.

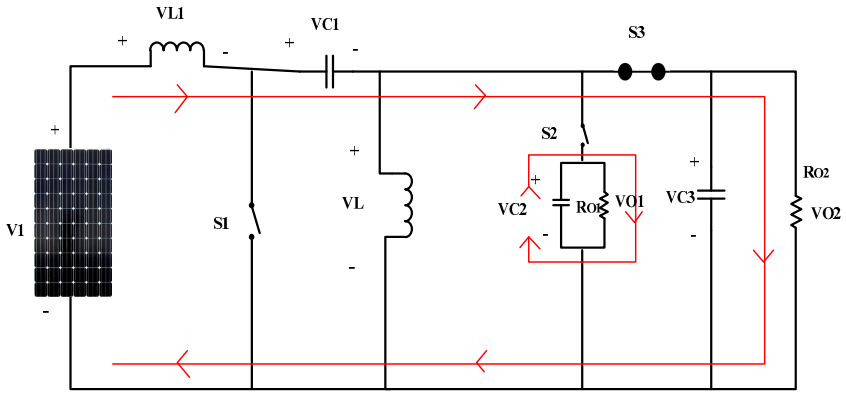


Figure 10. Mode-3 operation of the SIMO SEPIC.

2.4. Steady State Analysis of a Single Input Multi Output SEPIC

The three modes of operations are considered to be in CCM and assuming the ripple voltage and ripple current as negligible. The steady state equations of topology-1 are as follows, the steady state equations of each mode are described below:

$$L\frac{di_{L_1}}{dt} = (V_{C_1}D_1 - V_{C_3}D_{eff}) \quad (3)$$

$$C_1\frac{dV_{c_1}}{dt} = i_L D_1 + i_{L_1}(D_2 + D_{eff}) \quad (4)$$

$$C_2\frac{dV_{C_2}}{dt} = \frac{-V_2}{R_1}(D_1 + D_2 + D_{eff}) + i_{L_1}D_2 + i_L D_2 \quad (5)$$

$$C_3\frac{dV_{C_2}}{dt} = \frac{V_3}{R_2}(D_1 + D_2 + D_{eff}) + i_{L_1}(D_2 + D_{eff}) + i_L(D_2 + D_{eff}) \quad (6)$$

At the state assuming:

$$\frac{di_L}{dt} = 0 \text{ And } V_{C_2} = V_2;\ V_2; V_{C_3} = V_3;\ V_{C_1} = V_1 \tag{7}$$

From Equation (7):

$$V_1 = \frac{D_1}{1 - D_1} V_1 \tag{8}$$

$$V_2 \left[\frac{D_1}{D_2} \left[\frac{1 - D_1 - D_{eff}}{1 - D_1} \right] V_1 \right] \tag{9}$$

On solving the steady state Equations (7) to (9) considering the left hand side as zero, the six state variables can be derived (i_{L1} I_{L12}, i_L, V_{C_1} and V_{C_2}).

2.5. Small Signal Approximation model of Single Input Multi output SEPIC Converter

In this section, the expressions for all the circuit parameters are described. Following the individual mode equations from Equations (3) to (7), the expressions of L_1, L_2, L, C_1, C_2 and C with respect to current and voltage ripples is described below. Considering three modes (i.e., D_1, D_2 and D_{eff}) operating for periods t_1, t_2 and t_3, respectively:

$$t_{A_1} = D_1\ T,\ t_2 = D_2\ T,\ t_3 = D_{eff}\ T \tag{10}$$

In mode-1 the inductor current increases from a low level to high level, say I_{L11} to I_{L12} and in second and third mode, the current falls from I_{L12} to I_{L11}, so the current ripple is considered to be $\Delta\ I_{L1} = I_{L12} - I_{L11}$:

Therefore:

$$L_1 \frac{di_{L_1}}{dt} = V_1 \tag{11}$$

$$L_1 \frac{i\Delta_{L_1}}{dt} = V_1 \tag{12}$$

t_1, t_2 and t_3 can be written as D_1 T, D_2 T and D_{eff} T, respectively, where, T is the total time period. Similarly, the voltage ripples can be calculated from the mode equations. The voltage across C_1 rises (assuming linearly) from a low value to a high value, say V_{11} to V_{12} during the time t_2 and t_3. This gives a voltage ripple $\Delta V_{C1} = V_{C12} - V_{C11}$. In this period the capacitor charges by the source current of V_1, i.e., $I_1 = i_{L1}$:

$$\Delta V_{C_1} = \frac{I_1}{C_1} \left(tD_2 + tD_{eff} \right) \tag{13}$$

$$C_1 = \frac{I_1}{f\Delta V_{C_1}} (D_2 + D_{eff}) \tag{14}$$

The capacitor C_2 discharges in period t_1 and t_3, i.e., this gives a voltage ripple:

$$\Delta V_{C_2} = V_{C_{22}} - V_{C_{21}} \tag{15}$$

$$\Delta V_{C_2} = \frac{V_2}{fR_1C_2} (D_1 + D_{eff}) \tag{16}$$

The output side capacitor C_3 discharges within the period t_1 and provides the load current. The voltage ripple can be written as $\Delta V_{C3} = V_{C32} - V_{C31}$

$$\Delta V_{C_3} = \frac{V_2}{fR_2C_3} (D_1) \tag{17}$$

So, the circuit parameters can be derived from Equations (13) to (16):

$$L_1 = \frac{V_1 D_1}{f \Delta I_{L_1}} \tag{18}$$

$$C_1 = \frac{I_1 D_{eff}}{f \Delta C_{C_1}} \tag{19}$$

$$L = \frac{V_2 (D_2 + D_{eff})}{f \Delta I_L} \tag{20}$$

$$C_2 = \frac{V_2 (D_2 + D_{eff})}{f \Delta V_{C_2} R_1} \tag{21}$$

$$L = \frac{V_3 (D_2 + D_{eff})}{f \Delta I_L} \tag{22}$$

$$C_3 = \frac{V_3 (D_1)}{f \Delta V_{C_3} R_2} \tag{23}$$

V_1 = 25 V, D_1 = 60%, D_2 = 30%, D_{eff} = 10%.

$$\Delta I_{L_1} = 0.5,\ \Delta I_L = 0.5\ \Delta I_{C_1} = 0.5,\ \Delta V_{C_2} = 0.5,\ \Delta V_{C_3} = 0.5$$

Allowed ripples and calculated values of the components are:

L_1 = 3 mH, C_1 = 416 µf,
L = 3.08 mH, C_2 = 539 µf,
L = 3.08 mH, C_3 = 462 µf

Estimated ripples from simulation are:

$$\Delta I_{L_1} = 0.55, \Delta I_L = 0.45$$

3. Multi Input Multi Output SEPIC Converter

In the proposed topology both of the input sources used is PV. The converter works as a unidirectional one where power flows from source to load only. The comparisons of components are listed in Table 2. The loads used in the circuit are a DC motor and a lamp load. The inputs are connected in parallel and even the outputs are parallelly connected. To use both the sources effectively [7,8], the duty cycles for both the sources should be different. The greater the duty cycle, the lower is the pulse and the output obtained is greater. This is due to the fact that the longer the inductors are charged, the greater the voltage will be. The loads are connected across the capacitors C_3 and C_4. Therefore, the voltage across the respective capacitors is the same as the load voltage for both the loads are explained in Figure 11.

Table 2. Comparisons of the components in conventional MPC and the proposed SEPIC/SEPIC MPC.

Components	*n* Port SEPIC/SEPIC Converter	(*n* − 2) Individual SEPIC Converter
Capacitors	N	$2(n-2)$
Inductors	N	$2(n-2)$
Switches	$n-2$	$n-2$

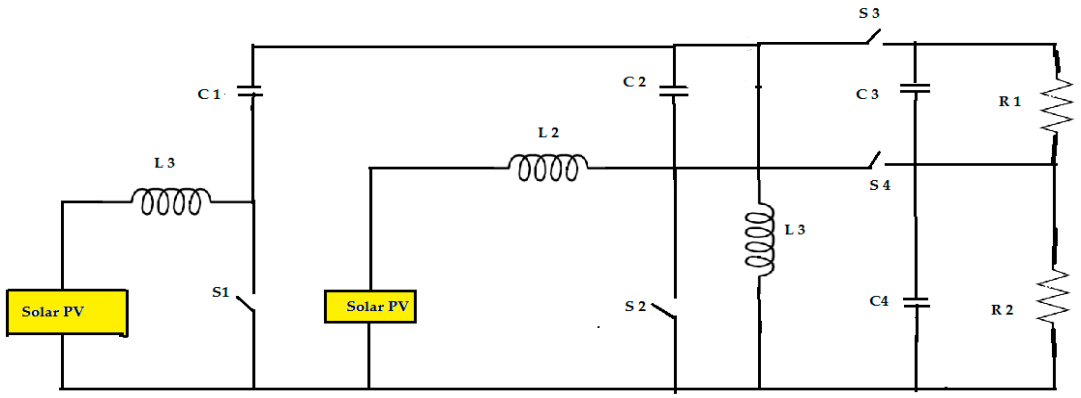


Figure 11. Four Port SEPIC/SEPIC Converters.

3.1. Unidirectional Power Flow

Two separate sources (both photovoltaic cells) having same power ratings have been considered. To use both the sources effectively, the two sources operate at different duty cycles. The source having the higher value of voltage operates for lower duty cycle whereas the source having the lower value of voltage operates for higher duty cycle.

Assuming V_1 as the voltage value for the first source and V_2 as the voltage value for the second source; D_1 and D_2 are the duty cycles for PVSC1 and PVSC2 respectively. If the voltage value of source 1 is greater than that of source 2, then the duty cycle of source 2 is greater than that of source 1. The operation can be categorized into four modes. The duty cycles for different modes is shown in the Figure 12. D_1, D_2, D_3 and D_4 are the duty cycles for different modes of operation of the circuit.

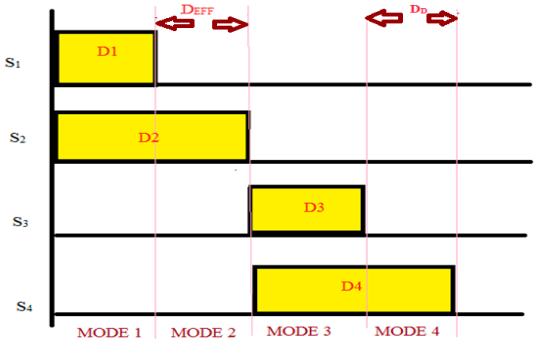


Figure 12. Modes of operation of MIMO.

Here, $D_{eff} = D_1 - D_2$ and $D_D = D_4 - D_3$. Each input source is connected in parallel through a power semiconductor switch and shares a common inductor (L). Only unidirectional power flow from the sources to inductor is allowed in this configuration. Power flow from each source i.e., source 1 and source 2, to load is controlled by operating switches S_1 and S_2 with different duty ratios for the same switching frequency. Hence, it results in four modes of operation of the converter. The modes with their respective duty cycle are explained below in Table 3.

Table 3. Modes of Operation.

MODES	ON	OFF
Mode A	S_1	S_2, S_3, S_4
Mode B	S_2	S_1, S_3, S_4
Mode C	S_3, S_4	S_1, S_2
Mode D	S_4	S_1, S_2, S_3

3.1.1. Mode A: S_1 and S_2 ON but only S_1 conducts, S_3 and S_4 is OFF

The equivalent circuit of mode A is shown in the Figure 13. In this mode, the switches S_1 and S_2 are ON. As S_2 is reverse biased only switch S_1 conducts. In steady state, voltages on the input capacitors C_1 and C_2 are V_1 and V_2 respectively. Since V_1 value is greater than V_2, S_2 blocks the possibility of flow of inverse current through the second input leg. Since S_2 is reverse biased it does not conduct and the load is sustained by the output capacitors C_3 and C_4. The inductor L charges during this mode of operation. Also, the capacitors C_3 and C_4 on the load side discharge.

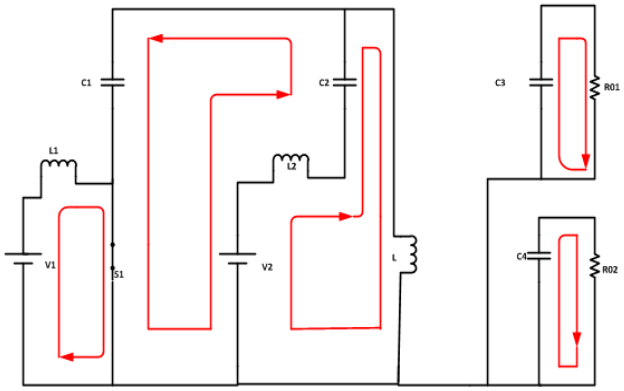


Figure 13. Mode-A of the proposed circuit.

3.1.2. Mode B: S_1 OFF and S_2 ON, S_3 and S_4 is OFF

Once the switch S_1 is OFF, the switch S_2 gets forward biased and starts conducting since the duty cycle of S_2 is greater than that of S_2.The load current is maintained by the capacitors on the output side. The inductor L is charged during this mode by the discharge of the capacitor C_2. The capacitors C_3 and C_4 discharges and the output voltages are obtained across them. The inductor L is charged during both mode A and mode B through the discharge of the capacitors C_1 and C_2, respectively shown in Figure 14.

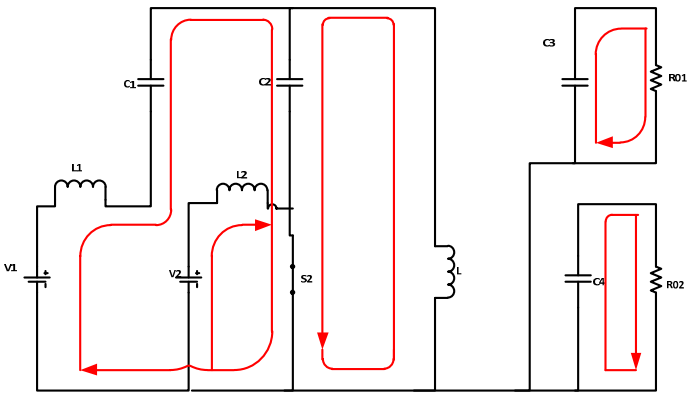


Figure 14. Mode-B of the proposed circuit.

3.1.3. Mode C: S_1 OFF and S_2 OFF, S_3 and S_4 is OFF

The equivalent circuit of mode C is shown in Figure 15. Both the switches S_1 and S_2 are in OFF state while the switches S_3 and S_4 conduct. The load is now supplied by both the sources V_1 and V_2 through the input sides inductors and capacitors. During the mode 3, the capacitors C_3 and C_4 on the load side charges through the discharge of the inductor L in the circuit.

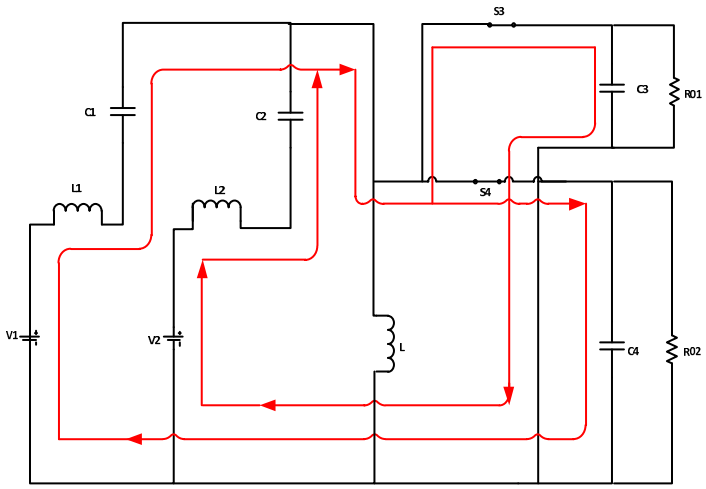


Figure 15. Mode-C of the proposed circuit.

3.1.4. Mode D: S_1 OFF and S_2 OFF, S_3 is OFF and S_4 is ON

The equivalent circuit of mode D is shown in Figure 16. Both the switches S_1 and S_2 are in OFF. Also the switch S_3 is OFF and S_4 is ON. The duty cycle for mode D is D_D where $D_D = D_4 - D_3$. In this mode of operation, the load side capacitor C_3 discharges as the switch S_3 is open. Also, the inductor L discharges while the capacitor C_4 on the load side charges.

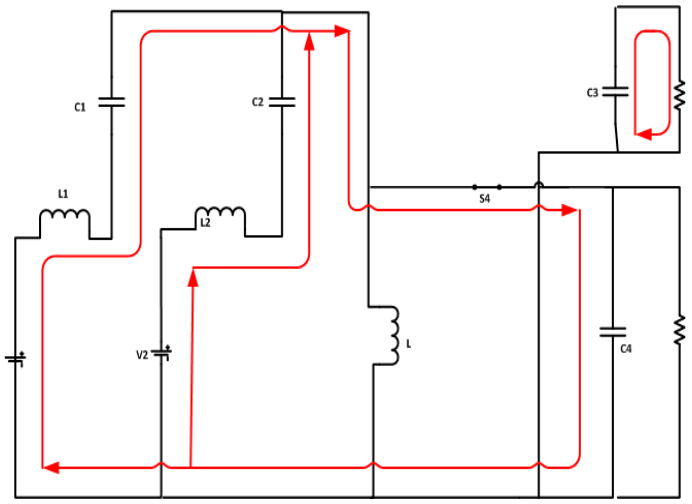


Figure 16. Mode-D of the proposed circuit.

3.2. Steady State Analysis of Multi Input Multi Output SEPIC Converter

The steady state equations of the proposed topology can be derived:

$$V_{01}D_3 + V_{02}(D_3 + D_4) = V_1D_1 + V_2D_2 \quad (24)$$

Steady state average conditions:

$$\frac{diL}{dt} = 0 \tag{25}$$

$$V_{c_1} = V_1, V_{c_2} = V_2, V_{c_3} = V_{01}, V_{42} = V_{02} \tag{26}$$

Using the above steady state average conditions in the equations (from (24) to (26)), we have:

$$V_{c_1} D_1 + V_2 D_{eff} = V_{c_4} D_D \tag{27}$$

The above equations represent the output voltage equations for the first and second load, respectively.

3.3. Small Ripple Approximation of Multi Input Multi Output SEPIC Converter

Following the individual mode equations from (28) to (34), the expressions of L_1, L_2, L, C_1, C_2 and C with respect to current and voltage ripples is described below. Considering three modes i.e., D_1, D_{eff}, D_3 and D_D operating for T_1, T_2, T_3 and T_4 periods respectively.T_1, T_2, T_3 and T_4 can be written as D_1 T, D_{eff} T, D_3 T and D_D T, respectively, where, T is the total time period.

Therefore, the voltage ripples can similarly be calculated from the mode equations. The voltage across C_1 rises (assuming linearly) from a low value to a high value, say V_{11} to V_{12} during the time T_2, T_3 and T_4.Therefore, the circuit parameters are:

$$L_1 = \frac{V_1 D_1}{f \Delta i_{L_1}} \tag{28}$$

$$L_2 = \frac{V_2 D_2}{f \Delta i_{L_2}} \tag{29}$$

$$L = \frac{VC_3}{f \Delta i_L} (D_3) \tag{30}$$

$$C_1 = \frac{I_1}{f \Delta V C_1} (1 - D_1) \tag{31}$$

$$C_2 = \frac{I_2}{f \Delta V C_2} (D_1 + D_4) \tag{32}$$

$$C_3 = \frac{VC_3}{fR \Delta V C_3} (D_2 + D_D) \tag{33}$$

$$C_4 = \frac{VC_4}{fR \Delta V C_4} (D_2) \tag{34}$$

4. Results and Discussion

Analysis of a Single Input Multi Output SEPIC the Simulink model for a three port unidirectional SEPIC details are shown in Figure 17.

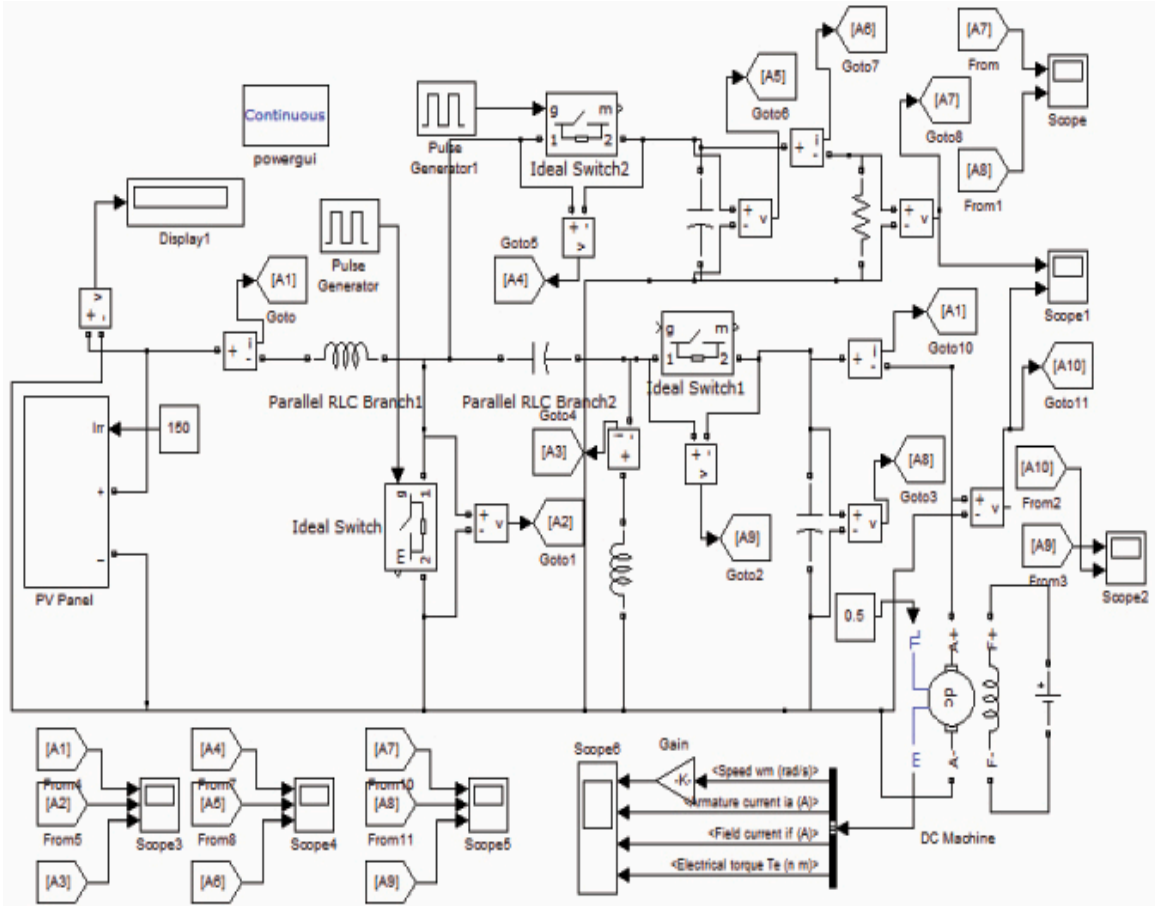


Figure 17. Simulink model for a three port unidirectional SEPIC.

In Figure 18 shows the output voltage and current waveforms of a SIMO SEPIC and Figure 19 shows second values of the output voltage and current waveforms of a SIMO SEPIC.

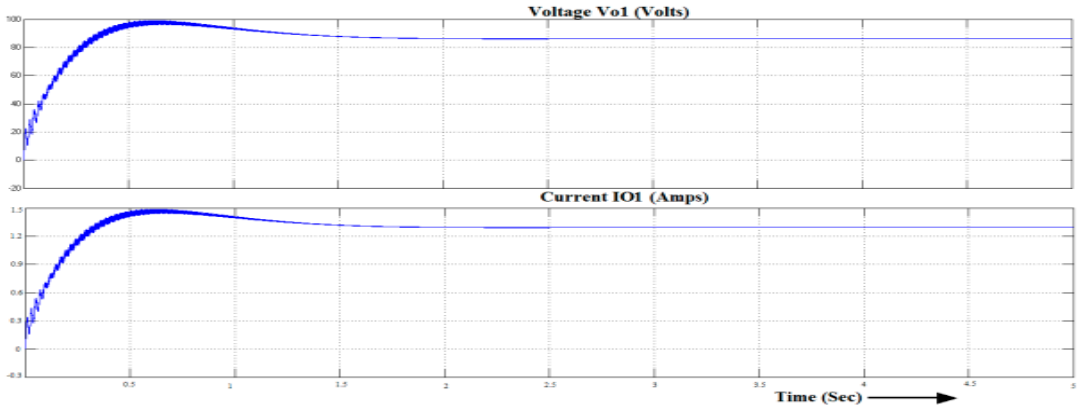


Figure 18. Output voltage and current waveforms of a SIMO SEPIC.

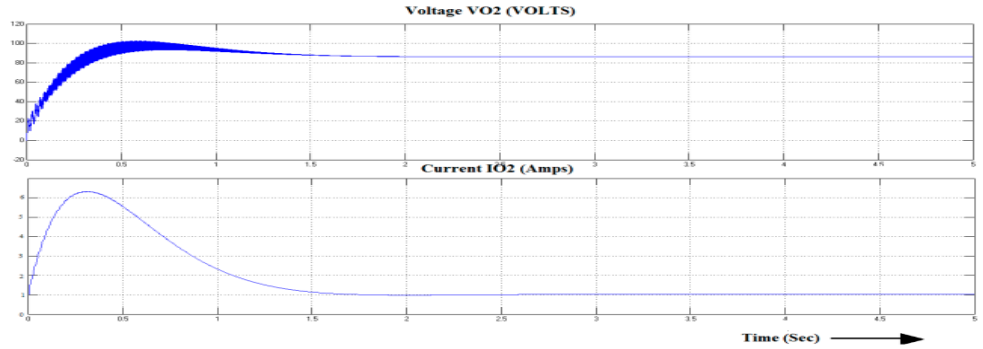


Figure 19. Output voltage and current waveforms of a SIMO SEPIC.

Table 4 shows the comparison of measured output voltages (V_2 and V_3) (from the Simulink model) and estimated output voltage from (24) to (27) for different set of input voltage (V_1) and duty cycles (D_1, D_2 and D_{eff}) and also explained the voltage and current of components in PVSC, PVlC2 and PVLC2 shown in Figure 20.

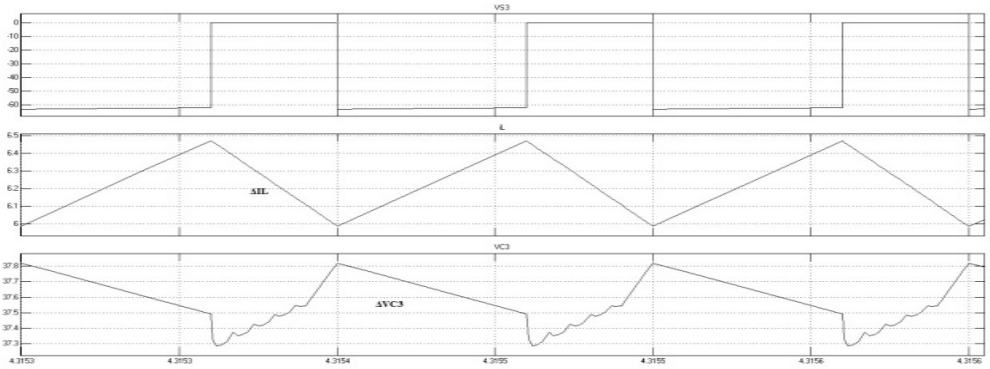


Figure 20. Waveforms of voltage and current of components in PVSC, PVlC2 and PVLC2, respectively.

The three modes of operations are clearly visualized in the waveforms of capacitor voltages and inductor currents of PVSC, PVLC1 and PVLC2. Also the comparison of measured and estimated output voltages (V_1 (act) and V_1 (est.)) and voltages (V_2 (act) and V_2 (est.)) shows approximately the same values for each different set of input values. And the speed and torque of motor is shown in Figure 21. In Figure 22 shown in simulink model for a port of SEPIC converter working operations and simulink details of output voltages 1 and 2.

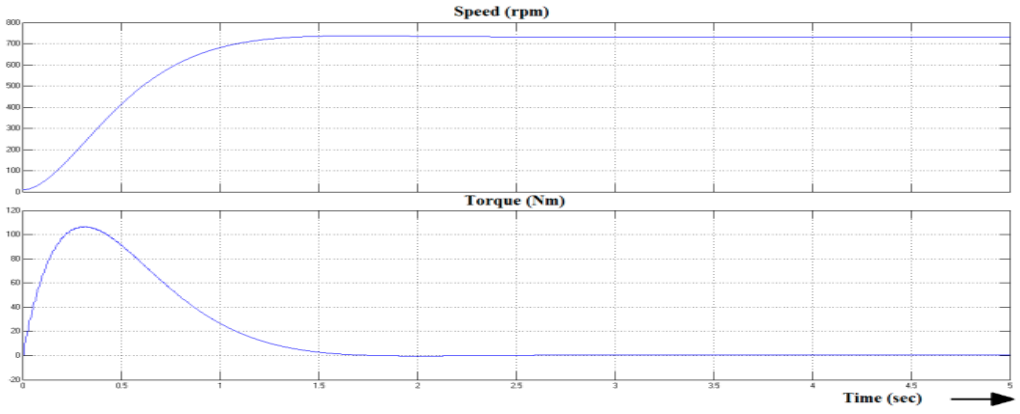


Figure 21. Waveform of speed and torque of motor.

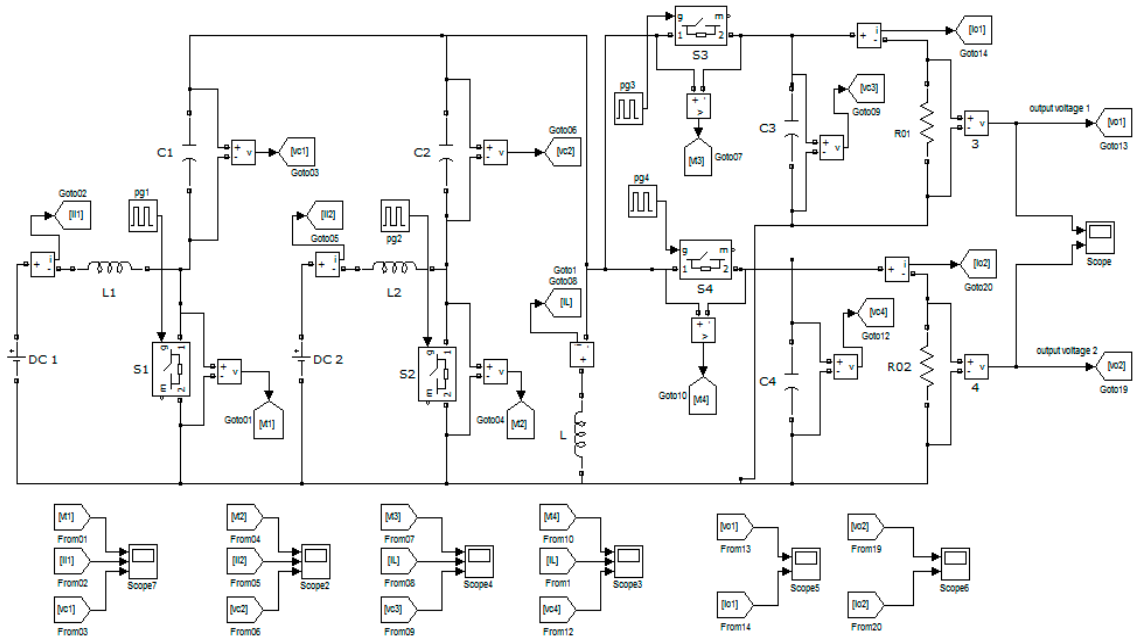


Figure 22. Simulink Model for a Four Port SEPIC.

Table 4. Actual and estimated values of output voltage for different set of supplies.

V_1	D_1	D_2	D_3	V_2 (act)	V_2 (est.)	V_3 (act)	V_3 (est.)
25	60	30	10	37.5	35.97	37.5	35.93
25	50	30	20	25	24.63	25	24.59
30	30	20	50	13	12.55	13	12.51
30	40	40	20	20	19.75	20	19.71
36	60	30	10	54	51.8	54	51.7
36	70	20	10	84	78.43	84	78.29

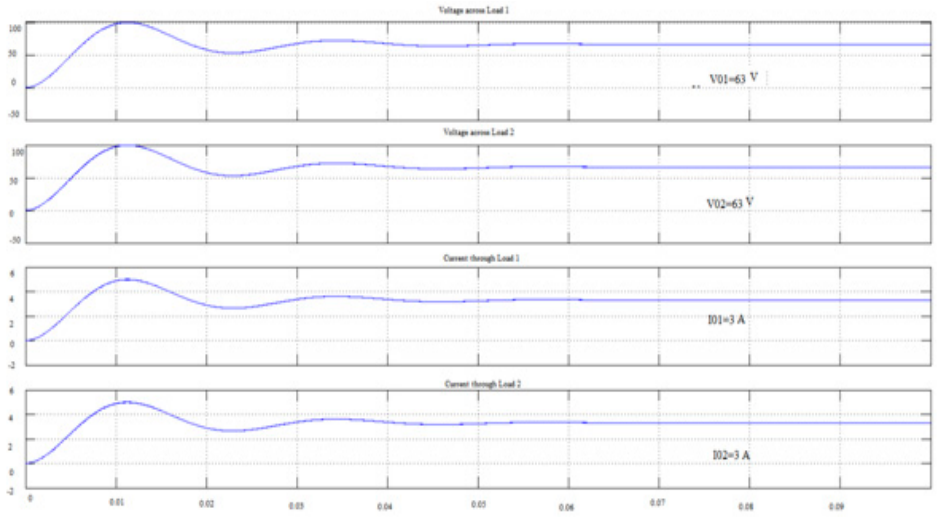


Figure 23. Output Voltage and Current Waveforms of the Proposed Topology.

In the above Figure 23 shows the output voltage and current waveforms of the proposed topology and also explain the detailed operations of Waveforms of voltage and currents across the components of PVSC2 in Figure 24.

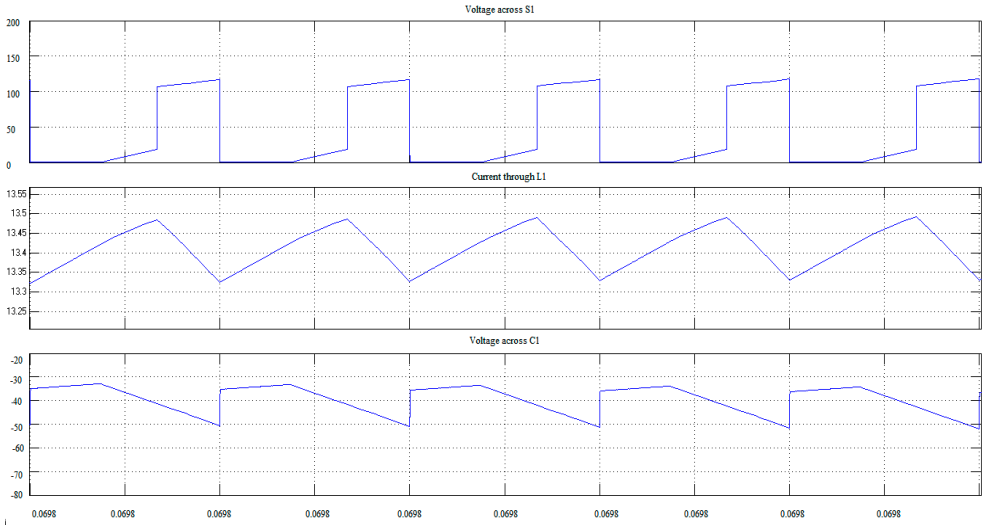


Figure 24. Waveforms of voltage and currents across the components of PVSC2.

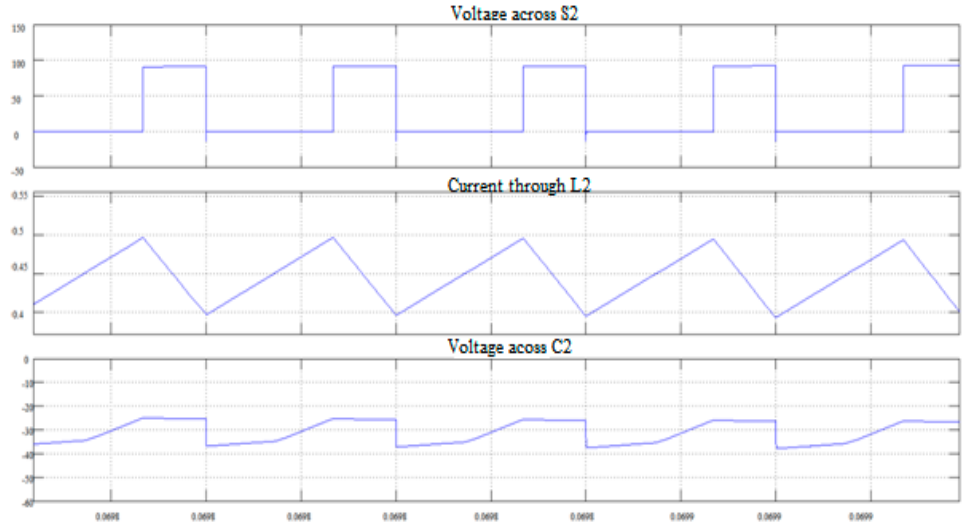


Figure 25. Waveforms of voltage and currents across the components of PVLC1.

In above the Figure 25 shows the detailed voltage and currents across the components of PVLC1.

In Figure 26 shows the voltage and currents across the components of PVLC2.The four modes of operation are visualized in the waveforms of capacitor voltages and inductor currents of the source and load sides. The ripple present in inductor currents and capacitor voltages obtained through MATLAB (R2016a, MathWorks, Natick, MA, USA) is concurrent with an estimated ripple of 0.5. In the output voltages of load 1, Speed torque characteristics PVSC1, PVSC2, PVLC1 and PVLC2shown in Figures 27–29.

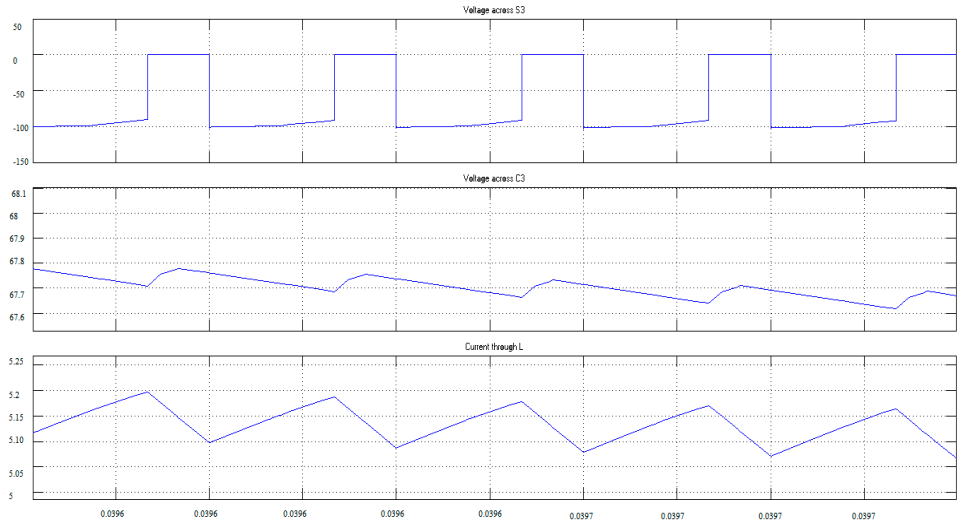


Figure 26. Waveforms of voltage and currents across the components of PVLC2.

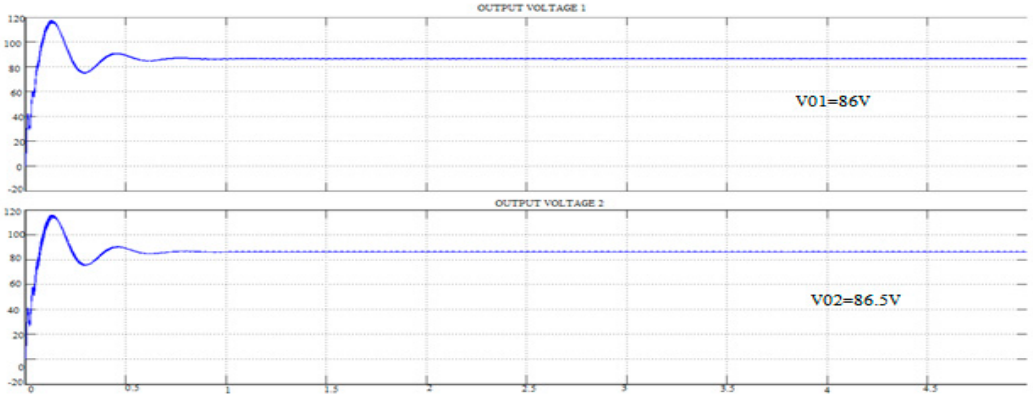


Figure 27. Waveforms for Load 1.

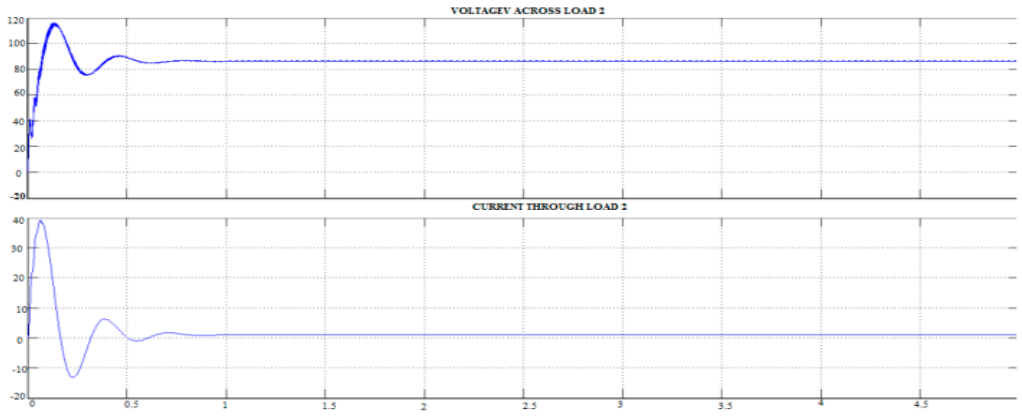
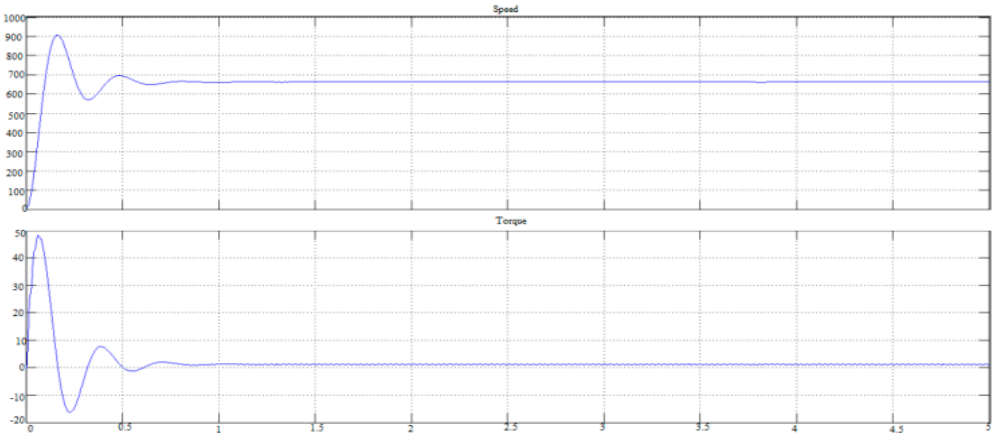
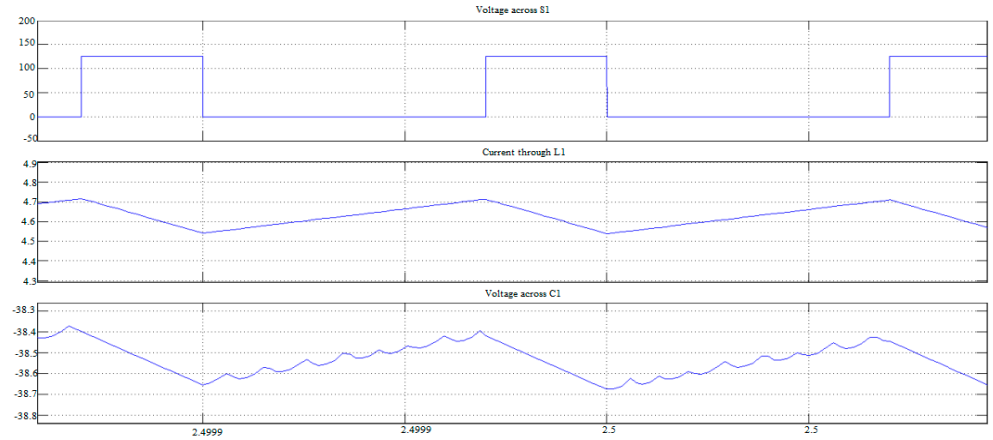


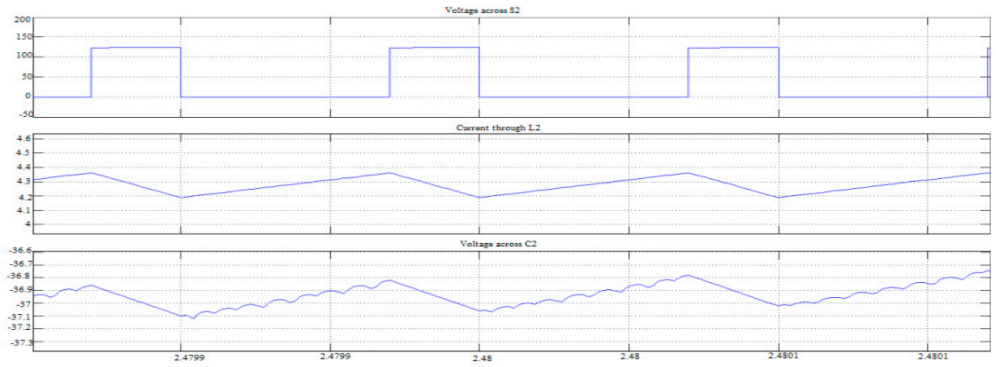
Figure 28. Speed-torque characteristics.



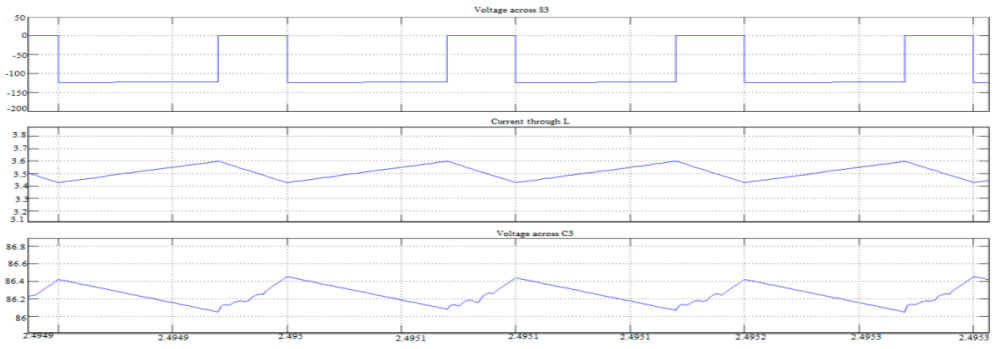
(**a**)



(**b**)

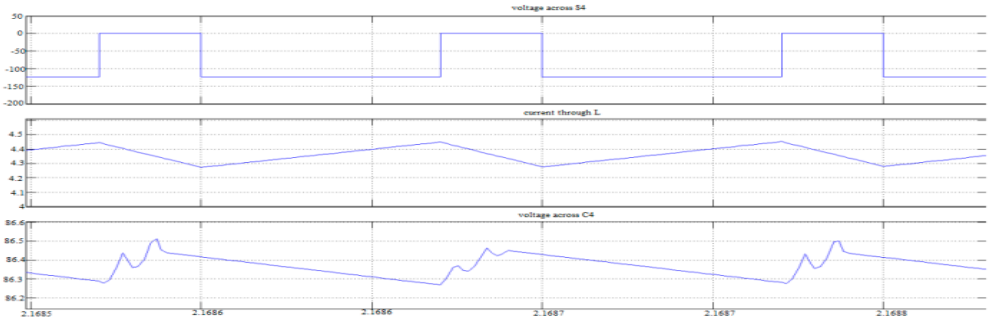


(**c**)



(**d**)

Figure 29. *Cont.*



(**e**)

Figure 29. (**a**) Waveforms for PVSC1; (**b**) Waveforms for PVSC2; (**c**) Waveforms for PVLC1; (**d**) Waveforms for PVLC2; and (**e**) Waveforms of voltage and currents across the components of PVSC1, PVSC2, PVLC1 and PVLC2.

The waveforms of capacitor voltages and inductor currents of PVSC1, PVSC2 and PVLC1 and PVLC2. Also the comparison of measured and estimated output voltages (V_0 (act)) and V_0 (est.)) shows approximately the same values for a set of input sources (V_1, V_2) and duty cycles (D_1, D_2).

5. Hardware Implementation of Multi Port SEPIC Converter

The simulation analysis of the open loop unidirectional topology is verified with a real time hardware setup. The hardware setup is realized with one IGBT (FGA15N1) (Fairchild Semiconductor and this IGBT short description IGBT NPT 1200V 15A TO-3P) and two MOSFETs (N-channel MOSFET and 600V 4A MOSFET).A DSPIC30F2010 microcontroller (Microchip Technology, Wide operating voltage range (2.5 V to 5.5 V) dsPIC30F Motor Control 16-bit Digital Signal Controller) is used for generating the switching pulses. The research laboratories and Researchers mainly used for in this version of Matlab software Experiments are carried out in continuous current mode. In the input port, supply is provided by solar PV of almost equal power rating. The input to PVSC is V_1 = 35 V. The duty cycle for two corresponding switches D_1 = 60%, D_2 = 30% and D_3 = 10%. A 50 W universal motor is given as load to the unit. The components of the setup are designed to operate maximum at 1 kW. The component design parameters of the setup are given in Table 5.

Table 5. Design of parameters.

PVSC Inductor, L_1	15 mH
Common inductor, L	15 mH
PVSC1 capacitor, C_1	0.54 mF
PVLC1 capacitor, C_2	0.54 mF
PVLC2 capacitor, C_3	0.46 mF
Switching frequency, f	5000 Hz

With the given input and duty cycle, the calculated value of the output voltages for V_1 is V_{01} = 85.6 V and V_{02} = 86 V. The output of MATLAB simulation of the proposed topology for the similar parameters is approximately V_{01} = 86.66 and V_{02} = 85.66 V. The output voltages of the proposed hardware setup for the given input and duty cycle are V_{01} = 85 V and V_{02} = 84 V. This indicates that for the similar value of parameters and inputs, the output corresponding to mathematical analysis, MATLAB simulation and hardware setup is approximately the same. In Figure 30 shows the block diagram of hardware arrangements.

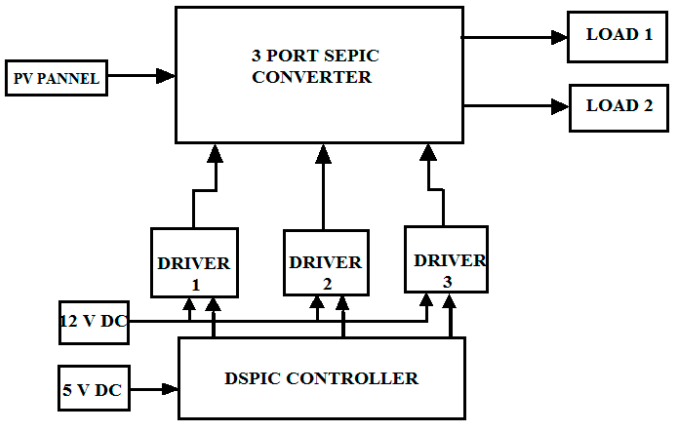


Figure 30. Block diagram of the hardware setup.

In Table 6 Explain the microcontroller and driver, IGBT, MOSFET components specifications and models details.

Table 6. Component specifications.

Component	Model	Specification
Microcontroller	DSPIC30F2010	28 IC pins 6 PWM channel (21–26) 5 V operating voltage 10 MHz operating frequency (9–10)
Driver	TLP250	8 pins 12 V operating voltage
IGBT	FGA15N120	15 A maximum current 1200 V maximum voltage
MOSFET	ISA04N60A	1 MHz maximum frequency 600 V maximum voltage 4 A maximum current

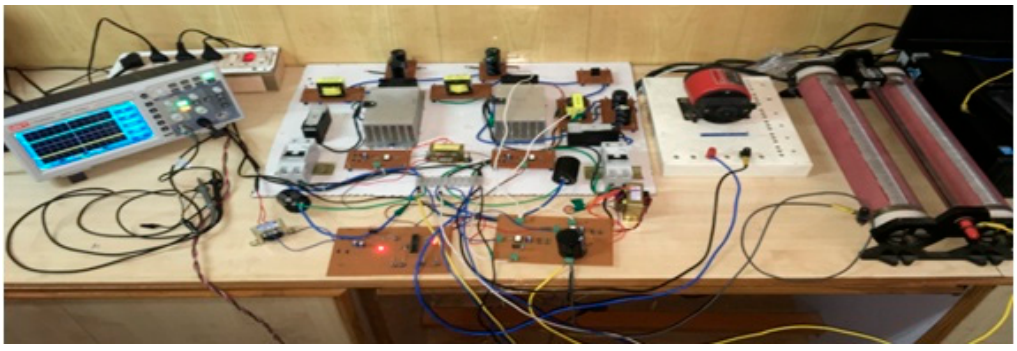


Figure 31. The complete circuit of the three port SIMO structure.

In the above Figure 31 is shown in the complete circuit of the three port SIMO structures details Table 7 shows the comparison of measured output voltage (from MATLAB Simulink) and timed output voltages for different sets of input voltages and duty cycles. Therefore it operates in buck, boost and buck-boost modes. All the hardware output voltage, capacitor output voltages & load 1 and 2 is given in Figures 32–41.

Table 7. Actual and Estimated Output Voltages for Different Sets of Input Voltages.

V_1	V_2	D_1	D_2	D_3	D_4	V_{01} (Act)	V_{01} (Est.)	V_{02} (Act)	V_{02} (Est.)
50	25	0.37	0.67	0.15	0.33	80	79	80	78.78
50	35	0.25	0.70	0.15	0.30	95	94.17	95	94.16
60	30	0.20	0.50	0.30	0.50	45	42	45	42
60	40	0.42	0.60	0.25	0.40	82	81	82	81
35	20	0.30	0.55	0.20	0.45	32.5	34.45	32.5	34.44

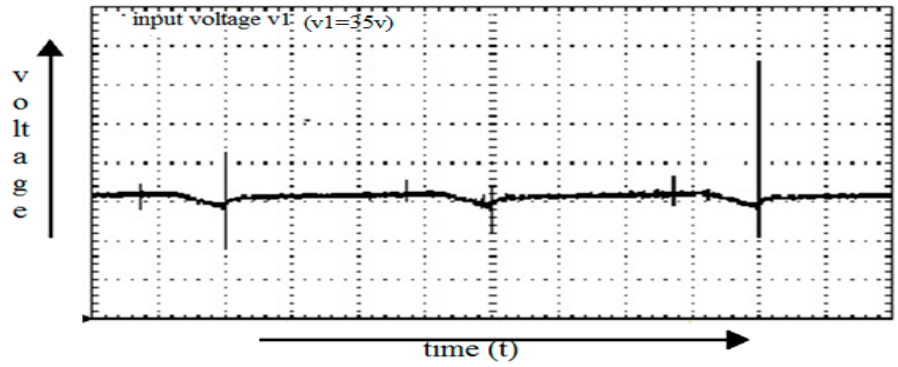


Figure 32. Input voltage V_1.

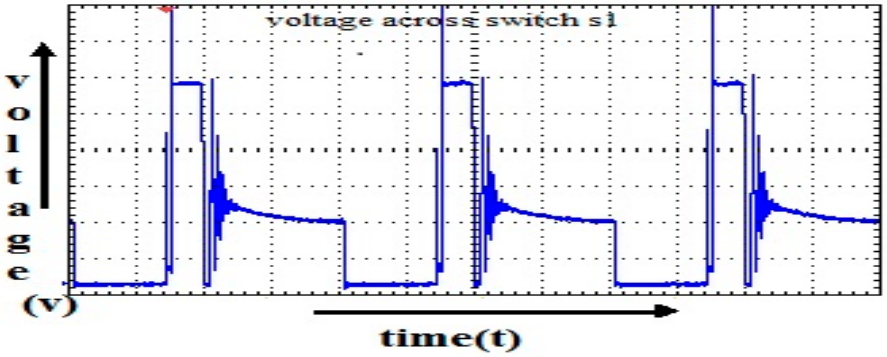


Figure 33. Voltage across switch S1.

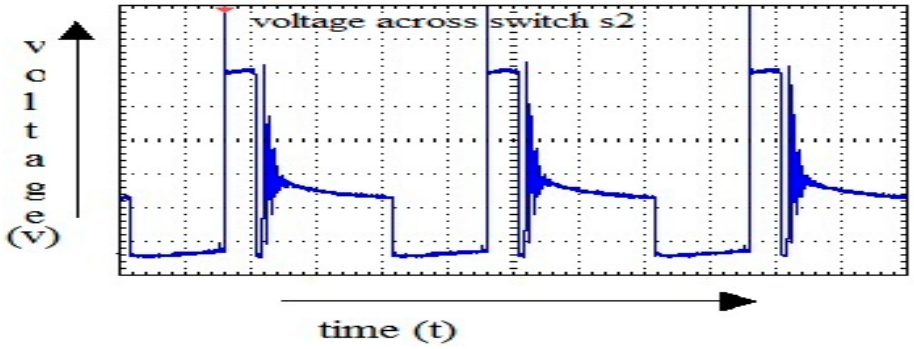


Figure 34. Voltage across switch S2.

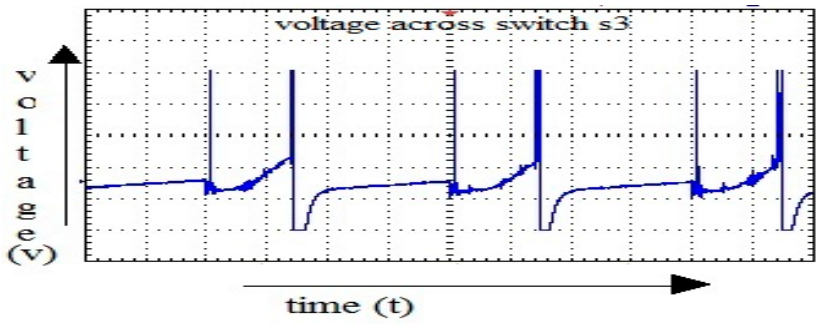


Figure 35. Voltage across switch S3.

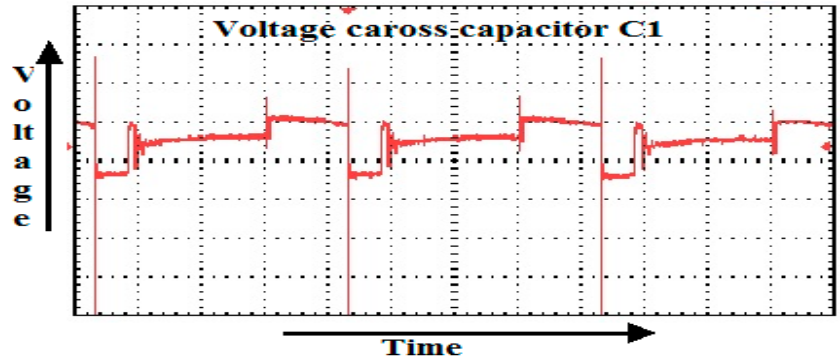


Figure 36. Voltage across capacitor C_1.

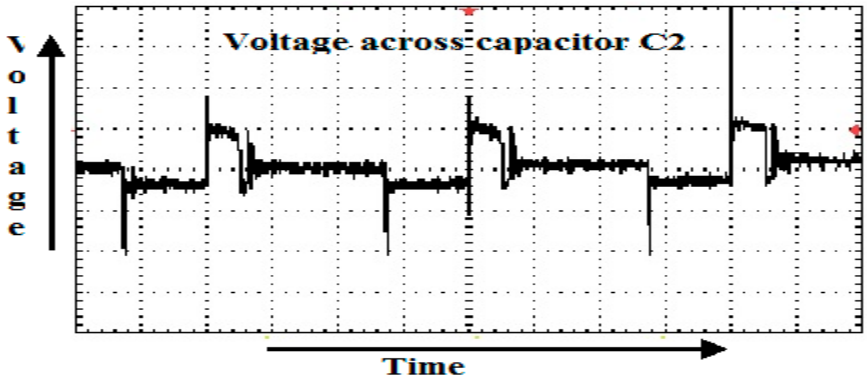


Figure 37. Voltage across capacitor C_2.

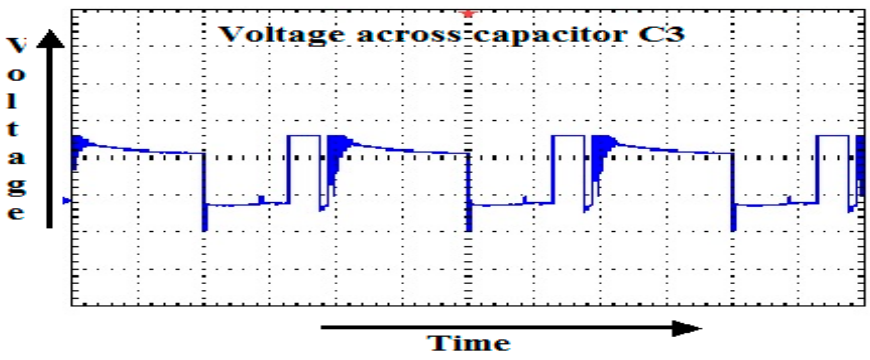


Figure 38. Voltage across C_3.

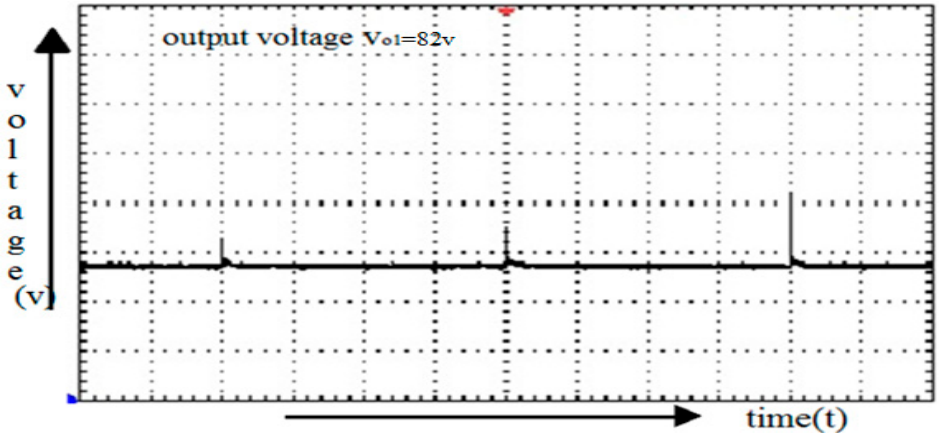


Figure 39. Output voltage V_{01}.

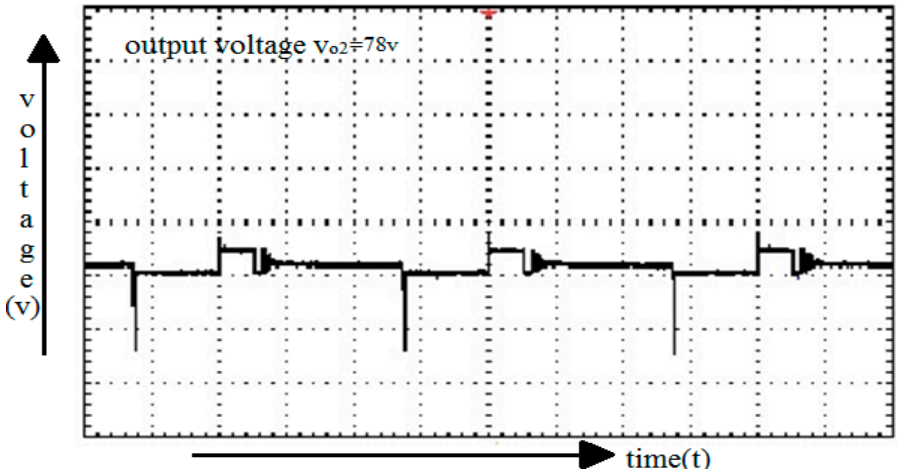
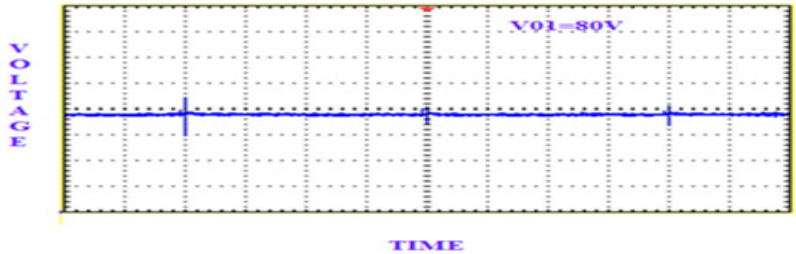
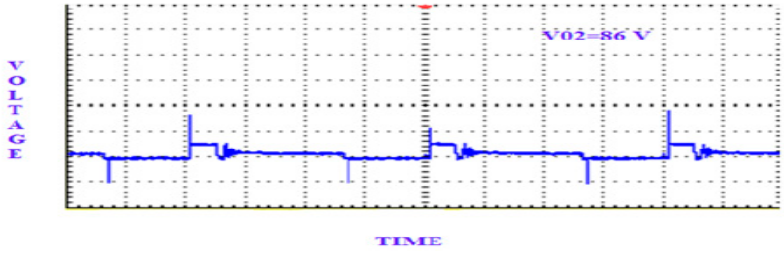


Figure 40. Output voltage V_{02}.



(**a**)



(**b**)

Figure 41. (**a**) Ripple waveform for voltage of load 1; (**b**) Ripple waveform for voltage of load 2.

6. Conclusions

The multiport topology for SEPIC converter was studied. A three-port unidirectional model is proposed. The proposed multiport converter is capable of interfacing two outputs by using a single voltage source such as a photovoltaic (PV) cell. The operation of the proposed converter with single a voltage source with a PV is verified. The authentication for the performance and operation of the converter is done with MATLAB simulations and mathematical analysis. The proposed circuit is efficient in interfacing the renewable energy due to its advantages of simple configuration, high efficiency, and reduced devices. The work is carried further with implementation of real time hardware with a DSPIC microcontroller. The authentication of simulation results and mathematical analysis of the proposed open loop topology have been proved by a real time hardware setup. Input to the hardware setup is provided from a solar PV of 35 V, and the unit operates with duty cycles of 67%. The output voltage of the hardware unit was 85 V, which matches the output voltage of the simulation and mathematical model. Also the modes of operation of the proposed open loop topology have been verified with the hardware results.

The multiport converter topology of a SEPIC was studied and a four port SEPIC for unidirectional properties is proposed. The two sources coupled to the converter are two PV cells. Four port power management systems can accommodate two sources and combine their advantages by using only a single conversion stage to interface four power ports. The operation of the proposed converter having two sources has been verified. The authentication for the performance and operation of the converter is done using MATLAB simulations and mathematical analysis. The calculation for small ripple approximation is done to find the parameter values of the different components used in the circuit. Analysis of the dual-input, dual-output converter with the simulation and experimental results are presented. Performance comparisons between the ideal calculation and results obtained from the hardware and simulation are closely matched.

Acknowledgments: We thank C. Anuradha and N. Chellammal for their technical assistance, comments on the manuscript, and fruitful discussions that improved the analytical part of the paper.

Author Contributions: All authors contributed equally for the research work and its final decimation as article in its current form.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wu, H.; Zhang, J.; Xing, Y. A Family of Multiport Buck–Boost Converters Based on DC-Link Inductors (DLIs). *IEEE Trans. Power Electron.* **2015**, *30*, 735–746. [CrossRef]
2. Rehman, Z.; Al-Bahadly, I.; Mukhopadhyay, S.C. Multi-input DC–DC converters in renewable energy applications—An Overview. *Renew. Sustain. Energy Rev.* **2015**, *41*, 521–539. [CrossRef]
3. Tao, H.; Kotsopoulos, A.; Duarte, J.L.; Hendrix, M.A.M. Family of multiport bidirectional DC–DC converters. *IEE Proc. Electr. Power Appl.* **2006**, *153*, 451–458. [CrossRef]
4. Ferrera, M.B.; Litrán, S.P.; Durán, E.; Andújar, J.M. A Converter for Bipolar DC Link Based on SEPIC-Cuk Combination. *IEEE Trans. Power Electron.* **2015**, *30*, 6483–6487. [CrossRef]
5. Jiang, W.; Fahimi, B. Multiport Power Electronic Interface—Concept, Modeling, and Design. *IEEE Trans. Power Electron.* **2011**, *26*, 1890–1900. [CrossRef]
6. Palma, L.; Enjeti, P.N. A modular fuel cell, modular DC–DC converter concept for high performance and enhanced reliability. *IEEE Trans. Power Electron.* **2009**, *24*, 1437–1443. [CrossRef]
7. Todorovic, M.H.; Palma, L.; Enjeti, P.N. Design of a wide input range DC-DC converter with a robust power control scheme suitable for fuel cell power conversion. *IEEE Trans. Ind. Electron.* **2008**, *55*, 1247–1255. [CrossRef]
8. Hawke, J.T.; Krishnamoorthy, H.S.; Enjeti, P.N. A new utility-scale power converter for large fuel cell power plants with individual stack power control. In Proceedings of the 27th IEEE Annual Applied Power Electronic Conference Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 1482–1488.

9. Yuehui, H.; Tse, C.K. Circuit theoretic classification of parallel connected DC-DC converters. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2007**, *54*, 1099–1108.
10. Wai, R.J.; Chen, C.Y.; Chen, B.H. High-efficiency DC–DC converter with two input power sources. *IEEE Trans. Power Electron.* **2012**, *27*, 1862–1875. [CrossRef]
11. Cao, F.; Zhang, J.; Wu, H.; Hu, H.; Xing, Y.; Ma, X. A dual-input boost-buck converter with coupled inductors for TEG applications. In Proceedings of the IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013; pp. 2020–2025.
12. Ouyang, Z.; Zhang, Z.; Andersen, M.A.E.; Thomsen, O.C. Four quadrants integrated transformers for dual-input isolated DC–DC converters. *IEEE Trans. Power Electron.* **2012**, *27*, 2697–2702. [CrossRef]
13. Li, Y.; Ruan, X.; Yang, D.; Liu, F.; Tse, C.K. Synthesis of multiple input DC/DC converters. *IEEE Trans. Power Electron.* **2010**, *25*, 2372–2385. [CrossRef]
14. Shen, Z.; Chang, X.; Wang, W.; Tan, X.; Yan, N.; Min, H. Predictive digital current control of single-inductor multiple-output converters in CCM with low cross regulation. *IEEE Trans. Power Electron.* **2012**, *27*, 1917–1925. [CrossRef]
15. Patra, P.; Patra, A.; Misra, N. A single-inductor multiple-output switcher with simultaneous Buck, Boost, and inverted outputs. *IEEE Trans. Power Electron.* **2012**, *27*, 1936–1951. [CrossRef]
16. Wu, H.; Sun, K.; Chen, R.; Hu, H.; Xing, Y. Full-bridge three-port converter with wide input voltage range for renewable power systems. *IEEE Trans. Power Electron.* **2012**, *27*, 3965–3974. [CrossRef]
17. Wu, H.; Chen, R.; Zhang, J.; Xing, Y.; Hu, H.; Ge, H. A family of three port half-bridge converters for a stand-alone renewable power system. *IEEE Trans. Power Electron.* **2011**, *26*, 2697–2706. [CrossRef]
18. Behjati, H.; Davoudi, A. Power budgeting between diversified energy sources and loads using a multiple-input-multiple-output DC/DC converter. *IEEE Trans. Ind. Appl.* **2013**, *49*, 2761–2772. [CrossRef]
19. Wu, H.; Xu, P.; Hu, H.; Zhou, Z.; Xing, Y. Multiport Converters Based on Integration of Full-Bridge and Bidirectional DC–DC Topologies for Renewable Generation Systems. *IEEE Trans. Ind. Electron.* **2014**, *61*, 856–869. [CrossRef]
20. Zhao, C.; Round, S.D.; Kolar, J.W. An isolated three-port bidirectional dc–dc converter with decoupled power flow management. *IEEE Trans. Power Electron.* **2008**, *23*, 2443–2453. [CrossRef]
21. Wu, H.; Xing, Y.; Xia, Y.; Ma, X. A family of non-isolated three-port converters for stand-alone renewable power system. In Proceedings of the 37th Annual Conference on IEEE Industrial Electronics Society, Melbourne, Australia, 7–10 November 2011; pp. 1030–1035.
22. Nielsen, H.R.; Andersen, M.A.E.; Zhang, Z.; Thomsen, O.C. Dual-input isolated full bridge boost DC–DC converter based on the distributed transformers. *J. IET Power Electron.* **2012**, *5*, 1074–1083.
23. Zhang, Z.; Thomsen, O.C.; Andersen, M.A.E. Modeling and control of a dual-input isolated full-bridge boost converter. In Proceedings of the Twenty-Seventh Annual IEEEAsia International Model Simulation Conference (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 1048–2334.
24. Yalamanchili, K.P.; Ferdowsi, M. Review of multiple input DC–DC converters for electric and hybrid vehicles. In Proceedings of the IEEE Vehicle Power Propulsion Conference, Chicago, IL, USA, 7–9 September 2005; pp. 552–555.
25. Chen, Y.; Liu, Y.; Lin, S. Double-input PWM DC/DC converter for high-/low-voltage sources. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1538–1545. [CrossRef]
26. Liu, Y.; Chen, Y. A systematic approach to synthesizing multi-input DC–DC converters. *IEEE Trans. Power Electron.* **2009**, *24*, 116–127. [CrossRef]
27. Kumar, L.; Jain, S. A multiple source DC/DC converter topology. *J. Electr. Power Energy Syst.* **2013**, *51*, 278–291. [CrossRef]
28. Rojas-gonz, M.A.; Edgar, S. An integrated dual-output buck converter based on sliding mode control. In Proceedings of the IEEE Third Latin American Symposium on Circuits and Systems, Playa del Carmen, Mexico, 29 February–2 March 2012; pp. 1–4.